Growth of High Quality CdTe on Si Substrates by Molecular Beam Epitaxy

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We have systematically studied the growth of CdTe (111)B on Si(001)with different atomic step structures, defined uniquely by miscut tilt angle and direction. X-ray double crystal rocking curve (DCRC) analysis has been used to evaluate the crystalline quality and twin content of the films. High-resolution electron microscopy has been used to examine the CdTe(111)B/Si(001) interface and to follow the microstructural evolution as a function of distance from the interface. Our results show that the formation of double domains and twins is very sensitive to the tilt parameters. When growth conditions are optimized, twins are not observed at distances greater than about 2.5 microns from the substrate surface. The best quality films exhibit a DCRC FWHM of 60 arc sec, for a film thickness of 17 μm, the lowest value ever reported for heteroepitaxial growth of CdTe on Si or GaAs. In efforts to improve the nucleation process, precursors such as Te and As have been used, and we have shown that they improve the stability of the heterointerface.

Key words: CdTe, defects, heteroepitaxy, HgCdTe, molecular beam epitaxy, Si substrate

INTRODUCTION

Successful growth of CdTe on Si substrates provides inexpensive, rugged, large-area substrates for subsequent growth of HgCdTe. Furthermore, CdTe/Si provides an opportunity to integrate a Si-based signal processing system and HgCdTe-based infrared detectors onto a single chip resulting in an extremely compact focal-plane array. The Microphysics Laboratory at the University of Illinois at Chicago reported the first direct growth of CdTe on Si substrates in 1989.[1] Since that time, tremendous progress has been made both in the material quality of the CdTe epilayer and in the fundamental understanding of this challenging heteroepitaxial interface.

The heteroepitaxial growth of CdTe on Si poses some extreme difficulties due to the large lattice mismatch (~19%), thermal expansion coefficient mismatch and the valence mismatch between the substrate and epilayer. These lead to large dislocation densities at the interface and a drastic change in the nature of the bonding at the interface. The large lattice mismatch also induces a change in symmetry of the heteroepitaxy. For example, on a Si (001) substrate, CdTe grows preferentially in the (111)B orientations.[1] Double domains and twins are the most commonly observed defects that severely degrade the quality of the CdTe(111)B heteroepitaxial film. The successful growth of high quality CdTe epilayers depends crucially upon effective suppression of these defects close to the interface.

Double domains and twins arise from the change in symmetry from the nominal Si(001) surface to the CdTe (111)B growth surface. By using Si wafers with surfaces deliberately tilted away from (001), this study correlates defect formation in CdTe epilayers with Si surfaces exhibiting different atomic step structures. These surface configurations are defined by the two tilt parameters θ and ϕ, where θ is the angle between Si [001] and the surface normal, and ϕ is the

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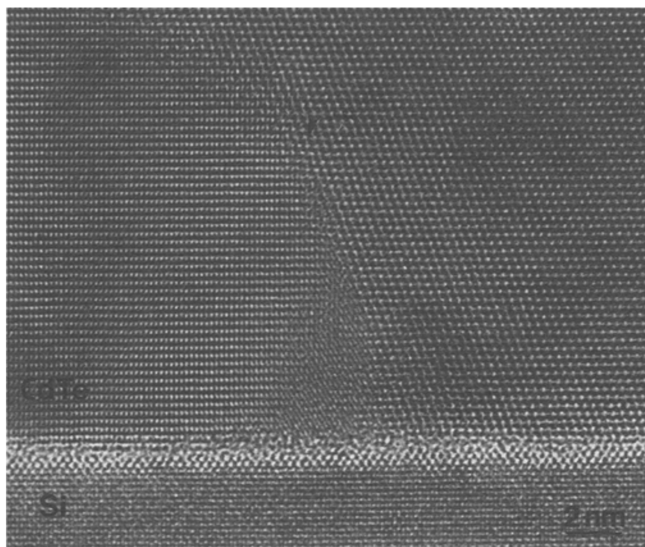

Fig. 1. High-resolution electron micrograph showing curved domain boundary (arrowed) extending from coherent CdTe/Si interface.

azimuthal angle with respect to Si [110]. Defect densities are determined by double-crystal rocking curve (DCRC) analysis as well as high-resolution transmission electron microscopy (TEM), which can reveal atomic-scale features throughout the epilayer.[2] The TEM images demonstrate an abrupt CdTe/Si interface and confirm the relationship between tilt parameters and defect suppression. Both DCRC and TEM indicated that small θ (~1°) is sufficient to suppress the formation of double domains[3] and that the parameter ϕ can greatly influence the propagation of lamellar twinning defects.[4]

EXPERIMENT

All Si substrates were cleaned using modified RCA cleaning methods. The substrates were first degreased in H_2O:NH_4OH:H_2O_2 (5:1:1), rinsed in deionized H_2O, then etched in HF (~2%). Finally, a thin protective oxide was chemically grown using H_2O:HCl:H_2O_2 (5:1:1) before loading the sample into vacuum. MBE growth was carried out in a Riber OPUS 45 prototype manufacturing system, capable of growing one 5 inch wafer or three 2 inch wafers. The latter capability was extremely useful for this study since three wafers with different substrate tilt parameters could be grown under identical growth conditions. The wafers were outgassed at ~400°C in a preparation chamber before they were transferred into the growth chamber, where the protective oxide was thermally removed at ~850°C. Oxide removal was monitored with *in situ* reflection high energy electron diffraction (RHEED). The wafer was finally cooled to the appropriate deposition temperatures.

During the cooling process various precursor fluxes (i.e. As, Te, ZnTe) were introduced to modify the surface. Our best layers have been achieved by exposing the Si surface to an As flux while the substrate cools from 750–350°C and to a Te flux during cooling from ~450–350°C. The role of the As precursor is under investigation. We hypothesize that As may act as a surfactant, surface passivant, or an interfacial layer or in some combination of these functions. We have confirmed[1] that a ZnTe buffer layer preserves the crystallographic orientation of the substrate, which thus makes possible the growth of CdTe(001) onto Si(001) and of CdTe(211) onto Si(211).

The CdTe layer is grown according to the following typical multi-step process: 210°C for 2 min; 250°C for 10 min; annealing under a Te flux 360°C for 10 min; and growth at 310°C for 16 h.

Cross-sectional TEM specimens were prepared for observation along Si [110] and $[\bar{1}10]$ directions using a rod-and-tube method similar to that used by Bravman and Sinclair.[5] Following mechanically thinning and dimpling to thicknesses of 15–25 μm, the specimens were ion-milled to perforation with 5 keV Ar^+ ions. A JEM-4000EX 400 keV high-resolution electron microscope (HREM) with an interpretable resolution of ~0.16 nm was used for observation.

RESULTS

Suppression of Double-Domain Formation by Optimization of the Tilt Angle (θ)

The nominal Si (001) reconstructed surface with atomic-scale roughness has two types of domains, circumscribed by atomic steps. These domains are identified by the orientation of the dimerized bonds, either parallel or perpendicular to the step edges.[6] The introduction of a tilt to the Si surface reduces the symmetry of the surface, creates a dominant step direction and thereby establishes a preferential domain orientation for CdTe growth.

Growth of CdTe (111)B on the nominal Si (001) surface is characterized by the formation of double domain regions, with CdTe$[\bar{1}10]$ || Si[110] and CdTe$[11\bar{2}]$ || Si[110]. This result has been confirmed by x-ray double-crystal rocking curve[3] analysis as well as by TEM imaging.[7] The typical lateral size of each domain is 2 μm, and they often extend from the interface to the top surface of the epilayer. In comparison, the average terrace size on the Si surface is about two orders of magnitude less, implying that the actual terrace size is not so important in influencing the domain structure.

The introduction of even a small ($\theta = 1°$) substrate tilt angle toward [110] ($\phi = 0$) effectively suppresses the formation of double domain regions in the epilayer. TEM results show that CdTe $[11\bar{2}]$ aligns preferentially along the directions of the step edges, either Si$[\bar{1}10]$ or $[1\bar{1}0]$. The lattice mismatch is reduced to 3.4%, rather than 19% in the orthogonal direction. Regions characterized by CdTe$[11\bar{2}]$ || Si[110], which are observed at the interface, are mostly suppressed, typically within 30–40 nm of the interface, and CdTe$[11\bar{2}]$ || Si$[\bar{1}10]$ rapidly becomes the dominant orientation. This effect can be clearly seen in Fig. 1 where the initially vertical domain boundary rapidly becomes curved toward a direction parallel to the interface.

Suppression of Twin Defects by Optimization of Tilt Orientation (ϕ)

Both lamellar twins and double positioning twins were observed in the CdTe epilayers. Double-positioning twins result from island growth near the interface; they form at the boundaries between coalescing islands. Lamellar twins form along the growth direction; they can be characterized by 180° rotation about CdTe [111]; i.e. CdTe $[11\bar{2}]$ || Si $[1\bar{1}0]$ or Si $[\bar{1}10]$. Previous DCRC studies[4] have shown that both tilt parameters, θ and ϕ can have a profound effect on twin density. However, DCRC analysis suffers from the drawback that it provides an average measure of material properties throughout the depth of x-ray penetration. The localized nature of transmission electron microscopy imaging provides more reliable information about the variation of twin density throughout the epilayer.

Transmission electron microscopy observations[7] suggest that three factors had an influence on the density of lamellar twins, namely, proximity to the interface, proximity to double domain boundaries and small values of ϕ (0–10°). All samples, independent of tilt parameters, exhibited large twin densities near the interface (76–92/μm). For double domain CdTe films, grown on nominal Si (001) twinning persists throughout the layer. In one sample at a distance of 0.9 μm above the interface, the density of lamellar twins decreased from 47/μm near a domain boundary to 20/μm at a distance of 1.5 μm away from the boundary.

The observed correlation of lamellar twin density and the proximity to domain boundaries implies a strain field influence on lamellar twin formation. A small increase in tilt orientation (θ = 1°, ϕ = 4°) localizes twinning densities to within 5 μm of the interface. By increasing ϕ to 24–30°, the formation of twins is effectively suppressed in regions of the epilayer further than about 2 μm from the interface. In the most recently grown samples, the twinning is localized to within about 0.5 μm above the interface.

Influence of Growth Temperature on Twin Formation

The preceding results on twin suppression related to substrate tilt assume that an optimized growth sequence has been established. To determine the appropriate growth temperature, a series of six CdTe layers were grown on identical 3 inch, doped, misoriented Si (001) substrates (θ = 1.5° and ϕ = 30°). The temperature sequence was different for each sample, while all other growth parameters were unchanged. The CdTe layers were evaluated by DCRC, and all were found to exhibit single domains. The sample grown with the previously cited growth sequence (210/2 min; 250/10 min; 310/16 h) was twin-free. As the growth temperatures were raised the twin content increased. Using a growth sequence of (250/2 min; 290/10 min; 340/16 h) resulted in a completely twinned layer.

CdTe (111)B Layer Quality

Figure 2 records some of the lowest DCRC FWHM we have measured for CdTe (111) B on Si of various epilayer thicknesses. The thickness dependence of the FWHM can be analyzed on the basis of the TEM images of the interface and the effect of x-ray penetration depth on DCRC results. Defect densities are always high near the interface but tend to dissipate as the layer grows. Thus, their overall effect is reduced in thicker layers. The 17 μm layer exhibited the lowest FWHM of 60 arc sec. The 1° samples and the 4° samples had somewhat different oxide removal processes. The 4° samples experienced a slower heating process, but all samples are single domain and twin-free. The discrepancy between the 1 and 4° samples is currently under investigation.

Dislocation densities are a crucial characteristic of CdTe epilayers intended for use as substrates for HgCdTe growth, since dislocations propagate into the MCT and significantly degrade device performance. No direct etch pit density (EPD) counts of these CdTe epilayers have been performed. However, some CdTe (111)B/Si (001) layers have been used as substrates for both liquid phase epitaxial (LPE) and MBE growth of MCT,[8] and EPD counts were taken on the MCT. MBE grown MCT showed typical EPD values of 3×10^7 cm^{-2} and a best value of 4.3×10^6. LPE grown MCT epilayers exhibited EPDs as low as 5×10^5 cm^{-2}, which is comparable to the best reported values for MCT grown on CdTe/GaAs/Si.

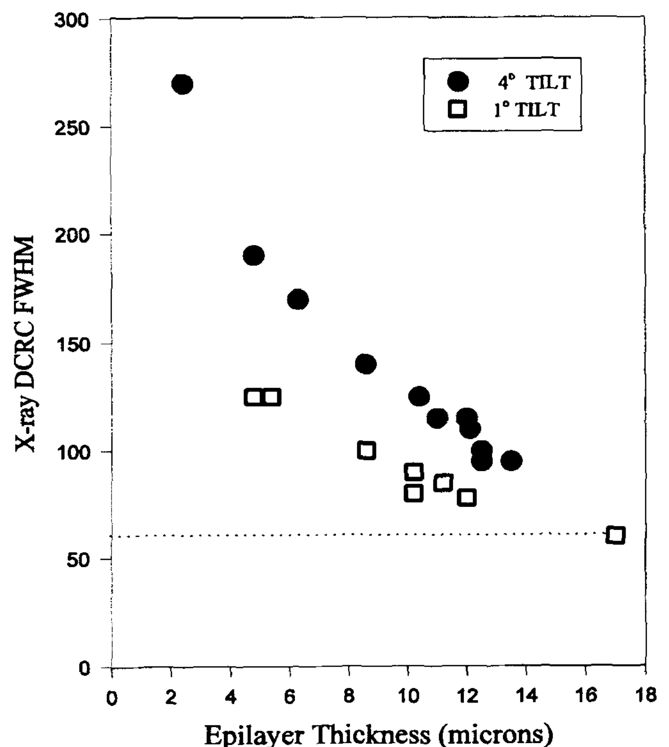

Fig. 2. Highest quality CdTe (111)B layers grown on Si(001) with θ =1 °, ϕ = 30° ( ) and θ = 4°, ϕ = 28° (●). All layers were single domain and twin-free.

Influence of Precursors

In order to improve the nucleation process several precursors, including As, Te, and ZnTe, have been used prior to CdTe growth. All samples indicated in Fig. 2 were grown using a high temperature As predeposition and a lower temperature Te predeposition as described above. Our results show that predeposition of Te is essential for the growth of high quality single crystal CdTe (111)B. Layers grown without Te deposit have exhibited nonspecular surface morphology and very broad DCRCs, indicative of CdTe (111)A or a mixed A-B phase. Similar dependence of the use of Te predeposition and CdTe polarity has been reported by Sugiyama and Nishijima.[9] Their results are consistent with our observations despite differences in experimental details. For example, in their experiment Te exposure occurs at constant substrate temperature, while our predeposit occurs while the substrate cools from the oxide desorption temperature toward the growth temperature. Additionally, we use CdTe as a predeposition source of Te. This dictates our low temperature limit to the predeposit (~350°C) since we wish to avoid the initiation of CdTe growth during the cooling process, when the substrate temperature is unstable. The predeposition initiation temperature has no upper limit. Layers grown with CdTe flux initiated shortly after oxide removal (~800°C) exhibit specular surface morphologies, and narrow DCRCs, indicative of B-face growth. We have not systematically established the low temperature limit for predeposition initialization.

The deposition of As shortly after oxide removal seems to improve the interface stability. High temperature oxide removal causes outgassing of chamber walls, which in turn introduces damaging contaminants (i.e., carbon, oxygen) to the active Si surface. Arsenic tends to passivate the active Si surface. During TEM sample preparation, it was found that CdTe layers grown on Si without As predeposition tended to peel off the substrate whereas those with As did not. This weak adhesion of the epilayer was further confirmed by temperature cycling experiments on thick CdTe/Si. A 25 μm CdTe epilayer grown on a doped, $\theta = 1.5°$, Si substrate was cycled rapidly five times from room temperature to 77K by dipping into liquid nitrogen. Layers grown without As predeposition peeled off or cracked, whereas layers with As predeposition exhibited no observable cracking or peeling.

As reported earlier,[1] experiments with ZnTe as a buffer layer show that it maintains the crystallographic orientation of the substrate. We have grown CdTe (001)/Si (001) and CdTe (211) B/Si (211) by depositing a thin ZnTe interfacial layer.

CONCLUSIONS

We can routinely grow single domain, twin-free CdTe(111)B heteroepitaxial layers on misoriented Si (001) substrates. TEM images of these layers generally reveal sharp interfaces, characteristic of coherent growth. These images and x-ray DCRC analysis have been used to systematically investigate the role of substrate misorientation in epilayer quality. The tilt parameter θ is important for the formation of single domain epilayers and the tilt parameter ϕ is related to the formation of lamellar twin defects. Temperatures used during the different steps of the growth process are very important parameters for defect suppression. High growth temperatures cause high densities of twinning defects and overall poor quality epilayers. Under optimized growth and tilt parameters ($\theta = 1°$ and $\phi = 30°$), DCRC FWHM of less than 100 arc sec can be routinely grown. The best layer has a FWHM of 60 arc sec. The use of precursors such as As, Te, and/or ZnTe helps in stabilizing the heterointerface and/or the crystallographic orientation.

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