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THE INFLUENCE OF SILICON HEAT TREATMENTS ON THE MINORITY CARRIER GENERATION AND THE DIELECTRIC BREAKDOWN IN MOS STRUCTURES

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The minority carrier lifetime of Si and the dielectric breakdown of SiO_2 on Si has been investigated as a function of various high temperature treatments preceding the formation of the SiO_2 layer.

Annealing wafers in H_2 or certain H_2-containing ambients prior to oxidation led to a dramatic decrease in the number of breakdown defects found in capacitors. The higher the temperature the more effective is the defect removal. Using this process the defect density could be reproducibly controlled at ≤ 10 defects/cm^2, and in some cases wafers with no defects were found. The defects appear to be related to some airborn contamination and can be increased by exposure to air and to certain aqueous cleaning steps.

By "soaking" the Si wafers in an equilibrium gas mixture containing SiH_4 as well as HCl, it was possible to prevent etching of the Si but yet expose the wafer to approximately 4% HCl for longer times and at higher temperatures, 1275°C, than is possible with the well known HCl-oxidation process. It was found that this treatment will remove Au, Fe, and Cu from intentionally contaminated wafers but at rates much slower than would be expected from bulk-diffusion, rate-limited transport. Soaking at 1275°C led to minority carrier

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lifetimes comparable but not significantly better than for HCl-oxidized wafers.

Key words: silicon wafer cleaning, dielectric breakdown, minority carrier generation.

Introduction

The fabrication of highly reliable MOSFET devices places several requirements on the quality of the starting silicon wafers. One of these exigencies is that the silicon dioxide that is thermally grown on silicon must have uniformly high dielectric breakdown strength to insure gate oxide integrity. Furthermore, the minority carrier generation rate in the silicon must be minimized to reduce diode leakage and to increase charge storage times in dynamic devices; thus generation-recombination centers such as copper, gold, and iron must be removed from the Si. The present study shows that both these objectives can be partially attained, by suitable high temperature treatments of silicon wafers before device fabrication *per se* is initiated.

Although low dielectric strength of SiO_2 has been attributed in part to defects in the oxide or at the silicon surface [1-11], the exact nature of these defects has not been elucidated. Many sources of defects have been observed or postulated: silicon crystalline imperfections, impurities that were not removed or even deposited by wafer cleaning [4], particulate matter on the wafer or in the oxidation ambient, impurities on the wafer or in the ambient that are removed by anhydrous hydrogen chloride (HCl)[4,5], oxide pinholes that can be filled with a second layer such as phosphosilicate glass (PSG) [2,6], partial devitrification of the oxide [2,6-8], unannealed interface states [4], and electrode reacted with the oxide [2,4,9]. In addition, mobile impurities [10-12] and localized interface states [9] were proposed as "defects" responsible for time-dependent dielectric breakdown. The numerous models suggest that in actual practice several types of defects may be present; depending upon processing conditions certain types may variably be dominant while others are nonexistent. Processing improvements may eliminate the major defect contributor, but still not yield devices totally without defects. For instance oxidation of silicon in the presence of HCl [5]

or the addition of a second PSG layer [4] are two techniques to reduce the defect density significantly, yet neither has resulted in wafers with less than 5-10 defects/cm^2 under the most favorable conditions. Some of the treatments to be described in this paper were successful in achieving even lower defect densities (reproducibility $\leq$10 defects/cm^2) with standard processing after the initial treatment, and on occasion samples with zero defects/cm^2 were obtained; indeed, these treatments provide the best breakdown properties reported to date.

Anomalously high minority carrier generation rates (or low minority carrier lifetimes) have generally been attributed to impurities and have been reduced by several procedures including: removal of damaged or contaminated surface layers by silicon etching [13] or cleaning, elimination of Si microsplits [14], cleaning the oxidation tube with HCl, and oxidation or annealing in a chlorine containing ambient [15-17]. The improvement in lifetime attributed to the HCl oxidation process is very large (10-100x), but has always been variable from lot-to-lot of starting wafers; presumeably this is because of variations of impurity content in the wafers and possibly because of incomplete removal of the impurities by the HCl oxidation. The extension of this process to longer times, higher temperatures, and HCl concentrations has been limited by the desired oxide thickness or by substrate attack. This paper reports the extraction of heavy metals at high concentrations in intentionally contaminated Si and indicates that the extraction is very much slower than would be expected from diffusion rate limited processes. This paper also discusses the use of so called "equilibrium mixtures" of $HCl/SiH_4/H_2$ which enables the HCl treatments to be carried out for longer times and at higher temperatures. This "soak" mixture was employed in anticipation of improving minority carrier lifetime; however, as will be discussed below, defective breakdown benefits were more significant than lifetime increases. This breakdown improvement was subsequently attributed to the presence of hydrogen.

Experimental

The starting substrates were Czochralski-grown, (100)-oriented, 1-1/4-inch diameter silicon wafers which were

chem-mechanically polished on one side and etched on the reverse side to remove saw damage. Both P and N-type wafers from several vendors were tested. In this work, wafers were usually cleaned in solutions of NH_4OH-H_2O_2, HCl-H_2O_2, HF and finally DI water [18]. The peroxide solutions were ultrasonically agitated at 60-70°C. After the final DI water rinse (to 18 MΩ-cm) the wafers were blown dry in filtered (0.45μm) nitrogen.

The pre-oxidation heat-treatments were effected in a relatively standard epitaxial reaction chamber (60cm long by 6cm diameter) which was fabricated from fused silica. The wafers were supported horizontally by a silicon-carbide coated graphite susceptor which was heated by r-f induction. The hydrogen was purified by passing the gas through a palladium-silver membrane. Helium was purified by passing it over a titanium bed held at ∿800°C, and nitrogen was purified by passing it over a magnesium bed at ∿500°C. Typically the total flow through the chamber was with a gas stream velocity of ∿6 cm/sec referenced to room temperature. The temperature was measured using a disappearing filament optical pyrometer which was calibrated at the melting points of germanium, copper, and silicon.

The samples were heat treated in one of the following gaseous ambients as the experiment required: pure hydrogen or helium, forming gas (20% purified hydrogen in purified nitrogen), or ∿5% anhydrous hydrogen chloride in pure hydrogen. Alternatively the wafers were "soaked" at elevated temperatures in a near "equilibrium mixture" of silane, anhydrous hydrogen chloride, and hydrogen (such that silicon neither deposits nor is etched and where the vapor phase chloride concentration is ∿4%). This last "equilibrium mixture", which was shown to exist thermodynamically by Lever [19] and by Hunt and Sirtl [20], was determined experimentally for the temperatures 1000 and 1275°C using the following procedure: First, in order to approximate the correct silane concentration, clean sapphire wafers were loaded into the chamber and brought to temperature in the presence of 5% HCl/H_2. Then the silane flow rate was increased very slowly until there was a change in the wafers' optical emissivity which indicated the deposition of a silicon film. Next the silane flow rate was slowly reduced until the silicon film disappeared. Finally, silicon wafers were processed in this composition range, and material loss or gain was determined gravimetrically in a

balance sensitive to one microgram. The composition of the "equilibrium mixtures" used for the high temperature heat treatments (soaks) were chosen so as to remove ∿2μm Si in 30 min. These compositions were approximately 0.6% SiH_4, 4% HCl, 11% He, balance H_2 for 1275°C and 0.7% SiH_4, 4% HCl, 14% He, balance H_2 for 1000°C. The helium functioned only as a cylinder diluent for the silane. In some cases phosphine was added to the mixture to prevent phosphorus out-diffusion and hence to control the silicon dopant concentration.

After the high temperature treatment, silicon dioxide films (∿400Å) were thermally grown on the silicon using either a standard dry oxygen process at 1000°C for 33 min or a 3% HCl in oxygen mixture for 21 min. After oxidation an array of one hundred aluminum capacitor dots (32 or 50 mil diam) was electron-beam evaporated and the resulting MOS capacitors were annealed 5 min in N_2 to remove interface states.

Dielectric breakdown was measured by applying a ramp voltage to each capacitor and noting the voltage of the first breakdown event without regard as to whether it was shorting or non-shorting (self-healing). The defect density, ρ, was calculated using the following relationship: [1-3]

$$- \ln P = \rho A,$$

where A is the capacitor area and P is the experimentally determined probability of the capacitor's breaking down within some defined high-field breakdown range. For this work, the high-field breakdown range was defined to be between 0.8 x E_{max} and 1.0 x E_{max}. (E_{max} is the maximum dielectric strength of SiO_2 and varies with oxide thickness, substrate doping, temperature, and ramp rate.) Typically two-hundred, fifty-mil-diameter capacitors were measured to determine P.

Minority carrier generation was measured on fifty MOS capacitors as described in earlier work [17]. Each MOS capacitor was pulsed into deep depletion, and the time required to reach a steady-state inversion capacitance was measured. In the absence of surface generation, this relaxation time has been shown [21] to be proportional to minority carrier lifetime.

In order to understand more fully the gettering effect of HCl treatments, a series of wafers was intentionally

contaminated with about 100 PPM of Fe, Au, Cu or a combination of all three. The contamination was introduced by evaporating a thin layer of metal and then diffusing the metal in at 1275°C for one half hour. The various heat treatments were then performed. For analysis, the wafers were subsequently powdered and the average impurity concentrations were determined by Optical Emission Spectroscopy.

Results and Discussions

Dielectric Breakdown. The high temperature heat treatments were found to have a most pronounced and in some cases a most beneficial influence on dielectric breakdown distributions of oxides that were thermally grown after treatment without any intervening cleaning step. Figure 1 shows such distributions for untreated (control) wafers, wafers that were soaked for 1/2 h at 1275°C and cleaned prior to oxidation, and wafers that were oxidized immediately after a soak

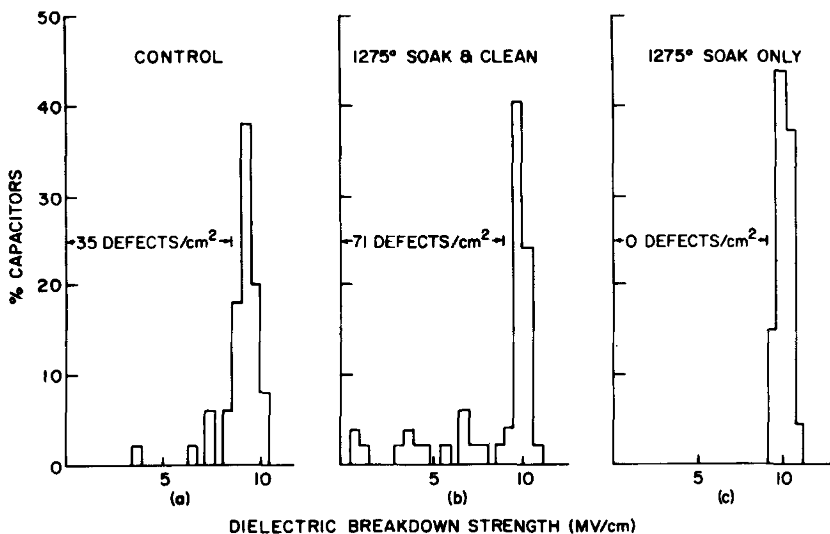

Fig. 1. Dielectric breakdown distributions of 32 mil diam., 400Å SiO_2 capacitors: a) control, b) after 1/2 h 1275°C soak in 4% $HCl/SiH_4/H_2$ followed by standard cleaning prior to oxidation, c) after 1/2 h 1275°C soak in 4% $HCl/SiH_4/H_2$ followed immediately by oxidation.

Table I. Effect of Silicon Heat Treatment on Defect-Related Dielectric Breakdown of SiO_2

Treatment	Per Cent Defective Capacitors*
Control	59
1/2 h H_2 @ 1275°C	12.5
1/2 h He @ 1275°C	100
1/2 h 20% H_2 + 80% N_2 @ 1275°C	wafer corroded
1/2 h soak @ 1275°C	11.8
1/2 h soak @ 1275°C + clean	94.4
1 min HCl etch @ 1275°C	68.5
1 min HCl etch @ 1275°C + clean	100

* 50 mil diam.

for 1/2 h, at 1275°C. If the criterion established earlier to compute defect density, ρ, is used, the soaked wafers had zero defect/cm^2 compared to 35/cm^2 and 71/cm^2 for the control and the soaked plus cleaned wafers respectively.

Wafers were treated in ambients other than $HCl/SiH_4/H_2$, and the results are summarized in Table I. In this series, the control with 59% defective capacitors had 73 defects/cm^2 while wafers heated 1/2 h in either H_2 or soaked in $HCl/SiH_4/H_2$ had 12% defective capacitors or 10 defects/cm^2. What is interesting is that the hydrogen and not the HCl plus SiH_4 is responsible for the improvement. Revesz [22,29] earlier used hydrogen treatments to remove any native oxide on Si. Helium annealing was shown to be actually detrimental even though it was pure enough to allow removal of any residual silicon dioxide from the wafer. At 1275°C forming gas (20% H_2 + 80% N_2) severely attacked the wafers. Nitrogen annealing alone left a non-uniform film on the silicon that could not be removed by hydrogen at 1275°C (possibly Si_3N_4); the use of nitrogen purified with a hot magnesium bed resulted in a more uniform film. Yet the combination of hydrogen and nitrogen was considerably more corrosive than nitrogen alone. Etching wafers in HCl/H_2 to remove 2.4μm did not result in better breakdown properties.

In all cases wafers that were recleaned between heat treatment and oxidation gave no better than average properties; in fact they were often poorer than control samples. It

Table II. Effect of Deionized Water Rinsing on Recontaminating Treated Wafers

Treatment	Defect Density ($/cm^2$)
Control	200
1/2 h 1275°C H_2	30
1/2 h 1275°C H_2 + 5 min DI	88
1/2 h 1275°C H_2 + 5 min DI + 1/2 h 1275°C H_2	16
1/2 h 1275°C H_2 + 5 min DI + 1/2 h 1275°C H_2 + 5 min DI	88

was determined that a short rinse in deionized water (>18 MΩ-cm) followed by drying in high-purity, filtered nitrogen was sufficient to recontaminate the wafer; this result is demonstrated in Table II. Here the control defect density ($200/cm^2$) was higher than normal possibly because of higher than usual contamination on the starting wafer lot; nevertheless the ratio of defect densities of the 1275°C treated wafers to the controls was 0.15, the same as for the lot of wafers shown in Table I. A five minute DI water rinse was detrimental, a second H_2 treatment restored the superior properties; and another DI rinse degraded the wafers again. Additional experiments demonstrated that wafer drying in filtered (0.45µm) nitrogen rather than the DI rinse was a primary source of this contamination. Wafers that were cleaned without being blown dry had considerably lower (one-half) defect densities than dried wafers.

The deterioration of breakdown properties was also observed to occur while the wafers were stored in a Class-100 clean hood as well when they were rinsed in DI water and blown dry in filtered nitrogen. The defect density increased with the length of wafer storage in air. (See Fig. 2.) Thus it appears that airborn particulate matter has a high affinity for freshly exposed silicon and promotes defects in subsequently grown oxides. To achieve the optimum breakdown properties, very high hydrogen annealing temperatures were required as seen in Fig. 3. A slight improvement could be discerned with 600°C annealing but 1200°C or higher was necessary to achieve a 4x reduction in the defect density. However, it should be pointed out that oxidation of untreated wafers in HCl at 1000°C would also reduce the defect level by ∿4x [5].

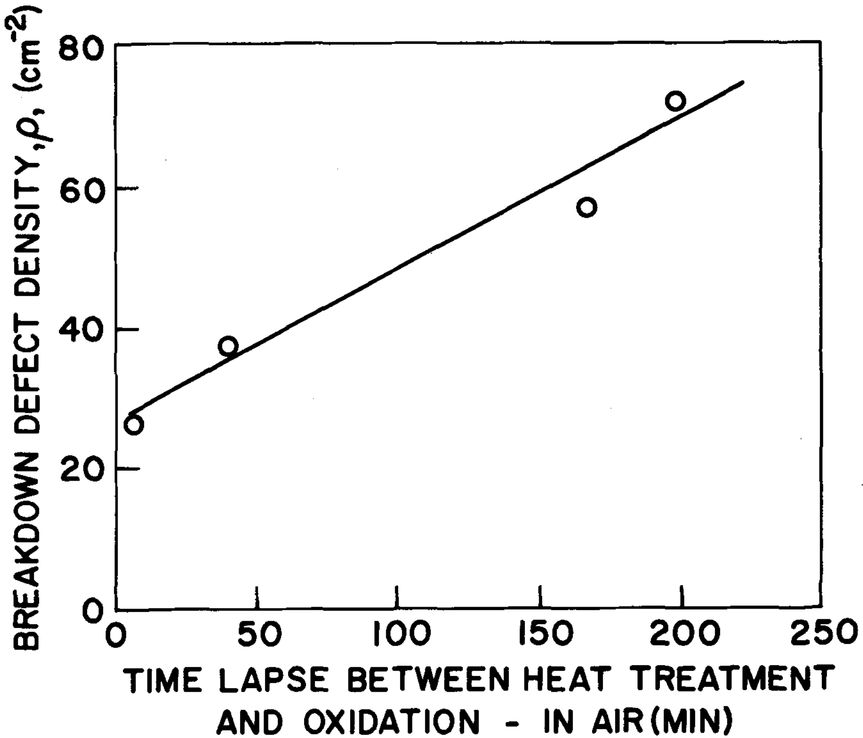

Fig. 2. Increase in the breakdown defect density, ρ, as a function of the wafer storage time in filtered (0.5μm) air.

Because of the recontamination effect, it was not possible to determine the 1275°C annealing time needed to remove all defects. With wafers from one vendor, three minutes or less at 1275°C appeared to be adequate; whereas, Table II shows, with wafers from another vendor, a second 1/2 h anneal was helpful.

Auger spectra, Fig. 4, were taken on annealed and unannealed wafers to determine what contaminants are present and which ones are removed by the treatments. A Physical Electronics Auger spectrometer having oil-free pumping was operated at 2kV primary electron beam at 30μA with a 5V modulating signal. In all samples spatial non-uniformities could not be detected with the one-millimeter diameter Auger beam.

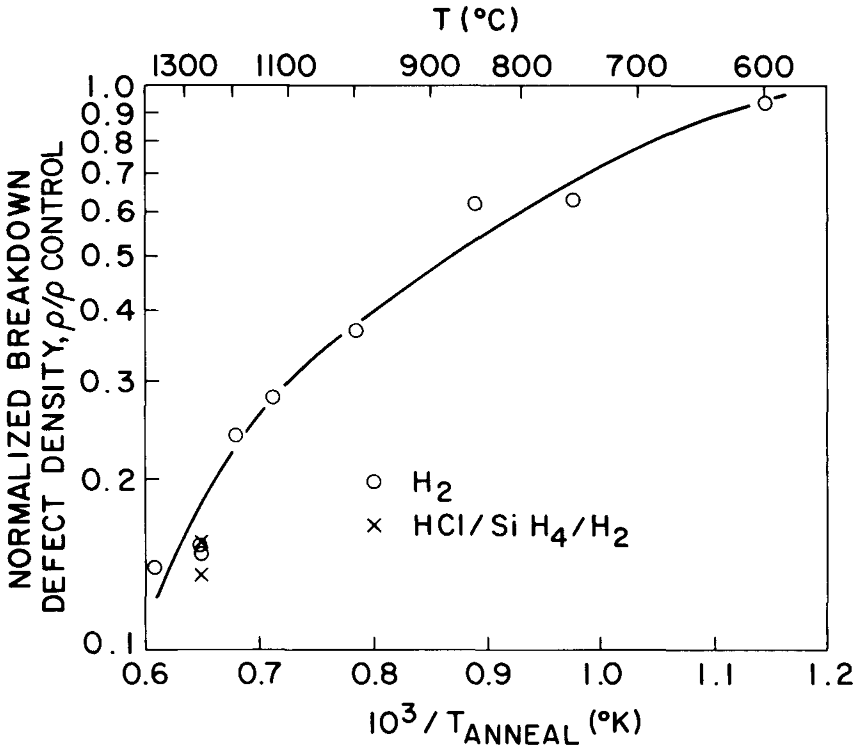

Fig. 3. Temperature dependence of the defect density of annealed wafers (1/2 h) normalized to the defect density of control wafers (ρ/ρ control).

The as-received wafer after a five minute DI rinse, (a), had a large oxygen and a large bonded silicon peak as expected with a native oxide; otherwise, carbon was the only detected impurity. Cleaning the sample, (b), reduced the oxygen peaks but actually left a larger carbon contamination. The 1275°C H_2 anneal (c) and (d) somewhat reduced the carbon level. This carbon reduction was also reported in other studies of high temperature vacuum or H_2 annealing [24,25]. It should be noted that one of these studies [24] found an increase in heavy metal contamination after high temperature heat treatments; hence, it may be possible to have capacitors that have excellent breakdown properties but poor lifetime.

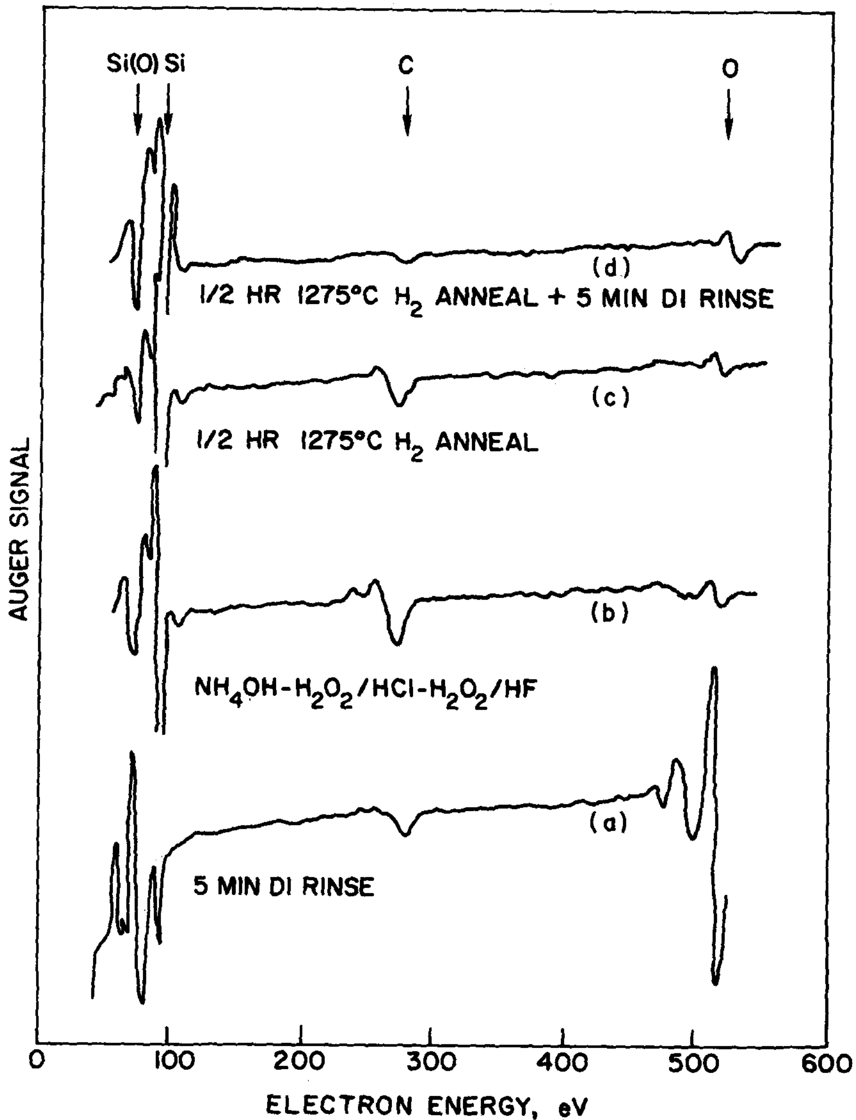

Fig. 4. Auger spectra of silicon wafers: (a) rinsed in DI water after receiving, (b) cleaned in NH_4OH-H_2O_2/HCl-H_2O_2/HF and rinsed in DI water, (c) annealed at 1275°C in H_2 for 1/2 h, and (d) annealed at 1275°C in H_2 for 1/2 h followed by 5 min. DI rinse.

The larger carbon signal of sample (c) is probably due to the fact that it was recontaminated while stored in air while sample (d) was merely rinsed. It is not believed that the rinse (d) was effective in removing carbon.

The Auger measured reduction in carbon after hydrogen annealing does not correlate with defect removal. It has been reported [25] that hydrogen annealing can remove small SiC crystallites on Si. The hydrogen at 1275°C could easily reduce free carbon to volatile hydrocarbon. In order to test the hypothesis that breakdown defects are due to such SiC crystallites, Auger and breakdown results were compared using identical processing for each test. Wafers with the lowest carbon level, (d), had the highest defect density; wafers with moderate levels, (c), had the lowest defect density; and wafers having either low (d) or high (b) carbon levels had nearly equal defect densities. This complete lack of correlation suggests that C and SiC are not primarily responsible for breakdown defects. In addition no relationship between carbon and either oxide charge or interface state density could be discerned.

Minority Carrier Lifetime. The influence of different silicon heat treatments on the average pulsed capacitance relaxation time (lifetime) is summarized in Table III. With the wafers tested, oxidation in 3% HCl/97% O_2 at 1000°C gave a ten-fold increase in relaxation time, while a 1/2 h soak in 4% $HCl/SiH_4/H_2$ at 1275°C gave a five-fold improvement. Etching the wafers *in situ* after the soak (2.4μm removed) did not further enhance the lifetime. Surprisingly, recleaning the wafers after soak but before oxidation substantially reduced the relaxation time apparently because of contamination introduced during cleaning. It was also noted that HCl oxidation following HCl soaking was not as beneficial as HCl oxidation alone, but in all cases HCl oxidation was superior to standard oxidation without HCl.

The experiments with phosphine added to the soak mixture and those with a post etch in 5%HCl/H_2 were designed to counter the loss of phosphorus from the wafer surface. This dopant leaching would be analagous to the impurity leaching but with the difference that the diffusion rate of phosphorus is several orders of magnitude lower than that of the metals of concern. Indeed MOS capacitance measurements did show some evidence of a light phosphorus depletion in wafers

Table III. Effect of Silicon Heat Treatment on Pulsed Capacitance Relaxation Times

Treatment	Oxidation Ambient	Relaxation Time (sec)
Control	O_2	6.2
Control	3%/HCl/97% O_2	65
1/2 h soak @ 1275°C	O_2	30
1/2 h soak @ 1275°C	3%/HCl/97% O_2	35
1/2 h soak @ 1276°C + clean	O_2	12
1/2 h soak @ 1275°C + clean	3%/HCl/97% O_2	27
1/2 h soak @ 1000°C + clean	O_2	16
1/2 h soak @ 1275°C + etch	O_2	20
1/2 h soak @ 1275°C + etch + clean	O_2	12

soaked at 1275°C without phosphine added. No evidence was seen of boron depletion from p-type silicon.

It is interesting now to consider the gettering effect of these treatments on the intentionally contaminated wafers. These wafers initially had an intentionally high level (∿100 ppm) of Fe, Cu and/or Au contamination. Figures 5-7 show the Fe, Au, and Cu concentrations, respectively, as a function of heat treatment time. At 1000°C, neither a 5% HCl oxidation nor a 4% $HCl/SiH_4/H_2$ soak removed Fe or Au, and 20-100 minutes was needed to reduce the average Cu level by a factor of ten. At 1275°C the concentrations of these impurities were substantially reduced by the soak with Cu being gettered most rapidly. A very pronounced cooperative effect is also seen in Figs 5-7 the removal of each impurity is retarded by the presence of the other impurities.

The above data contrast sharply with expectations based on theoretical calculations: If it is assumed that the metal impurities are distributed homogeneously throughout the silicon wafer and that during gettering there is a perfect sink at the surface and that the rate limiting process is diffusion through the bulk, then the concentration of copper midway through the wafer after a 30 min soak at 1275°C should

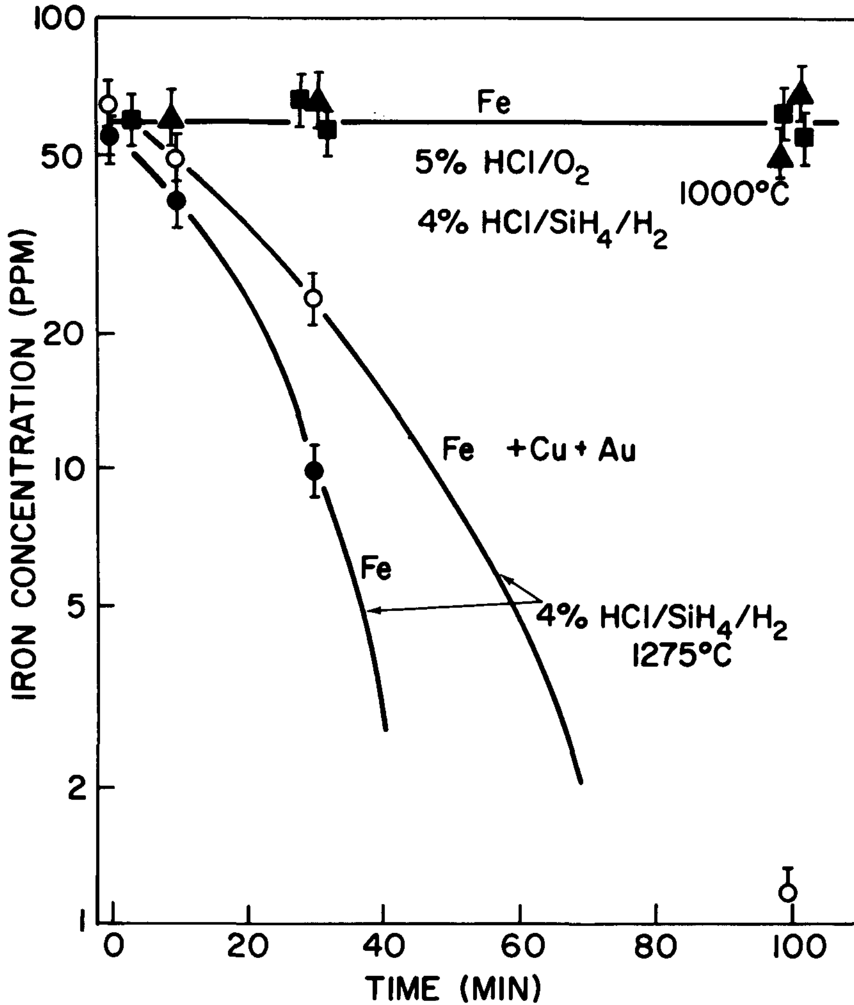

Fig. 5. Reduction of average Fe level or a function of time by different HCl treatments. (solid symbols - wafers contaiminated with Fe only; open symbols - contaminated with Fe + Au + Cu)

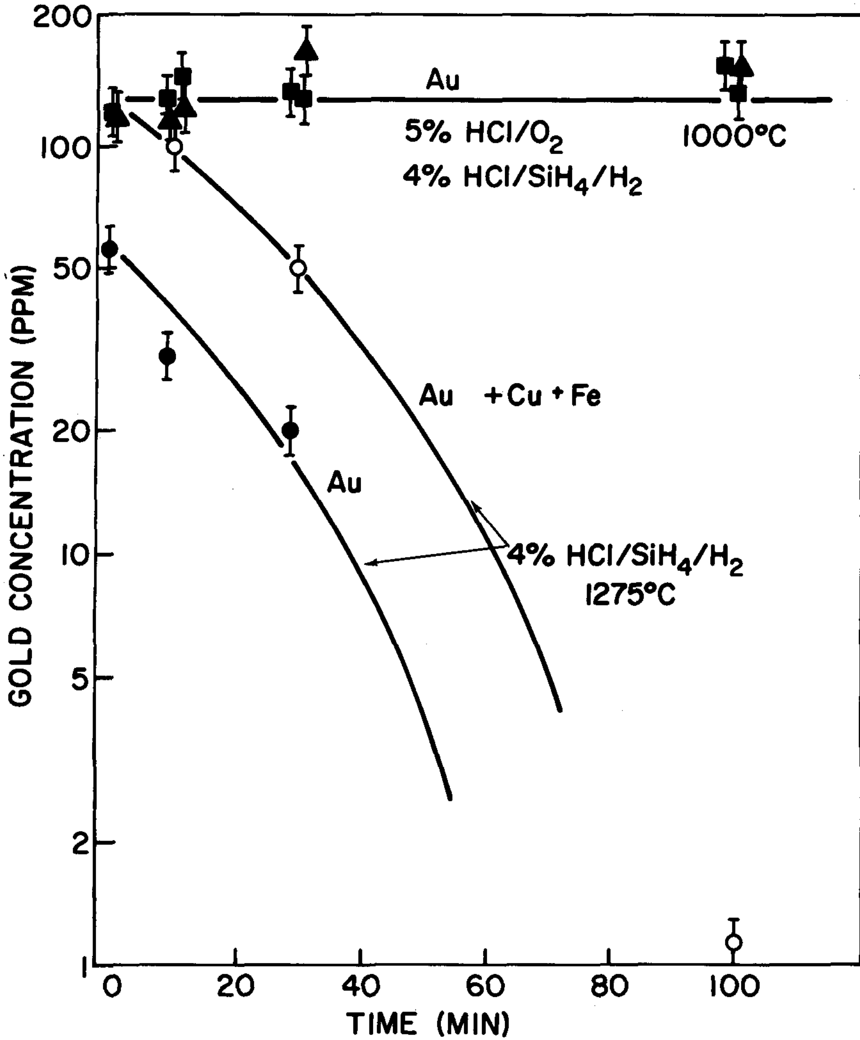

Fig. 6. Reduction of average Au level as a function of time by different HCl treatments. (solid symbols - wafers contaminated with Au only; open symbols - contaminated with Fe + Au + Cu)

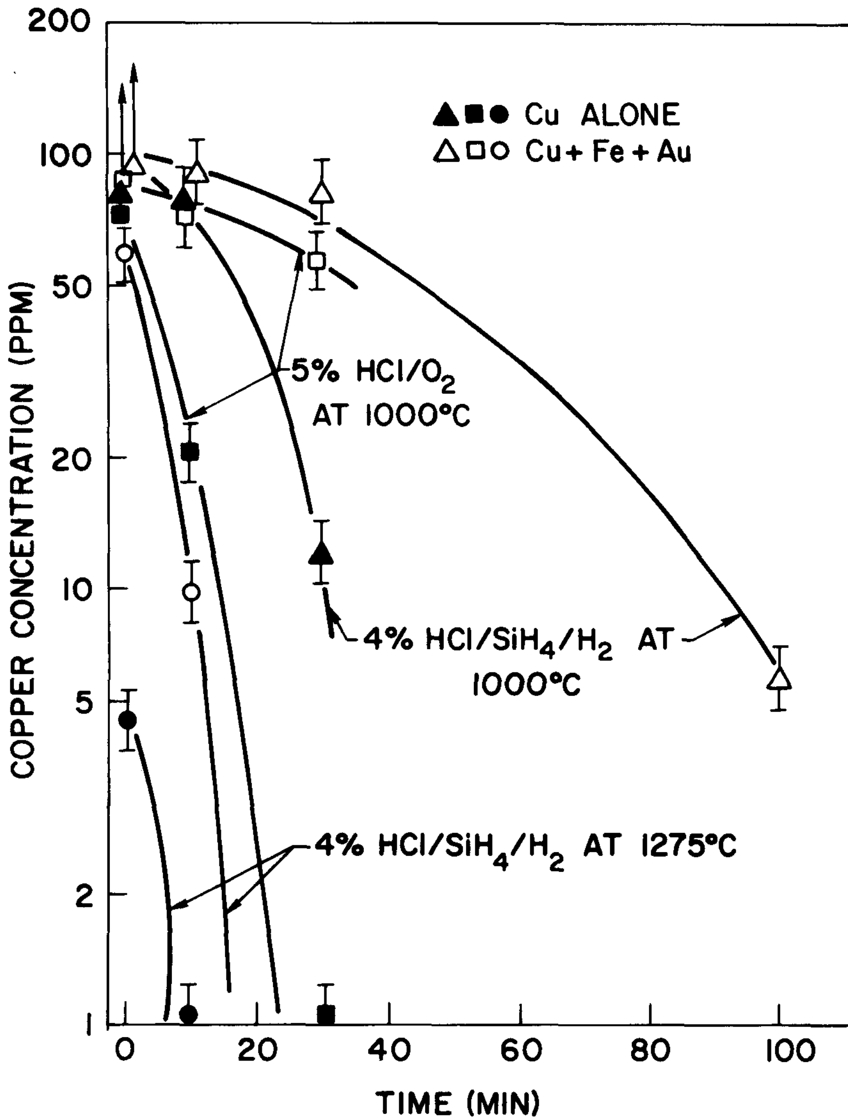

Fig. 7. Reduction of average Cu level as a function of time by different HCl treatments. (solid symbols - wafers contaminated with Cu only; open symbols - contaminated with Fe + Au + Cu)

be down by ∿2220 orders of magnitude and that of iron by ∿109 orders! At 1000°C the corresponding ratios are 110 for copper and 27 for iron. These calculations are based on Ficks laws [26] and the following diffusion data: for copper [27] ΔH=9.9 kcal/mole and D_o=0.0047 cm^2/sec, for iron [18] ΔH=20 kcal/mole and D_o=0.0062 cm^2/sec (valid in the ranges of 400-1000°C for Cu and 900-1300°C for Fe). For the purpose of this calculation the wafer thickness was taken to be 10 mils.

The gettering efficiency of these impurities is obviously far from the theoretical prediction, which would indicate a faulty assumption. The vapor pressure of both copper and iron chlorides at 1275°C is well over 100 mm Hg, and the surface reaction rate and evaporation rates of the halide reaction products are believed to be rapid so it is not expected that surface processes would be rate limiting. Rather it would seem that the heavy metals may be associated with crystalline defects of one kind or another and hence the rate limiting process may be the release of the metal from the defect or from a precipitate.

It is well known that copper is often precipitated at lattice faults or in copper-oxygen complexes. [27,29,30] The high impurity concentrations (up to 100 ppm) used in this work virtually insured that the impurities were precipitated as would be expected in actual device structures rather than uniformly dispersed at low concentrations. Earlier work [27,30] noteably on copper revealed that phosphorus gettering from precipitates is indeed slower than anticipated. Even though phosphorus and HCl gettering may occur via different mechanisms, it appears that it is more difficult to getter impurities which are precipitated.

Careful attention was paid to the influence of these high temperature heat treatments on the crystallographic perfection of the silicon wafers. Sirtl etching of moderate dislocation density Czochralski Si (∿1000 d/cm^2) showed that the dislocation density need not increase as a result of a 1275°C annealing. Some evidence could be seen for a slight reduction, as previously noted [31], of Sirtl etch pit density on the back surface of the wafer as a result of annealing; other work has shown much of this back surface damage was shallow. Faceting of the back obscurred more careful comparisons. Unfortunately, however, slip lines were almost

always generated by such a treatment; although the slip could not be completely eliminated, it could be minimized by starting with selected lots of wafers. As reported earlier, slip generation was most pronounced from the wafer flat or pheriphery. Wafers soaked in $HCl/SiH_4/H_2$ often became more brittle. The rapid diffusion of H_2 in silicon [32] should allow the wafer to become saturated rapidly; the dissolved hydrogen probably enhanced the brittleness as it does in other metals [33].

Summary

Silicon wafers were annealed at high temperatures ($\geq$1000°C) in different ambients in order to reduce both the density of defects responsible for low-field dielectric breakdown in SiO_2 and the generation rate of minority carriers in Si. High temperature annealing in the presence of hydrogen resulted in a dramatic decrease in the dielectric breakdown defect density. For instance, the defect density of wafers annealed at 1275°C is about one-seventh that of unannealed wafers. The improvement is very sensitive to the annealing temperature; to achieve a 4x reduction in defects, temperatures over 1200°C must be used. Such a defect reduction is typically attained with an HCl oxidation. Above 1200°C, the hydrogen anneal is superior to an HCl oxidation.

The improvement in breakdown characteristics resulting from high temperature hydrogen annealing was attributed to removal of surface contamination. If annealed wafers were exposed to filtered room air for a period of time prior to oxidation, the defect density increased. In fact, annealed wafers that were merely rinsed in DI water and blown dry in filtered N_2 were no better than unannealed ones. The evidence suggested that particulate matter was a substantial source of breakdown defects.

Mixtures of $HCl/SiH_4/H_2$ which were in equilibrium with respect to Si etching or deposition were employed to provide an HCl ambient to getter impurities responsible for generation-recombination currents. Such a treatment using 4% HCl at 1275°C reduced the minority carrier generation rate by a factor of 5; improvements this substantial could also be achieved with HCl oxidation at 1000°C.

Wafers contaminated with Fe, Au, or Cu were partially gettered with HCl at 1000°C and at 1275°C. At 1000°C only Cu was removed while all three impurities were gettered at 1275°C. Impurity removal was hindered by the presence of a combination of all three species compared to removal when only one species was present and was considerably less than predicted by bulk diffusion constants.

Acknowledgments

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