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High Resolution CMOS Current Comparators: Design and Applications to Current-Mode Function Generation

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Abstract. This paper uses fundamental models to derive design conditions for maximum speed and resolution in CMOS transimpedance comparators. We distinguish two basic comparator architectures depending on whether the input sensing node is resistive or capacitive, and show that each type yields advantages for different ranges of input current. Then, we introduce a class of current comparator structures which use nonlinear sensing and/or feedback to combine the advantages of capacitive-input and resistive-input architectures. Two members of this class are presented demonstrating resolution levels (measured on silicon prototypes) in the range of pAs. They exhibit complementary functional features: one, the current steering comparator, displays better transient response in the very comparison function, while operation of the other, the current switch comparator, is easily extended to support systematic generation of nonlinear transfer functions in current domain. The paper explores also this latter extension, and presents current-mode circuit blocks for systematic generation of nonlinear functions based on piecewise-linear (PWL) approximation. Proposals made in the paper are demonstrated via CMOS prototypes in two single-poly CMOS n-well technologies: 2 μm and 1.6 μm. These prototypes show measured input current comparison range of 140 dB, resolution and offset below 10 pA, and operation speed two orders of magnitude better than that of conventional resistive-input circuits. Also, measurements from the PWL prototypes show excellent rectification properties (down to a few pAs) and small linearity errors (down to 0.13%).

1. Introduction

Analog current-mode techniques are drawing strong attention today due to their potential application in the design of high-speed mixed-signal processing circuits in low-voltage standard VLSI CMOS technologies. Industrial interest in the field has been propelled by the proposal of innovative ideas for filters [1] and data converter design [2, 3], demonstrated by IC prototypes in the video frequency range [4]. Also current-mode circuits are natural candidates for image sensory information processing using novel neural and fuzzy signal processing architectures [5, 6, 7, 8].

A current comparator is intended to detect the capability of a high impedance node to either source or sink a current. Current sensing and comparison is necessary for different applications. Current comparators are basic building blocks for nonlinear current mode signal processing and analog to digital converters. The availability of large current ranges is an appealing feature for both fields. Also, efficient small current level detection is fundamental for high operation speed in high resolution applications. Low level, high speed current detection is also required in different light and radiation sensing applications: for instance, γ-detectors using wide band gap semiconductors [9], or controllability and reconfigurability issues in E-beam testing of integrated circuits [10]. For instance, in the latter the need arises to detect current levels as low as 1nA in a few μs. Subthreshold CMOS current mode massive computation architectures [5] also require efficient detection of low current levels for fast discriminating function evaluation. To highlight another application, current detection is also required in I_{DDQ} VLSI testing approaches [11].

The most common current comparator structure follows the proposal of Freitas and Current in 1983 [12], where the input current is first sensed at a low-impedance node and then amplified using a single-pole voltage gain mechanism. We will call this architecture the *resistive-input* comparator; it yields proper speed

figures for large current levels, but is somewhat inaccurate. An alternative structure uses a high-impedance node at the sensing front-end—*capacitive-input* comparator. This obtains enlarged resolution, at the cost of increasing voltage excursions at the input node and, consequently, decreasing the operation speed [2]. Recently, an advanced current comparator architecture which uses nonlinear feedback to combine advantages of the capacitive and the resistive input architectures has been proposed quasi-simultaneously by the authors [13, 14] and Traff [15], and demonstrated with CMOS circuits by the authors [14]. However, clear justifications of the merits of the different architectures or criteria for optimum design still lack. This paper aims to provide these justifications and criteria by focusing on the topic of CMOS current comparator design from a fundamental point of view, based on the use of simplified, conceptual models. This fundamentalist development evolves into two practical CMOS circuit structures which obtain resolution and offset of pAs in the comparison function—about three orders of magnitude better than that attained with conventional methods [12]. One of these structures relies on current *switching*, similar to the proposal in [14, 15], and obtains a linear transient evolution dominated by a Miller capacitance. The other, called current *steering* comparator, uses a different principle to reduce Miller effect and thus obtains better transient response (quadratic instead of linear) while preserving the high-resolution feature. However, the former structure is simple to modify to route rectified versions of the input current to a high-impedance output node—this cannot be achieved using the current steering comparator. Consequently, each structure yields specific advantages over the other, depending on the application context. Current steering structure is advantageous for pure comparison, i.e., to codify the sign of the input current in binary form, as is required for analog-to-digital conversion. The other is advantageous for applications where both the sign of the input current and the input current itself are significant to the circuits operation—as in *function generation.*

The paper is organized as follows: Section 2 introduces some basic terminology on current comparators and then analyzes resolution and operation speed of the basic resistive-input and capacitive-input architectures. Section 3 presents the current switching and current steering structures, and outlines extensions for current rectification. The topic of function generation is covered in Section 4, which introduces circuit blocks to support systematic design of *piecewise-linear* (PWL) functions. Finally, Section 5 presents results from practical CMOS circuits.

2. Basic CMOS Current Comparator Architectures

2.1. *Current Comparator Concept and Specification*

The current comparator function is to detect the sign of an input current, to provide an output signal (voltage or current) which codifies this sign in binary form. This paper focuses on *transimpedance* structures. Current transfer structures are obtained by cascading the former with voltage-controlled current switches, which can be built using for instance a differential amplifier.

Figure 1(a) shows the ideal current comparator transfer characteristics for voltage codification. E_{OL} and E_{OH} in this figure denote the boundary values for the output logical states; Figure 1(b) shows the ideal comparator transient response. These figures illustrate the ideal current comparator features: a) *infinite transimpedance* in the transition region; b) *zero offset*; and c) *zero delay*. Also, to reduce loading errors due to finite output resistance of the driving source, the input voltage of an ideal current comparator should be kept constant for the full range of input current. Finally, all these characteristics should hold true for the largest possible input current range.

Practical circuit performance deviates from these ideal features and is characterized by a set of *static* and *dynamic* specification parameters, among which the most significant for design are:

- *offset* (I_{os}), defined as the input current required to annul the output voltage,
- *gain error* (Δ), or static resolution, defined as the input increase needed to drive the output voltage from E_{OL} to E_{OH}; any input level larger than static resolution is called an *overdrive*,
- *resolution time* (T_R), defined as the time required for the output to change from 0 up to E_{OH} (or down to E_{OL}), following the application of an overdrive input step, and
- *response time* (T_D), defined as the time required for the output to change between the two logical states, following an input edge between two opposite-sign overdrive levels.

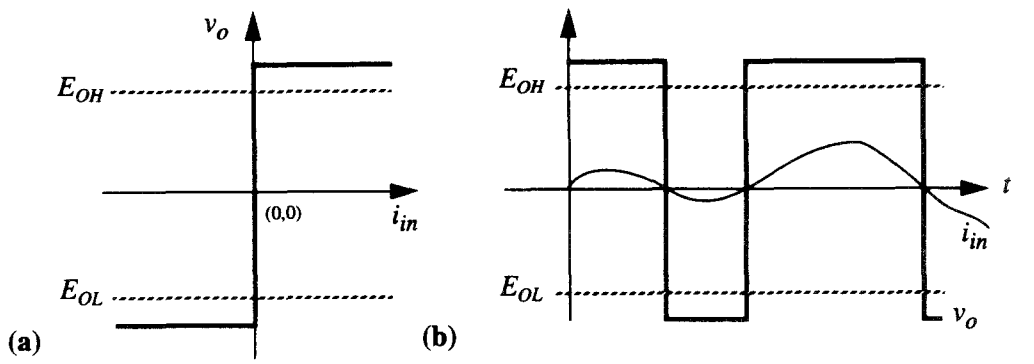

Fig. 1. Ideal current comparator operation: (a) Transfer characteristics; (b) transient response.

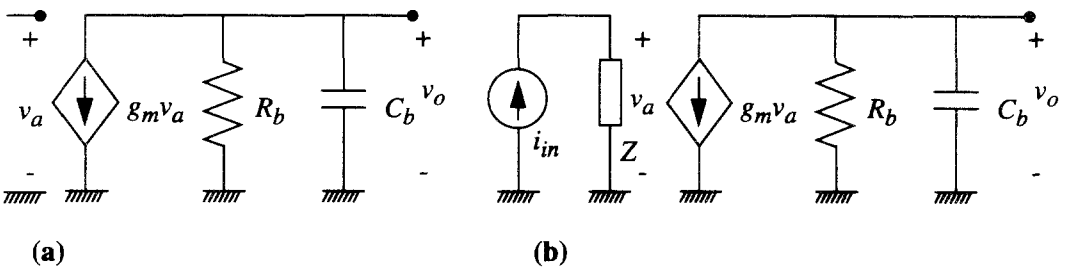

Fig. 2. Basic CMOS gain mechanisms: (a) Voltage amplification; (b) transimpedance amplification.

A figure closely related to the resolution time is the *amplification time* (T_A) [16], defined as the time required to achieve a given equivalent amplification following the application of an input step (not necessarily an overdrive).

2.2. *Basic CMOS Transimpedance Mechanism*

Essentially, for current comparator design purposes we must look for mechanisms that provide transimpedance gain. However, unlike linear amplifier applications where the significant figure is the steady-state gain, in comparator applications the issue is that the output reaches a suitable amplitude level in the shortest time possible.

Figure 2(a) shows a conceptual circuit for the basic gain mechanism available in CMOS technology, consisting of a VCCS modelling the MOS transistor transconductance, a linear resistor accounting for the device's equivalent Early voltage, and a capacitor modelling the finite gain-bandwidth product. This mechanism provides *voltage* amplification, which can be exploited to design voltage comparators using *one-stage* CMOS OTA architectures [17]. A current sensing stage must be used in front of Figure 2(a) for current-to-voltage amplification, as shown in Figure 2(b), where a general sensing component is considered, represented as an impedance Z. The input current i_{in} is first converted to a voltage v_a via the input impedance; then, a voltage amplifier is used to yield the output voltage v_o. There are many possible design choices for Z, depending on whether it is predominantly resistive or capacitive. The nominal extreme cases correspond to those using either purely *resistive* input, as is the case for Freitas–Current's architecture [12], or purely *capacitive* input, similar to the architecture used in charge preamplifiers for radiation sensors [18].

To compare the speed capability of capacitive-input and resistive-input architectures we must take into account that in practice the input sensing node is neither purely resistive nor purely capacitive, due to parasitics. For comparison let us focus on the conceptual two-stage model of Figure 3. The resistance R_a and capacitance C_a in the input stage model the parallel combination of the nominal sensing elements and the parasitics from the driving and amplifying stages.

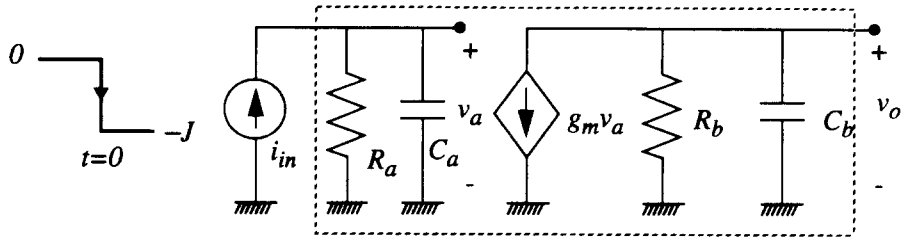

Fig. 3. Transimpedance CMOS gain mechanism with generic input current sensing.

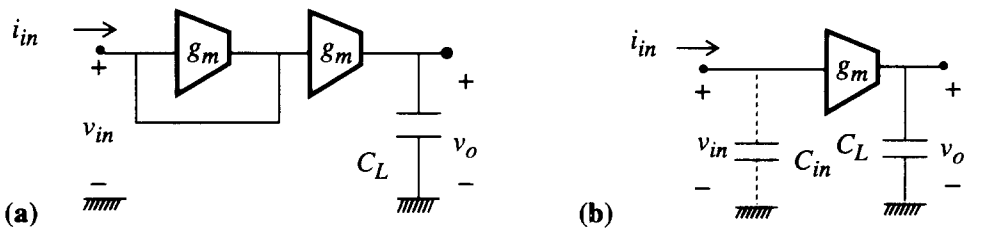

Fig. 4. Basic CMOS current comparator concepts: (a) Resistive input; (b) capacitive input.

This means that in an optimum design C_a will be of the same order of magnitude as C_b and that the maximum attainable R_a value is limited by the device's Early voltage, similar to what occurs for R_b.

Assume that an overdriving negative input current step of magnitude J is applied in Figure 3 at $t = 0$, and that the circuit is relaxed prior to application of the step. Routine analysis obtains the following expression for the output voltage waveform:

$$v_0(t) = g_m R_a R_b J \left(1 - \frac{\tau_a}{\tau_a - \tau_b} e^{-\frac{t}{\tau_a}} - \frac{\tau_b}{\tau_b - \tau_a} e^{-\frac{t}{\tau_b}}\right), \quad t > 0 \tag{1}$$

The resolution time T_R can be calculated from (1) by making $v_o(T_R) = E_{OH}$. Similarly, the amplification time T_A can be calculated by solving the equation

$$R_m \equiv \frac{v_o(T_A)}{J} \tag{2}$$

for a specific required value of the *equivalent transimpedance* amplification R_m. The general expressions for T_A and T_R are rather involved, hence these figures will be calculated separately for the resistive and the capacitive input comparator in the following.

2.3. *Resistive-Input Comparator*

Figure 4(a) shows a conceptual implementation of the resistive input architecture, consisting of a cascade of two inverting transconductors, where the first is connected as a self-conductor. This causes the input node to be the low impedance type, so that $R_a \ll R_b$; also, since $C_a \approx C_b$, we can conclude that the time constant of the input stage is much lower than that of the output stage. Under these conditions, and assuming $t \ll t_b$, (1) is simplified to

$$v_o(t) \cong \frac{g_m R_a J}{C_b} t, \quad t \ll \tau_b \tag{3}$$

since both amplifiers have the same value of g_m, (3) simplifies further to $v_o = (J/C_b)t$, from which the following expression for the resolution time is obtained:

$$T_R = \frac{E_{OH} C_b}{g_m R_a J} \tag{4}$$

According to this formula, a resolution time of about 100 μs results for an input step of $J = 1$ nA, assuming $E_{OH} = 1$ V, a typical inverter capacitance of $C_b = 0.1$ pF, and using a typical value of 10^8s^{-1} for g_m/C_b (corresponding to a MOST with bias current of 1 μA and $V_{GS} - V_T = 0.2$ V). On the other hand, for an input step of $J = 10$ μA, under the same assumptions, (4) gives $T_R = 10$ ns.

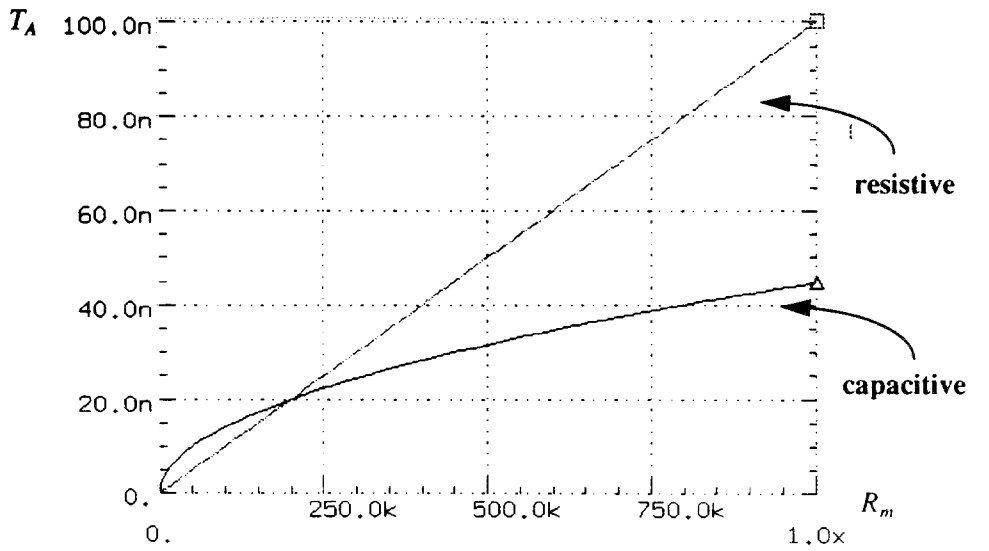

Fig. 5. Comparison of the amplification time for capacitive and resistive current comparator architectures.

2.4. *Capacitive-Input Comparator*

Figure 4(b) shows a basic implementation of this architecture, which consists of an inverter and associated parasitic input capacitor. Since in this case the input node is the high impedance type, input resistance is determined by the Early voltage of the driving stage, and consequently $R_a \approx R_b$. On the other hand, $C_a \approx C_b$, so both time constants are of the same order of magnitude. Under these conditions both the linear and the quadratic terms of the Taylor expansion of (1) must be considered, which results in

$$v_o(t) \cong \frac{g_m J}{2C_a C_b} t^2, \quad t \ll \tau_b \tag{5}$$

and thus,

$$T_R = \sqrt{\frac{2E_{OH} C_a C_b}{g_m J}} \tag{6}$$

Assuming, as for the resistive input case, that $J = 1$ nA, $C_a = 0.1$ pF, $g_m/C_b = 10^8$ s^{-1}, $E_{OH} = 1$ V, the resulting resolution time is 1.4 μs, approximately two orders of magnitude smaller than that obtained for resistive input architecture under the same conditions. However, if $J = 10$ μA, (6) gives $T_R = 14$ ns, slightly larger than the 10 ns obtained for resistive input architecture.

2.5. *Comparison of Basic Architectures*

Figure 5 has been obtained using (2), (3), and (5) to display the amplification time required to achieve different values of the equivalent transimpedance gain for both comparator architectures. The two curves intersect at a value R_{mcrit},

$$R_{mcrit} = \frac{2C_a}{g_m C_b} \tag{7}$$

where $g_m = 1/R_a$. For equivalent transimpedance gain values below R_{mcrit}, the amplification time required for resistive input architecture is slightly smaller than that for capacitive input architecture. However, for $R_m > R_{mcrit}$, capacitive input architecture is clearly advantageous. For the numerical values applied previously, R_{mcrit} amounts to 0.2 MΩ (requested for the correct coding of a 5 μA input current), and can be increased by decreasing g_m.

Advantages of capacitive input architecture for low currents are also evident regarding static performance features. Calculation of the gain errors (defined as $(E_{OH} - E_{OL}) = R_m \Delta$, where R_m is the transimpedance of the comparator) of Figure 4(a) and

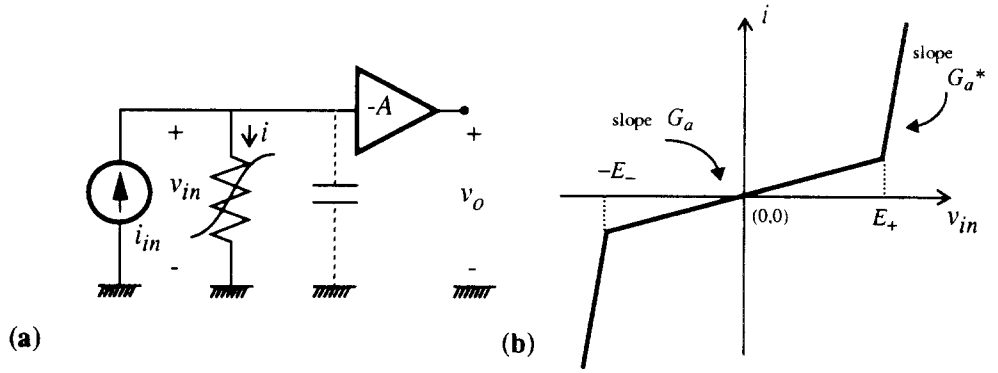

Fig. 6. Improved capacitive input current comparator: (a) Concept; (b) i–v input curve.

Figure 4(b) as functions of the bias conditions of the underlying MOS transistors gives

$$\Delta = \begin{cases} (E_{OH} - E_{OL})\dfrac{I_Q(V_{GS} - V_T)_Q}{2V_A^2} & \text{capacitive} \\ (E_{OH} - E_{OL})\dfrac{I_Q}{V_A} & \text{resistive} \end{cases} \tag{8}$$

where I_Q is the bias current in the MOS transistors, V_A denotes the device's equivalent Early voltage, $(V_{GS} - V_T)_Q$ represents the gate-to-source voltage at the MOST bias point, and we have assumed $g_m = 1/R_a$ for the resistive-input architecture. It is seen that the DC resolution of capacitive input architecture is larger by a factor $2V_A/(V_{GS} - V_T)_Q$ (> 200 for channel lengths above 5 μm in a typical CMOS technology). Actually, for ideal capacitive input architectures where losses at the input node are null, the input current would be integrated in the input capacitor and produce a continuous increase of the input voltage; consequently, an infinitely large value for the DC transimpedance would be obtained, giving $\Delta = 0$. Also, and due to the integrating feature, virtually zero current offset is obtained (the only offset term is due to leakage currents) without relying on precise device matching, which is an important advantage when compared to resistive input architecture.

3. High Resolution CMOS Current Comparators

3.1. *Current Comparator with Nonlinear Sensing Device*

A major drawback in the capacitive-input comparator is that the voltage at the input node exhibits very large variations due to the integrating feature. This can be corrected by decreasing R_a; however, it leads to the resistive-input architecture and consequently, high resolution features are lost. The challenge is to modify Figure 4(b) to obtain a circuit which combines the advantages of capacitive and resistive input architectures: high resolution and reduced amplification time for low current levels, and reduced input voltage excursion for large current levels.

Figure 6(a), whose distinctive feature is the use of a nonlinear resistor to sense the input current is intended to these purposes. Figure 6(b) shows the required resistor characteristics, which we assume include the contribution of the output resistance of the driving current source. The basic idea is to make the equivalent resistance of the inner piece (R_a) very large, so that Figure 6 reduces to the capacitive input architecture for low currents, thus preserving the high-resolution feature. On the other hand, for large currents the equivalent resistance R_a^* is made much smaller, so that the input voltage varies only slightly and, consequently, the useful current range increases and response time decreases.

The simplest way to implement the concept of Figure 6(a) is to use an MOS diode structure, as shown in Figure 7(a) [19] or Figure 7(b). However, they produce wide dead zones of amplitude $|V_{Tp}| + V_{Tn}$ (V_T denotes the MOST threshold voltage). This amplitude is reduced if the gates of M_n and M_p are biased separately at $V_{Gn} = V_{Tn} - E_-$ and $V_{Gp} = -V_{Tp} + E_+$, respectively. However, it requires rather involved bias circuitry to extract threshold voltages in a very strong substrate effect. In any case, E_+ and E_- should be large enough to guarantee that the driving-point characteristics transition region matches (under global and local statistical variations of the technological parameters) that of the voltage amplifier. Besides, the aspect

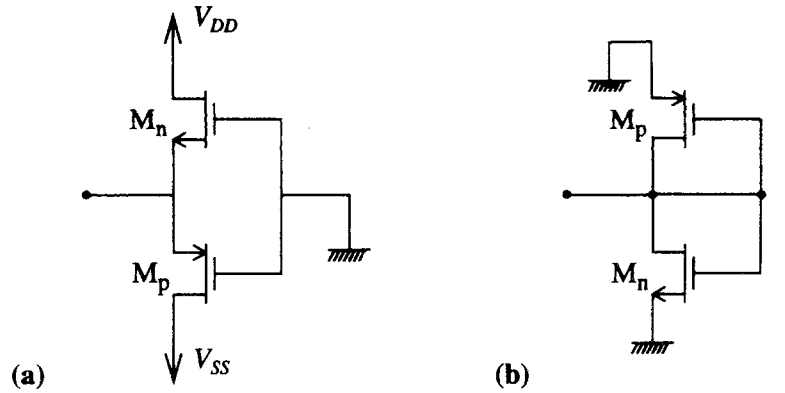

Fig. 7. Basic CMOS dead zone nonlinearity implementation.

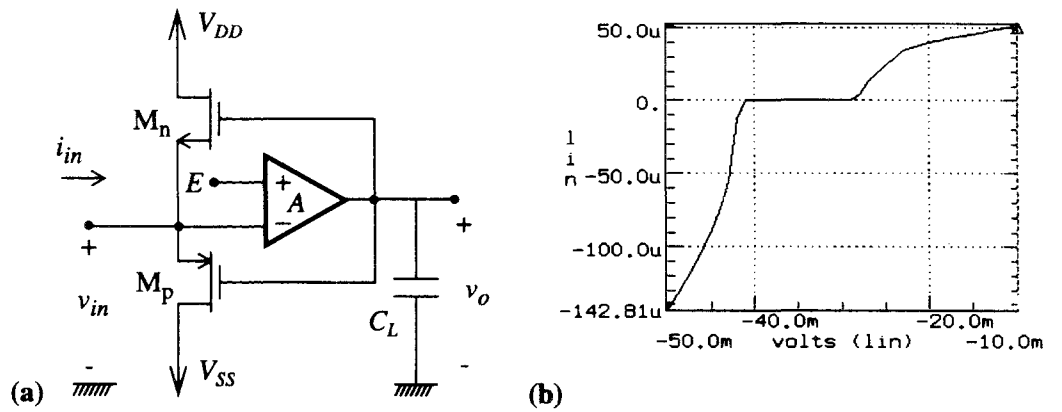

Fig. 8. (a) Nonlinear feedback capacitive input CMOS current comparator; (b) driving point characteristics at the input node.

ratios of M_p and M_n must be large enough to increase G_a^* and consequently, the equivalent capacitance at the input node will be large and the response time further degraded. A convenient technique to overcome all these drawbacks uses nonlinear feedback—described in the next section.

3.2. *Feedback Current-Switching Comparator: Static Operation*

Consider the circuit of Figure 8(a) whose operation involves different regions. For small changes of the current around the quiescent point ($v_{in} = E$, $i_{in} = 0$), transistors M_n and M_p are OFF, so that the equivalent resistance at the input node is large and, consequently, the circuit preserves the high resolution feature of capacitive input. For positive currents, v_{in} increases and the amplifier causes v_o to decrease so that M_p is driven into the ON state and a feedback loop is created around the amplifier. It obtains virtual ground at the amplifier input, thus fixing the voltage at the input node. A similar situation occurs for negative currents, where M_n becomes ON. Actual clamping values are given by

$$E_- = E\frac{A}{1+A} - \frac{V_{Tn}}{1+A}; \quad E_+ = E\frac{A}{1+A} + \frac{|V_{Tp}|}{1+A} \tag{9}$$

where A denotes the amplifier gain.

Figure 8(b) illustrates the shape of the i_{in} vs. v_{in} static characteristics of Figure 8(a). An interesting feature of these characteristics is that their transition region track in construction that of the voltage amplifier, which enables using minimum size transistors with associated small parasitic capacitors. Also, due to the feedback action, voltage excursions at the input node remain small for large input currents, which guarantees that transistors in the amplifier will operate in

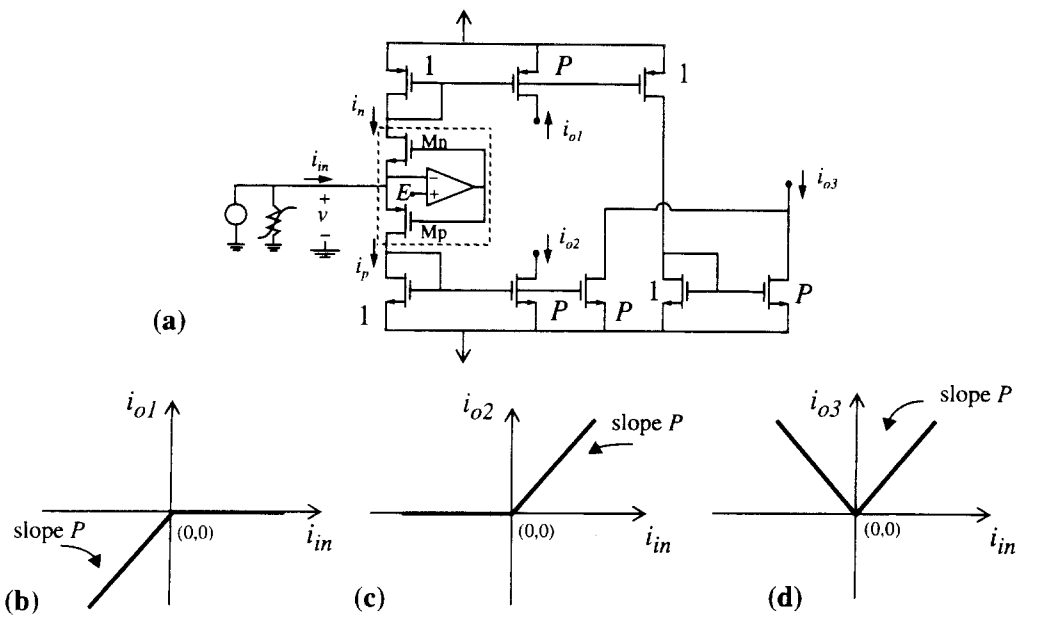

Fig. 9. Current rectification through a feedback current switch: (a) Circuit schematics; (b)–(c) half-wave rectification characteristics; (d) full-wave rectification charateristics.

saturation for the whole current range, and reduces loading errors in the driving stage. Benefits from the feedback are increased by increasing the amplifier gain. In many practical applications a simple single-ended CMOS inverter can be used to this purpose, as proposed in [13], [14], and [15]. However, this obtains clamping levels for input voltage which are determined by technological parameters, threshold voltages, and large signal transconductance of the transistors and, consequently, subjected to large statistical variations.

3.3. *Application to High-Resolution Current Rectification*

An appealing feature of Figure 8(a) is its application to current rectification—a basic operation for nonlinear current-mode circuit design. A similar property was already anticipated by Wang regarding the structure of Figure 7(a) [19]. This application exploits the low sensitivity of Figure 8(a) to variations in the supply voltage, which enables sensing drain currents of transistors M_n and M_p by using current mirrors, as is shown in Figure 9(a). Rectification is implicit to the operation of the current switch, enclosed inside the dashed box in Figure 9(a): current drawn by M_p is null for negative input currents and follows the input current otherwise, while the current which circulates through M_n is its complementary. This obtains a double rail rectification. Remaining circuitry in Figure 9(a) senses these basic currents, and scales and combines them to obtain the two complementary half-wave rectifier characteristics of Figure 9(b) and Figure 9(c), as well as the full-wave rectifier characteristics of Figure 9(d). These basic characteristics support systematic design of current-mode function generators [20], based on the mathematical formulation by Kang and Chua [21]. Also, the feedback current-switch is advantageous as compared to using the inherent rectification property at the input node of a current mirror [22]. On the one hand, it achieves concave and convex curves with no input current replication needed. On the other, since it provides paths for both negative and positive input currents, it precludes that parasitics charge be accumulated at the input node, and hence has potential for larger operation speed [20]. Finally, the use of feedback guarantees much smaller voltage excursions at the input node and thus decreases errors due to loading of the driving stages. As a matter of fact, experimental results in Section 5 demonstrates current rectification in the range of pAs using Figure 9—much better resolution than reported for previous CMOS proposals [22, 23].

3.4. *Transient Response of the Current Switch Comparator*

Let us now focus on the calculation of transient behavior of the current switch comparator of Figure 8(a), in particular the response time parameter T_D. Assume that $E = 0$, consequently the output voltage remains inside the interval $(\alpha V_{tp}, \alpha V_{tn})$, with $\alpha = A/(1+A)$, and that the input current steps at $t = 0$ from a negative overdrive level $-J_-$ up to a positive overdrive level J_+. Calculation of the response time of Figure 8(a) obtains the following expression for the transient waveform,

$$v_o \approx \begin{cases} \alpha V_{Tn} - \frac{J_+ g_m}{2C_{eq}^2}\left[1 + \left(\frac{C_f}{C_{eq}}\right)^2 + \frac{C_f(C_{in}+C_f)}{AC_{eq}}\right] t^2 \\ \qquad \text{for } t < T_{QL} \equiv \frac{C_f}{g_m}\left(1 + \frac{C_{eq}^2}{C_f^2}\right) \\ \alpha V_{Tn} - \frac{J_+}{C_f(1+A^{-1})} t \\ \qquad \text{otherwise} \end{cases} \tag{10}$$

where C_f is the overlapping capacitor which connects input and output terminals of the amplifier in Figure 8, and $C_{eq}^2 = C_a C_b + C_a C_f + C_b C_f$. For large values of the amplifier gain parameter A, this expression is further simplified to

$$v_o \approx \begin{cases} \alpha V_{Tn} - \frac{J_+ g_m}{2C_{eq}^2}\left(1 + \left(\frac{C_f}{C_{eq}}\right)^2\right) t^2 \\ \qquad \text{for } t < T_{QL} \equiv \frac{1}{g_m}\left(C_f + \frac{C_{eq}^2}{C_f}\right) \\ \alpha V_{Tn} - \frac{J_+}{C_f} t \\ \qquad \text{otherwise} \end{cases} \tag{11}$$

The transient waveform contains two different pieces: for $t < T_{QL}$ and for $t > T_{QL}$. Initial evolution follows a quadratic law, as for capacitive-input architecture. However, for $t > T_{QL}$ the output slews up according to linear evolution law. Note that the value of this time breakpoint is a function of C_f. If this capacitance is negligible, T_{QL} is very large, and the transient is dominated by quadratic evolution law. However, for typical design conditions, T_{QL} is much smaller than T_D and consequently the transient is dominated by the bottom expression so that it obtains

$$T_D \approx \alpha \left(V_{Tn} + |V_{Tp}|\right) \frac{C_f}{J_+} \tag{12}$$

which implies that although the high resolution properties of the capacitive-input architecture remain, the quadratic response feature is lost due to the Miller effect created around C_f—significant even for minimum sized feedback transistors, in particular for low current.

The next subsection presents an improved comparator structure which overcomes dynamic limitations of Figure 8, using a different current feedback mechanism. Although this new circuit is better suited for pure comparison purposes, it does not preserve the current rectification properties and, hence, does not qualify directly for current-mode function generation.

3.5. *Current Steering Comparator*

Improved transient response of the feedback switch comparator requires using circuit strategies to decouple input and output nodes of the amplifier and, hence, reduce Miller capacitance. On one hand, cascode transistors should be used at the amplifier input; on the other, the feedback mechanism used to obtain the nonlinear driving-point characteristics should be modified. The circuit in Figure 10(a) incorporates a strategy to this end. Its static operation follows principles similar to that of Figure 8(a). At the center point ($v_{in} = E$, $i_{in} = 0$) both transistors are OFF and the circuit yields capacitive-input behavior. Positive currents ($i_{in} > 0$) integrate in the input capacitor increasing v_{in}, and consequently decreasing v_o until the transistor M_n becomes conductive, absorbing the input current and stabilizing the voltage. The same occurs for negative currents, where M_p is the conductive transistor. Figure 10(b) illustrates the shape of the static driving point characteristics of this steering comparator—similar to that observed for Figure 8. Regarding the transient behavior, analysis confirms that it is dominated by a quadratic, instead of linear, term. Consequently, this circuit obtains delay time,

$$T_D \approx \sqrt{\frac{2\alpha(V_{Tn} + |V_{Tp}|)C_a C_b}{J_+ g_m}} \tag{13}$$

much smaller than (12). As a matter of fact, calculations using same typical values as for (6), with $\alpha = 1$, and $V_{Tn} = |V_{Tp}| = 1$ V, obtain two orders of magnitude improvement.

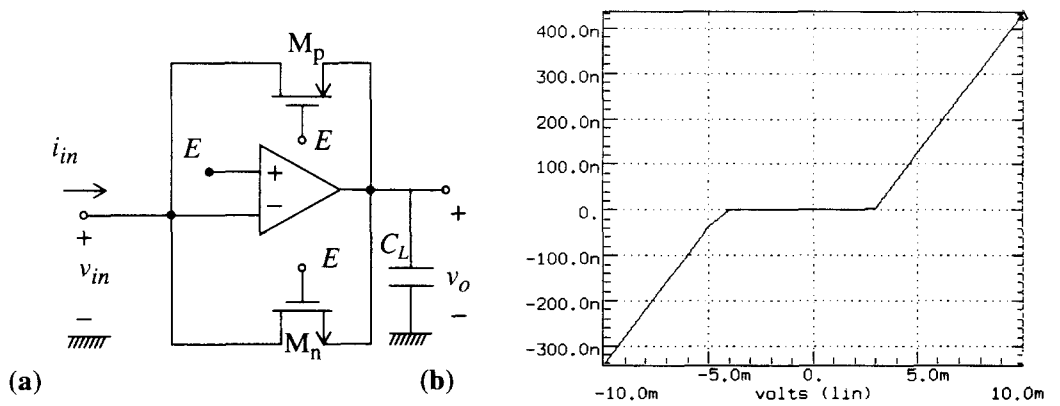

Fig. 10. (a) Enhanced current comparator schematic; (b) driving point characteristics at the input node.

4. Extension to Current-Mode Function Generation

Function approximation is a necessary step in electronic function generator design. In particular, piecewise-linear (PWL) circuits are simple to design and do not have the accuracy and calibration problems, which are typical for circuits based on multipliers [24]. As [25] demonstrates, any continuous PWL function $f(x) : R \rightarrow R$, consisting of N pieces of slope $m_1, m_2, \ldots, m_N$, respectively, and breakpoints at $P_1, P_2, \ldots, P_{N-1}$ can be expanded as follows,

$$f(x) = Ax + B + \sum_{j=1}^{N_p} M_j u_p(x - E_j) + \sum_{j=-N_n}^{-1} M_j u_n(x - E_j) \quad (14a)$$

where $u_p(\bullet)$ and $u_n(\bullet)$ are *elementary* functions defined as,

$$u_p(x - E_j) = \begin{cases} (x - E_j), & x > E_j \\ 0, & \text{otherwise} \end{cases}$$

$$u_n(x - E_j) = \begin{cases} 0 & x > E_j \\ (x - E_j), & \text{otherwise} \end{cases} \quad (14b)$$

and where A, B, M_j, and E_j are real numbers, and N_p and N_n are positive integers with $N_p + N_n = N$. Parameters A, B, M_j, and E_j of the expansion must be calculated from the slopes, breakpoints, and $f(0)$ value of the original function. This can be done by inspection, as illustrated in Figure 11(b), showing a possible decomposition of Figure 11(a). The results of elementary calculations are $N_n = 1$, $N_p = 2$, $E_{-1} = P_1$, $E_1 = P_2$, $E_3 = P_3$, $A = m_2$, $B = f(0)$, $M_{-1} = (m_1 - m_2)$, $M_1 = (m_3 - m_2)$, and $M_2 = (m_4 - m_3)$.

In the case of Figure 11(b), the extension operator decomposition has been made around the second piece of the PWL function. Generally, any piece in the original curve may be chosen as the central piece—the extension operator decomposition is not unique. In practical circuits, decomposition should be made to yield M_j spread as low as possible, to optimize area and power consumption of the monolithic implementation. A second PWL function expansion methodology is the use of base functions. From mathematical approximation theory [26], it is well known that any PL function can be expressed as a linear combination of elementary base functions, one per breakpoint, so that

$$f(x) = \sum_{j=1}^{N-1} f(P_j)\varphi(x, P_j) \quad (15)$$

where $f(P_j)$ denotes the value of $f(x)$ at the P_j breakpoint, and the base functions $\varphi(x, P_j)$ have the generic shape represented in Figure 11(c) involving two adjacent intervals of the function domain partition. Figure 11(d) illustrates the decomposition of Figure 11(a) using this technique. Unlike the technique based on (14), decomposition by base functions is unique and, hence, more systematic. This technique is also appealing for programmable implementations over predefined partitions (P_j fixed), since each interpolation data $f(P_j)$ influences only one term in (15).

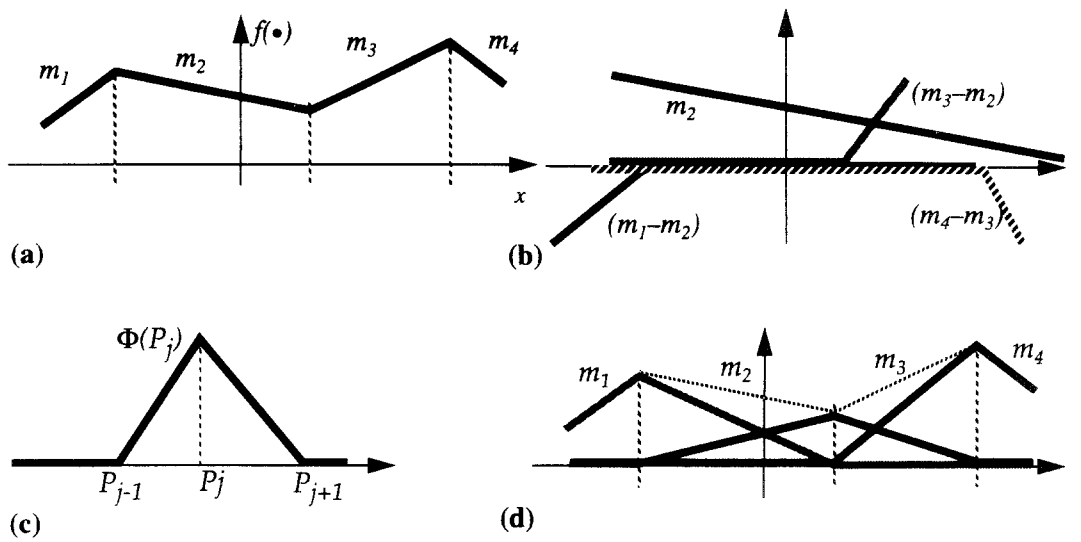

Fig. 11. (a)–(b) Illustrating the decomposition of a P_L function as a summation of half-wave rectifier curves; (c) P_L basis function; (d) decomposition of a P_L function using basis functions.

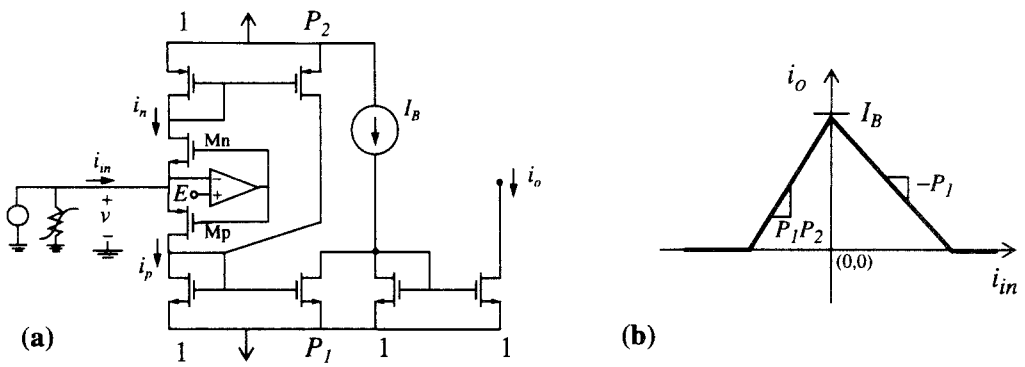

Fig. 12. PWL base function through a feedback current switch: (a) Circuit schematics; (b) transfer characteristics.

All elementary functions in (14) and (15) are realized with very high accuracy in current domain, by exploiting rectification properties of the current switch. Functions $u_p(\bullet)$ and $u_n(\bullet)$ in (14) use the circuit of Figure 9(a). Their slopes in the ON region are controlled by mirror gains which are determined by transistor aspect ratios. Negative slopes are simply obtained by cascading an extra current mirror. Finally, shifted versions of the basic characteristics of Figure 9 are obtained by providing a bias current at the block input. On the other hand, Figure 12 shows a circuit to realize the base functions in current domain, intended for positive interpolation data. Negative interpolation data are implemented by a similar circuit.

5. Practical Results

5.1. *High-Resolution CMOS Current Comparators: Current-Switch versus Resistive-Input*

Figure 13(a) shows the schematics of a CMOS prototype of the resistive-input comparator of Figure 4(a), for a single-poly n-well 2 μm technology. Cascode transistors are used to increase the amplifier voltage gain. Also, a CMOS inverter has been added to drive pad load and regenerate output voltage logic levels. The schematics for a current switching prototype, according to the concept of Figure 8(a), is shown in Figure 14(a). The amplifier of this circuit is built by using a simple CMOS inverter; an inverter is also used for buffering.

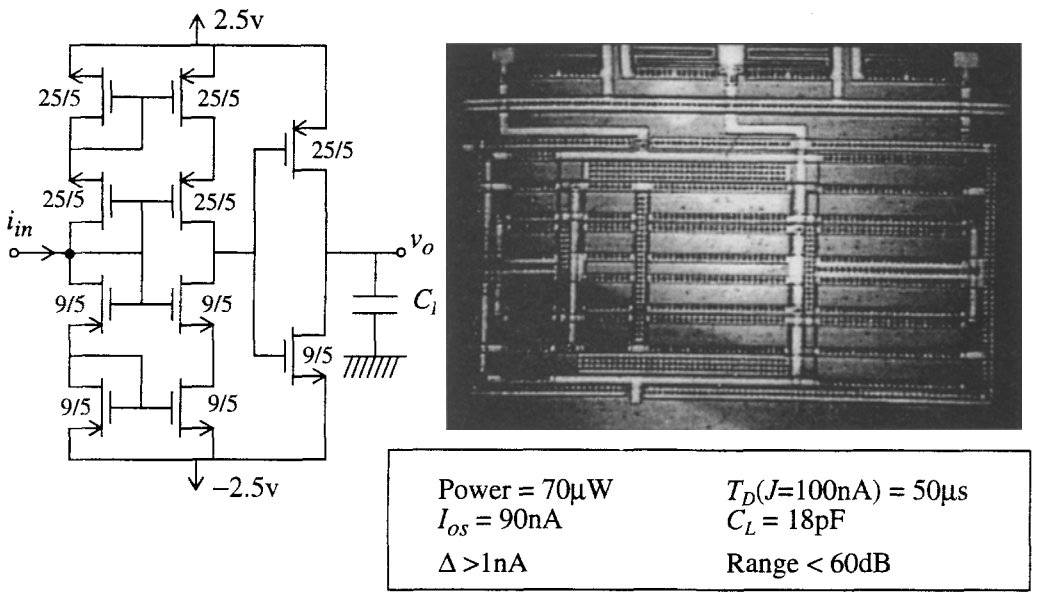

Fig. 13. Schematics, microphotograph, and measurements for a resistive-input CMOS current comparator prototype (transistor sizes are in μm's).

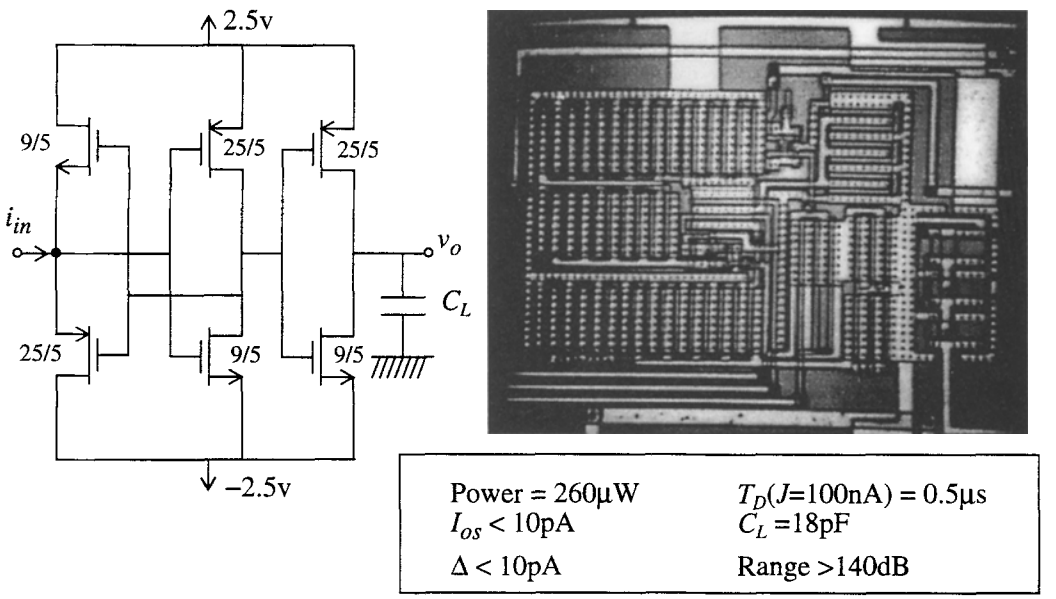

Fig. 14. Schematics, microphotograph, and measurements for a capacitive-input CMOS current comparator prototype (transistor sizes are in μm's).

Microphotographs for the two prototypes are shown also in Figure 13 and Figure 14, respectively. Measured data for each prototype are included in the corresponding figure. Results for the resistive input comparator confirms the theoretical prediction of low comparison range (less than 60 dB) and slow operation for reduced current levels (50 μs for a 100 nA current). Current offset is also significant (about 90 nA). Measured resolution range for the capacitive input comparator is more than four orders of magnitude larger (over 140 dB) and

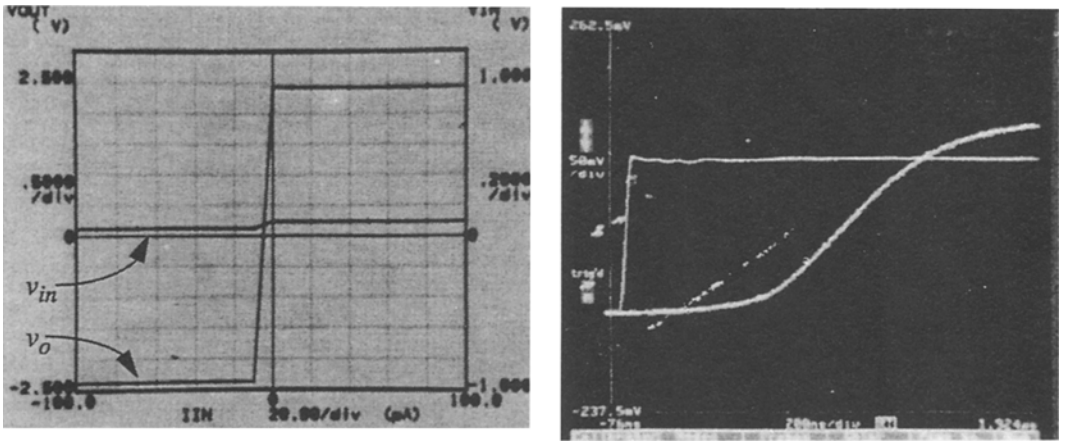

Fig. 15. Measured transfer characteristics and transient response for figure 14.

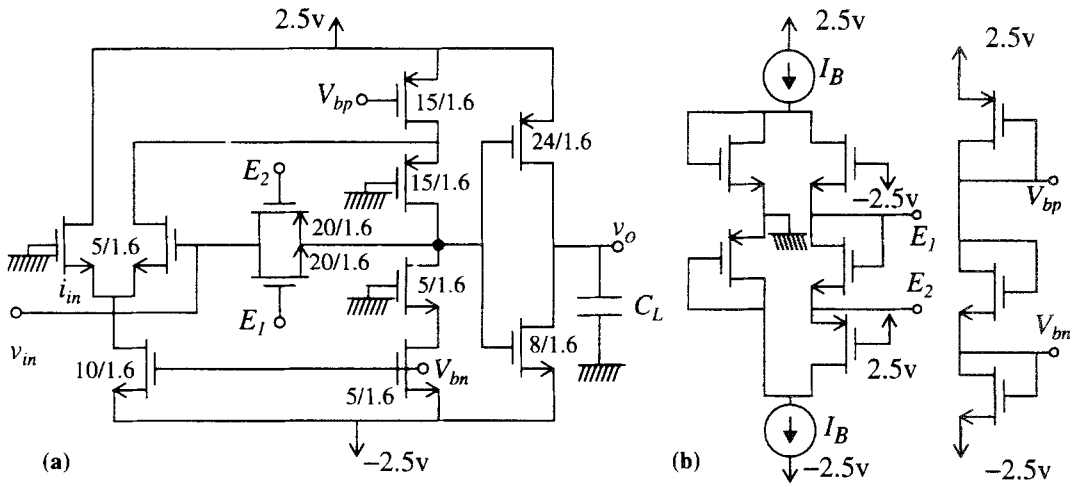

Fig. 16. CMOS 1.6 μm prototype of the current steering comparator: (a) Core circuit; (b) biasing circuitry.

the offset is negligible (less than 10 pA)—properties which were systematically observed in all the measured units (up to 10, the only available). On the other hand, operation speed for small currents is about two orders of magnitude larger for a power increase of less than 4, demonstrating much superior efficiency of the capacitive input architecture.

Figure 15 shows additional measurements for the current switching prototype. Figure 15(a) shows the measured static input and output characteristics. For currents up to 20 μA, the input voltage remains smaller than approximately 0.6 V. Figure 15(b) illustrates the transient waveform at the output node for a current step of 10 nA. The delay remained practically unchanged for the whole input current range, demonstrating that it is mostly due to the buffering inverter, not to the core comparator.

5.2. *Current Switching vs. Current Steering Comparators*

Figure 16(a) shows the schematic of a 1.6 μm CMOS prototype of Figure 10, and Figure 16(b) shows the associated biasing circuitry. The circuit employs a folded cascode differential amplifier to reduce capacitive

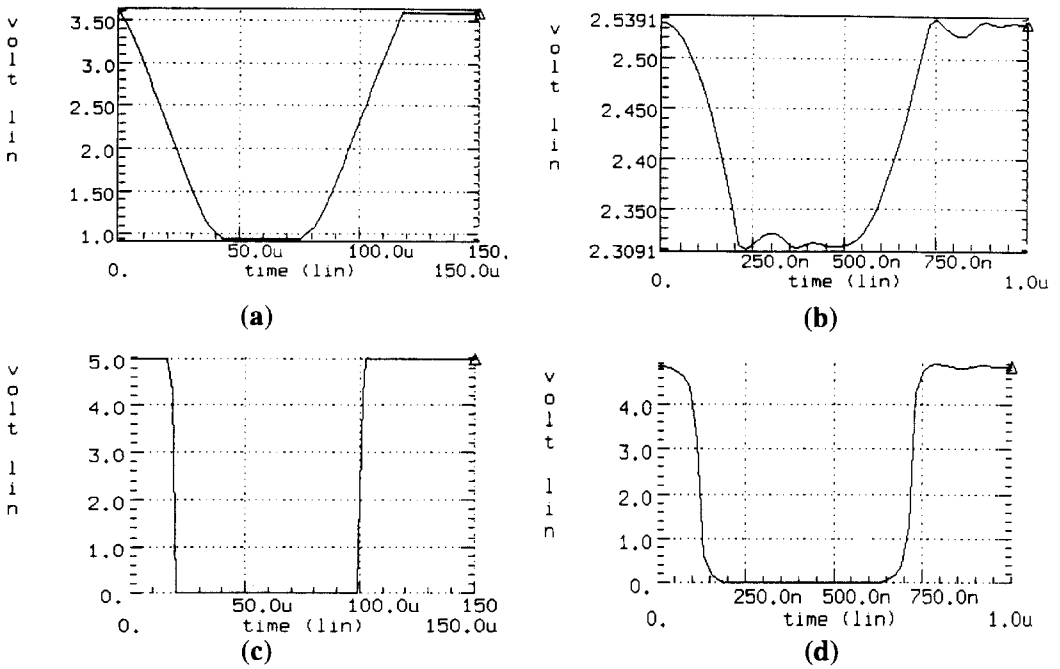

Fig. 17. Transients waveforms at the amplifier output for $J = 1$ nA: (a), (c) Amplifier output and inverter output for the current-switching comparator; (b), (d) current steering comparator.

Table 1.

	Current Steering Comparator	Current Switch Comparator
Power (core comparator)	750 μW	750 μW
Offset (I_{os})	<1 pA	<1 pA
Resolution (Δ)	<1 pA	<1 pA
Delay time (T_D)		
$J = 1$ nA	150 ns	25 μs
$J = 100$ nA	15 ns	250 ns
$J = 10$ μA	6 ns	10 ns
Load capacitor (C_L)	18 pF	18 pF
Comparison range	140 dB	140 dB

coupling between input and output nodes, and has been designed to yield sufficient output range to start feedback transistors, relatively high voltage gain, and large bandwidth; all of this was attained using a folded cascode amplifier structure with no feedback mirror to avoid parasitic poles which would provoke stability problems. The same amplifier and the same output inverter have been used to implement Figure 8(a), using minimum size for the transistors in the current switch.

Table 1 displays some significant performance figures measured from the current switch and current steering prototypes. We see that resolution and offset are similar for both structures, while response times are smaller for the current steering comparator, as expected. In particular, improvement for the 1 nA input current is about 170.

The quadratic transient exhibited by this latter structure is confirmed by the waveforms displayed in Figure 17. Each figure shows the transient evolution of the signals at the amplifier outputs and at the inverter output, for a 1nA current step. The figures show that transient evolution of the amplifier output in the current switching architecture is linear, while the other is quadratic.

5.3. Current-Mode PWL Circuits

Prototypes of the circuits of Figure 9(a) and Figure 12(a) have been fabricated in a 1.6 μm CMOS n-well single poly technology. Figure 18 shows measurements taken from the prototype for Figure 9(a). The half-wave rectifier characteristics of Figure 18(a) and (b) show measured families of curves for different values of an input bias current, in the range of μA's (0–100 μA). These curves illustrate the circuit operation for large currents. Figure 18(c) illustrates the operation for low currents. It also shows a family of full-wave rectifier characteristics for different values of an

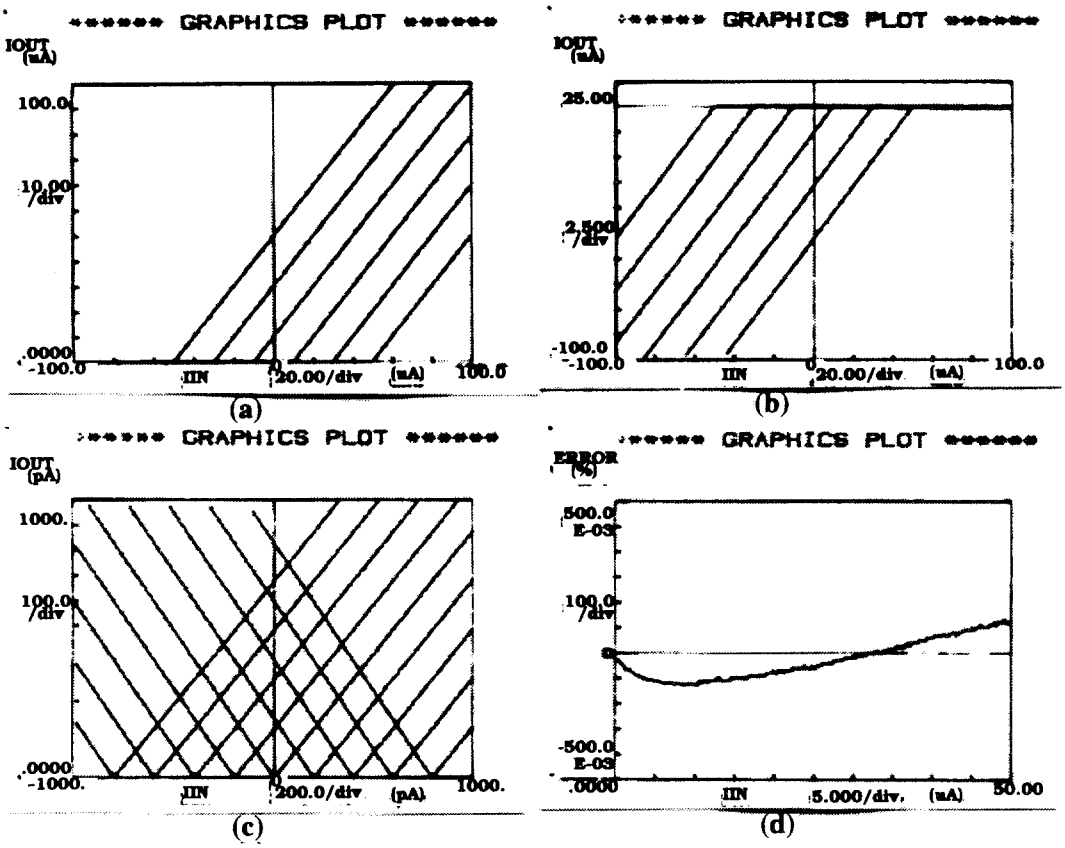

Fig. 18. Experimental results for a 1.6 μm CMOS prototype of Figure 9(a).

input bias current, but in the range below 1 nA (-1 nA to 1 nA). Measurements show that the circuit is able to discriminate current levels as small as 1 pA (this was the resolution limit of the measurement setup). On the other hand, the measured linearity was excellent for the whole current range; it is illustrated in Figure 18(d), showing the measured linearity errors were below 0.13%. Also, variations on the input voltage are small (about 0.5 V for a current range of 100 μA).

Figure 19 shows measurements taken from the prototype of Figure 12(a). Figure 19(a) gives a family of transfer characteristics for $I_B = 25$ μA and biasing the input node with different currents levels. Figure 19(b) shows another family of curves measured for this circuit, using different values of I_B and no bias current applied at the input node. The same comments regarding accuracy and resolution as for Figure 19 also apply to these measurements.

6. Conclusions

High resolution CMOS current comparators can be implemented using very simple circuits, based on a fundamental knowledge of the mechanisms underlying the operation of this block. It requires using nonlinear characteristics with well-controlled breakpoints and sharp transitions, which are better realized using feedback structures. Also, the self-tracking provided by these feedback structures guarantees robust high resolution (<1 pA) and low offset (<1 pA) operation in a standard VLSI CMOS technology.

The core current switch comparator circuit is extended in a simple manner to define a family of high resolution nonlinear current-mode circuits with applications in sensor signal conditioning, artificial neural networks, and fuzzy interpolation systems. The proposed circuit also shows potential use as the second stage in voltage comparators to reduce the propagation time required to remove the charge accumulated in this stage input capacitor [14].

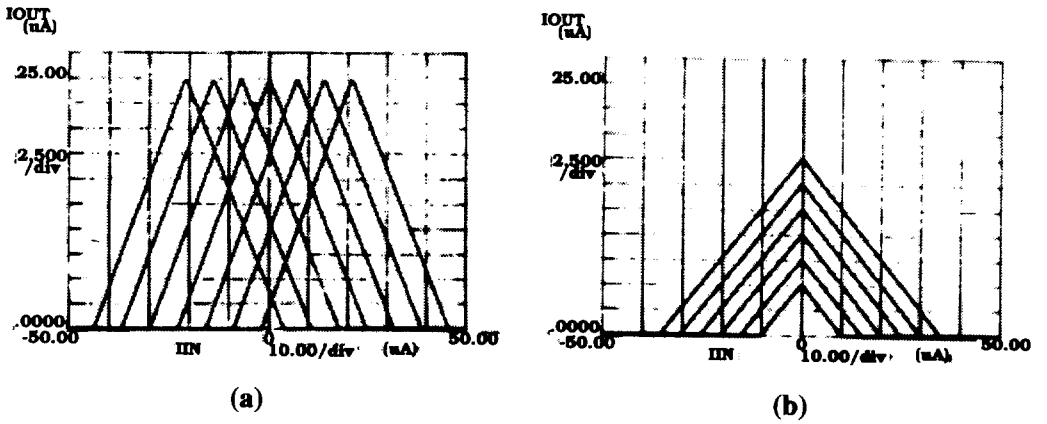

Fig. 19. Experimental results for a 1.6 μm CMOS prototype of Figure 12.

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