Analog Integrated Circuits and Signal Processing, 7, 113–129 (1995)

On the Frequency Limitations of the Circuits Based on Second Generation Current Conveyors

ALAIN FABRE

Laboratoire d'Electronique, Ecole Centrale de Paris, 92 295 Chatenay-Malabry, France
fabre@epap.ecp.fr

OMAR SAAID AND HERVÉ BARTHELEMY

Laboratoire d'Electronique, Ecole Centrale de Paris, 92 295 Chatenay-Malabry, France

Received January 20, 1994. Revised June 2, 1994.

Abstract. An equivalent circuit for the translinear implementation of the second generation current conveyors with positive or negative current transfer is given. This circuit takes into account the various parasitic elements of the conveyor which induce frequency limitations (gain values, poles of the transfers, and parasitic impedances). The methods allowing the determination of the values for these parasitic elements are indicated and discussed. The effect of each element on the frequency responses of the circuits using the conveyors are studied in every detail. The frequency behavior of two circuits are analyzed as examples: a voltage amplifier without feedback and two configurations for a second order biquad filter operating in current-mode. All the theoretical results of the analysis are well confirmed from SPICE simulations.

1. Introduction

The second generation current conveyor (CCII), introduced by SEDRA and SMITH in 1970 [1], rapidly appeared as a basic element of first importance. It has since given place to a great number of applications [1–6]. Thanks to its simultaneous voltage follower properties (between ports Y and X), and current follower properties (between ports X and Z), the circuit can be used to realize electronic functions operating in voltage-mode as well as in current-mode. Several implementations have been described to implement this building block [1–10]. The two most interesting ones from a point of view of a monolithic integration use a voltage follower to synthesize inputs Y and X and two complementary current mirrors that allow to recopy the current on port X to output Z. These two implementations differ only by the manner in which the voltage follower has been designed. When the former is obtained from an operational amplifier used like a buffer [2, 3, 5, 7], the CCII$^+$ takes advantage at low frequency of a low value for its parasitic resistance on port X. It has however all the drawbacks that result from the use of an operational amplifier: reduced -3 dB bandwith, more important power consumption, and also large silicon area.

When the voltage follower is implemented from a mixed translinear loop using complementary bipolar transistors [3, 5, 6, 7], the CCII$^+$ is characterized by cutoff frequencies around several hundred of MHz. It also possesses on port X a parasitic serial resistance which value, in spite of being negligible, has generally little variations up to some hundred of MHz. This property will sometimes allow to take advantage of the presence of this parasitic resistance. We only consider in this paper second generation current conveyors in translinear form. In a first part, after having recalled the definition of the CCII, we will indicate the different parasitic elements obtained from AC characterization of these conveyors. Then, we will discuss the manner to determine them from simulations or from experimental measures. We will also give the values for the parasitic elements obtained from SPICE simulations when the circuits are implemented with complementary high performance bipolar arrays. In a second part, we will indicate the frequency limitations which result from these parasitic elements. Two circuits using CCIIs will then be analysed as an example: a voltage

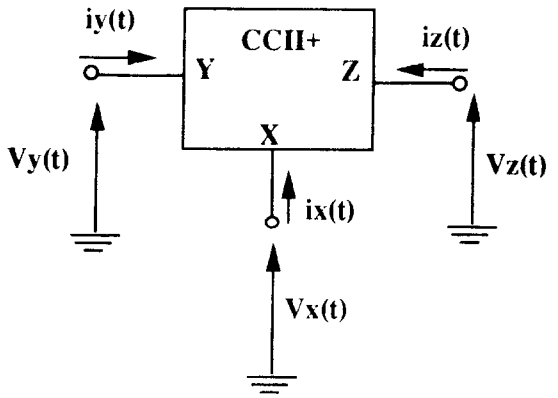


Fig. 1. Electrical symbol for the CCII showing the conventional orientation for its input–output variables.

amplifier without using feedback and two configurations for a second order biquad filter operating in current-mode. We will emphasize on the frequency response deviations due to the parasitic elements of the conveyors. The theoretical results of the analysis will in all cases be confirmed by the simulations.

2. Second Generation Current Conveyors

2.1. *Definition of the Ideal CCII*

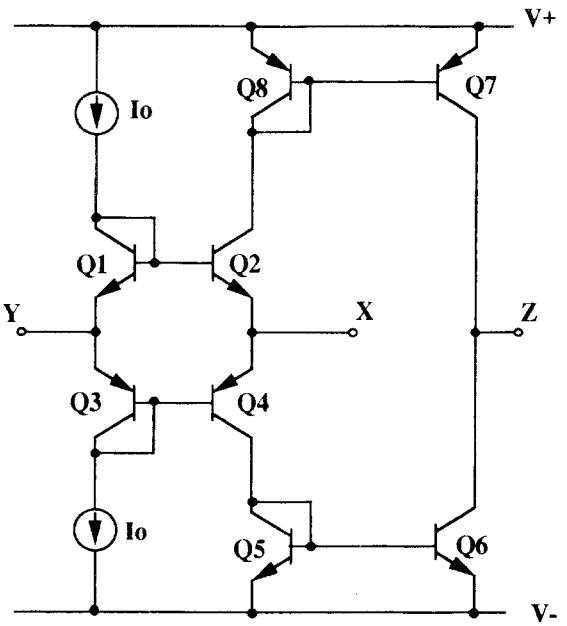
The ideal second generation current conveyor (Figure 1) is described by the matrix relationship that exists between voltages and currents of its input–output ports:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

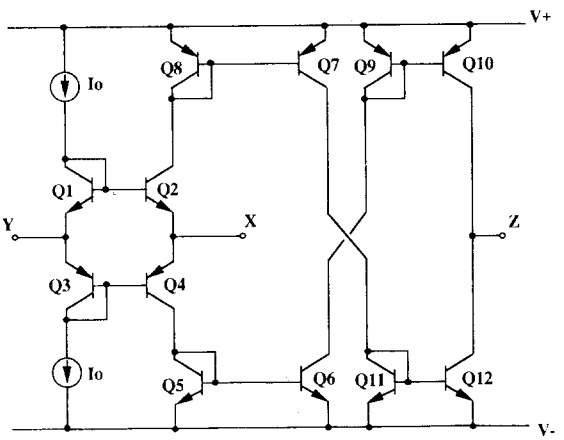
In this expression, the current transfer I_Z/I_X is equal to $+1$ for a positive current transfer conveyor (CCII$^+$) and equal to -1 for a negative transfer conveyor (CCII$^-$). The input impedances for the ideal CCII are respectively: infinite on port Y and null on port X. The port Z, that is equivalent to a current generator, possesses in consequence an infinite output impedance.

2.2. *Translinear implementation for the CCII*

Figure 2(a) and (b) show respectively the basic implementations of the CCII$^+$ and the CCII$^-$ in the translinear form. The two circuits use a mixed translinear loop DC biased by two current sources I_0, in order to have



(a)



(b)

Fig. 2. (a) Schematic implementation for the translinear CCII$^+$; (b) translinear implementation for the CCII$^-$.

a high input impedance at port Y. For the CCII$^+$, two complementary current mirrors allow to duplicate on port Z the input current flowing through port X. To obtain the CCII$^-$, two additional crosscoupled current mirrors have been added to the preceding circuit, in order to reverse the current on port Z. The circuits which have been used for the various simulations were implemented with minor variations from the schematic forms

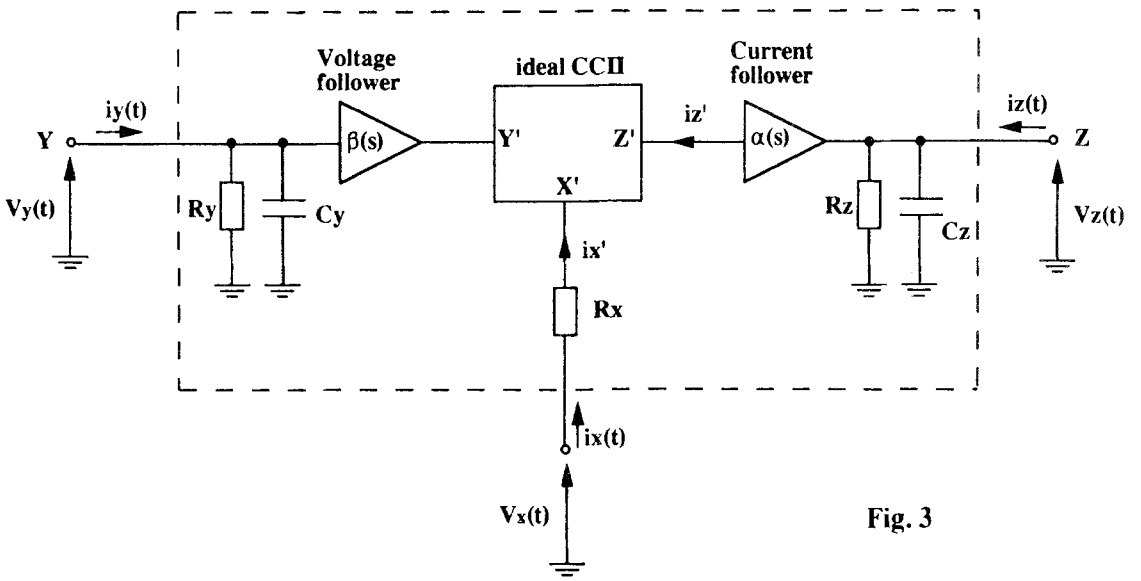


Fig. 3. The real CCII, its parasitics, and the ideal CCII.

given in Figure 2(a,b). Notably particular attention has been paid when designing the input Y, to increase the input impedance at port Y.

2.3. *The Real Conveyor and Its Parasitic Elements*

The ideal conveyor in Figure 1, just as the general equation, allows only an approximate analysis of a circuit implemented from CCIIs. Thus, when the possibilities of an electronic function will have to be determined and notably its performance at frequencies above the MHz range, it will be necessary to consider a simplified circuit for the CCII. But this must be relatively close to the real CCII. This model will have to include the different parasitic impedances of the circuit as well as the possible variations, according to the frequency, of the voltage and current transfers.

Some relatively complete models of the CCII$^+$ whose input follower cell is realized from an operational amplifier have previously been used [11–15]. However, the values for their parameters are not adapted to the translinear conveyors whose frequential possibilities are much more extended. Figure 3 represents the general equivalent circuit that will be used to represent the behavior of the real translinear conveyors. The CCII is represented by dotted lines. The circuit contains an ideal CCII defined by the relationship (1). Following the case, it will be a CCII$^+$ or a CCII$^-$. Between respectively each port Y and Z and the ground, the circuit contains a parallel equivalent parasitic impedance. R_X is the output resistance of the equivalent Thevenin generator seen from port X. $\beta(s)$ and $\alpha(s)$ are respectively the voltage and current transfers of the conveyor that will generally be described by the following first order functions:

$$\beta(s) = \frac{\beta_0}{1 + s/\omega_\beta} \tag{2}$$

$$\alpha(s) = \frac{\alpha_0}{1 + s/\omega_\alpha} \tag{3}$$

where β_0 and α_0 are the values of these transfers at low frequencies (the values for β_0 and α_0 are very close to the unit), ω_β and ω_α represent their corresponding poles. Then, the circuit in Figure 3 allows you to complete the matrix equation (1) relative to the ideal CCII, in order to describe correctly the real CCII. It then becomes

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 1/(R_Y//C_Y) & 0 & 0 \\ \beta(s) & R_X & 0 \\ 0 & \pm\alpha(s) & 1/(R_Z//C_Z) \end{bmatrix} \times \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{4}$$

3. How to Determine the Parameters of the Real Conveyor

In this part we will briefly indicate the measures to undertake and the manner to proceed to determine the different circuits' elements of Figure 3, either by simulations or from experimental measures. The relationship (4) that allows to define each of the parasitic elements also indicates the manner in which they will have to be determined.

3.1. Characterization by Simulation

Using of SPICE simulations is the simplest manner that allows you to determine, by AC analysis, the various elements in Figure 3. With a simulator that is a mathematical tool, difficulties linked to physical measures (i.e., values too low to measure, maladjusted too high or too low impedances, measures at high frequency, etc.) do not appear by just only taking some precautions. To determine the current flowing through a component is for example very simple with a simulator. Experimentally, this is not as easy.

$\beta(s) = V_X/V_Y$ is the voltage transfer of the conveyor. It will have to be determined as a function of the frequency, an infinite load RL connected at X, the conveyor being driven on Y by a voltage generator with zero output resistance, and with output Z grounded.

$\alpha(s) = I_Z/I_X$ is the current transfer of the conveyor that will be determined with an input current applied on port X. The current I_Z is then the current that flows through port Z grounded; port Y being also grounded.

The values for R_Y and C_Y will be determined with port X loaded by an infinite impedance, port Z grounded. The input voltage is in this case applied at Y from a generator with zero output resistance. Then the variation according to the frequency of the current I_Y that goes into the conveyor allows to determine the evolution of the input impedance $Z_Y = (R_Y//C_Y) = V_Y/I_Y$. R_Y is the value of this impedance at low frequency. The value of C_Y is then deduced from the -3 dB cutoff frequency, f_Y, of Z_Y, $C_Y = 1/2\pi f_Y R_Y$.

The value of R_X is determined with outputs Y and Z grounded. When an input current I_X is applied on port X, the resulting voltage V_X allows to determine R_X: $R_X = V_X/I_X$. Also note that it will sometimes be necessary to add an inductance L_X in series with R_X to the model in Figure 3. Similarly that previously its value would have to be determined, after calculation of R_X, from the +3 dB cutoff frequency, f_X, of the impedance $Z_X = V_X/I_X$ by $L_X = R_X/2\pi f_X$.

The values for R_Z and C_Z, which constitute the output impedance of the current generator on port Z, will be determined for the conveyor driven by a current I_X on X, and with port Y grounded. Then the voltage V_Z, which results at port Z loaded by an infinite impedance, allows to determine R_Z at low frequency: $R_Z = V_Z/\alpha_0 I_X \cong V_Z/I_X$ (since the value of α_0 is very close to the unit). The value of C_Z is then deduced from the -3 dB cutoff frequency, f_Z, of this voltage: $C_Z = 1/2\pi f_Z R_Z$. Also note that, in order to obtain accurate values for R_Z and C_Z, it will often be necessary for this simulation to compensate the offset current existing on Z. Indeed the very important value of R_Z can lead, even for a very low value for the offset current, to an erroneous static operating point for the output transistors. The continuous offset current compensation will have to be applied on port X.

3.2. Experimental Determination

All the values for the parasitic impedances as well as β_0 and α_0 can be determined at frequencies inferior or equal to some hundred KHz by using a common measurement equipment. The determination of $\beta(s)$ and $\alpha(s)$, as well as their respective poles ω_β and ω_α require to undertake measures at high frequencies with the precautions of usage and the corresponding equipment [16]. The statement of the voltage gain variation $\beta(s)$ will be deduced from voltage measurements of V_X and V_Y for different frequencies with the same conditions as above (i.e., output Z grounded, port X open). Notice that it is necessary to measure the voltage on input Y well, since the equivalent output resistance R_g of the voltage generator produces with C_Y a pole ω_g that decreases V_Y when frequency increases (see Section 5.2).

The determination of the current gain $\alpha(s)$ can be obtained from voltage measurement, port Y grounded. Indeed, the input current I_X can be obtained from a voltage generator, V_e, adding a resistance R_e in series with input X: $I_X = V_e/(R_e + R_X)$. When a load resistance R_L is connected between Z and the ground (with $R_L \ll R_Z$) the output voltage is: $V_Z = R_Z \alpha(s) I_X$. It follows that $\alpha(s) = (V_Z/V_e)(R_e + R_X)/(R_L//R_Z)$. Notice that these measures do not pose particular problems at low frequency (resistances R_L and R_e on the

kΩ range are perfectly adapted). Nevertheless, it appears a parasitic pole located at $f_L = 1/2\pi R_L C_Z$. This will often necessitate to decrease the value of R_L (in order to increase f_L) and then to correct the response obtained by taking into account the attenuation due to this first order parasitic response.

The determination of the values for R_Y and C_Y, with X open and Z grounded, does not pose any particular problem. They are obtained from classical measures at low frequency. R_Y is deduced from the voltage V_Y when a voltage generator in series with a high resistance R_e is connected at Y. The value of C_Y is then deduced, as previously, from the -3 dB cutoff frequency, f_Y, of the voltage V_Y.

The value for the parasitic resistance R_X is easy to measure at low frequency, with X and Z grounded. A voltage generator V_e, in series with a resistance R_e being connected at X, the value of V_X will be equal to $V_e/2$ when $R_X = R_e$. The determination of the output impedance $(R_Z//C_Z)$ on port Z is done with the same conditions as above (Y grounded). The cancellation offset current (obtained from an adjustable DC voltage reference) being applied on port X through a resistance with high value R_{off}. A voltage generator V_e in series with a resistance connected at X (with $R_{\text{off}} \gg R_e$) generates the input current I_X. At low frequency, the voltage on Z is $V_{z\infty}$ when port Z is open. This voltage becomes $(V_{z\infty}/2)$ when a load resistance $R_L = R_Z$ is connected. The value for C_Z is then deduced as previously, from the -3 dB cutoff frequency, f_Z of the voltage V_Z with an infinite load R_L.

Table 1. (a) AC and DC characteristics for the CCII$^+$; ALA 200 bipolar arrays, with $V^+ = -V^- = 5$ V; $I_0 = 500$ μA.

AC Characteristics	
$\alpha_0 = 0.9914$	$\omega_\alpha = 3.8\ 10^9$ rad/s +3 dB bandwidth for α : 520 MHz
$\beta_0 = 0.999$	$\omega_\beta = 6.48\ 10^9$ rad/s −3 dB bandwidth for β : 1.03 GHz
$R_Y = 17.16$ MΩ $R_Z = 577$ KΩ $R_X = 30.2$ Ω	$C_Y = 1.4$ pF $C_Z = 1.2$ pF
DC Characteristics	
Input offset current at Y:	$I_{Y\text{off}} = 15.67$ μA
Output offset voltage at X:	$V_{X\text{off}} = 473$ μV
Output offset current at Z:	$I_{Z\text{off}} = -3.3$ μA

(b) AC and DC characteristics for the CCII$^-$; ALA 200 bipolar arrays, with $V^+ = -V^- = 5$ V; $I_0 = 500$ μA.

AC Characteristics	
$\alpha_0 = 1.005$	$\omega_\alpha = 3.8\ 10^9$ rad/s +3 dB bandwidth for α : 413 MHz
$\beta_0 = 0.999$	$\omega_\beta = 6.48\ 10^9$ rad/s −3 dB bandwidth for β : 1.03 GHz
$R_Y = 16.7$ MΩ $R_Z = 572$ KΩ $R_X = 30.2$ Ω	$C_Y = 1.5$ pF $C_Z = 1.2$ pF
DC Characteristics	
Input offset current at Y:	$I_{Y\text{off}} = 15.67$ μA
Output offset voltage at X:	$V_{X\text{off}} = 473$ μV
Output offset current at Z:	$I_{Z\text{off}} = -1.65$ μA

3.3. *Parasitic Elements of the Translinear Conveyors*

The values for the various elements of the equivalent circuit in Figure 3, relative to the two translinear conveyors deduced from Figures 2(a) and 2(b), have been determined from SPICE simulations. Nominal parameters for the transistors of the high performance bipolar array ALA200 from ATT were used. With a collector current about the mA, the transition frequencies of transistors NPN and PNP of this array [17] are respectively 4 GHz and 2.5 GHz. The two conveyors have been implemented from transistors with unit emitter areas (NPN1X and PNP1X). Table 1(a) and (b) give the values of the DC and AC parameters for the two conveyors supplied under ±5 V and with a bias current I_0 equal to 500 μA. Note that the DC offsets cannot degrade the frequency responses of circuits using conveyors. They could be compensated if necessary. They could also be reduced by using appropriate implementations for the conveyors. As for example, the input offset current at Y is reduced from 15.67 μA to 1.5 μA when two complementary cascode mirrors are used to generate I_0 from a single current source. Considering the AC characteristic, note that for the two conveyors the values for the resistances R_X vary from less than 20% in the range 0–360 MHZ. Figure 4 represents the variations of the current transfers $\alpha(s)$ according to the frequency of the signal, for the two conveyors. The two representative curves of $\beta(s)$ are practically superimposed for both circuits (Figure 5). The assimilation of $\alpha(s)$ and $\beta(s)$ variations to first order transfers in a purpose of simplification, as indicated by equations (2) and (3) and Tables 1 and 2, establishes to be often well sufficient.

Table 2. Characteristics of the amplifier in Figure 9, with $(R_X + R_1) = 100\ \Omega$.

G_0		R_2	−3 dB Bandwidth (MHz)		Slew Rate for $V_{out} = 1$ V ($V/\mu s$)	
Theoretical	Simulated	(Ω)	Theoretical	Simulated	Theoretical	Simulated
5.0	5.0	500.43	122	140	766	739
50.0	50.0	5.044 K	12.2	11.7	76.8	76.6
500	503	54.74 K	1.2	1.16	7.5	7.4

In some cases however (when for example the phase rotation plays the preponderant role) the two current transfers $\alpha(s)$, whose cutoff frequencies are the lowest, will be assimilated to lowpass higher order transfer functions.

4. Understanding the Frequency Limitations of Circuits Using Conveyors

4.1. *Effect of* $\alpha(s)$ *and* $\beta(s)$

The values of α_0 and β_0 for the CCII$^+$ and the CCII$^-$ are equal at low frequency to the unit with a precision better than 0.87% (see Table 1(a) and (b)). The poles of the voltage transfers ω_β for the two translinear conveyors are located at high frequencies (see Table 1(a) and (b)) so that the effect of $\beta(s)$ can generally be neglected. For example at 370 MHz, the phase rotation is only 10 degrees, while the magnitude variation, as compared to β_0, is inferior to 0.34 dB. The poles for the current transfers ω_α are located at lower frequencies (see Table 1(a) and (b)). For the CCII$^+$ the phase rotation is around 10 degree at 100 MHz. At this frequency, the magnitude variation is equal to 0.12 dB as compared with α_0. For the CCII$^-$, these values are, respectively, for the same frequency: 13.1 degrees and 0.2 dB. Thus, the impact of $\alpha(s)$ can generally be neglected until relatively high frequencies like about 100 MHZ for the CCII$^+$ and the CCII$^-$.

As shown in the following section by the theoretical analysis, low phase rotations and low magnitude variations (this induces low variations for Q and ω_0 in the case of filtering) may result around these frequencies principally due to the deviations of $\alpha(s)$.

4.2. *Effects of the Parasitic Impedances*

These parasitic effects will be determined considering the equivalent circuit on each port X, Y, and Z when a load resistance is connected.

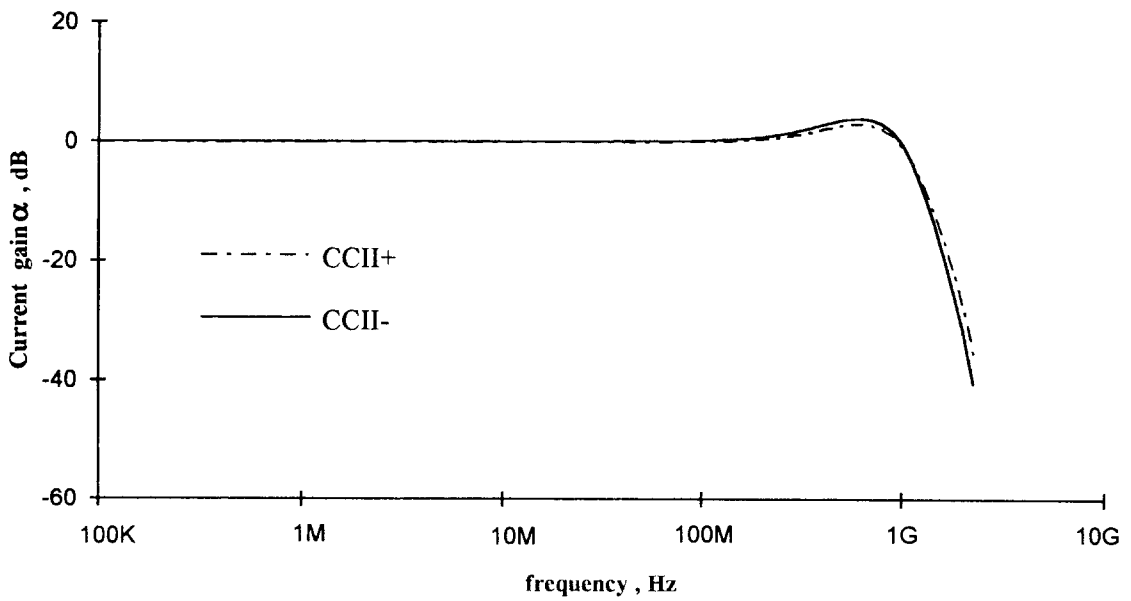


Fig. 4. Frequency variation of the current gains α for the conveyors in Figure 2; ALA 200 bipolar arrays, with $V^+ = -V^- = 5$ V; $I_0 = 500\ \mu$A.

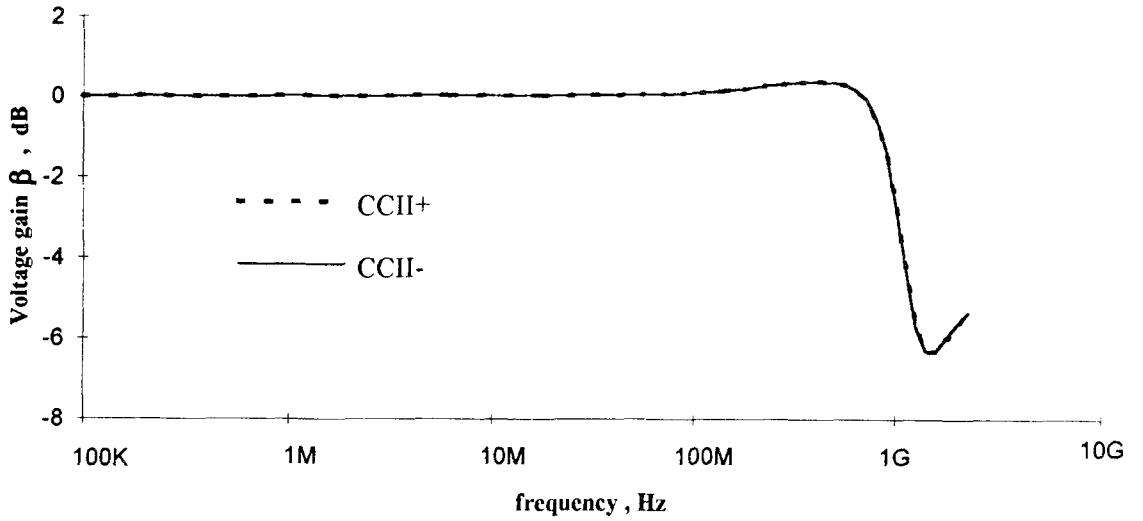


Fig. 5. Frequency variation of the voltage gains β for the conveyors in Figure 2; ALA 200 bipolar arrays, with $V^+ = -V^- = 5$ V; $I_0 = 500\ \mu$A.

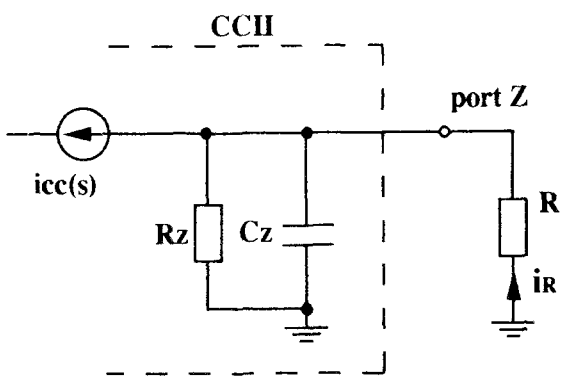


Fig. 6. Equivalent circuit with a load resistor R connected at port Z.

Figure 6 represents the circuit to be considered when a resistance is connected between port Z and the ground. $I_{CC}(s)$ is the short-circuited output current on this port. In the ideal case (i.e., without parasitic elements R_Z and C_Z) the current $I_{CC}(s)$ would be flowing in the resistance R. The current $I_R(s)$ that really flows through R is given by

$$I_R(s) = \frac{R_Z}{R_Z + R} \frac{1}{1 + (R_Z, /R)C_Z s} I_{CC}(s) \qquad (5)$$

This relationship shows that the value of $I_R(s)$ will be valid at low frequency if the condition $R \ll R_Z$ is satisfied. In this condition, a pole appears at the frequency $\omega_{ZR} = 1/(RC_Z)$. Then, the ideal transfer will be only valid for frequencies lower than $\omega_{ZR}/10$. Note that the value of ω_{ZR} will increase as R decreases. When the load R shown in Figure 6 is replaced by a capacitor C, the current $I_C(s)$ flowing through C can be expressed as

$$I_C(s) = \frac{C}{C + C_Z} \frac{R_Z(C + C_Z)s}{1 + R_Z(C + C_Z)s} I_{CC}(s) \qquad (6)$$

Now, the ideal value of $I_C(s)$ will be valid at high frequency when the condition $C \gg C_Z$ is satisfied. Equation (6) corresponds to a first highpass transfer. Therefore the expected ideal current $I_C(s)$ will not be valid for frequencies lower than $10\ \omega_{ZC}$; with $\omega_{ZC} \cong 1/R_Z C$.

Figure 7 represents the equivalent circuit which has to be considered when a resistance is connected between port Y and the ground. Without the parasitic elements R_Y and C_Y, the impedance on this port is equivalent to R, but in fact it is effectively equal to

$$Z_{YR} = \frac{(R//R_Y)}{1 + (R//R_Y)C_Y s} \qquad (7)$$

So, it is necessary to have a small value for R in comparison with R_Y. However, for frequencies higher than $0.1\ \omega_{YR}$ (with $\omega_{YR} \cong 1/RC_Y$) this impedance will move away from the value wished. When on the

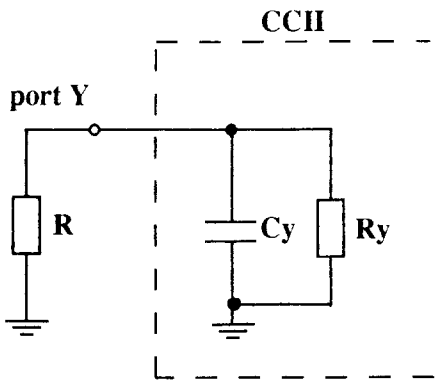


Fig. 7. Equivalent circuit with a load resistor R connected at port Y.

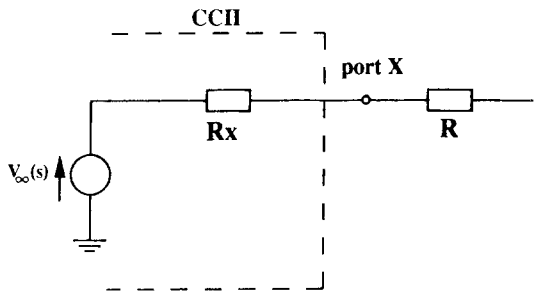


Fig. 8. Equivalent circuit with a load resistor R connected at port X.

circuit of Figure 7 the resistance R is replaced by a capacitor C, similarly the calculation of the equivalent impedance Z_{YC} shows that the value of C will have to be chosen greater than C_Y. In the same way, this impedance will keep off the value $1/Cs$ wished for the frequencies lower than $10\,\omega_{YC}$, with $\omega_{YC} \cong 1/R_Y C$.

In Figure 8, the equivalent circuit to consider when a resistance R is connected to port X is represented. This resistance appears in series with the parasitic resistance R_X (see Section 2.3). Therefore, it will be necessary to consider the value $(R + R_X)$ in place of the ideal value R. When on the circuit shown in Figure 8, the resistance R is replaced by a capacitor C, the equivalent impedance that effectively has to be considered is equal to

$$Z_{XC} = \frac{1 + R_X Cs}{Cs} \tag{8}$$

instead of the value $1/Cs$ with the ideal conveyor. Then, for frequencies higher than $0.1\ \omega_{XC}$ (with $\omega_{XC} = 1/R_X C$) the effective impedance moves away from the ideal value $1/Cs$. Also note that ω_{XC} increases as C decreases. All the theoretical analyses above have demonstrated that the parasitic impedances of the conveyors tend to modify the true nature of the transfer functions. Therefore, on some frequency range, the obtained transfers may differ considerably from the one expected.

We will illustrate this, in the following sections, in the cases of amplification and filtering.

5. Amplifier Example

5.1. Implementation

The voltage amplifier which will be considered is represented in Figure 9. It comprises two CCII$^+$ and uses two successive conversions: current-voltage and voltage-current achieved by the first conveyor. It does not use feedback. The second conveyor, whose output Z not used is grounded, acts as a voltage follower which allows to obtain low value for the output impedance of the amplifier. In Figure 9, the equivalent voltage source (E_g, R_g) of the preceding stage which drives at the input of the amplifier has also been represented.

5.2. Characteristics of the Amplifier

When we consider the equivalent circuit of the conveyor (Figure 3), the expression for the input voltage V_{in} of the amplifier is

$$V_{\text{in}} = \frac{R_Y}{R_Y + R_g} \frac{1}{1 + (R_Y // R_g) C_Y s} E_g \tag{9}$$

This relationship shows that this transfer will not exhibit any attenuation at low frequency if the condition $R_Y \gg R_g$ is satisfied. Note that this relationship will generally be always satisfied because of the high value of R_Y. This transfer is a first order lowpass with a pole located at $\omega_Y = (1/R_g C_Y)$. Thus, the limitations induced by the driving stage of the amplifier will become insignificant when R_g is small.

Then, taking into account the parasitic elements of both conveyors (which will be assumed identical) the voltage gain G_v of the amplifier can be expressed for an infinite load as

$$G_v = \frac{V_{\text{out}}}{V_{\text{in}}} = G_0 \frac{\alpha(s)\beta^2(s)}{1 + (R_2 // R_Y // R_Z)(C_Y + C_Z)s} \tag{10}$$

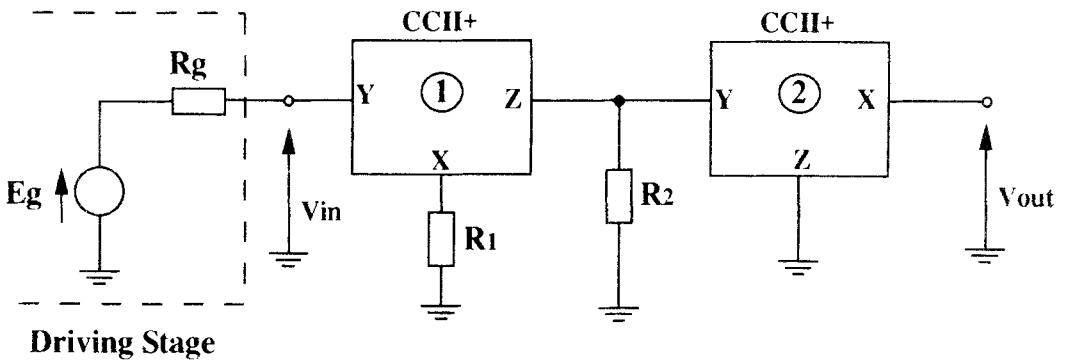


Fig. 9. Voltage amplifier implemented from CCII$^+$.

In the expression above, G_0 is the value of the amplifier gain at low frequency:

$$G_0 = \frac{(R_2//R_Y//R_Z)}{R_1 + R_X} \tag{11}$$

These relationships well illustrate the effects of all the parasitic elements that have to be taken into account to calculate the value for G_0 and also to determine the frequency response of the amplifier. Equation (10) indicates that the response of the amplifier is dependent on four poles. The pole ω_β (which is a double pole), relative to $\beta(s)$, is very high (see Tables 1(a,b). It has generally to be taken into account only for low values of G_0. This is the same for the pole ω_α relative to $\alpha(s)$. The last pole

$$\omega_Z = \frac{1}{(R_2//R_Y//R_Z)(C_Y + C_Z)} \tag{12}$$

whose value is practically equal to $1/(R_2(C_Y + C_Z)$, when $R_2 \ll (R_Y//R_Z)$, has to be considered for intermediate values of G_0. Therefore, its action will become preponderant when the value of R_2 is such that

$$R_2 \gg \frac{\omega_\alpha, \omega_\beta}{(C_Y + C_Z)} \tag{13}$$

5.3. *Compensated Amplifier*

The equations (10) and (11) above show that the pole ω_Z, whose value becomes preponderant for high values of G_0, can partly be compensated by placing a capacitor C_1 in parallel with resistance R_1 (Figure 10). The expression for the voltage gain of the amplifier in Figure 10 now becomes

$$G_v = \frac{V_{\text{out}}}{V_{\text{in}}} = G_0 \frac{\alpha(s)\beta^2(s)(1 + R_1C_1s)}{\left(1 + \frac{s}{\omega_Z}\right)(1 + (R_1//R_X)C_1s))} \tag{14}$$

Thus, when the value of C_1 is equal to

$$C_1 = G_0\left(1 + \frac{R_X}{R_1}\right)(C_Y + C_Z) \tag{15}$$

in order to compensate exactly the pole ω_Z, by a zero located at the same frequency, equation (14) becomes

$$G_v = \frac{V_{\text{out}}}{V_{\text{in}}} = G_0 \frac{\alpha(s)\beta^2(s)}{(1 + G_0R_X(C_Y + C_Z))} \tag{16}$$

Then, a new pole appears located at $\omega_{Z\,\text{comp.}} = (1/G_0R_X(C_Y + C_Z))$. This is characterized by the value of G_0 and the parasitic elements of the CCII$^+$. This new pole located at higher frequency than the initial pole is

$$\omega_{Z\,\text{comp.}} = \left(1 + \frac{R_1}{R_X}\right)\omega_Z \tag{17}$$

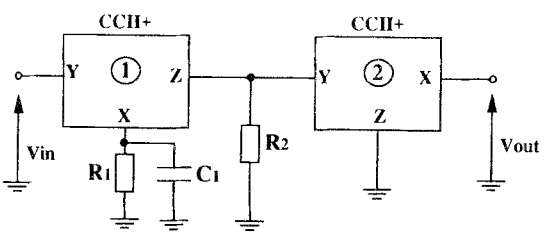


Fig. 10. Frequency compensated voltage amplifier.

Table 3. Characteristics of the compensated amplifier in Figure 10, with $(R_X + R_1) = 100\ \Omega$.

G_0	C_1 (pF)	−3 dB Bandwidth (MHz)		Slew Rate for $V_{out} = 1$ V ($V/\mu s$)	
		Theoretical	Simulated	Theoretical	Simulated
5.0	18.7	405	425	2544	1721
50.0	187	40.5	40.3	254	195.6
503	1870	4.05	6.42	25	24

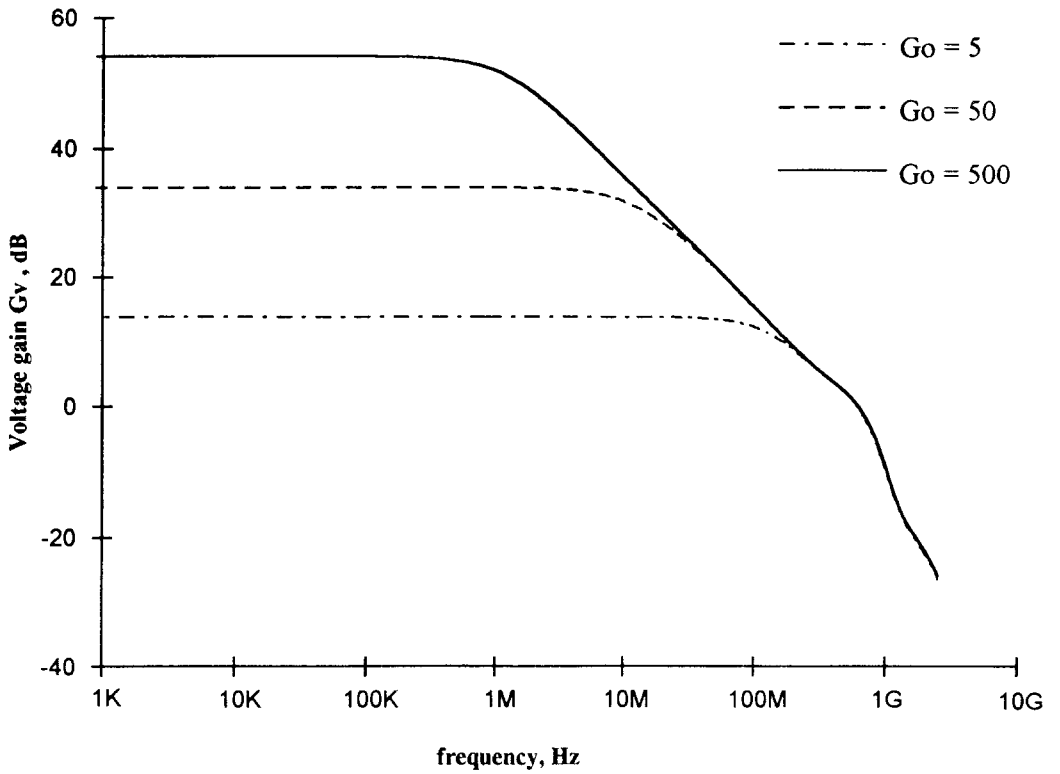


Fig. 11. Simulated frequency responses for the voltage amplifier with $(R_X + R_1) = 100\ \Omega$.

5.4. Simulation Results and Discussion

Features of the amplifier in Figure 9 have been characterized by simulation using the conveyor described in Section 3.3. Figure 11 represents the frequency response $G_v(s)$ of the amplifier obtained for several values of the gain G_0, with $(R_1 + R_X) = 100\ \Omega$. The evolution of the pole ω_Z, according to the value of R_2, appears well on this figure. Table 2 summarizes, the characteristics of the amplifier determined by simulation in these conditions. We have also indicated the theoretical values calculated from previously set relationships. The values of R_2 were determined from G_0 by taking into account the values of the parasitic resistances R_Y and R_Z (equation (11)). To calculate the theoretical values for the slew rate (SLWR), we have supposed that the amplifier behaves as a first order low-pass filter, so that the slew rate can be expressed as a function of its corresponding −3 dB cutoff frequency f_C by SLWR $= 2\pi f_C V_{out}$. We have chosen, for these measures, an output voltage magnitude equal to 1 V. Afterwards, the amplifier was compensated as shown in Figure 10, the value of C_1 being calculated from the equation (15). Its characteristics were also determined as previously. Figure 12 represents the responses obtained for three values of G_0 (5, 50, and 500). Its

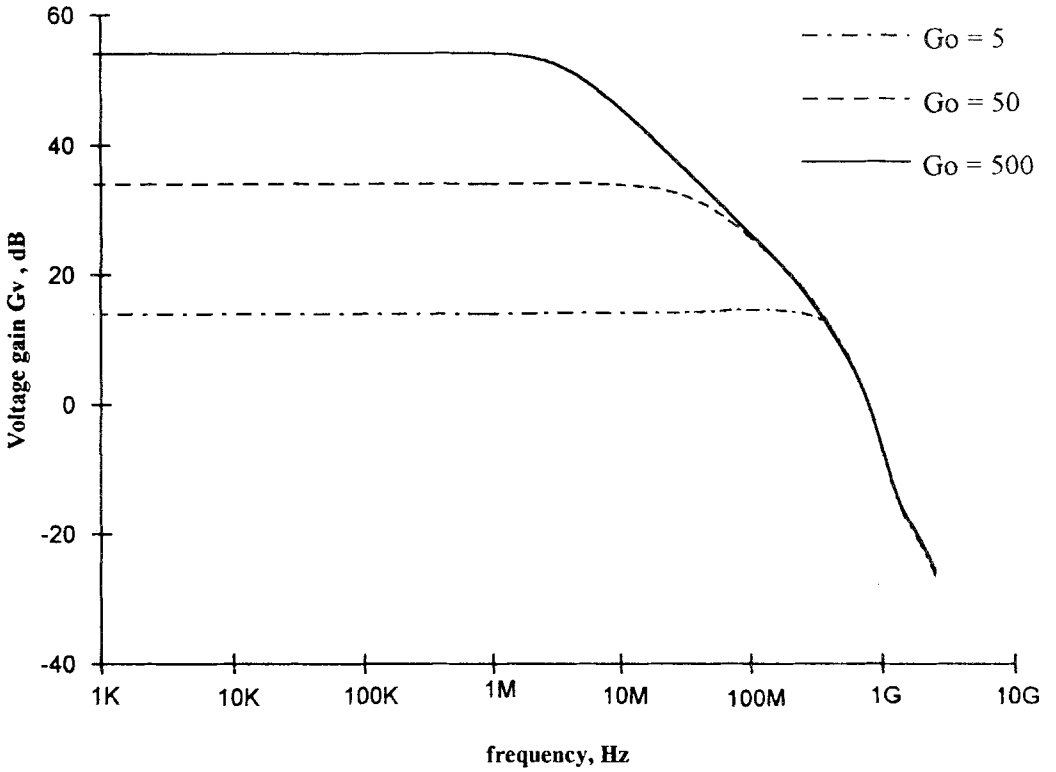


Fig. 12. Simulated frequency responses for the compensated voltage amplifier $(R_X + R_1) = 100\ \Omega$.

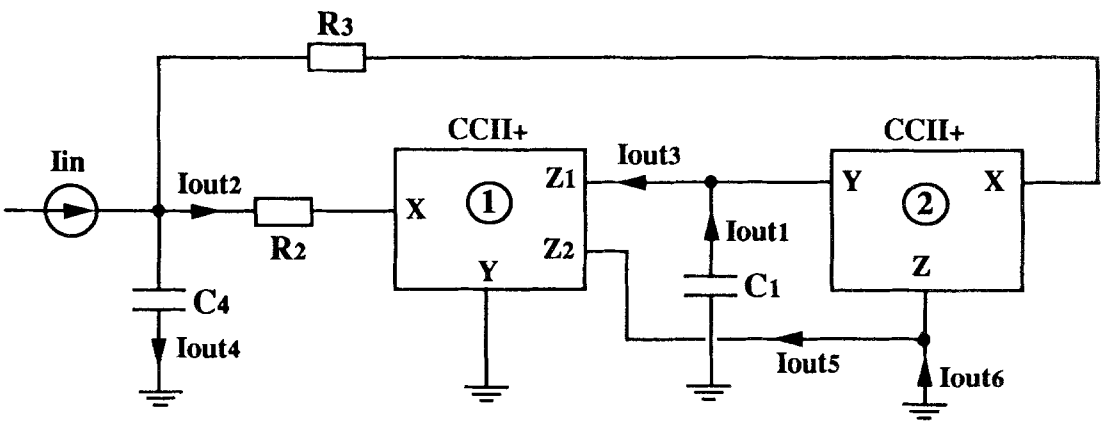


Fig. 13. Second order current mode biquad (configuration A).

characteristics are summarized in Table 3. The results in Tables 2 and 3 indicate a good agreement between theoretical and simulated values. They illustrate well the importance of the parasitic elements of the conveyors. They also underline the possibility that exists to take some advantage of them.

6. Current-Mode Filter Example

6.1. Two Basic Implementations

Figure 13 represents the first configuration for an insensitive second order filter (that we will call circuit A)

implemented from second generation current conveyors. The CCII$^+$ possesses two identical outputs Z that we have noted Z_1 and Z_2. The second output is obtained by just adding the transistors necessary for the constitution of a second output on each of the two complementary current mirrors that form the output Z of the conveyor in Figure 2(a). When $R_2 = R_3$, the filter, whose input and output variables are currents, is a biquad as it comprises the three second order elementary transfers (i.e., lowpass, bandpass, and highpass). The bandpass transfer is also available in several branches of the circuit. This will allow to explain the impact of the parasitic elements and to show that for a same transfer, all outputs will not always be equivalent because of these parasitic elements. When both conveyors are supposed to be without parasitic impedances, the expressions of the various transfers are

$$G_1(s) = \frac{I_{\text{out4}}}{I_{\text{in}}} = \frac{\left(\frac{R_2R_3C_1C_4}{\alpha_1\beta_2}\right)s^2}{1 + \left(\frac{R_2+R_3}{\alpha_1\beta_2}\right)C_1s + \left(\frac{R_2R_3C_1C_4}{\alpha_1\beta_2}\right)s^2} \tag{18}$$

$$G_2(s) = \frac{I_{\text{out1}}}{I_{\text{in}}} = \frac{\left(\frac{R_3C_1}{\alpha_1\beta_2}\right)s}{1 + \left(\frac{R_2+R_3}{\alpha_1\beta_2}\right)C_1s + \left(\frac{R_2R_3C_1C_4}{\alpha_1\beta_2}\right)s^2} \tag{19}$$

$$G_3(s) = \frac{I_{\text{out6}}}{I_{\text{in}}} = \frac{-\alpha_2 + (\alpha_1R_3 - \alpha_2R_2)C_1s}{1 + \left(\frac{R_2R_3}{\alpha_1\beta_2}\right)C_1s + \left(\frac{R_2R_3C_1C_4}{\alpha_1\beta_2}\right)s^2} \tag{20}$$

In these expressions the indexes 1 and 2 for the transfers α and β are respectively related to the numbers of each current conveyor that we have indicated in Figure 3. $G_1(s)$ and $G_3(s)$ will be respectively highpass and lowpass functions with unit gain, as long as the transfers α_1, α_2, and β_2 remain very close to the unit because resistances R_2 and R_3 are equal.

$G_2(s)$ is a bandpass function having at ω_0 a gain magnitude equal to $R_3/(R_2 + R_3) = (1/2)$. As with ideal conveyors $I_{\text{out1}} = I_{\text{out3}} = I_{\text{out5}} = (1/a_1)I_{\text{out2}}$, it follows that this bandpass function is also available in several branches of the circuit. These transfer functions are also characterized by

$$\omega_0 = \left(\frac{\alpha_1\beta_2}{R_2R_3C_1C_4}\right)^{1/2} \tag{21}$$

$$Q = (\alpha_1\beta_2R_2R_3)^{1/2}(R_2 + R_3)^{-1}\left(\frac{C_4}{C_1}\right)^{1/2} \tag{22}$$

The second configuration for the filter, which will be called circuit B, is obtained by replacing resistances R_2 and R_3, respectively, by capacitors C_2 and C_3, and in the same way C_1 and C_4 by resistances R_1 and R_4. The biquad will be obtained here when capacitors C_2 and C_3 have identical values. Therefore, the expressions and the characteristics of the transfer functions are easily deduced from equations (18) to (22) above. Then we obtain

$$G_1(s) = \frac{I_{\text{out4}}}{I_{\text{in}}} = \frac{1}{1 + R_4(C_2 + C_3)s + (\alpha_1\beta_2R_1R_4C_2C_3)s^2} \tag{23}$$

$$G_2(s) = \frac{I_{\text{out1}}}{I_{\text{in}}} = \frac{R_4C_2s}{1 + R_4(C_2 + C_3)s + (\alpha_1\beta_2R_1R_4C_2C_3)s^2} \tag{24}$$

$$G_3(s) = \frac{I_{\text{out6}}}{I_{\text{in}}} = \frac{-\alpha_1\beta_2(\alpha_2R_1R_4C_2C_3s^2 + R_4(\alpha_2C_3 - \alpha_1C_2)s)}{1 + R_4(C_2 + C_3)s + (\alpha_1\beta_2R_1R_4C_2C_3)s^2} \tag{25}$$

$$\omega_0 = (\alpha_1\beta_2R_1R_4C_2C_3)^{-1/2} \tag{26}$$

$$Q = (\alpha_1\beta_2C_2C_3)^{1/2}(C_2 + C_3)^{-1}\left(\frac{R_1}{R_4}\right)^{1/2} \tag{27}$$

Now, $G_1(s)$ and $G_3(s)$ becomes respectively a lowpass and a highpass with unity gain (because $C_2 = C_3$) as long as the transfers of the conveyors remain very close to the unit. $G_2(s)$ remains a bandpass function with a gain magnitude equal to 1/2 at ω_0.

6.2. *Frequency Limitations Due to the Parasitic Elements*

Calculations on equations (18) to (22), and (23) to (27) indicate that all the passive and active sensitivities related to ω_0, Q, and the gains are, for both configurations of the filter, inferior or equal to unit. In consequence, these two filters can be classified as insensitive [1, 18, 19]. Besides, as already previously indicated, the incidence of the transfer conveyors $\alpha(s)$ and $\beta(s)$ on the

values of ω_0, Q, and the gains will be negligible as long as ω_0 remains much smaller than ω_α and ω_β. This is not the same for the parasitic impedances depending on the configuration (A or B) of the filter and the values of the passive components, they can affect in an important manner the different transfer functions. Thus, for circuit A, the values of the resistances R_2 and R_3 that will have effectively to be taken into account in the various expressions are $(R_2 + R_X)$ and $(R_3 + R_X)$, because of the parasitic resistance R_X on ports X. The current I_{out1}, which flows through capacitor C_1 connected on ports Z and Y, will be equal to the calculated value only if $C_1 \gg (C_Y + C_Z)$. Thus, we obtain on the frequency range where the parasitic impedance $(R_Y // R_Z)$ does not have to be taken into account:

$$I_{out1}(s) = \frac{C_1}{C_1 + C_Y + C_2} I_{ZCC}(s) \quad (28)$$

Besides, the transfer functions will become incorrect at frequencies lower than $10\,\omega_{ZYC}$. The frequency ω_{ZYC} is defined by

$$\omega_{ZYC} \cong 1/(R_Y // R_Z)C_1 \quad (29)$$

For circuit B, the capacitors C_2 and C_3 appear in series, on port X, with the parasitic resistance R_X. Thus, as indicated in Section 4.2 the transfer function will be incorrect for frequencies higher than approximately $0.1\,\omega_{XC}$ (the incidence coming here from both C_2 and C_3).This frequency is defined (with $C_2 = C_3$) by

$$\omega_{XC} = 1/(R_X C_2) \quad (30)$$

Similarly, as for circuit A, the current I_{out1} that flows into R_1 can be expressed as a function of the corresponding conductances by

$$I_{out1}(s) = \frac{G_1}{G_1 + G_Y + G_Z} I_{ZCC}(s) \quad (31)$$

Therefore, on the frequency range where the parasitic capacitor $(C_Y + C_Z)$ does not have to be taken into account, this current will be found lessened if the condition $R_1 \ll (R_Y // R_Z)$ is not satisfied. Besides, the deformation of the transfer functions will appear for frequencies higher than $0.1\,\omega_{ZYR}$. This frequency is defined by

$$\omega_{ZYR} = 1/R_1(C_Y + C_Z) \quad (32)$$

6.3. *Simulation Results and Discussion*

The limitations due to the parasitic impedances established in the sections above show for circuit A that all increase of the value of the capacitor C_1 induces an expansion of the range of frequency on which the transfer functions are exactly valid. However considering the bandpass output (and in consequence the highpass, too), this transfer response remains exactly valid for $\omega_0 \gg \omega_{ZYC}$; ω_0 is the central frequency of the filter in equation (21); ω_{ZYC} is defined by equation (29). The current I_{out1} will however be lessened if condition $C_1 \gg (C_Y + C_Z)$ is not satisfied. This attenuation will not be harmful because the bandpass function is also available for example on the output port Z_2.

With circuit B, it is noticed that when ω_0 and Q are fixed (equations (26) and (27)) it will not be possible to decrease both the capacitor values $C_2 = C_3$ (to increase ω_{XC} (equations (30)) and R_1 (to increase ω_{ZYR} (equation (32)). This second configuration is therefore less interesting than the precedent. Indeed it will not allow to take advantage of the high frequency potentialities of translinear CCIIs.

So as to confirm the preceding theoretical analysis, we have determined from SPICE simulations, using the translinear conveyors described in Sections 2.2 and 2.3, the frequency responses of the two configurations of this filter. The values of the components have been calculated in order to obtain a theoretical central frequency f_0 at 3.16 MHz and a Q-factor equal to 4.96. In the calculations, as already indicated, the values of the parasitic impedances were taken into account. The used component values were respectively: $R_2 = R_3 = 1\,\text{K}\Omega$; $C_4 = 500\,\text{pF}$; $C_1 = 2\,\text{pF}$ (circuit A); $C_2 = C_3 = 500\,\text{pF}$; $R_4 = 100\,\Omega$; $R_1 = 10\,\text{K}\Omega$ (circuit B). Figure 14 which represents the bandpass transfers available in I_{out5} (see Figure 13) for both configurations of the filter underlines the superiority of circuit A and well confirms the theoretical analysis. In Table 4, we have indicated the simulated values for the parameters of the two configurations in conjunction with theoretical values. The values indicated for the gains are those relative to the output I_{out5}. If for circuit A, the obtained values are in good agreement with theoretical ones, this is not the same for circuit B. In Table 5 are indicated the gain magnitudes at f_0 for the various bandpass outputs of each of the two configurations of the filter (see Figure 13). These values also validate perfectly the preceding analysis (equations (28) for circuit A, and (31)

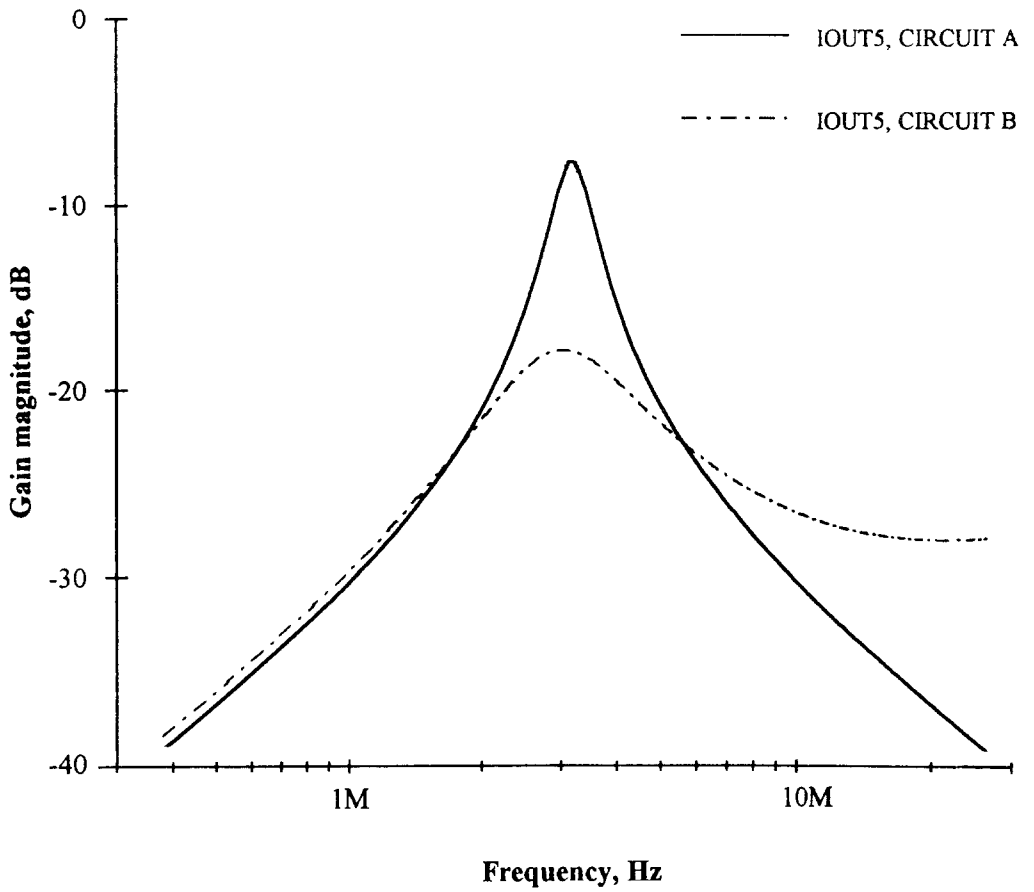


Fig. 14. Frequency responses for the bandpass output I_{out5} for circuits A and B.

Table 4. Theoretical and simulated values for the parameters of circuits A and B.

Parameter	Theoretical Value	Circuit A	Circuit B
f_0 (MHz)	3.16	3.18	3.02
Q factor	4.96	4.88	1.23
Gain (dB)	−6	−7.68	−17.8

Table 5. Gain magnitudes at f_0 for the bandpass outputs of circuits A and B.

Output Current	Theoretical Value	Circuit A	Circuit B
I_{out1}	−6 dB	−14 dB	−18.1 dB
I_{out2}	−6 dB	−6.52 dB	−17.1 dB
I_{out3}	−6 dB	−9.1 dB	−31.3 dB
I_{out5}	−6 dB	−7.68 dB	−17.8 dB

for circuit B). They also confirm the superiority of circuit A. Also notice that for circuit A, the magnitude values of current on ports X and Z_2 of the CCII$^+$ are, well obviously, the closest to the theoretical ones. These currents are practically identical to the short circuit output currents of ports Z_1 and Z_2 of the CCII$^+$. Indeed, they include the currents flowing through the parasitic capacitors in parallel with C_1. On the contrary, I_{out3} comprises the current which flows through the parasitic capacitor C_Y , but it does not include the current through C_{Z1}. Figure 15 and Figure 16 represent respectively the lowpass and highpass transfers of each of the two circuits. They also show that the responses are not correct for circuit B. In Figure 16 and for circuit A, we can notice a modification of the asymptotic slope of the response. This occurs for a frequency of about 60 KHz. This is in perfect agreement with the theoretical analysis (ω_{ZYC}, in equation (29)) when we take into account the effective value of the capacitor: $(C_1 + C_Y + C_{Z1})$ on output Z_1 and its corresponding parasitic resistance $(R_Y // R_{Z1})$. This slope variation

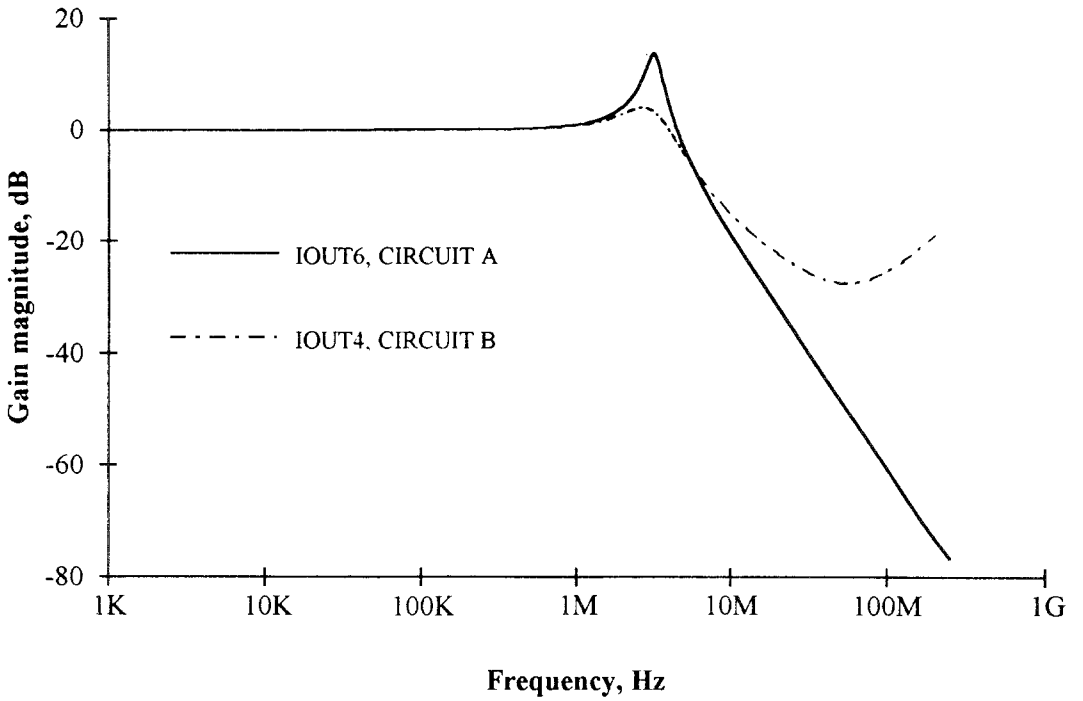


Fig. 15. Frequency responses for the lowpass outputs for circuits A and B.

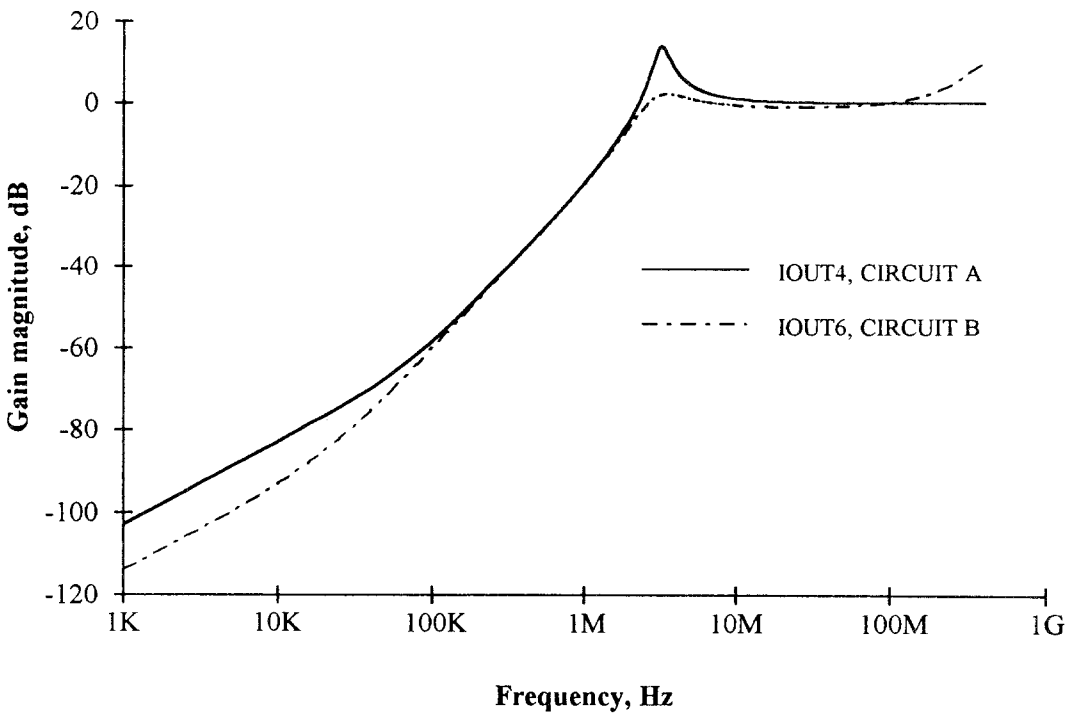


Fig. 16. Frequency responses for the highpass outputs for circuits A and B.

also occurs on the bandpass response, but this will be without effect because $\omega_0 \gg \omega_{ZYC}$. However it does not affect the lowpass output as indicated in Figure 15. Indeed, at low frequencies, the corresponding output currents I_{out6} is directly built from currents flowing through the resistances R_2 and R_3, and whose sum is equal to I_{in}.

A limitation of circuit A, such that it is represented in Figure 13, comes from the value of the ratio C_4/C_1 that for $R_2 = R_3$ is equal to $4Q^2$. Two possibilities simultaneously usable allow however to decrease the value of C_4:

(i) to suppress the capacitor C_1 and to use only the parasitic capacitor $(C_Y + C_{Z1})$, as the bandpass output current is again available in I_{out5}. We have checked that this circuit works always correctly and that the gain of this output is similar to that indicated in Table 5.

(ii) to increase, in a same ratio, the emitter areas of the output transistors of the current mirrors which form the outputs Z_1 and Z_2 of the CCII$^+$ and Z of the CCII$^-$ (this is equivalent to use for α_1 and α_2 equal values which are greater than the unit). Thus, for the same value of the ratio C_4/C_1, both values of ω_0 and Q become multiplied by $(\alpha_1)^{1/2}$.

7. Conclusion

First at all in this paper we have underlined the differences existing between the ideal and real conveyors. The parasitic elements of the second generation current conveyors implemented in their translinear form have been determined. The way to take it into account for the various analysis has also been indicated. Then, we have considered as an example a voltage amplifier without feedback and two configurations for a 2$^{\text{nd}}$ order biquad filter operating in current-mode. We have analyzed them and put in obviousness their limitations due to the parasitic elements of the conveyors. We have also indicated the better ways to take profit of it, when this is possible. The various theoretical analyses have always been confirmed by SPICE simulation results. This paper also underlines the precautions to have to take during the design of circuits using current conveyors. It also shows that some circuits previously published in the literature will only be able to function correctly at low frequency, because the parasitic impedances modify considerably the nature of the transfer responses at high frequencies.

References

1. Fabre, A., Alami, M., "Insensitive current-mode biquad implementation based on translinear current conveyors," *IEEE Proceedings of the EUROASIC'90 Conf.*, pp. 126–130, Paris, 2–4 June, 1992.
2. Toumazou, C., Lidgey, F. G., Haigh, D. G., *Analog IC Design: The Current Mode Approach*, Peter Peregrinus: London, 1990.
3. Wilson, B., "Recent developments in current conveyors and current mode circuit," *IEE Proceedings*, Pt. G, Vol. 137, pp. 63–77, 1990.
4. Sedra, A. S., Smith, K. C., "A second generation current conveyor and its applications," *IEEE Transactions on Circuit Theory*, Vol. CT17, pp. 132–134, 1970.
5. Sedra, A. S., Roberts, G. W., Gohh, F., "The current conveyor: history, progress and new results," *IEE Proceedings*, Pt. G, Vol. 137, pp. 78–87, 1990.
6. Fabre, A., Alami, M., "A versatile translinear cell-library to implement high performance analog ASICS," *IEEE Proceedings of the EUROASIC'90 Conf.*, pp. 89–94, Paris, 29–31 May, 1990.
7. Wilson, B., "High performance conveyor implementation," *Electronics Letters*, Vol. 20, pp. 990–991, 1984.
8. Fabre, A., "Translinear current conveyors implementation," *International Journal of Electronics*, Vol. 59, pp. 619–623, 1985.
9. Huertas, J. L., "Circuit implementation of current conveyor," *Electronics Letters*, Vol. 15, pp. 225–226, 1980.
10. Normand, G., "Translinear current conveyor," *International Journal of Electronics*, Vol. 59, pp. 771–777, 1985.
11. Wilson, B., "Current-mode circuits: Analysis and CAD modeling," *IEEE International Symposium on Circuits and Systems*, New Orleans, pp. 3242–3245, May 1990.
12. Wilson, B., "Performance analysis of current conveyors," *Electronics Letters*, Vol. 25, pp. 1596–1598, 1989.
13. Celma, S., Martinez, P. A., and Carlosena, A., "Minimal realisation for single resistor controlled sinusoidal oscillator using single CCII," *Electronics Letters*, Vol. 25, pp. 443–444, 1992.
14. Martinez, P. A. and Celma, S., "Design condition for sinusoidal oscillators using single CCII$^+$," *International Journal of Electronics*, Vol. 75, pp. 87–90, 1993.
15. Koli, K. and Halonen, K., "Current-conveyor subscriber line interface circuits," *IEEE International Symposium on Circuits and Systems*, pp. 1384–1387, 1992.
16. HP4396, *1.8 GHz Network and Spectrum Analyser, Technical Data*, 1993, Palo Alto, CA 94304: Hewlett Packard.
17. *ALA200 Family, Instruction Manual*, Allentown, PA 18103: AT&T Microelectronics, 1989.
18. Fabre, A., "Insensitive voltage-mode and current-mode filters from commercially available transimpedance op amps," *IEE Proceedings*, Pt. G, Vol. 140, pp. 319–321, 1993.
19. Fabre, A. and Alami, M., " Insensitive current-mode bandpass filter implemented from two current conveyors," *Electronics Letters*, Vol. 27, pp. 897–899, 1991.

Alain Fabre was born in Perpignan, France, in 1947. He took the M.S. degree in electronics in 1972 and the Ph.D. (Thése de 3ème cycle) in physics in 1974, both from the University of Bordeaux, France. His Ph.D. research was concerned with the development of a tunable spectrometer for the 12–18 GHz range. From 1974 to 1987, he was employed as an assistant professor in electronics in a cooperation program with the University of Oran, Algeria. In this university in 1983, he started researches concerning the exploitation of translinear elements in the design of analog circuits. In 1987, he received for this work the Post Doctoral Thesis (Thése d'état) in physics from the University of Perpignan, France. In September 1987, he joined the Ecole Centrale Paris, France, where he is currently an assistant professor in electronics, teaching graduate and undergraduate courses. Since 1988, he is the head of the analog IC design group at the Laboratoire d'Electronique et de Physique Appliquée at the Ecole Centrale Paris, France. In 1983 and 1984 in Algeria, Alain published (O.P.U, Algiers) 2 volumes of a book devoted to the practical aspects of electrical and electronic measures. He is also the author or coauthor of about 50 papers published in scientific reviews or conference proceedings. His current field of research concerns principally the various areas of design of high speed analog circuits, analog filters, ASICs, current mode circuits as well as the theoretical tasks of translinear circuits. His leisure interests include smimming, yoga, walking, painting, and photography.

Omar Saaid was born in Beni-Mellal, Morocco, in 1966. He received the Diplôme d'Etudes Supérieures Spécialisées degree (D.E.S.S.) in electrical engineering in 1990 from the University of Rennes I, France, and the M.Sc. degree in electrical engineering in 1991 from the National Polytechnic Institute of Toulouse, France. He received the Ph.D. degree in January 1995, from the Ecole Centrale Paris, France working at the analog IC design group of the Laboratoire d'Electronique, Physique Appliquée at the Ecole Centrale of Paris. His main research interests are design of current-mode analog integrated circuits in translinear form as well as analog signal processing applications.

Hervé Bathelemy was born in Antony, France, in 1967. He received the bachelor's degree and the master's degree in electrical engineering from the Institut d'Electronique Fondamentale at the University of Paris XI Orsay, France, in 1990 and 1992, respectively. He is currently studying toward the Ph.D. degree, sponsored by the French government, in electronics at the University of Paris XI Orsay, France. His research activities are in the area of analog circuit design using new translinear basic cells at the analog IC design group of the Laboratoire d'Electronique et de Physique Appliquée at the Ecole Centrale Paris, France.