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A Study of Electronic States Near the Interface in Ferroelectric-Semiconductor Heterojunction Prepared by rf Sputtering of $PbTiO_3$

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Abstract. Interface states in the ferroelectric-semiconductor junction have been investigated from analyses of DLTS and C-V data. Two trap levels are located at 0.21 and 0.36 eV below the conduction band near the silicon side of the interface in the MFS (Metal-Ferroelectric-Semiconductor) structure. The interface states density has been drastically reduced by putting an oxide layer between ferroelectric and semiconductor with certain heat treatment in H_2 atmosphere at 500 °C. It has been found that the MFMOS (Metal-Ferroelectric-Metal-Oxide-Semiconductor) structure shows the least interface states density (less than $10^{11}\,cm^{-2}\,eV^{-1}$) with the maximal dielectric constant of $PbTiO_3$ thin films.

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Much attention has been recently paid on ferroelectric thin films from a viewpoint of its wide applications in electronic [1], optoelectronic devices [2], and optical integrated circuit elements [3]. A number of efforts have been undertaken to prepare good ferroelectric thin films with various method such as rf sputtering [4–7], electron beam evaporation [8], and ion beam sputtering [9]. Among ferroelectric materials, $PbTiO_3$ shows considerably good ferroelectric properties [10] also with excellent pyroelectric [11] and piezoelectric properties [12]. We have recently succeeded in preparing $PbTiO_3$ thin films with good dielectric properties by rf sputtering at substrate temperature of $400° \sim 500\,°C$ [13–16]. Growing these ferroelectric thin films on a gate of Si MOS–FET, some functional devices have been developed, that is, nonvolatile memory FET [17] infrared optical FET [18], stress-sensitive FET [19], and so on. These Si-monolithic devices combined with amplifiers possess some merits like feasibility of arrayed devices, high gain and easy connection with signal processors. In order to improve the performance of these functional devices, such as switching characteristics in the memory FET and the detectivity of the infrared sensor, electronic properties of Si–SiO_2 or Si-ferroelectric thin film interface are particularly important since they might be damaged by high-energy ions, molecules and electrons during the rf sputtering deposition of ferroelectric thin films.

In this work, the electronic properties near the interfaces between semiconductor and dielectric layers have been investigated in MOS, MFS (Al–$PbTiO_3$–Si), MFOS (Al–$PbTiO_3$–SiO_2–Si) and MFMOS (Al–$PbTiO_3$–Pt–SiO_2–Si) structures through $C-V$ and DLTS measurements, with particular emphasis on influences of fabrication processes and junction structures. It has been found from these systematic measurements that these interface states and traps can be reduced in the MFMOS structure having both the internal metal (Pt) and the SiO_2 layers to avoid introduction of damage into the Si surface region during the rf sputtering deposition of the ferroelectrics.

1. $PbTiO_3$ Thin Film Preparation on Si Substrate by rf Sputtering

$PbTiO_3$ thin films were deposited by rf sputtering at various substrate temperatures of $200° \sim 600\,°C$. The target used was a powder mixture of Pb_3O_4 and TiO_2 pressed on a quartz plate. The $PbTiO_3$ films were

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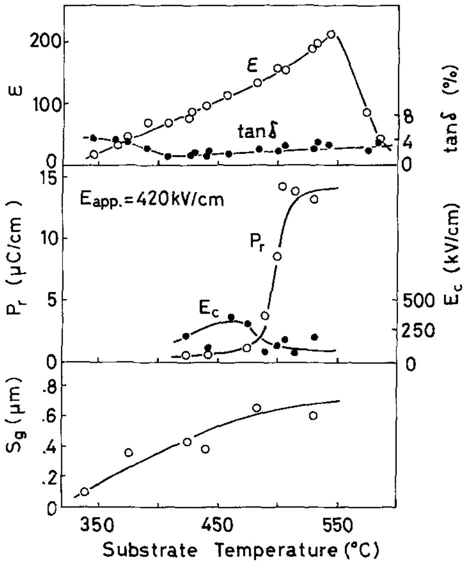

Fig. 1. Substrate temperature dependence of dielectric constant ε, loss $\tan\delta$, remanent polarization P_r, coersive force E_c and grain size S_g of $PbTiO_3$ films

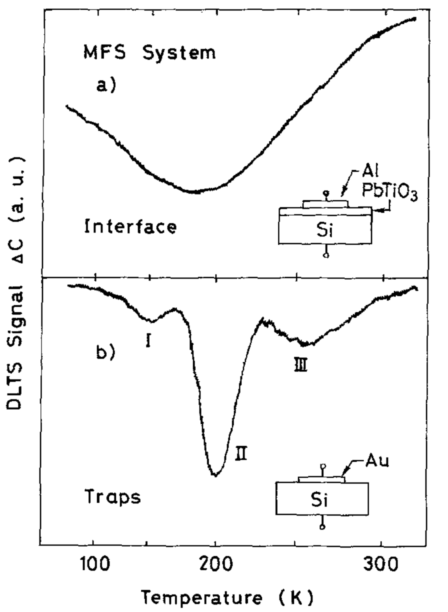

Fig. 2. (a) Typical DLTS signal in MFS diode and (b) Typical DLTS signal in Schottky barrier diode fabricated from an MFS diode (chemical etched)

deposited on Pt foil and Si wafers in an atmosphere of 90% argon and 10% oxygen gas mixture at a pressure of 27 Pa. Rf input power density was $\sim$3W/cm^2 and the deposition rate was $\sim$40 Å/min on the average. Dielectric properties of the film strongly depend on deposition conditions, especially the substrate temperatures and crystalline properties of substrate materials. Crystalline and dielectric properties were compared in the $PbTiO_3$ films prepared on several kinds of substrates, such as, Pt foil, SiO_2 ($\sim$500 Å) on Si and Si single crystal. Consequently, it has been found that Pt is the most appropriate substrate, the second is SiO_2 on Si and the third is Si single crystal in the case of the film deposition at the substrate temperature of 500 °C. Figure 1 shows the substrate temperature dependence of dielectric constant ε, loss $\tan\delta$, remanent polarization P_r, coercive force E_c and grain size S_g of the $PbTiO_3$ films of 2.1 μm thickness deposited on a Pt substrate. The ε and $\tan\delta$ were measured with capacitance bridge at 100 kHz, P_r and E_c using Sawyer-Tower circuit under 420 kV/cm and S_g from SEM observation. ε, P_r and S_g increase with the increase of the substrate temperature since the high substrate temperature helps growth of large grains with perovskite structure. However, an abrupt decrease of ε appears above 550 °C since the sputtering at high temperatures produces degradation of the film due to dissociation of the sputtered material. These results suggest that the substrate temperature should be set below $\sim$600 °C to prevent such degradation of $PbTiO_3$ thin films. Therefore we used a substrate temperature about 500 °C during the deposition of the $PbTiO_3$ films.

2. Electronic Properties Near Interface Between Si and Dielectrics

2.1. Interface of Si–$PbTiO_3$ *in MFS Structure*

The MFS structure without SiO_2 layer is, in principle, the best among some structures described in this paper. Because the SiO_2 layer reduces controllability of the Si surface potential by electric polarization of $PbTiO_3$ although the SiO_2 is usually used as a kind of buffer layer to protect the crystalline Si from rf sputter-induced damage. $PbTiO_3$ thin films were deposited on an n-Si substrate of resistivity 3$\sim$6 Ω cm at a substrate temperature of $\sim$500 °C to study the interface between $PbTiO_3$ and Si in the MFS structure. The thicknesses of $PbTiO_3$ thin films on Si wafers were 5000 Å to avoid a hysteresis effect of dielectric polarization on $C-V$ characteristics because thin $PbTiO_3$ films show no large $D-E$ hysteresis. The Si substrate used was washed in boiled trichloroethylene, boiled aceton and alcohol, and slightly etched by a mixture of HF and pure water after rinsing in HNO_3 and H_2SO_4 to remove metal ions. MFS diodes were fabricated by forming an Al dot electrode on the $PbTiO_3$ layer and their $C-V$ characteristics were measured to confirm the formation of a MIS type junction. The DLTS measurement was used for investigating deep centers in the interface region between $PbTiO_3$ and Si [20]. The DLTS measurements were carried out using a $C-V$ plotter (PAR 410) with a probe frequency of 1 MHz and a boxcar integrator (PAR 162, 164).

Figure 2a shows a typical example of DLTS signals of the MFS diodes which was obtained by applying the injection and emission voltages to vary the semiconductor surface potential from enough accumulation to inversion states (method I). This signal is considered to be due to interface states between Si and $PbTiO_3$, because its spectrum is very broad compared to that of bulk traps and its peak position is changed by an amount of injection voltage. The interface states density is calculated to be more than $10^{12}\,cm^{-2}eV^{-1}$. But its energy dependence could not be obtained because the peak position of the signal was too unstable to decide its energy position as electrons are trapped in excess deep defects near the interface.

Figure 2b shows DLTS signal of a Schottky barrier diode which was made by removing the $PbTiO_3$ layer of the MFS and subsequent deposition of Al electrode. The diode was heat-treated at 500 °C for 5 min in oxygen ambient before Al electrode deposition in order to make the I–V characteristics better [21]. In this figure, peak I and II are originated from bulk traps in the surface region of Si. Peak III is originated from interface states of very thin SiO_2 (some tens Å)-Si since the peak position of the signal moves with injection pulse height. These trap levels I and II in the Schottky diode were not observed in the MFS structure, because the large signal due to interface states between $PbTiO_3$ and Si masks these signals due to the bulk traps. The depth distribution of trap densities was obtained from DLTS signals measured under various reverse bias voltages. The densities of these bulk traps near the surface of the Si substrate, decrease with the depth. Especially, the trap I density promptly decreases with the depth, and could not be found in the region of $0.8 \sim 1.2$ µm far from the interface. On the other hand, the trap II density distributes more homogeneously in the depletion layer within ~ 1 µm deep from the surface. Figure 3 shows the depth profile of the densities of the trap II and the dopant phosphorus donor. This trap II concentrates near the surface while the shallow donor spreads homogeneously as expected.

Although the microscopic origin of these bulk traps can not be clarified clearly at the present stage, they might be attributed to some imperfections induced by the sputtering process which are related to migration of deposited ions, knocked ions or lattice defects. The trap I localized near the interface might be due to sputtered Ti atoms migrating into Si, since it has been reported that Ti-doped Si has an electron trap at $E_c - 0.26$ eV [22]. The density of the trap II decreases gradually till ~ 1 µm depth from the surface and its activation energy is $E_c - 0.36$ eV. This activation energy agrees well with that of a trap observed in Pb-doped Si which has been fabricated by Pb deposition on Si, heating at 850 °C for 2 h and subsequent thermal quenching. But there is another report that Pb-implanted Si produces an electron trap level at $E_c - 0.17$ eV [23]. Therefore, it is not straightforward to consider that the trap II is related to Pb impurity incorporated into the Si by the rf sputtering of $PbTiO_3$. The trap II distributes into the deep region (~ 1 µm) of Si, and hence there remains the possibility that such trap might be related to the other origin such as thermally induced oxygen donors [24].

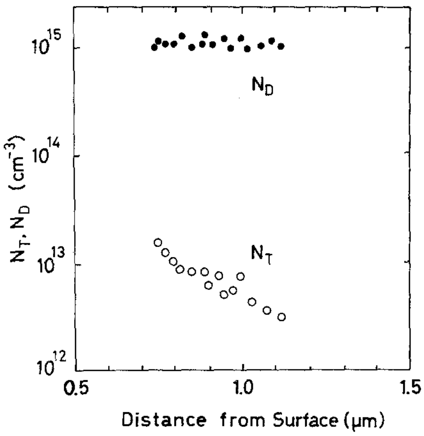

Fig. 3. Depth distributions of bulk trap and shallow donor densities in MFS system

Table 1. Typical results in MFS structure

Structure	E_T [eV]	σ [cm^2]	N_{ss} [cm^{-2} eV^{-1}] N_T [cm^{-3}]
MFS		$\sim 10^{-16}$	$\sim 10^{12}$
Schottky barrier			
I	$0.21 \sim 0.22$	$10^{-17} \sim 10^{-16}$	$\sim 10^{12}$
II	$0.34 \sim 0.38$	$10^{-16} \sim 10^{-15}$	$10^{12} \sim 10^{13}$
III		$\sim 10^{-17}$	$\sim 10^{12}$

Typical parameters about these traps of the activation energy, the density and the capture cross section are summarized in Table 1. From these experimental results, it is concluded that the direct deposition of $PbTiO_3$ on the bare Si surface is not appropriate for ferroelectric-semiconductor junction as it induces a lot of interface states of SiO_2–Si and imperfections in bulk Si near the interface.

2.2. *Interface of* Si–SiO_2 *in* MFOS *and* MFMOS *Structures*

In order to prevent bulk traps from being induced in Si, we have tried to insert a blocking layer of SiO_2 between the Si substrate and the ferroelectric film. The

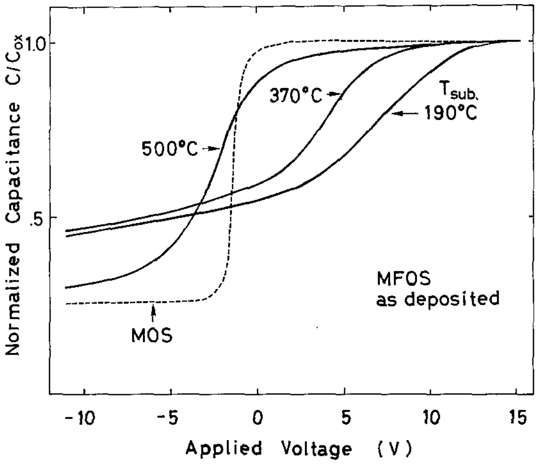

Fig. 4. Substrate temperature dependence of $C-V$ characteristics in MFOS diodes

thin SiO_2 layer of $\sim$500 Å thickness was formed by thermal oxidation of Si in dry oxygen at 1200 °C because a thicker SiO_2 layer reduces controllability of the Si surface potential induced by electric polarization of the ferroelectric layer. In the MFOS structure prepared by the $PbTiO_3$ deposition on the SiO_2–Si substrate, any bulk trap in Si has not been observed in DLTS measurements of Schottky diodes fabricated in the same way as the case of the MFS structure, because the SiO_2 layer blocks ion migration induced during the sputtering of $PbTiO_3$.

Figure 4 shows $C-V$ characteristics of the MFOS diodes as a function of substrate temperature. The $C-V$ curve of the MOS diode is also shown by a broken line for reference. The slopes of these $C-V$ curves near zero volt increase with substrate temperature, the result indicating that the controllability of the Si surface potential by bias voltage is improved with increasing substrate temperature. These high substrate temperatures of 500° $\sim$ 550 °C are suitable not only for Si surface potential controllability, but also for fabrication of good $PbTiO_3$ thin films because the good ferroelectric properties can be obtained at a substrate temperatures of 500° $\sim$ 550 °C, as shown in Fig. 1. Fixed charge in the dielectrics (SiO_2 and $PbTiO_3$) induced during the sputtering of the $PbTiO_3$ was also estimated from voltage shifts of the $C-V$ curve and became small as the substrate temperature increases. The polarity of the fixed charge in the films deposited at high substrate temperatures is positive as observed in MOS diodes commonly, however, with the decrease of the substrate temperature, the charge density gradually decreases and finally the polarity changes to the negative. This reason is not clear but may be due to ion migration or electron trapping in the dielectric layers.

Figure 5 shows an annealing effect of the $C-V$ characteristics and a fixed charge in the dielectric layers. The heat treatment was carried out in atmospheres of Ar and H_2 at an annealing temperature of 500 °C which is conventionally good for suppressing the interface states in MOS diodes. The annealing in H_2 atmosphere is effective as $C-V$ curves become steep with the increase of annealing time, but the annealing in Ar does not improve $C-V$ characteristics in the MFOS diodes. The fixed charges in the dielectric layers are also reduced in both the MOS and the MFOS diodes by the H_2 annealing. As a result, the H_2 treatment is more effective to improve the controllability of the Si surface potential in the MFOS diode. This is due to the reason why hydrogen ions can terminate dangling bonds at the Si–SiO_2 interface as usually explained in the MOS structure [25]. But this effective H_2 treatment might deteriorate the ferroelectric properties of $PbTiO_3$ films because of release of oxygen in $PbTiO_3$, and ad-

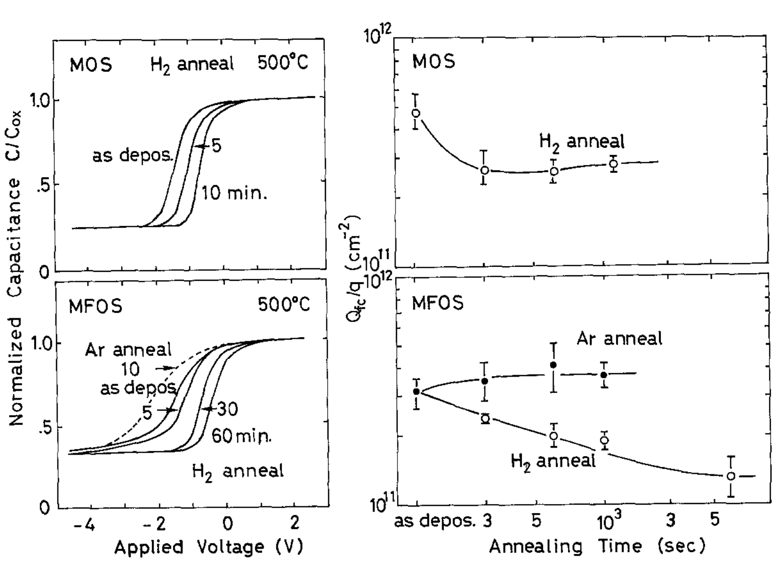

Fig. 5. Annealing effects of $C-V$ characteristics and fixed charges in MFOS and MOS diodes before and after Ar and H_2 annealing

ditionally the interface states in the MFOS structure is still large. So we have attempted to insert an additive metal layer between ferroelectrics and SiO_2 to suppress ion damage, and we call this structure MFMOS (Al–$PbTiO_3$–Pt–SiO_2–Si). DLTS measurements have been carried out on these MFMOS diodes together with the MFOS and the MFOS diodes annealed in H_2.

First of all, we have tried to measure energy dependence of the capture cross section of interface states [26]. The results are shown in Fig. 6. Open circles and closed circles show the capture cross sections and interface states density obtained from DLTS measurements, respectively, in which signals were measured by setting the difference between the injection and emission voltage to 0.1 V and scanning the emission voltage of the Fermi level at the interface to change over the forbidden band (method II). In this method II, the electron population at the interface only near the Fermi level is charged by the injection pulse, and so the information on the interface states in the very narrow energy region can be clarified. The capture cross sections were estimated from the temperature dependence of DLTS signals, and scatter around $10^{-16}\,cm^2$. The energy range of the measured capture cross section is limited to $E_c-0.1 \sim E_c-0.4$ eV because the signal due to minority carrier generation disturbs the signal from the interface states at high temperature. Their clear energy dependence could not be found, as can be seen in the figure. Using this method the precise capture cross sections and interface states density can be obtained but such measurement is very troublesome. On the other hand, the solid line in Fig. 6 indicates the energy dependence of the interface states N_{ss} obtained from the DLTS data which were measured by applying the injection and emission voltages to vary the semiconductor surface potential from enough accumulation to inversion states (method I). The interface-states density was analyzed by assuming the constant capture cross section equal to $10^{-16}\,cm^2$. The energy distribution of the interface-states density, which was estimated directly from the easier DLTS measurements (method I), is almost the same as that obtained from the above-mentioned DLTS measurements (method II) by setting the constant difference between the injection and emission voltage to a small value. Hereafter DLTS data were measured by the latter method I.

Figure 7 shows DLTS signals for the MOS, the MFOS and the MFOS diodes annealed in H_2. For comparison, the signal of the MOS is ten times expanded, as seen in the figure. It has been confirmed from the bias voltage dependences of the signals that each signals is originated by interface states. The signal of the H_2 annealed MFOS structure is smaller by an

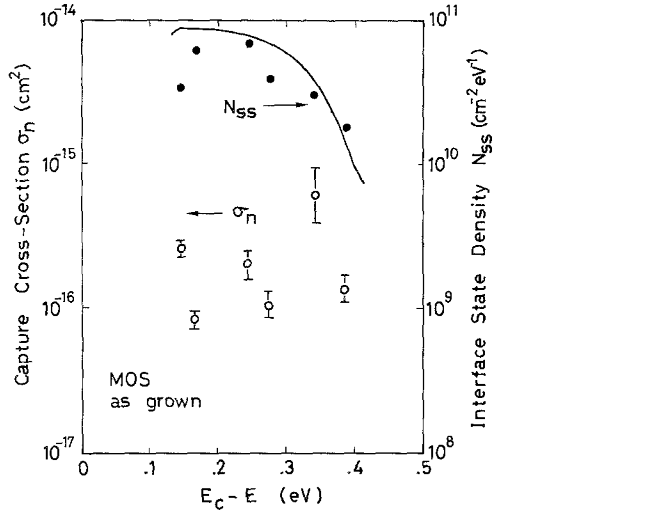

Fig. 6. Energy dependences of interface states and capture cross sections in MOS diode

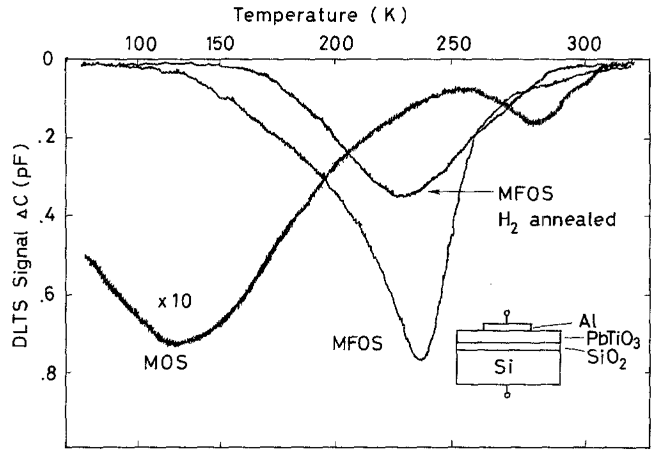

Fig. 7. DLTS signals in MOS, MFOS and H_2-annealed MFOS diodes

amount of about half that of the MFOS without annealling. The signal of the MOS diode is ten times smaller than that of the MFOS structure. The small peak near 280 K in the MOS DLTS signal is originated from minority carrier generation. The energy distributions of the interface states densities calculated from the DLTS signals are shown in Fig. 8. Though the as-deposited MFOS structure exhibits the interface states density of $\sim 3\times10^{12}\,cm^{-2}\,eV^{-1}$, the H_2-annealed MFOS structure exhibits a density of less than $10^{12}\,cm^{-2}\,eV^{-1}$. The interface states density of the MFMOS diodes is the least in all the ferroelectric-semiconductor junctions fabricated in this work and is in the same order as that of the conventional MOS diodes. Moreover, from the view point of the growth of good $PbTiO_3$ ferroelectric thin films, the Pt substrate is the most appropriate, as mentioned in Sect. 1. Then, these results show that the MFMOS structure is the

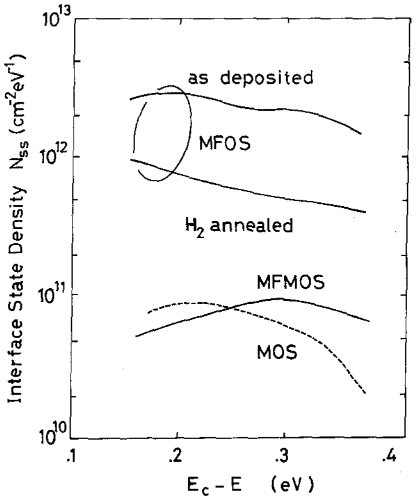

Fig. 8. Energy distributions of interface states density in MOS, MFOS, H_2-annealed MFOS and MFMOS diodes

Table 2. Summarized results in $PbTiO_3$-Si interface

Structure	Interface states $[cm^{-2} eV^{-1}]$	Bulk trap $[cm^{-3}]$	Dielectric constant of $PbTiO_3$
MFS	$\sim 10^{12}$	$\sim 10^{13}$	$\sim$ 50
MFOS as-depos.	$\sim 3 \times 10^{12}$	–	$\sim$100
H_2 annealed	$\sim 10^{12}$	–	$\sim$100
MFMOS	$< 10^{11}$	–	$\sim$200

most appropriate in ferroelectric-semiconductor junction devices. Except for the H_2-annealed sample, all the diodes show a slight hump at $\sim$0.3 eV in the interface-states distribution. This hump was always observed in the diodes made by using a sputtering process, and hence the hump might be due to ion damage during the sputtering process. H_2 annealing is effective to eliminate the hump.

Summary

A series of experiments on the electronic properties of some types of the dielectric-semiconductor interfaces has been carried out in the ferroelectric-semiconductor heterojunctions fabricated by rf sputtering. Two bulk traps near the surface region of the Si substrate were found in the structure of $PbTiO_3$–Si, and its large DLTS signal corresponding to the interface states was also observed as the interface was strongly damaged by rf sputtering. It has been found that the insertion of the SiO_2 layer is effective to suppress the generation of the traps, and furthermore the Pt layer on SiO_2 is also effective to prevent the ion damage from impairing the interface. The electronic properties of the interface in all the structures fabricated are summarized in Table 2. The best ferroelectric properties have been obtained in the $PbTiO_3$ film of the MFMOS structure. The MFMOS structure is the most appropriate for the ferroelectric-semiconductor junction and can be applied widely to various functional devices such as a nonvolatile memory FET, a infrared-optical FET and a pressuresensitive FET.

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