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Schottky Barrier and pn-Junction I/V Plots – Small Signal Evaluation

Jürgen H. Werner

Max Planck Institut für Festkörperforschung, Heisenbergstrasse 1, D-7000 Stuttgart 80, Fed. Rep. Germany

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Abstract. This paper proposes and examines three different plots for the determination of the saturation current, the ideality factor, and the series resistance of Schottky diodes and solar cells from the measurement of a single current(I)/voltage(V) curve. All three plots utilize the small signal conductance and avoid the traditional Norde plot completely. A test reveals that the series resistance and the barrier height of a test diode can be determined with an accuracy of better than 1%. Finally it is shown that a numerical agreement between measured and fitted I/V curves is generally insufficient to prove the physical validity of current transport models.

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The current I_d flowing across a rectifying metal/semiconductor contact or a pn-junction under bias V_d is usually modeled with the help of a diode equation:

$$I_d = I_s\left(\exp\left(\frac{\beta}{n}V_d\right)-1\right), \tag{1}$$

where $\beta = e/kT$ is the inverse thermal voltage. For a pn-junction the saturation current I_s depends on the diffusion length and diffusion constant of the injected *minority carriers* [1]. For a Schottky diode the current I_d is explainable by thermionic emission of the semiconductor's *majority carriers* across the Schottky barrier Σ [2]. The saturation current I_s depends then on the Richardson constant A^{**} and diode area A according to

$$I_s = A^{**}AT^2\exp(-\beta\Sigma). \tag{2}$$

The ideality $n \geqq 1$ in (1) is used to force the measured data to agree numerically with these models for current transport. Deviations from $n=1$ in the case of a Schottky contact might for example be ascribed to voltage dependent Schottky barriers Σ due to image force lowering [3] or interface states [4]. In pn-junctions values $n>1$ may result from recombination currents within the space charge region [1].

Eq. (1) is often used to judge the n value (and quality) of diodes by means of a semi-logarithmic delineation of measured current/voltage data. This plot yields for $V_d \gg nkT/e$ a straight line with slope $d(\ln I_d)/dV_d = \beta/n$ and an extrapolated I_d-axis intercept I_s; for a Schottky diode the current I_s yields then the barrier Σ with the help of (2).

This simple analysis is not applicable to *real* Schottky diodes and pn-junctions in solar cells when the series resistance R_s of substrate, front contacts and back contact as well as a possible shunt or parallel conductance G_p distort the linear behavior in the semi-logarithmic I/V plot. Figure 1 shows an example where the measured I/V curve α of a Schottky diode is strongly affected by shunt and series resistances. Curve γ represents the underlying (theoretical) I/V curve when shunt and series resistance effects are absent. The voltage drop at the substrate influences the measured curve α for forward bias voltages above 0.3 V. On the other hand, for voltages below 0.25 V, curve α is dominated by currents that flow over a surface shunt path between the front and the backside contact of the sample. The measured curve α reveals practically no voltage regime that can be described by (1). It is impossible to reconstruct the underlying, theoretically expected curve γ from the measured curve α with the

help of the usual extrapolation to zero bias. The linear part between 0.25 V and 0.3 V is just not wide enough.

The present paper discusses simple methods to obtain reliable information from I/V curves of Schottky contacts or pn-junctions when their inherent barrier properties are strongly masked by parallel and series resistances. In short, I show here how to get curve γ in Fig. 1 from the measured curve α. The evaluation methods are exemplified with the help of the analysis of I/V curves from Schottky contacts.

1. Previous Work

Norde [5] was the first who proposed a method for the extraction of the series resistance R_s from forward bias I/V curves of Schottky diodes. He defined the function

$$F(V)=V/2-\beta^{-1}\ln(I/A^{**}AT^2). \quad (3)$$

Plotting $F(V)$ versus applied voltage V yields a curve with a minimum [5]. From the value of $F(V)$ at the minimum and the corresponding current I the Schottky barrier Σ as well as the series resistance R_s were then obtained. The original approach of Norde [5] was only applicable to ideal Schottky contacts, i.e. for diodes with idealities $n=1$; several authors [6–9] introduced therefore in different ways the ideality n in Nordes approach of the $F(V)$ minimum. All of these procedures [6–9] suffer, however, from the principle application of Norde's [5] F-minimum method: The evaluation of the minimum of $F(V)$ uses first of all just a few data points around the minimum, i.e. just of few I/V data pairs; most data of the measured I/V curve are not used in the evaluation. Secondly, the method was originally not intended for non-ideal diodes with $n>1$ and requires therefore a complicated evaluation [6–9]. Even then it still seems difficult to tell from the Norde-plot only, whether the minimum is really caused by a series resistance or by a non-ohmic backside contact [5].

In the following, three alternatives are discussed for the evaluation of I/V curves of diodes. These plots are far simpler than the Norde-plot [5] and its extensions [6–9]. The three plots, which are termed A, B, and C all are based on the small signal conductance G and yield series resistance R_s and ideality n. When the series resistance is known from one of these plots the saturation current I_s is obtained from the usual semi-logarithmic I/V plot after correcting the voltage axis for the drop at the series resistance R_s. The shunt conductance G_p is derived from the reverse bias characteristics.

One of the three plots, plot C, was recently used independently by Cheung and Cheung [10]. It seems, however, that this plot was first proposed by Paoli and Barnes [11] as well as Dixon [12] who made use of ac measurements. Cheung and Cheung [10] used dc data only and supported their analysis in addition with the function

$$H(I)=V-\beta^{-1}\ln(I/A^{**}AT^2). \quad (4)$$

Saturation current I_s, ideality n, and series resistance R_s are, however, obtainable without ac measurements or defining any artificial function $H(I)$ or $F(V)$. The experimentally accessible voltage V, current I, and the *small signal conductance* $G=dI/dV$ already contain this information. There are, however, different possibilities to extract I_s, n, and R_s, from the measured V, I, and G.

2. Equivalent Circuit Elements

The I/V curve of a real diode as shown in Fig. 1 is modeled by the equivalent circuit in the lower inset of Fig. 1 and the following equation for the measured

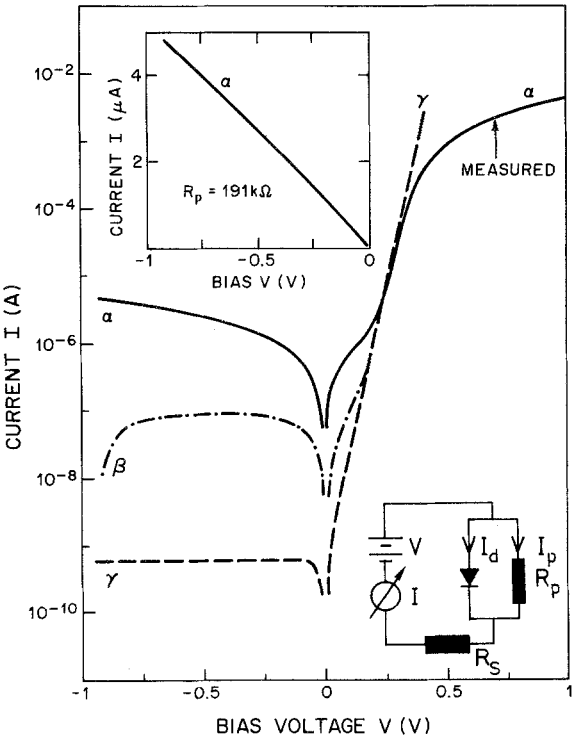


Fig. 1. Current/voltage curves of a PtSi/Si diode. Reverse bias and small forward bias regime of measured curve α are dominated by shunt currents. Upper inset reveals the ohmic shunt path. The substrate resistances causes the curved shape for voltages $V>0.3$ V. Curve β is obtained after correcting curve α for shunt currents. Curve γ gives theoretical behavior without series and shunt resistances. Lower inset shows equivalent circuit with series resistance R_s and shunt resistance $R_p=1/G_p$. The evaluation of curve α yields Schottky barrier $\Sigma=0.830$ eV, ideality $n=1.08$, series resistance $R_s=120\Omega$, and shunt resistance $R_p=191$ kΩ

current I at bias V:

$$I = I_d + I_p = I_s\left(\exp\left(\frac{\beta}{n}(V - IR_s)\right) - 1\right) + G_p(V - IR_s). \quad (5)$$

Here I_d is the diode current and I_p describes the shunt current through a possible parallel conductance G_p with the resistance $R_p = 1/G_p$. It is assumed that the saturation current I_s, ideality n, series resistance R_s and parallel conductance G_p all are independent of the bias voltage V. Deviations from the "ideal" behavior such as recombination within the space charge region, voltage dependent Schottky barriers due to image forces or interface states, or, minority carrier injection in Schottky diodes, are all additional effects that are hidden in the "ideality" n.

2.1. Shunt Resistance R_p

The data in Fig. 1 originate from a PtSi/Si contact which is prepared by annealing 100 nm of evaporated Pt on a Si wafer. The leakage current I_p flows from the front diode with an area of 5.6×10^{-3} cm^2 over the surface of the sample to the ohmic backside metallization. This shunt current stems from microscopic metal particles on the surface and could be suppressed by mesa etches. The shunt conductance G_p is calculated from the reverse bias characteristics for large negative bias voltages $-eV \gg kT$. Eq. (5) yields then with $R_p \gg R_s$ for the measured small signal conductance $G = dI/dV$, i.e. the slope of the I/V curve:

$$G_{\text{reverse}} = G_p. \quad (6)$$

A simple least squares fit to the linear part of the reverse bias I/V curve therefore yields G_p; from Fig. 1 we find $1/G_p = R_p = (191 \pm 0.5)\,\text{k}\Omega$. The measured current I in curve α is then corrected for the shunt current $I_p = G_p V$ to yield the current $I_d = I - G_p V$ across the Schottky barrier in curve β. The corrected reverse current in curve β is still about two orders of magnitude higher than the theoretically expected value, curve v. The incomplete correction stems from the small deviation of the measured reverse bias curve α from ohmic behavior making the correction very sensitive to the precise value of R_p. A precise study of the saturation current I_s with the help of the reverse bias characteristics requires therefore high shunt resistances and guard rings [14]. The correction for shunt currents here, however, does not influence the determination of series resistance R_s, ideality n, and Schottky barrier Σ.

2.2. Series Resistance R_s and Ideality n

The series resistance R_s influences the I/V curve in Fig. 1 for voltages above 0.3 V. The simplest experiment to determine R_s seems to use such high forward bias voltages that the I/V curve is dominated by R_s alone. Figure 2 shows the current I_d and the conductance G of the measured curve α from Fig. 1 on a linear scale. For $V > 0.5$ V the current I_d seems to vary linearly with voltage V and one might consider to deduce the series resistance R_s from the slope of this I_d/V curve. The numerically determined conductance G in Fig. 2 reveals however that the slope of the linear I_d/V plot is not constant for $V > 0.5$ V. Even at 1 V the conductance G has not yet reached a saturation value that would correspond to the inverse of the series resistance R_s. Larger bias currents change, however, the series resistance by heating. Heating might be prevented in a experiment with pulsed currents. But under these conditions and for Schottky diodes with barriers $\Sigma > 0.65$ eV, for low doping, and in particular for diodes grown on thin epi-layers, minority carriers that are injected under forward bias can lead to a significant change of the substrate resistance by *conductivity modulation* [1, 15–17]. Similar effects are well known from pn-junctions.

The analysis therefore requires methods that avoid large forward bias voltages with heating and high injection effects as well as the regime around zero bias which is dominated by shunt currents. Instead, the *intermediate* voltage regime of the I/V curve should be

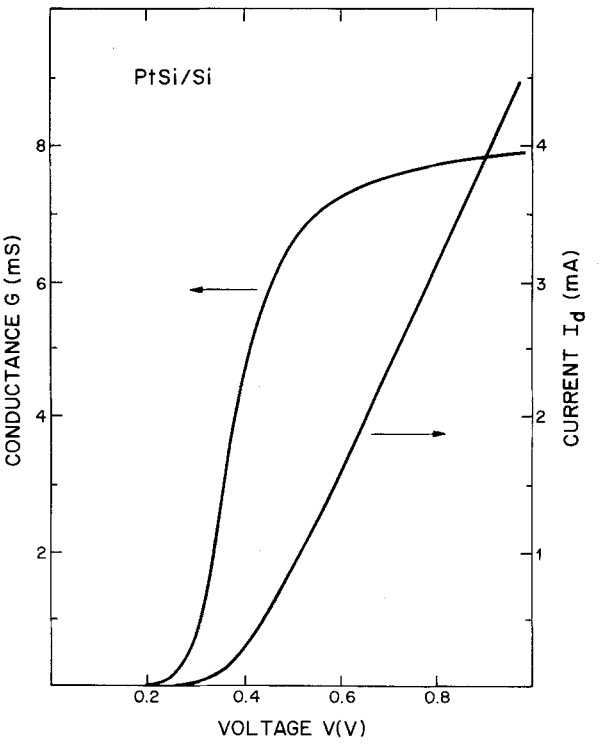


Fig. 2. Linear plot of conductance $G = dI_d/dV$ and diode current I_d of curve β from Fig. 1. The conductance G is numerically determined with $G = (1/I_d)\,d(\ln I_d)/dV$ in order obtain a better approximation to the slope of the steep I_d/V curve

used where the voltage drops at the series resistance and at the diode are comparable. An analysis that uses this regime does not need Nordes $F(V)$ plot. Instead, the small signal properties of the I/V curve, the following simple equations and in particular the resulting plot A are here proposed for this purpose.

Under forward bias for $V_d = V - IR_s \gg kT$, the thermionic diode current I_d is given by

$$I_d = I_s \exp\left(\frac{\beta}{n}(V - IR_s)\right). \tag{7}$$

Eq. (7) yields for the small signal conductance $G = dI_d/dV$:

$$\frac{G}{I_d} = \frac{\beta}{n}(1 - GR_s). \tag{8}$$

Eq. (8) shows that a plot of G/I_d versus conductance G (here termed as plot A) yields a straight line with y-axis intercept β/n, x-axis intercept $1/R_s$ and slope $-\beta R_s/n$. Figure 3a delineates the data from curve β in Fig. 1. The scatter in the data reflects the noise of the measured I/V curve which was taken with voltage steps of 10 mV. The fit between 0.3 V and 1 V yields $R_{sA} = (120 \pm 1)\Omega$, $n_{A1} = (1.08 \pm 0.008)$ for series resistance and ideality, respectively.

From (8) two other possibilities for plots can be derived: The first plot is obtained by solving (8) for $1/G =: R_{dr}$, the differential resistance of the I/V curve. This transformation yields:

$$R_{dr} = \frac{n}{\beta I_d} + R_s. \tag{9}$$

Eq. (9) suggests a plot (here termed as plot B) of the differential resistance R_{dr} versus inverse current $1/I_d$. A straight line with slope n/β and y-axis intercept R_s is obtained. The data from Fig. 1 are re-drawn in Fig. 3b. The fit between 0.3 V and 1.0 V yields $R_{sB} = (119 \pm 0.6)\Omega$, and $n_{B1} = (1.11 \pm 0.05)$.

The third possibility – plot C – is finally found by using the identity $R_{dr} = 1/G = dV/dI_d = (1/I_d)dV/d\ln I_d$. One obtains from Eq. (9):

$$\frac{dV}{d\ln I_d} = R_s I_d + \frac{n}{\beta}. \tag{10}$$

Eq. (10) was recently also used by Cheung and Cheung [10] for the determination of R_s and β although they derived the equation differently. According to (10), a plot of $dV/d\ln I_d$ (i.e. the inverse slope of the usual semi-logarithmic I/V plot like Fig. 1) yields a straight line with slope R_s and y-axis intercept n/β. Note that the left-hand side of (10) is just equal to I_d/G. Figure 3c represents the data from Fig. 1; the fit yields $R_{sC} = (120 \pm 0.4)\Omega$, $n_{C1} = (1.09 \pm 0.04)$.

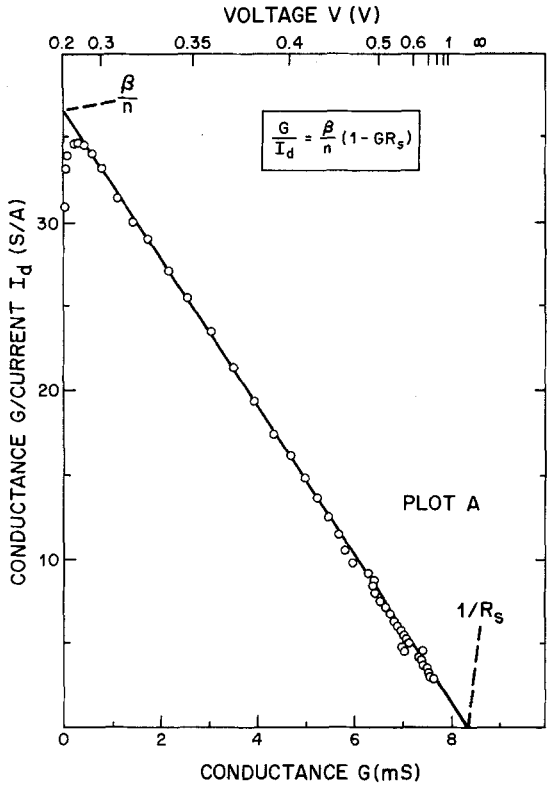
Three simple plots which all avoid the traditional Norde [5] plot and its extensions [6–9] completely are therefore possible on basis of (8–10) to determine ideality n and series resistance R_s. Apart from their striking simplicity, the three plots have another advantage when compared to the Norde plot: All of them use the measurable conductance G. The *experimental* determination of G requires a small ac voltage δU and a lock-in amplifier to measure the in-phase component δI of the ac current to obtain the conductance $G = \delta I/\delta U$ directly [12, 18]. One has, however, to consider the exponential increase of the I/V curve and to keep the ac voltage as small as possible. Any ac method bears the additional difficulty that the conductance G may depend on frequency, as found due to interface states at Au/GaAs Schottky diodes with an interfacial layer [4].

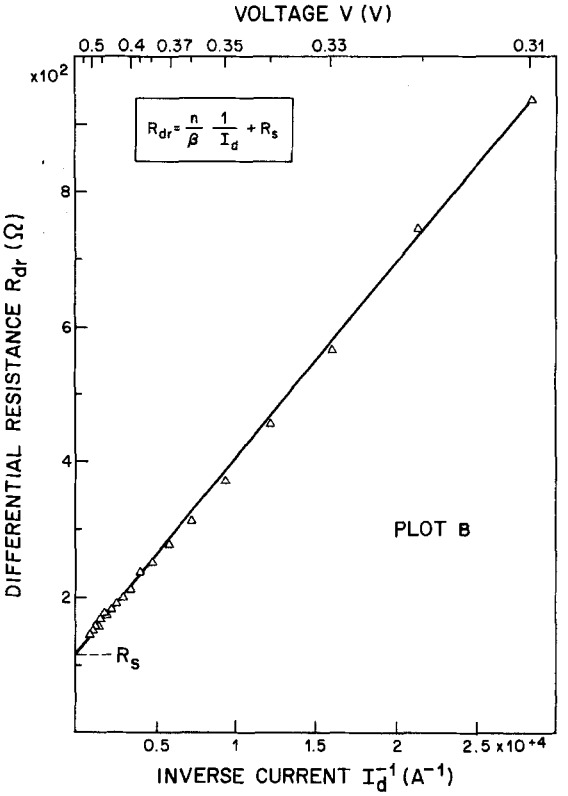
The *numerical* determination of $G = dI_d/dV$ from the steep I/V curve requires dc voltage steps typically of less than 1 mV in order to get the real slope of the curve and not just a secant line. Instead of measuring the current/voltage curves with such small voltage steps one may instead determine G from the less steep logarithmic curve (as in Fig. 1) with the help of the identity $G = I_d d(\ln I_d)/dV$. In this case even voltage steps of 10 mV are found to be small enough to yield a good approximation to the true slope of the I/V curve.

2.3. Schottky Barrier Σ

The series resistances R_s from the three possible plots as in Figs. 3a–c are now usable to correct the voltage axis of the I/V plot to determine the saturation current. For the diode from Fig. 1 we thus also obtain three values Σ_A, Σ_B, and Σ_C for the Schottky barrier corresponding to the three values R_{sA}, R_{sB}, R_{sC} for the series resistances. Three additional idealities n_{A2}, n_{B2}, n_{C2} are also obtained from the slopes of the corrected plots. These additional ideality data allow one to test the accuracy and selfconsistency of the evaluation. For the PtSi/Si-diode from Fig. 1 we obtain $\Sigma_A = (830 \pm 0.9)$ meV, $n_{A2} = (1.08 \pm 0.002)$ when the series resistance R_{sA} from plot A is used for the correction. The resistances from plots B and C yield $\Sigma_B = (817 \pm 0.2)$ meV, $n_{B2} = (1.13 \pm 0.005)$, $\Sigma_C = (830 \pm 1)$ meV, $n_{C2} = (1.09 \pm 0.002)$. A value of $A^{**} = 112$ A/cm^2 K^2 is here used for the Richardson constant [14].

With these data for the Schottky barrier Σ, ideality n and series resistance R_s, the measured I/V curve α in Fig. 1 is completely reproducible. The deviation between measured and recalculated forward bias currents is less than 1%. Curve γ in Fig. 1 gives the resulting theoretical I/V curve for a Schottky barrier $\Sigma = 830$ meV, an ideality $n = 1.08$, and with a series resistance $R_s = 0$ and a shunt conductance $G_p = 0$.





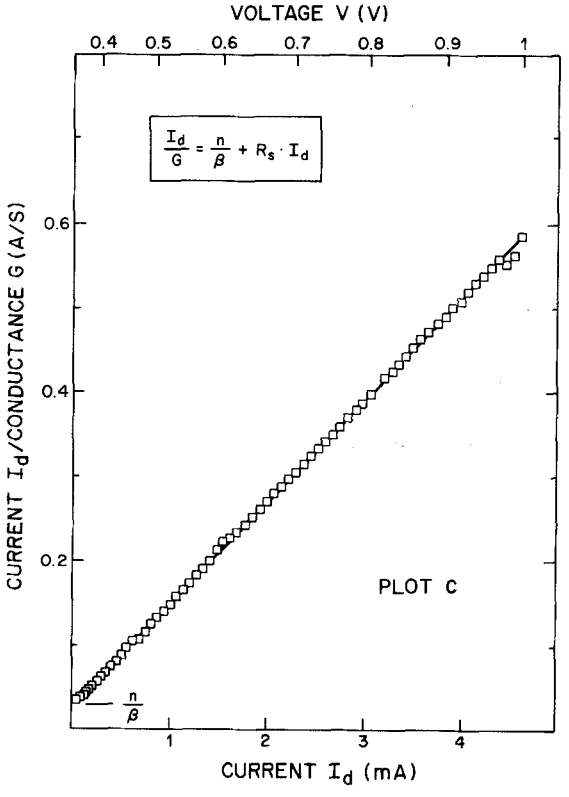


Fig. 3. (a) Data from curve β, Fig. 1 are here redrawn. The evaluation yields series resistance R_s and ideality n form the axis intercepts. The additional voltage ordinate demonstrates that the data are compressed at low and high voltages. The deviation from the straight line for $V<0.3$ V stems from incomplete correction of curve β in Fig. 1 for shunt currents. (b) Plot B for the data for curve β from Fig. 1 yields resistance R_s from y-axis intercept and ideality n from slope. The inverse current $1/I_d$ as ordinate compresses the measured I/V data at small x-values which correspond to large forward bias. Fits based on this plot B depend therefore sensitively on scatter of few low-voltage data. Data for $V>0.5$ V are graphically not represented. (c) Plot C for curve β from Fig. 1 yields ideality n from y-axis intercept and series resistance R_s from slope. The data points appear almost equidistantly but are compressed at $V<0.4$ V. The slight deviation from linearity at voltages $V<0.4$ V as caused by incomplete correction of curve β, Fig. 1 for shunt currents is hardly detectable. The ordinate I_d/G is identical to $dV/d\ln(I_d)$, the inverse of the slope of curve β in Fig. 1

The fits to Figs. 3a–c show already that the calculated barriers, idealities and series resistances depend somewhat on the evaluation method. The scatter of the three series resistance data is less than 1%. The scatter over all six idealities is about 3%. The idealities n_{A1}, n_{A2} as well as n_{C1}, n_{C2} from plots A and C are identical, the two values n_{B1}, n_{B2} for plot B differ by 0.02, indicating a higher redundancy for the plots A and C. The barrier $\Sigma_A = \Sigma_C = 830$ meV from plots A and C agrees with barrier heights measured on PtSi/Si-samples grown on thin epi-layers with series resistances around 1Ω, and a high shunt resistances around 16MΩ. The evaluation based on plots A and C seems therefore more redundant and reliable than an analysis with the help of plot B. This supposition is confirmed below.

3. Test of the Plots

A test of the reliability, self consistency and the accuracy of the evaluation based on each of the three plots is carried out: A Schottky diode of Au/Cr/GaAs is used, which is fabricated by growing 3 μm GaAs with a Si doping of $2 \times 10^{16}\,cm^{-3}$ by molecular beam epitaxy on a degenerately doped GaAs-substrate. The Au/Cr contact with an area of $2.6 \times 10^{-3}\,cm^2$ is evaporated in a high vacuum. Indium serves as ohmic back-contact. Different series resistances R_s are then simulated by connecting external metal film resistors in series to the sample.

The forward bias I/V curve for the as-grown sample without external series resistance is shown in Fig. 4. The reverse bias curve yields $R_p = 81\,M\Omega$ for the shunt resistance. Evaluating the I/V curve of the as-grown sample with plot A yields $R_{sA} = (101.3 \pm 0.2)\Omega$, $n_{A1} = (1.049 \pm 0.001)$. The corrected I/V curve yields then $n_{A2} = (1.048 \pm 0.0002)$, $\Sigma_A = (861.1 \pm 0.09)$ meV; a Richardson constant $A^{**} = 8.16\,A/cm^2\,K^2$ is used [2]. Plot C yields $R_{sC} = (101.4 \pm 0.06)\Omega$ and $n_{C1} = (1.049 \pm 0.002)$. The I/V curve corrected for R_{sC} yields $n_{C2} = (1.048 \pm 0.003)$, $\Sigma_C = (861.2 \pm 0.1)$ meV. These results are all obtained from least square fits to the data between 0.2 V and 0.8 V. The variation of these lower and upper boundary voltages is not critical for the fits based on plots A and C. For the same voltage regime a least squares fit with the help of plot B fails, however, to provide any reasonable results. Negative values for the series resistance R_{sB} are obtained as long as the lower boundary voltage for the fit is smaller than about 0.4 V.

The failure of plot B is caused by its inherent disadvantages, which are also visible in Fig. 3b: The use of the inverse current, $1/I_d$, as an ordinate compresses the measured data for high voltages. Data points that are recorded at low voltages have, on the other hand, larger interdistances on the inverse current

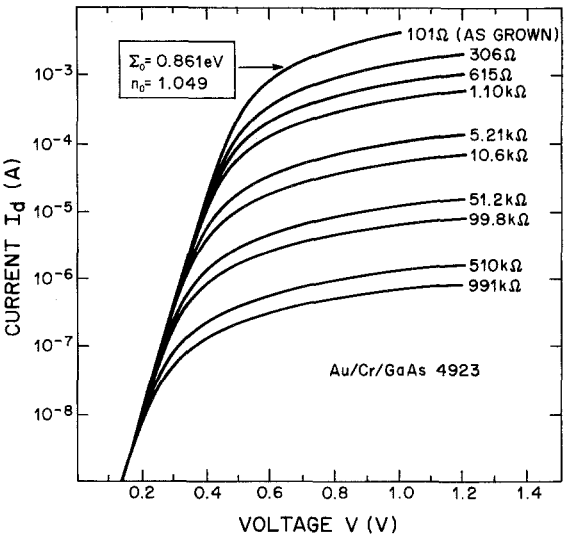


Fig. 4. Forward bias I/V curve of a Au/Cr/GaAs diode. Schottky barrier $\Sigma_0 = 0.861$ eV, ideality $n_0 = 1.049$, and series resistance $R_0 = 101\Omega$ are obtained from curve "as-grown". External metal film resistors in series with the diode serve to test the accuracy of the evaluation based on plots A, B, C. Results are shown in Figs. 5–7

axis. When there are a few data points at low voltages (as around 0.32 V in Fig. 3b), which – due to electrical noise, random scatter, shunt currents or incomplete correction for shunt currents – deviate only slightly from the expected linear behavior, then these few data points will have a drastic effect on the least squares fit. The slope and y-axis intercept of the whole fit are changed and result in unreliable values for the corresponding ideality and series resistance. This instability of the evaluation can be avoided by fitting only the part of the curve that corresponds to higher voltages and is dominated by the series resistance. Plots like the one in Fig. 3b have therefore to be zoomed around $1/I_d = 0$ and the voltage range for the fit has to be adjusted for each different I/V curve. The original measured data have to be carefully smoothed and selected before the fit; "blind fitting" – meaning a numerical least squares fit without a careful visual inspection of the data – is practically impossible. Only the visual inspection of the plot could reveal that the results from the fit are strongly influenced by a few unreliable data points. The evaluation based on plot B with the sensitive dependence of the results on the choice of the voltage range is therefore intricate, clumsy and unreliable.

Plots A and C weight on the other hand all data points about equally and are therefore relatively insensitive to scatter in the I/V data. And indeed, both plots yield here identical values for the barrier Σ as well as identical and selfconsistent results for the ideality n.

3.1. Accuracy Test

a) Test Conditions. For the test it is assumed that the initial values for the Schottky barrier $\Sigma_0 = 0.861$ meV, the ideality $n_0 = 1.049$ and $R_0 = 101\Omega$ for the series resistance from the I/V curve of the as-grown sample are the "true" nominal values of this diode. Different metal film resistors are then connected in series with the sample. The resulting I/V curves are also shown in Fig. 4. All measurements are then evaluated with the help of the three plots A, B, C to obtain values R_{sA}, R_{sB}, R_{sC} for the series resistance which are compared to the nominal values. The evaluation yields also two values for the ideality, i.e. plot A yields n_{A1}, n_{A2}, plot B yields n_{B1}, n_{B2}, and plot C yields n_{C1}, n_{C2}, which are to be compared to each other (e.g. n_{A1} with n_{A2}) as well as to $n_0 = 1.049$. The three values Σ_A, Σ_B, Σ_C for the barrier height are compared to Σ_0. The test examines therefore the accuracy, consistency and the reliability as well as versatility of the three plots over the four orders of magnitude over which the series resistance is purposely changed.

The I/V curves with voltage steps of 2 mV are taken at room temperature with the sample in a shielded box. The raw I/V data are not smoothed for the evaluation and all data between 0.2 V and 0.8 V are used in the least square fits according to (8–10). The conductance G is deduced from the logarithmic derivative of the steep I/V curves. Results are shown in Figs. 5–7.

b) Test Results. Figure 5 shows results for the reproducibility of the series resistance. The nominal value for the series resistance $R_s = R_0 + R_{ext}$ is calculated from the series resistance R_0 of the as-grown sample and the external metal film resistor R_{ext}. Figure 5 shows the deviation

$$\Delta R = (R_{sX} - R_s)/R_s \tag{11}$$

with X = A, B, C for the four orders of magnitude over which the external resistor R_{ext} is purposely varied. The quantity $\overline{\Delta R}$ which gives the deviation averaged over all nine ΔR values is 0.25% for plot A, 67% for plot B, and 0.65% for plot C. The evaluation based on plot A yields thus the smallest deviations from the nominal values and that based on plot B is particularly unreliable.

Figure 6 shows results for the idealities n_{A1}, n_{B1}, n_{C1} which are obtained together with the resistances R_{sA}, R_{sB}, R_{sC} for Fig. 5. The values n_{A2}, n_{B2}, n_{C2} stem from the slope of the semi-logarithmic I/V plot after correcting the voltage axis of Fig. 4 for the voltage drops at the respective series resistances R_{sA}, R_{sB}, R_{sC}. Figure 6 illustrates that the deviation

$$\Delta n = n_{Xi} - n_0 \tag{12}$$

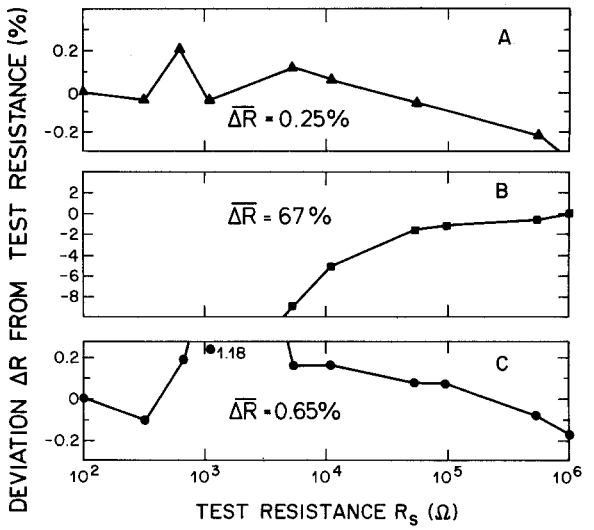


Fig. 5. Deviation of evaluated series resistance from nominal resistance when I/V curves from Fig. 4 are evaluated with plots A, B, C. The analysis based on plot A yields the best average deviation of 0.25%. Plot B is only suitable for large series resistances

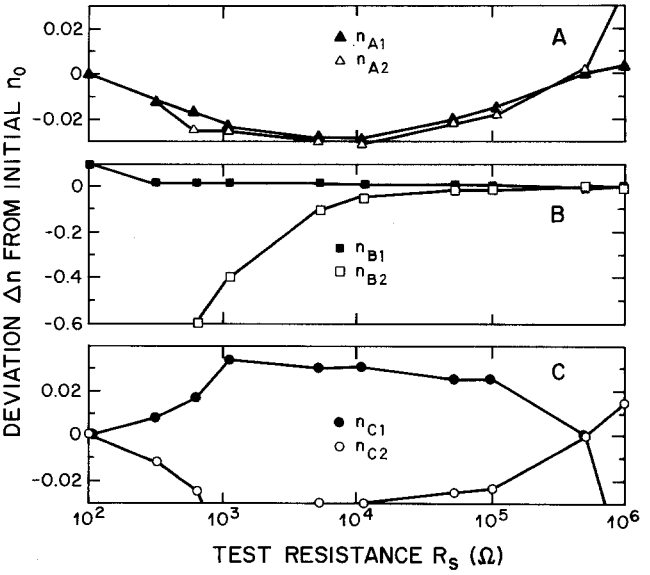


Fig. 6. Deviation of idealities from the nominal value $n_0 = 1.049$ when the curves from Fig. 4 are evaluated with plots A, B, C. Idealities n_{A1}, n_{B1}, n_{C1} are obtained in plots similar to Figs. 3a–c together with the resistance data for Fig. 5. Idealities n_{A2}, n_{B2}, n_{C2} stem from the evaluation of the curves in Fig. 4 after a correction of the voltage axis for the drop at the series resistances. Plot A yields results are more accurate and redundant that those from plots B and C

with X = A, B, C and $i = 1, 2$ is roughly comparable for plots A and C, which are both more reliable than plot B. Plot A yields the smallest deviations which amount to maximal 0.03 (corresponding to 3%). Moreover, plot A also yields the most redundant results: The

deviation between n_{A1} and n_{A2} of about 0.01 is better than the deviation from plot C of up to 0.06 between n_{C1} and n_{C2}.

Figure 7 shows finally the results of the percentage deviation

$$\Delta\Sigma = (\Sigma_X - \Sigma_0)/\Sigma_0 \quad (13)$$

with X = A, B, C for the barriers Σ_A, Σ_B, Σ_C from the nominal value Σ_0. The superiority and versatility of plot A is again demonstrated. For low series resistances plot B yields again large deviations from the nominal values. The deviation $\overline{\Delta\Sigma}$ averaged over all results in Fig. 7 is less than 0.85% for plot A, 13.4% for plot B, and 0.95% for plot C.

c) Discussion. It is emphasized here that in the test described exactly the same I/V data are evaluated with the help of plots A, B, C. Nevertheless, the test results demonstrate that the evaluation based on the three plots may yield significantly different values, as for example elucidated in Fig. 7 for the Schottky barrier Σ.

The deviation between the evaluation results of the three plots originates solely from the different weighing of different parts of the original I/V curve: The experimental I/V data were originally equidistantly distributed over the voltage axis; the three plots redistribute these data, however, differently over their abscissa as demonstrated in Fig. 3a–c. The least square fits weight therefore not all regimes of the current voltage curve equally.

Plot B is particularly unreliable because it uses the inverse current $1/I_d$ as abscissa and the differential resistance R_{dr} in a *linear* ordinate. Figure 4 shows that for series resistances $R_s < 10\text{k}\Omega$ the current I_d (and so do $1/I_d$ and the differential resistance R_{dr}) changes over about three orders of magnitude for voltages between 0.2 V and 0.8 V. All data points are, however, equally weighed in the linear fit. The fit emphasizes therefore data at large values for $1/I_d$ and R_{dr} which (as for example demonstrated in Fig. 3b) correspond to small voltages where electrical noise and shunt currents may influence the underlying I/V measurements. The *linear* extrapolation over orders of magnitude yields therefore unreliable fit results for the series resistance R_s.

Plot C uses the current I_d as abscissa and I_d/G as ordinate. The voltage dependence of I_d/G is smaller than the dependence of the R_{dr}-ordinate of plot B. This weaker voltage dependence can be seen in a comparison of Figs. 3b, c: Fig. 3c delineates a much wider voltage regime of the I/V data from Fig. 1 than Fig. 3b. Moreover, plot C distributes the measured data more equidistantly and yields therefore a better data basis for the least square fit than plot B. Nevertheless, plot C is not the optimum choice for an evaluation: The use of the linear current axis as abscissa emphasizes data at high currents. This emphasis is not too important in the present test with an external resistor of fixed value, but may, however, yield unreliable results in the case of diodes with large series resistances due to a low doped substrate. An evaluation which makes in particular use of the high current regime of the measured I/V curve may yield erroneous results because the series resistance may depend on voltage due to heating or minority carrier conductivity modulation.

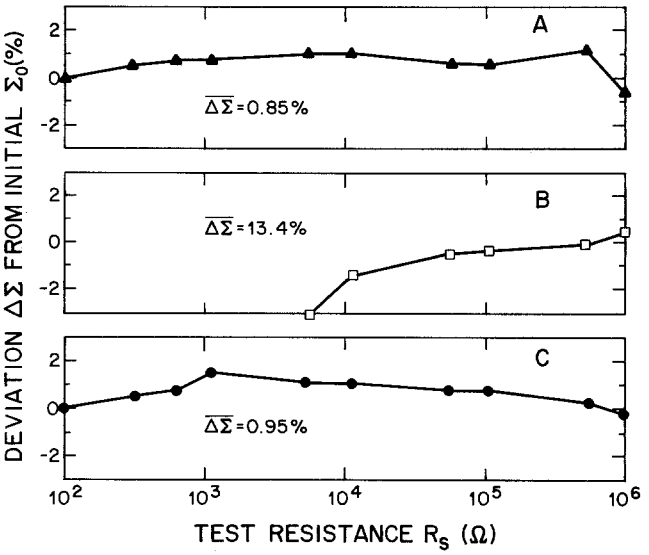


Fig. 7. Correction of the voltage axis in Fig. 4 for series resistances enables to determine the Schottky barrier Σ. Figure shows the deviation of Σ from the nominal value Σ_0 when series resistances from plot A, B, C are used for the correction. Plot A yields the best deviation of 0.85% averaged over all test resistances

Plot A turns therefore out to yield the best basis for a reliable evaluation of I/V data. This plot is even superior to plot C. This slight advantage is based on the use of the conductance G as abscissa. The main influence in the fit stems then from data at intermediate voltages. The data at high currents (dominating plot C) as well as the low voltage regime (dominating plot B) are both de-emphasized. Moreover, Fig. 2 shows that the conductance G varies even less with voltage than the current I_d. A wide voltage regime is therefore linearly delineated in plot A as demonstrated, for example, in Fig. 3a. The test in Figs. 5 and 7 elucidates that the evaluation with plot A yields the series resistance R_s and the Schottky barrier Σ with an accuracy of about 1%. According to Fig. 6 the ideality from plot A agrees within 3% with the value of the as-grown Au/Cr/GaAs diode from Fig. 4. The maximum deviation of 3% is already explainable by a slight voltage dependent ideality n_0 of the as-grown Au/Cr/GaAs diode.

4. Dangers and Pitfalls

The three plots from Sect. 2 are based on (1) and (5) and the assumption that the saturation current I_s, i.e. the Schottky barrier Σ, the ideality n, and the series resistance R_s all are independent of bias voltage V. Moreover, the use of (1) and (5) for the fitting of I/V curves implies also that the ideality $n \approx 1$. Slightly higher values up to $n = 1.1$ could be caused by image force lowering [2] or tunneling currents [19]. However, fits for low-doped samples which yield $n \geqq 1.2$ should be regarded with caution. Such high n-values could for example be caused by an interfacial layer with or without interface states [3, 4], by minority carrier currents [13], or, by a general voltage dependence of Σ, n, R_s. In any case, fits with $n \geqq 1.1$ require measurements in addition to the I/V curve in order to confirm the dc characterization. The Schottky barrier could, for example, be confirmed with the barrier from capacitance/voltage curves; interface states are detectable with the help of frequency dependent admittances [4]. Numerical agreement between measured and modeled I/V curves alone does not give conclusive proof for the validity and applicability of the thermionic emission model.

In fact one could argue that a decent computer program should *always* be able to fit *any* I/V curve like curve β in Fig. 1 with some values for the three fit parameters Σ, n, R_s. It is therefore stressed that the here proposed plots all are not based on the I/V data alone but also on the slope of this curve, i.e. the conductance G. Validity of any model which could be described by (1) requires not only numerical prediction of the I/V data but also a linear relationship in the three plots A, B, C which use the *conductance* data. The three plots based on (5–7) can therefore be used to verify the validity of the used theory. The plots use in their linear representation of the data not three but only *two* parameters (n, R_s) and any deviation from linearity in these plots indicates an inapplicability of the model.

Figures 8 and 9 demonstrate, for example, how plot A is usable to indicate a failure of the used thermionic emission model with voltage independent values for Σ, n, R_s. The measured I/V curve from Fig. 8 is taken from a Au/Si Schottky diode. Before the evaporation of the Au, the Si wafer with a nominal series resistance of 3Ω is treated in a hydrogen plasma with bias voltages around 600 V [20]. The plasma results in surface damage and an interfacial layer. The dashed curve in Fig. 8 represents a fit to the I/V curve which is found by the variation of Σ, n, R_s. This trial and error fit on basis of (2) and (7) yields $\Sigma = 0.68$ eV, $n = 2.2$, $R_s = 220\Omega$. The model I/V curve agrees *numerically* well with the measured data and is only for $V < 0.15$ V and for $V > 0.8$ V distinguishable from the experimental curve.

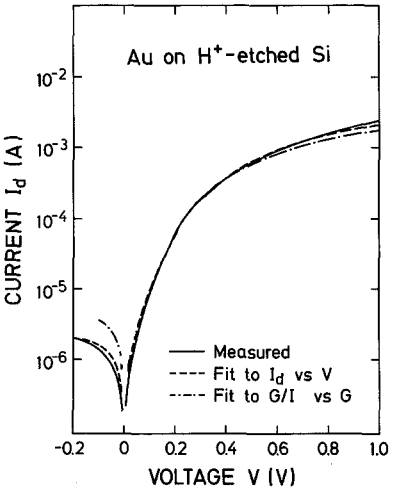


Fig. 8. I/V curves of a surface damaged, plasma treated Au/Si diode. The dashed theory curve with $\Sigma = 0.68$ eV, $n = 2.20$, $R_s = 220\Omega$ agrees *numerically* with the measured curve. Figure 9 demonstrates, however, that the measured curve cannot be *physically* meaningful fitted with voltage independent parameters n, R_s. Dash-dotted curve stems from the best linear fit to the measured data in Fig. 9 between 0.1 V and 0.8 V

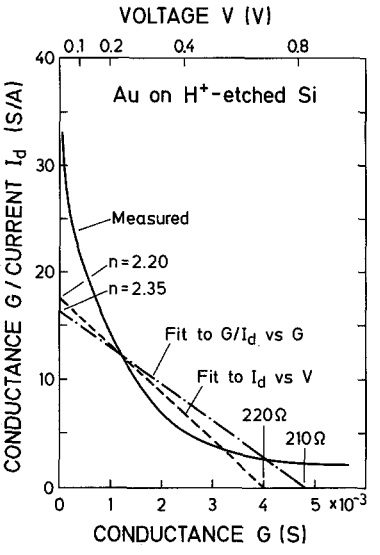


Fig. 9. The deviation from linear behavior demonstrates that it is impossible to fit the measured I/V curve of Fig. 8 *physically* meaningfully with the thermionic emission theory of (7) and (8). The dashed curve indicates the theoretical thermionic curve for $n = 2.20$, $R_s = 220\Omega$, which (together with $\Sigma = 0.68$ eV) yields the *numerical* agreement with the measured I/V data in Fig. 8. The dashed-dotted line represents the best linear fit between 0.1 V and 0.8 V

The delineation of the I/V data from Fig. 8 with the help of plot A in Fig. 9 elucidates, however, that it is impossible to model the experimental data *physically* meaningful with voltage independent values for ideality n and series resistances R_s. The measured data in the G/I_d versus G plot deviate considerably from the

linear behavior which is predicted by (8). The dashed curve in Fig. 9 indicates the expected behavior for an ideality $n=2.2$ and the series resistance $R_s=220\Omega$, which (together with $\Sigma=0.68$ eV) yield the good agreement with the measured data in Fig. 8. Only the use of all *three* parameters at the same time enables obviously this apparent good fit in Fig. 8. Figure 9 uses only two of the three parameters and reveals therefore the failure of the model. The I/V curve of Fig. 8 which is caused by the interfacial layer of this surface damaged Schottky diode displays in fact a voltage dependent ideality. The diode should therefore be analyzed with the help of admittance measurements and the so-called trap transistor model [4] to deduce the energy distribution of interface states.

Figure 9 also shows results when one starts the evaluation with the analysis of the conductance data. The dash-dotted line represents the best linear fit with $n=2.35$ and $R_s=210\Omega$ which one obtains to the G/I_d versus G data for voltages between 0.1 V and 0.8 V. The series resistance of 210Ω is then used to correct the I/V curve for the determination of the Schottky barrier. The recalculated I/V curve based on this fit is indicated by the dashed-dotted line in Fig. 8.

The discussion here clearly demonstrates that it is *not* sufficient to obtain a numerical agreement between measured and fitted I/V data to verify the validity of a theory. Instead, prediction of the I/V curve as well as of the *conductances* has to be achieved. The conductance data are conveniently delineated in plots like Fig. 3a and Fig. 9, which reduce the three fit parameters used here to two, and therefore enable one either to verify or to invalidate the model used for the current transport mechanisms.

5. Conclusions

Three different plots for the fit of forward bias current/voltage curves of Schottky diodes have been discussed. The analysis based on plot A which is shown in Fig. 3a turns out to yield the most reliable and accurate values for the Schottky barrier Σ, the ideality n, and the series resistance R_s. It has also been demonstrated that the delineation and analysis of the measured I/V data with the help of plot A is really necessary in order to either confirm the validity or to reveal the failure of the model used for the current transport. Not only modeled and measured I/V curves, but also the *conductance* data (represented in plot A) have to be predicted in order to demonstrate the physical applicability of the used theory.

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