Time Synchronized Sensor Network with IEEE1588 for Vibration Measurement in Structural Health Monitoring of Railway System

Guotao Jiang(✉), Yong Liu, Yu lv, and Haiyan Wu

CRRC Zhuzhou Electric Locomotive Research Institute Co., Ltd., Zhuzhou, China
{jianggt,liuyong3,lvyu,wuhy2}@csrzic.com

Abstract. Sensor network has become an important area of research and various new applications for remote sensing are expected to emerge. One of the promising applications is structural health monitoring of building or civil engineering structure and it often requires vibration measurement. For the vibration measurement via network, time synchronization is indispensable. This paper clarifies the importance of time synchronization of sensor network for vibration measurement. And the rationale of IEEE1588 precision time protocol is described. A distributed synchronized measurement system based on the IEEE1588 is presented in this paper and the test result are also introduced.

Keywords: Sensor Network · IEEE1588 · Time Synchronization

1 Introduction

For vibration measurements based on Ethernet, time synchronization is important because the vibration data simultaneously measured at multi-point sensor nodes are often transmitted via multi-hop relayed network devices [1]. Due to the queuing process in switched Ethernet, the data arrived at the destination with a random time delay [2]. So the data measurement timing based on the time of receipt of command or data message is imprecise and not suitable for synchronized measurement with high-accuracies. Since in data analysis, a time difference may be misunderstood as a phase shift [1]. To maintain precise time consistency among network nodes, time synchronization is indispensable. In the following section, adverse effects on vibration sensing caused by a fault timing and the reason why time synchronization is needed are described in detail. Section 3 introduces the rationale of IEEE1588. In Sect. 4, we presents a synchronized measurement system based on the IEEE1588. In Sect. 5, test result of time synchronization precision are presented.

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2 Time-Delayed Effects on Vibration Measurement

In vibration measurement applications, sensors usually need to be placed at several points on different place in buildings or structures [3]. The measurement system,which includes a host station as a node of the network, is often composed of multi-hops network with numbers of nodes. In such cases, especially the numbers of nodes is considerable, the communication delay between the host station and sensor nodes is uncertain. Therefore, if the host station send the data acquisition command to sensor nodes, the arrival time may be different. This fact introduces errors in modal analysis of the measured data. Figure 1 (a) demonstrates the motion of a bending beam with three measured points. In the bending process, the tip of the beam moves from P1 to P2 and P3. Assume that the transmission of sampled data on the tip of the beam is delayed, it actually presents that the tip is still at P2 position even though other points moves forward (see Fig. 1 (b)).

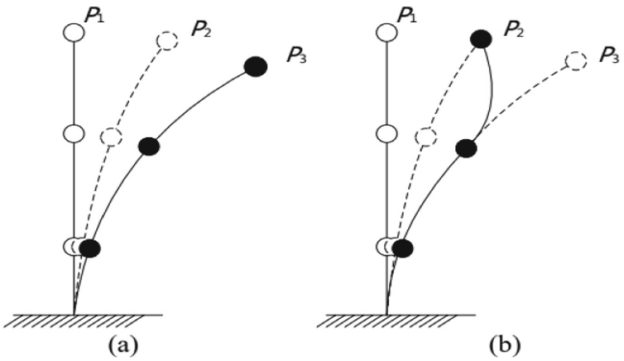

Fig. 1. Time-delayed effects on vibration measurement

To resolve this problem, we propose a synchronized measurement system with 4 key functions: firstly, the network maintain a synchronized global clock; secondly, the sensor sampling is based on triggering the specified events referenced to the time of the synchronized local clock; thirdly, the command of measurement sending from the host station is consist of start time of sampling and the sampling cycle; finally, the sampled data is combined with the timestamp of the moment when the data is sampled. The network synchronization is achieved by IEEE1588, which is discussed in the next section.

3 The Rationale of IEEE 1588

A common sense of time is established by having each network node contain a real-time clock synchronized to its peers. This may be accomplished using IEEE 1588, which is a Standard for Precision Clock Synchronization Protocol for Networked Measurement and Control Systems [4]. It is also known as Precision Time Protocol (PTP) and is used for time/clock synchronization in packet-based networks [5]. PTP was introduced to

achieve synchronization accuracies in the order of sub microseconds. Influenced by the multi-task schedule scheme of the processor, to acquire timestamp in the application level (e.g. the Network Time Protocol (NTP) and Simple Network Time Protocol (SNTP)) is unable to achieve synchronization accuracies in the order of sub microseconds, as depicted in Fig. 2 [6]. Timestamp acquired in the MII interface between MAC layer and Physical layer is adopted in this paper according to IEEE1588, which can avoid the jitter in the software execution [7]. The timestamp acquired in the MII interface is only related with the network data transmission delay and jitter.

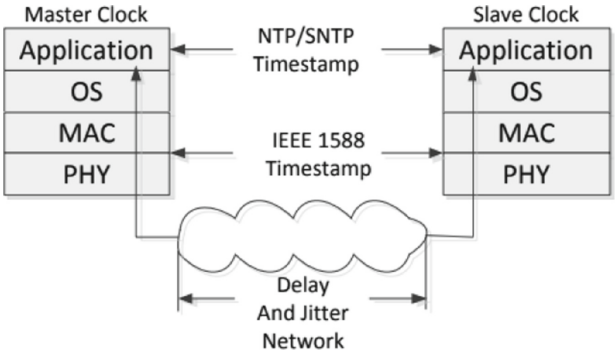

Fig. 2. Timestamp point in message processing

The proposed measurement system relies on a communication infrastructure based on switched Ethernet, which includes both end nodes and network equipment (e.g., switches). Precise computation of the offset between two nodes can be obtained by estimating the propagation delay of the network link (path delay). Path delays can be evaluated in the peer delay mechanism. The PTP end nodes are Ordinary Clocks (OCs), including Master Clocks (MCs) and Slave Clocks (SCs). The network equipment, switches, are Transparent Clocks (TCs), which are able to calculate the residence time and compensate propagation delays over network links by using a suitable peer delay mechanism. The schematic to demonstrate the calculation of residence time and peer delay mechanism are schematically represented in Fig. 3. As shown in the this figure, the peer delay mechanism, which is based on the exchange of two messages, enables a port B (requestor) to estimate the propagation delay with respect to a port A (responder).

The port B records the timestamp T_{t1} at the point in time (PIT) of sending a Pdelay_Req (peer delay request) message to port A. The timestamp T_{m1} is taken at the PIT of the receiving request message by port A. Then, as quickly as possible, B records a timestamp T_{m2} at the PIT of replying a Pdelay_Resp (peer delay response) message. The port B embeds the difference $T_{m2} - T_{m1}$ in Pdelay_Resp message. The time stamping, calculation difference $T_{m2} - T_{m1}$ and embedding Timestamp in Pdelay_Resp message is processed on-the-fly by hardware. T_{t2} is recorded by port B at the PIT of response message arrival. With the assumption that the time T_{A2B}, to transfer a packet along the path between two nodes A and B is the same as the time T_{B2A}, spent travelling in the

opposite direction, the path delay $T_{Dlink\text{-}mt}$ is then computed by the TC as follows:

$$T_{Dlink-mt} = [(T_{t2} - T_{t1}) - (T_{m2} - T_{m1})]/2 \tag{1}$$

Processed as the same way as $T_{Dlink\text{-}mt}$,the path delay $T_{Dlink\text{-}ts}$ between port C and port D can be calculated by the SC as follows:

$$T_{Dlink-ts} = [(T_{s2} - T_{s1}) - (T_{t4} - T_{t3})]/2 \tag{2}$$

The time spent by a PTP message in traversing a network device is the residence time. As shown in Fig. 3, the residence time $T_{Dswitch}$ can be calculated as follows:

$$T_{Dswitch} = T_{Sync-out} - T_{Sync-in} \tag{3}$$

where $T_{sync\text{-}in}$ is the PIT of Sync message entering the switch and $T_{sync\text{-}out}$ is the PIT of Sync message leaving the switch. The correction field of Sync message is updated when the timestamp $T_{sync\text{-}out}$ is recorded:

$$CorrectionField = CorrectionField' + T_{Dswitch} + T_{Dlink-mt} \tag{4}$$

And the path delay between the MC and the SC can be computed in SC as follows:

$$T_D = T_{Dlink-mt} + T_{Dswitch} + T_{Dlink-ts} \tag{5}$$

And the Time offset T_{offset} can be computed as follows:

$$T_{offset} = T_{s0} - T_{m0} - T_D \tag{6}$$

The T_{offset} can be used for synchronization of the local clock of SC.

4 The Synchronized Measurement System Design

Based on the switched Ethernet, the synchronized measurement device can be placed in the place of the target building or structure. a typical configuration of such a synchronized measurement network is shown in Fig. 4 [8]. Measurement devices (MDs) can be designed with multi-sensors (and can be expanded) [9]. The measurement device is synchronized and other ordinary devices (ODs, e.g., IP camera and other equipment) can also be integrated into the network. The measurement device is based on the FPGA platform, which is main consist of Altera Cyclone IV FPGA, analog-todigital convertors (ADCs) and other peripheral circuits, as depicted in the Fig. 5. A SOPC (system-on-programmable-chip) is built in the FPGA, which contains the NIOS II processor, Ethernet MAC, data measurement unit (DMU), hardware assisted 1588 unit (HA1588) and other IPs [10]. The DMU and HA1588 are user-defined Avalon devices.

The functional blocks in HA1588 provide the following characteristics and functions:

RX/TX TSU: Time stamping unit for incoming and outgoing PTP frames with the free running or the real time clock (RTC) and buffering timestamps in the internal FIFOs.

RGS: Memory-mapped registers used to provide interface for the processor to control the HA1588.

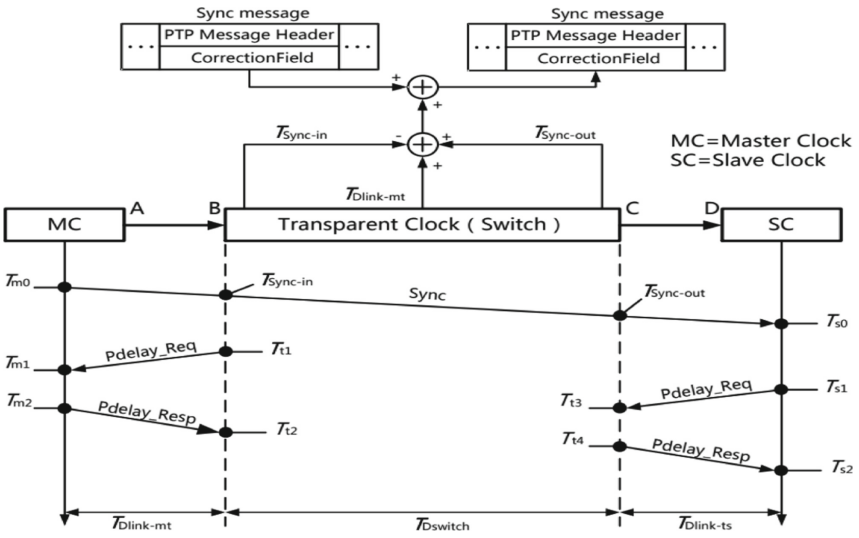

Fig. 3. Synchronization process with peer delay mechanism

RTC: frequency compensated real time clock, depicted as Fig. 6, which can be configured by the processor, providing time to the DMU. Architecture of frequency compensated real time clock is shown in Fig. 7. It consists of a 48 bits second counter, a 38 bits nano-second accumulator and a 16 bits compensation register, which is dynamic configured by the processor. The accumulator adds compensation register and the result is stored in the accumulator at every pose edge of the oscillator clock pulse. The accumulator is designed with a carry flag to indicate overflow.

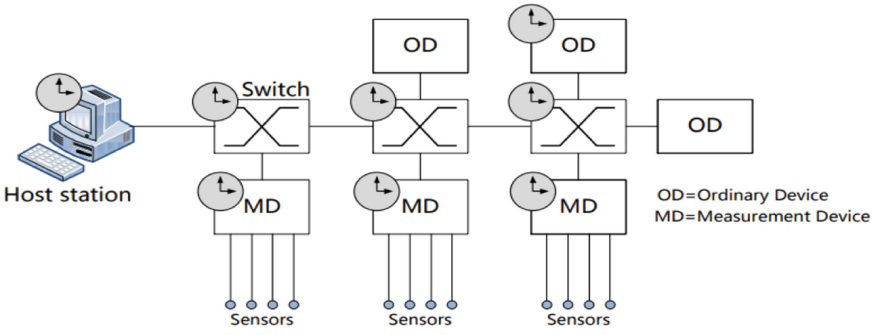

Fig. 4. Synchronized measurement network.

The functional blocks in DMU provide the following characteristics and functions:

SPI controller: SPI controller providing serial peripheral interface to the ADCs, and parallelizing the serial data.

TTU: Time trigger unit for triggering the ADCs sampling simultaneously with a preset time cycle and initiation time. The TTU can be configured dynamically for adjusting the sampling frequency.

MDTSU: Measurement data timestamp unit for recording the timestamp of the sampling event and concatenates the measurement data and timestamp together, and storing the concatenated data in buffers or RAM by DMA mechanism.

RGS: Memory-mapped registers used to provide interface for the processor to control the DMU.

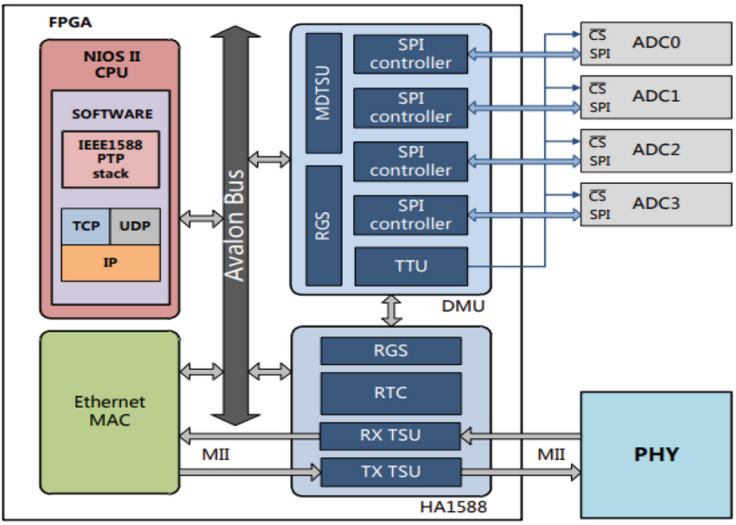

Fig. 5. Synchronized measurement device based on SOPC

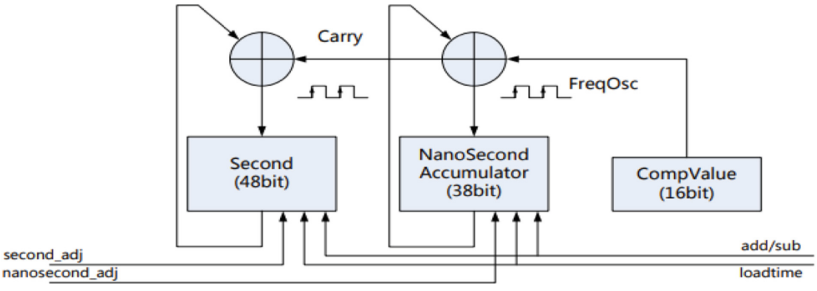

Fig. 6. Frequency compensation real time clock

5 Test and Experiment

To test the synchronization accuracies of proposed measurement system, a simple measurement device has been implemented with test signals of 1PPS (1 pulse per second). The test system is setup for experiments, as depicted in Fig. 7. 2 MDs, one configured as

MC and the other configured as SC, connect to a 1588 supported switch. And the 1PPS signals of the 2 MDs are connect the probes of the oscilloscope allowing visual verification of the synchronization accuracies. In the experiment, the Sync messsage interval is configured to 1 s, 2 s and 3 s. The RTC modules of the 2 MDs are operate at 125 MHz to provide 8 ns sampling granularity. Therefore, the quantization error of the RTC is 8 ns and a minimum of 32 ns jitter can be expected in the proposed experiment system. The Table 1 demonstrates the result of the experiment under different Sync message intervals.

The results show that, under 1 s Sync message intervals, the jitter of the 1PPS is below 300 ns. The experiment result indicates that synchronization accuracies is strongly correlated to the Sync message intervals as expected.

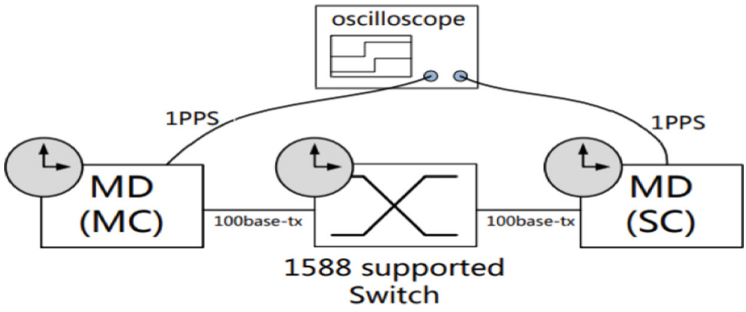

Fig. 7. Experiment setup

Table 1. Experimental result

Sync intervals (s)	Max offset (ns)	Min offset (ns)	Jitter (ns)
1	−134	+153	287
2	−277	+309	586
3	−603	+646	1249

6 Conclusion and Future Work

The prototype of the synchronized measurement system is performed with jitter under 300 ns and the sub micro-second synchronization accuracies is verified to meet the need of synchronized measurement. There is still room for reducing the jitter performance with a improved frequency compensation algorithm and control techniques. Further testing for the proposed system will focus on the synchronized data acquisition and more MDs will be implemented in the test system.

References

1. Yutaka, U., Tadashi, N., Motoichi, T.: Time synchronized wireless sensor network for vibration measurement. SICE Annual Conference 2007, pp. 2940–2945 (2007)
2. Xiaoya, H.: Study of Networked Control System Based on Switched Ethernet. Ph.D Dissertation. Huazhong University of Science and Technology (2006)
3. Xiaokai, Z.: The Research and Design of Wireless Sensor Network for Structure Health Monitoring. Master Thesis. Zhejiang Sci-Tech University (2010)
4. IEEE Instrumentation and Measurement Society: IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, IEEE Std. 1588–2008 (2008)
5. Trifonov, H., Heffernan, D.: OPC UA TSN: a next-generation network for Industry 4.0 and IIoT. Int. J. Pervasive Comput. Commun. **19**(3), 386–411 (2023)
6. Heffernan, D., Doyle, P.: Time-triggered Ethernet based on IEEE 1588 clock synchronisation. Assem. Autom. **24**(3), 264–269 (2004)
7. Chelik, M., Beghdad, R.: Proposed method: mean delays synchronization protocol (MDSP) for wireless sensor networks. Int. J. Pervasive Comput. Commun. **16**(1), 74–100 (2020)
8. Arestova, A., Maximilian, M., Kai-Steffen, H., Reinhard, G.: A service-oriented real-time communication scheme for AUTOSAR adaptive using OPC UA and time-sensitive networking. Sensors **21**(7), 2337 (2021)
9. Ferrari, P., Flammini, A., Marioli, D., Taroni, A.: IEEE-1588-based synchronization system for a displacement sensor network. IEEE Trans. Instrum. Meas. **57**(2), 254–260 (2008)
10. S.B., S., Sandi, M.A.: Design and analysis of buffer and bufferless routing based NoC for high throughput and low latency communication on FPGA. Int. J. Pervasive Comput. Commun. **18**(2), 250–265 (2022)