File System for Digital Signal Processing Equipment Based on FPGA

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Abstract. A file system for digital signal processing equipment based on FPGA is designed. The ZYNQ-7000 FPGA is the processing center of the file system. An NVMe hard disk is connected to the GTx bank of FPGA as a PCIe device. FPGA and DSP chips interconnect through SRIO switch chip. Data which needs to be memorized comes from DSP through X4 SRIO interface. In FPGA, PL side receives command and data from DSP. PL buffers data to be memorized in different double port RAMs according to the command.PS reads data from buffer rams according to command data reading from command buffer rams and writes data to a responding subarea. Experiments show the designed file system memorizes data from DSP in real time. When data packet is 128 KB, writing data rate can be 550 MB/s.

Keywords: ZYNQ-7000 · NVMe hard disk · DSP · SRIO

1 Introduction

Digital signal processing system is a key device in equipment like radar, sonar and communication equipment. Data sampled and processed by digital signal processing system is very important and precious to the developer, especially in developing course. It is very important to save original data and some of processed data, for it's very useful for the developer to ameliorate the processing algorithm. Sonar digital signal processing system is the key device in the equipment. It is used to sample, transmit, process and memorize data. For the special experiment condition, equipment must do experiment in deep and large water like lake and ocean. Cost of experiment is quite large. Thus data is very precious in every experiment. A memorizing device is necessary in the digital signal processing system. For data needs to be memorized include the original data and processed data, the memorizing bandwidth will be high. For previous reasons, in this paper, a digital signal processing device file system based on FPGA is designed.

2 System Design

A file system based on FPGA is designed. Data transmitted by the processing unit needs to be memorized wrote to the hard disk by the FPGA. File system can memorize data from any processor in the processing system. The writing bandwidth can reach 500 MB/s. Data in disk can be accessed through the net.

Y. Zhang et al. (Eds.): CENet 2023, LNEE 1125, pp. 119–124, 2024.
https://doi.org/10.1007/978-981-99-9239-3_11

Disk used in the system is an NVMe hard disk. The NVMe hard disk is connected to the GTx bank of the FPGA. The FPGA used in this system is a Xilinx ZYNQ7000 serial chip, XC7Z045. A PCIe hard core is integrated on the chip, the NVMe disk is connected to GTx bank through X4 PCIe. Processing center of the digital signal processing system is TMS320C6678, the DPS chip communicate with FPGA through Serial RapidIO(SRIO). For there are several DSP chips and one FPGA in the system communicate through SRIO, an SRIO switch chip is used. Any DSP core can communicate with FPGA through the SRIO switch. Data could be wrote to hard disk by any DSP core. What's more, DSP chips can be more according to the number of interface of SRIO switch. Data wrote to hard disk can be accessed through FPGA net. System design is shown in Fig. 1.

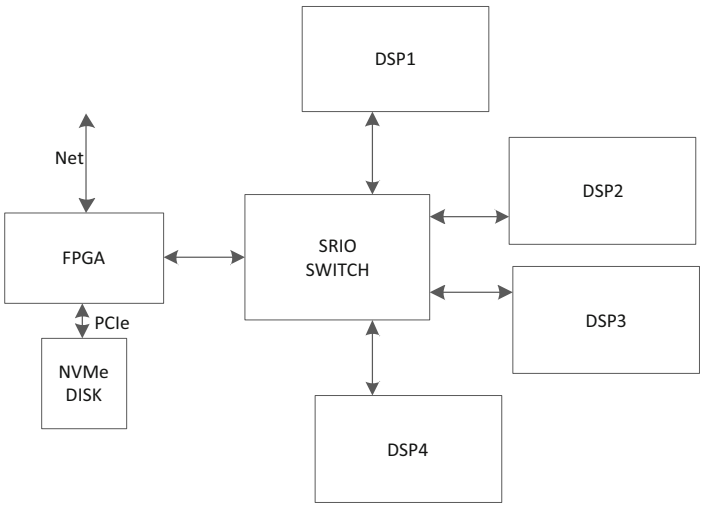

Fig. 1. System diagram of digital signal processing device fie system

3 PL Program Design

In FPGA, command and data comes from DSP through SRIO. Command received is buffered in a double port RAM, the double port RAM is connected to PS core through Bram controller core. PS can access the data in double port RAM through the Bram controller. According to number of subarea data wrote to disk, every kind data will be wrote to a corresponding subarea. Each subarea has a double port RAM in PL of FPGA. The ARM core controls the PCIe core to write data to the corresponding subarea according to the commands reading from the command buffer double port RAM. Data in buffer ram is wrote to the DDR3 SDRAM on PS side through HP channel. When data in buffer rams wrote to DDR3, PL writes a data valid byte to a BRAM. PS checks the data valid byte, when the valid byte checked, PS starts to read command data from the command buffer RAM. PS core controls the PCIe core writing data to NVMe hard disk according to command data. PS core connects to the PCIe core through GP channel,

Which is used to communicate the command data with PCIe core. Data memorize flow is shown in Fig. 2.

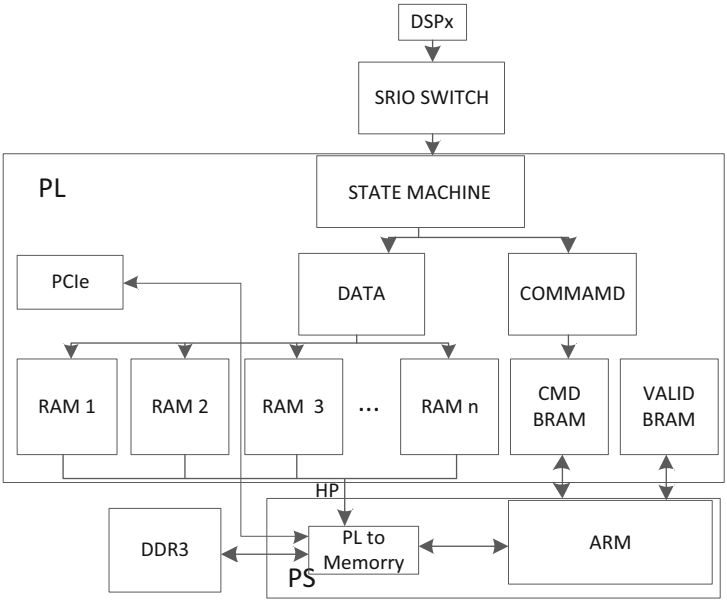

Fig. 2. Data memorize flow

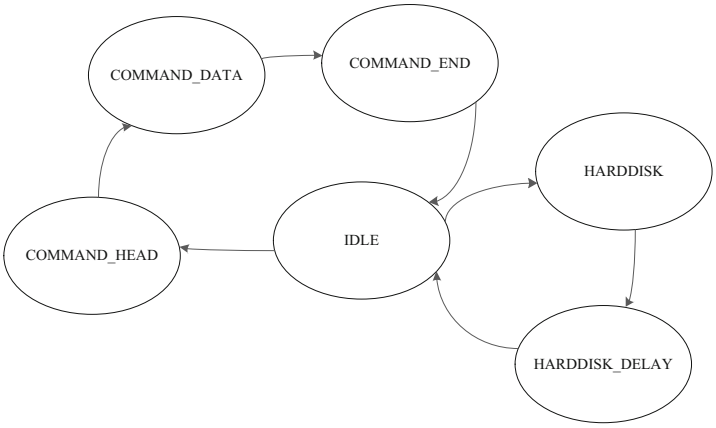

Fig. 3. File command data state machine

Command data state machine is shown in Fig. 3. Data received from DSP include command data and FR data. When command data head checked in the SRIO data packet, state machine runs to command branch. Command data from DSP includes FR initial, FR open, FR close, FR write, open file index, write file index and close file index.

Received file command is wrote to command buffer RAM and waits for PS reading. When a specific byte data received, state machine runs to HARDDISK branch. This brunch receive data to be wrote to the disk. FPGA operate data according to command received.

In HARDDISK brunch, received FR data is buffered in different RAMs according to command data. PL program check each double port RAM in sequence, when any RAM with data more than 128 bytes, program send data to the DDR3 on the PS side through HP channel. When all data according to command wrote to DDR3, PL write one given byte to a given DDR3 address. When PS checks the given byte, PS control the PCIe core to access data on the disk.

4 PS Program Design

Program for this system include PL program in FPGA hardware logic and PS program in ARM core. Hardware logic is the program in FPGA, as mentioned previously including data receiving, data state machine and data buffering. System software controlling center is on PS side. It is made up of one dual core Cortex-A9 processor, on chip memory and variety of interfaces. Which makes PS working independently with the PL.

4.1 Program Flow Design

PS can access data on PL side through BRAM controller. In this way, PS can control PL side and synchronize with the PS side. After system start up, PS sends a reset synchronization signal to PL side, which can ensure every module at the same beginning state. For PL will write data to the DDR3 on PS side, data in given address can be accessed by PL side through HP channel. DDR3 space accessed by the PL should be set to be uncached. Then program will initialize PCIe interface and NVMe hard disk. After initialization, program runs to a while(1), which process the FR data and command data. Software flow is shown in Fig. 4. The program checks the command valid byte, when checked, the program begin to do FR processing. Command processed include initialization, opening, closing, reading, writing, deleting, flushing, reparting and erasing. In each flow, the program do a responding operating.

5 Experiments and Discussing

The ZYNQ-7000 FPGA is processing center of the file system. Main processing task includes logic program and software. On PL side, logic communication with DSP through SRIO switch, parse command, data write to different buffer RAM, data writing to given address in DDR3, and communication of the PCIe core and NVMe hard disk. Software mainly deals with the file processing command comes from the DSP. PS reads command valid byte from PL side and dose the responding processing to the NVMe disk.

When debugging the program, integrated logic analyzer(ILA) is designed in the program. The key signal in the program can be watched from the Xilinx Chipscope tool,

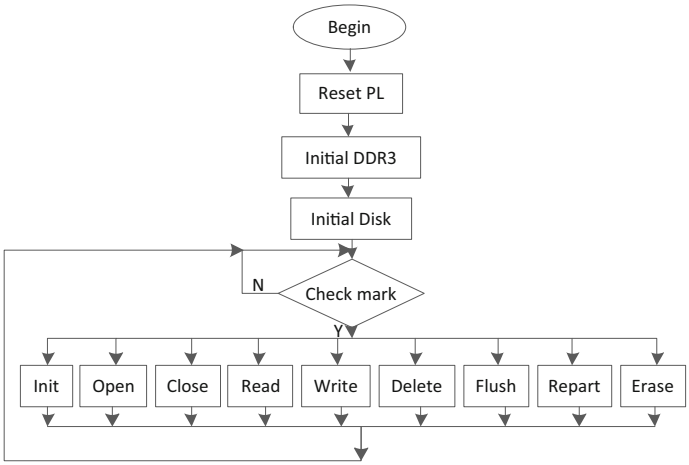

Fig. 4. Software flow

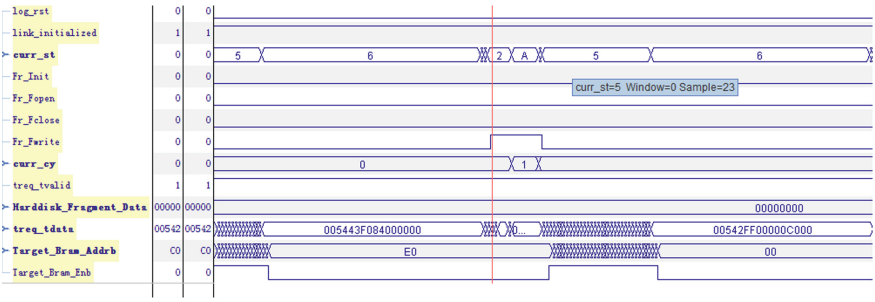

Fig. 5. Waveform from Chipscope

which will improve debugging efficiency. As shown in Fig. 5, when the PL received file command from SRIO, file initializing command is parsed. PL writes the command to BRAM, and responding command data was wrote to command data buffer BRAM.

According to data transmitted to ZYNQ from DSP, different data packets need to be memorized. There are some differences between different data packets in writing data rate. As shown in Table 1.

Table 1. Data rate between different packet

Packet size (KB)	Data rate (MB/s)
1	8
16	105
64	310
128	550
256	550

6 Conclusion

According to equipment in use, a digital signal processing device file system based on FPGA is designed. FR processing center is FPGA, NVMe hard disk is connected to a GTx bank of FPGA. FPGA receives command and data from DSP through SRIO. Command and data are pre-processed in FPGA, then wrote to given addresses in DDR3 on PS side. PS do processing according to command data. Experiments show when different data packets wrote to hard disk, the writing data rate is different. When data packets larger then 128 KB, writing data rate will be 550 MB/s.

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