Research on Buck Converter Based on Digital Control

Tonglin Wang, Hailong Ma, and Meimei Wu

Abstract With the rapid development of modern power electronics, digital technology is playing an increasingly important role in buck converters. The traditional analog-integrated chip-controlled buck converter requires a large number of components and is too large to meet the needs of power conversion development. The rapid development of digital control technology has led to the development of intelligent and miniaturized power conversion devices. To meet the development needs of miniaturization, digitalization, and efficiency of buck converter, this paper designs and verifies a buck converter based on digital control through the study of digital pulse modulation, signal processing, and PID algorithm. The device is controlled using an integrated chip and can achieve a wide range input of 50 V–240 V, a digitally adjustable output of 12 V–36 V, and a maximum output power of 100 W.

Keywords Buck converter · Digital control · PID algorithm

1 Introduction

With the rapid development of DC voltage generation technologies for renewable energy sources, such as fuel and photovoltaic cells, Buck converters are widely used in the power industry [1], such as DC motor drives, electric vehicles and home appliances [2]. Also buck converters are widely used in battery chargers, microprocessors, and motherboards [3]. With the massive access to various distributed energy sources, buck converters are widely used in DC microgrid systems [4], and as a bridge between DC power loads and DC grid energy exchange, DC converters have important research value due to their advantages such as high efficiency and good dynamic performance [5]. Along with the development of various technology

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fields to complete the update [6], buck converters are continuously improving their power density, efficiency, and fast dynamic response [7]. The traditional analog integrated chip-controlled buck converter requires a large number of components and is too bulky to meet the needs of power conversion development, so the use of digital control systems is the main area of innovation [8].

2 Digitally Controlled Buck Converter and Control Strategy

2.1 Digitally Controlled Buck Converter

Based on the converter function designed in this paper, the synchronous buck topology is selected as shown in Fig. 1. The synchronous buck converter achieves a lower conduction loss by replacing the diode of the asynchronous buck converter with a switching synchronous device. However, the synchronous buck circuit needs to control two transistors at the same time, and the control is more complicated. With the development of digital control technology, a digital chip with an internally integrated controller and upper and lower transistors can solve these problems very well. Synchronous Buck converter in the transistor Q1 conduction Q2 in the off state, at this time by the input power supply with inductors, capacitors and loads to form a circuit for inductor charging, so that the output voltage began to gradually rise. When the output reaches the required voltage level, transistor Q1 is turned off, and Q2 is in the on state, the circuit composed of the inductor, capacitor, and load, the power supply is not providing energy, but due to the characteristics of the inductor, the current cannot change abruptly, so the circuit does not have a power supply but the inductor continues to output power. The use of fast on and off switching tubes can be achieved on the DC voltage chopper buck.

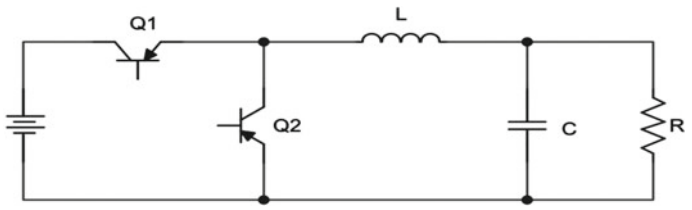

Fig. 1 Synchronous buck circuit

2.2 Control Strategy

PWM is considered as the core of the converter [9], the buck converter designed in this paper is controlled by digital PWM signal, which has better anti-noise performance and faster response to the change of output load when pulse width is adjusted [10], the PWM period is set by using the ARR of MCU timer reload value and the CCR of capture/comparison register value to set the PWM duty cycle, and the counter is set to count up. The control principle is shown in Fig. 2, in t1 time period, the count value is less than the comparison register value, output low; in t1t2 time period, the count value is greater than the comparison register value, output high; at t2, the count value is equal to the reload value, the counter overflows and starts from 0 again, and so on. Using the voltage loop feedback, the output is adjusted by the incremental PID algorithm. The incremental PID algorithm is shown in Fig. 3 to adjust the PWM output by proportional, integral, and differential operations of the error between the ADC detection value and the target value.

3 Main Circuit Component Selection

The main technical specifications of the device designed in this paper are shown in Table 1 design parameters.

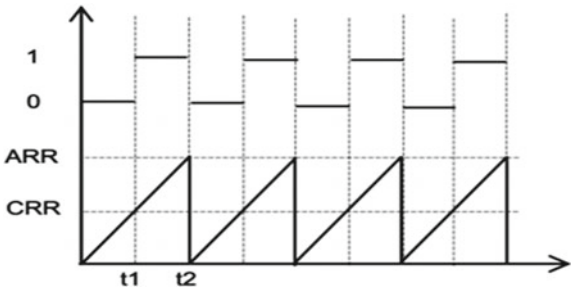

Fig. 2 PWM control principle

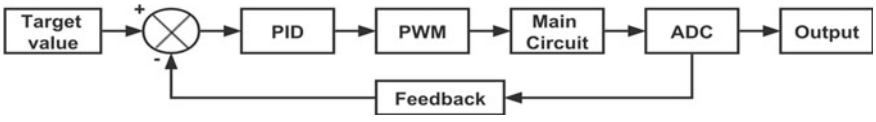

Fig. 3 Incremental PID

Table 1 Circuit design parameters

	Parameters	Numerical values
1	Input voltage range	50 V–240 V
2	Output voltage range	12 V–36 V
3	Switching frequency	13 kHz
4	Output power	100 W

Input and output voltage values versus minimum duty cycle are tried as:

$$D = \frac{U_{\mathrm{OUT}}}{U_{\mathrm{IN}}} = \frac{12}{240} = 0.05 \tag{1}$$

The theoretical maximum output current of the device should be 2.8 A. In the actual design, in order to prevent overload burned device, based on the output voltage IOUT for 10 A to calculate the required components, according to engineering practice, it is known that the general current ripple rate of 0.4, the peak current value formula can be obtained as follows:

$$I_{\mathrm{PP}} = (1 + 0.4) \times I_{\mathrm{OUT}} = 14\ \mathrm{A} \tag{2}$$

The switching frequency FSW is 13 kHz and the minimum inductance value is:

$$L_{\mathrm{MIN}} = \frac{V_{\mathrm{OUT}} \times (1 - D)}{0.4 \times I_{\mathrm{pp}} \times F_{\mathrm{SW}}} = 156\ \mathrm{uH} \tag{3}$$

According to engineering practice, inductance value needs to keep margin and combined with the actual inductor model, and this paper designs inductor selection 220 uH. The output voltage ripple is generally 0.01 of the rated voltage, so the output ripple voltage V_r is:

$$V_r = 0.01 \times (V_{\mathrm{max}} - V_{\mathrm{min}}) = 0.24\ \mathrm{V} \tag{4}$$

The switching tube frequency FSW is 13 kHz, so the on or off time of the switching tube can be approximated as:

$$\Delta t = \frac{1}{F_{\mathrm{SW}}} \times \frac{1}{2} = 38\ \mathrm{uS} \tag{5}$$

According to the formula $V_r = I_{\mathrm{OUT}} \times \frac{\Delta t}{C}$, the minimum capacitance value $C =$ 3.2 mF can be calculated. In order to reduce the voltage fluctuation more effectively and according to the actual capacitor type, two capacitors with a voltage withstand value of 50 V, 4700 uF are connected in parallel, and two more 0.1 uF capacitors are connected in parallel to reduce the high frequency interference.

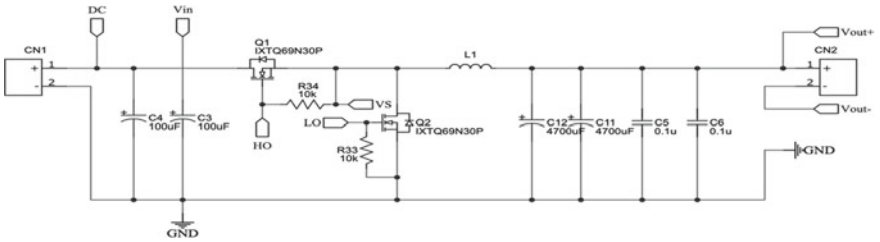

Fig. 4 Buck circuit

4 Converter Design

4.1 Main Circuit Design

The buck circuit design is shown in Fig. 4. The input voltage is filtered by two aluminum electrolytic capacitors with 450 V withstanding voltage and 100 uF capacity to make the input voltage waveform smoother and more stable. The output inductor is 220 uH, and the output capacitor is composed of two aluminum electrolytic capacitors with a voltage tolerance of 50 V and a capacity of 4700 uF in parallel with two 0.1 uF ceramic capacitors. The switching tube is IXTQ69N30P field effect tube, whose VDSS can reach 300 V and current can reach 69 A, with high switching speed and low switching loss. Vout+ and Vout− are the output voltage sampling interfaces, where Vout− is also the output current sampling interface, and HO and LO are controlled by the driver chip to turn on and off.

4.2 Sampling Circuit

The sampling circuit as shown in Fig. 5 is composed of LM358 op-amps, A is the output voltage sampling circuit, the use of differential op-amps can well suppress common mode interference and provide signal-to-noise ratio, and the amplification of the differential input voltage is R4 than R1; B is the output current sampling circuit, by sampling the voltage on R8 and convert it to current value through conversion algorithm; C is the input voltage detection circuit, is a voltage following circuit composed of op-amps, the output voltage value is the voltage value on R12, D is the protection circuit, is a comparator composed of op-amps, by the voltage division of the power supply and the current detection circuit, and the output voltage value is the voltage value on R12. C is the input voltage detection circuit, a voltage following circuit composed of op-amps, the output voltage value is the voltage value on R12, D is the protection circuit, a comparator composed of op-amps, by comparing the op-amp power divider value with the output value of the current detection circuit; when an overload occurs, the output value of the circuit detection circuit is greater

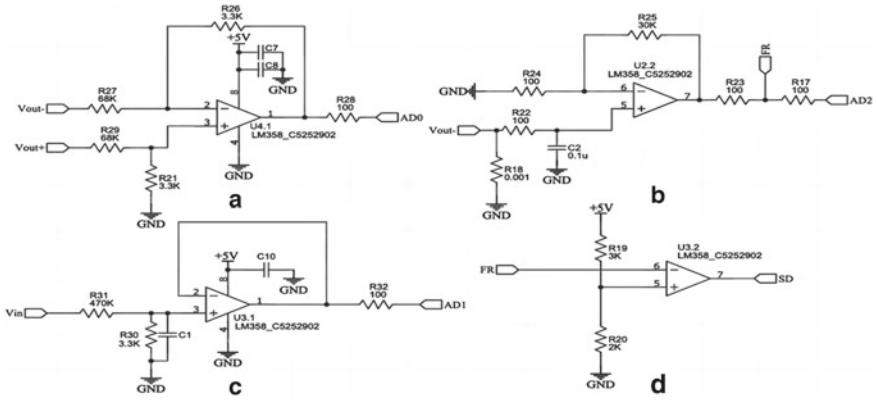

Fig. 5 Sampling circuit

than the op-amp power divider value, and the circuit outputs a low level to disable the driver chip.

4.3 Drive Circuit

The driver circuit design is shown in Fig. 6. The SD port is connected to the main control chip and the overcurrent protection circuit to control whether the chip works or not, and the IN port is connected to the main control chip to control the IR2104 chip to output PWM waves. The two MOS tubes of the synchronous buck converter can be controlled with only one PWM signal. When the MOS tube works, its drain level floats to ground, and the potential is not 0. At this time, it is necessary to place a bootstrap capacitor between VB and VS and charge it with a bootstrap diode to form a voltage difference between HO and VS, which can be used to open the upper bridge arm. In series with the gate resistor to increase the oscillation damping to reduce the sharp oscillation of the PWM waveform to avoid MOS damage, because the MOS tube gate and source input impedance is very high, in order to avoid MOS tube misconductor, so in parallel with a 10 K resistor between the source and the gate.

4.4 Master Control Chip Circuit

The main control chip circuit is shown in Fig. 7. The main control chip used in this paper is an STM32F030F4P6 chip with a maximum frequency of 48 MHz, a built-in 32-bit core, 256 KB of flash memory, 32 KB of static RAM, 20 ports, a 5-channel DMA controller, a 12-bit ADC with up to 16 channels, and six channels

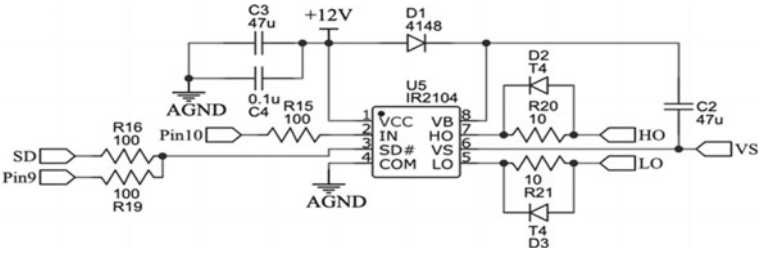

Fig. 6 Drive circuit

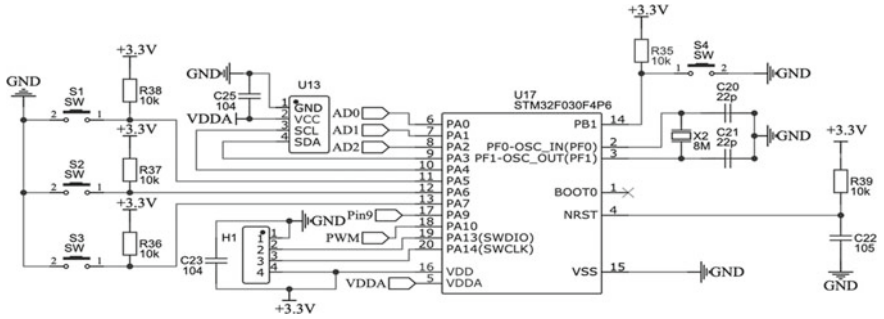

Fig. 7 Main control chip circuit

of PWM output. STM32 chip HSE default is 8 MHz, and using 8 MHz crystal can easily calculate the main clock frequency. When the microcontroller is powered on, the capacitor is charged, and after the capacitor is charged, the reset pin goes from low to high to complete the reset. VDD can effectively filter out the high-frequency components in the voltage by grounding the filter capacitor, which can ensure the stability of the power supply.

4.5 Programming

The main control program is shown in Fig. 8. After system initialization, the ADC subroutine is called for sampling. The ADC subroutine uses three channels to read the input voltage, output voltage, and output current, respectively, and the read values are averaged to reduce the error and converted to actual values by mathematical operations. If the setting mode is selected, the output voltage and output current limit values are set by key and displayed on the OLED; if no regulation mode is selected, the OLED directly displays the system operation parameters. After the output starts, the actual value of output current and voltage collected by ADC is compared with the protection value; if the output exceeds the protection value, the output is stopped immediately; if it does not exceed the protection value, the PID regulation program

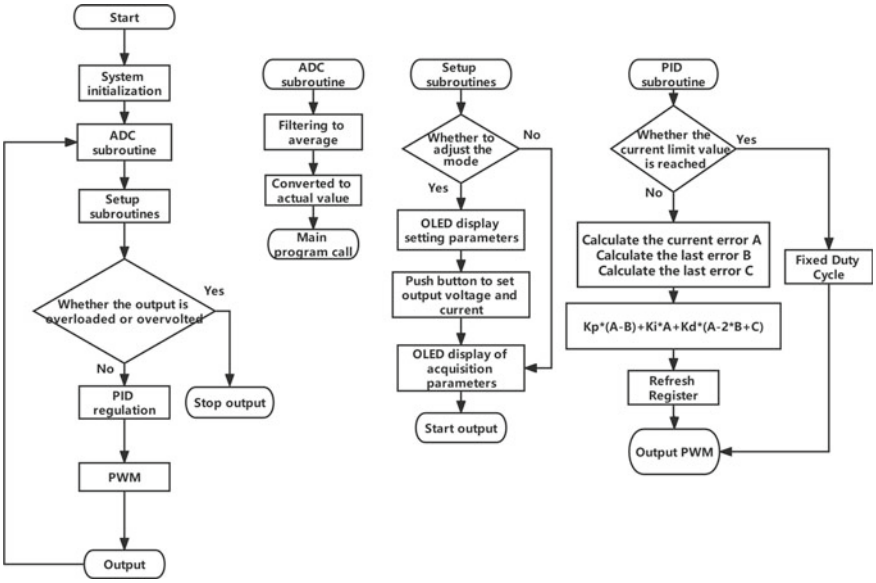

Fig. 8 Master control program

is entered. In the PID program, first judge whether the output current value reaches the set current limit value, if it reaches the limit value, then jump out of the PID program; if it does not reach, then calculate the current error value A, the last error value B, and the last error value C; through the incremental PID formula, update the register value to change the duty cycle.

5 Experimental Tests and Conclusions

5.1 Experimental Testing

The digitally controlled buck converter is physically shown in Fig. 9, using an adjustable DC source as the device input and a cement resistor as the load for testing.

After connecting the experimental device, adjust the input voltage to 50 V, set the output voltage to 12 V, and test its no-load output with MOS tube waveform as shown in Fig. 10.

At an input voltage of 50 V and an output voltage of 12 V no-load, the output is stable with a switching tube duty cycle of 21.8% and a drive voltage peak-to-peak of 12.20 V, which is consistent with the design.

While keeping the output voltage at 12 V, the input voltage is increased to 240 V, and the no-load output and MOS tube waveforms are tested as shown in Fig. 11.

Fig. 9 Physical device

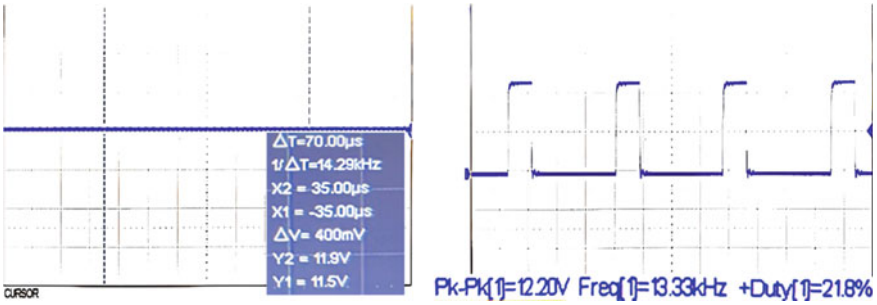

Fig. 10 No-load output and MOS tube waveform at 50 V input and 12 V output

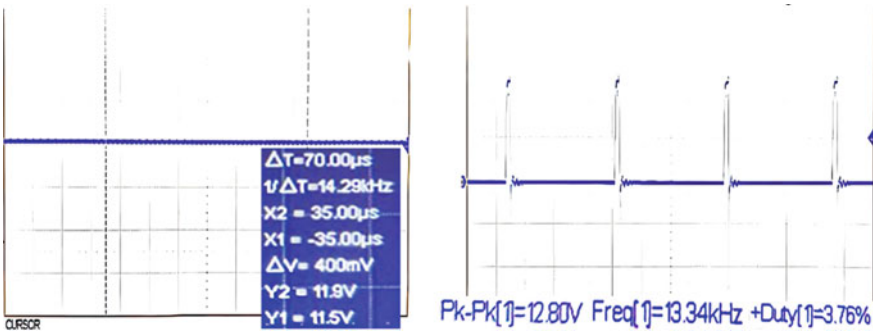

Fig. 11 Input 240 V output 12 V case, no-load output and MOS tube waveform

When the input voltage is raised to 240 V and the output voltage is 12 V no-load, the output remains stable with a switching tube duty cycle of 3.76% and a drive voltage peak-to-peak of 12.80 V, which is consistent with the design.

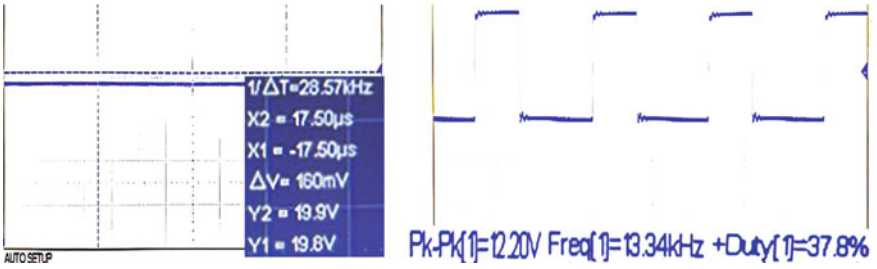

Fig. 12 Input 50 V output 40 W case, the output and MOS tube waveform

Set the input voltage to 50 V, test its 40 W power output, set the output voltage to 20 V, use 10R cement resistor as load, the output and MOS tube waveform as shown in Fig. 12.

At an input voltage of 50 V, output voltage of 20 V, and output power of 40 W, the output is stable, the duty cycle of the switching tube is 37.8%, and the peak-to-peak value of the driving voltage is 12.20 V, which is consistent with the design.

While keeping the output voltage at 20 V, the input voltage was increased to 180 V and the output and MOS tube waveforms were tested as shown in Fig. 13.

When the input voltage is raised to 180 V, the output voltage is 20 V, and the output power is 40 W, the output remains stable, the duty cycle of the switching tube is 10.4%, and the peak-to-peak value of the driving voltage is 13.80 V, which is consistent with the design.

Set the input voltage to 50 V, test its 100 W power output, set the output voltage to 36 V, use 12R cement resistor as load, the output waveform and MOS tube waveform as shown in Fig. 14.

At an input voltage of 50 V, an output voltage of 36 V, and an output power of 100 W, the output remains stable, the duty cycle of the switch is 78.4%, and the peak-to-peak drive voltage is 12.20 V, which is in accordance with the design.

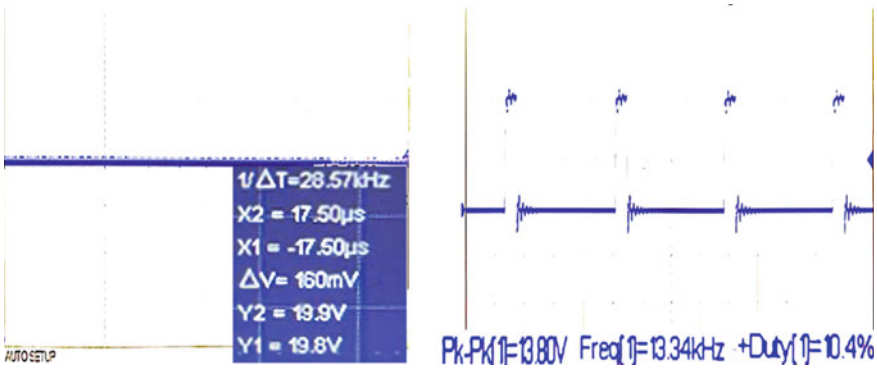

Fig. 13 Input 180 V output 40 W case, the output and MOS tube waveform

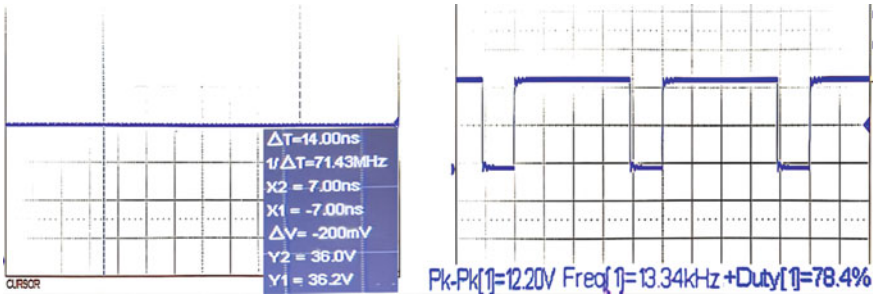

Fig. 14 Input 50 V output 100 W case, the output and MOS tube waveform

Through the test, the output can be stable, and the maximum power can reach 100 W when the input voltage varies in a wide range.

5.2 Conclusion

In this paper, a digitally controlled buck converter is designed by studying the principle of CNC buck converter. The main converter circuit, ADC sampling circuit, and protection circuit are designed by studying the synchronous buck topology. The main control program is designed through the study of digital incremental PID algorithm. Through the experimental demonstration of the real object, the device can realize a wide range of DC 50–240 V input to adapt to various application scenarios with different voltage level requirements and a digitally adjustable output of 12–36 V with a maximum output power of 100 W, which can be applied to the DC output module in the comprehensive training device of power electronics and the power supply device in electrical design.

Later, it can be replaced by components with higher voltage withstand values and more advanced control algorithms to achieve higher levels of accurate voltage conversion, apply it to voltage conversion in new energy electric vehicles, and to meet the need for voltage conversion in large electrical equipment.

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