Active Disturbance Rejection Control of a SEPIC Converter

Priyanshu Kumar and **Moina Ajmeri**

Abstract Single-ended primary inductor converter(SEPIC) is a high-gain buck-boost converter, but its controller's design is a challenging task as it is a fourth-order nonlinear system. This paper proposes an active disturbance rejection control (ADRC)-based controller for a SEPIC converter with high switching frequency. ADRC is an advanced control technique that does not rely on the exact information of the system as all the external and internal disturbances are estimated as separate variables and are canceled directly by the effect of the controller. Simulation results suggest that the proposed ADRC technique gives good setpoint tracking and robustness toward disturbances like input voltage fluctuations and load variations. The performance parameters have been calculated and analyzed to conclude that the proposed method has stable and robust performance.

Keywords DC-DC · SEPIC · PWM · ADRC · ESO

1 Introduction

The extraction of energy from renewable sources like solar and wind requires a DC-to-DC converter. Other applications for DC-to-DC converters are in DC motor drives personal communication equipment and power Computers, etc. [18]. DC-to-DC converters are of three types based on the transformer action, i.e., buck, boost, and buck-boost. Based on the requirement of output voltage with respect to the input, each of the converters has specific uses. Buck-boost converter topologies like cuk converter, zeta converter converters are suited for solar energy generation systems, where the input voltage keeps on fluctuating depending on the intensity of sunlight [5, 14, 23]. However, the low energy conversion efficiency, due to the hard-switched

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states, inverted output, and low voltage gain are the drawbacks of the Cuk and Zeta and some other buck-boost converters [21].

The above-noted problems can be handled by the use of single-ended primary inductor converter (SEPIC) converters [3]. These converters are suitable for off-grid solar power plants due to the possibility of connecting it to the various batteries and PV applications, where they can match the characteristics of current and voltage [3, 10, 22]. SEPIC converter is a fourth-order nonlinear system whose behavior depends on operating conditions like input voltage, duty cycle, and load variations. It requires an advanced control technique to meet goals of guaranteed stability, good set-point tracking, efficient and fast attenuation of the load disturbance and satisfactory robustness toward parametric variations. Various nonlinear control methods such as back-stepping and passivity-based control[2], fuzzy logic-based control [6], sliding mode control [9, 20] have been reported in the literature for controlling SEPIC converters. Sliding mode control is known for better robustness; however, methods proposed in [9, 20] resulted in slow response, and they also failed to reject disturbances of large magnitudes. Authors have designed indirect sliding mode control for the SEPIC using the current mode control in [16]. The output response is satisfactory in the above-cited work however the tuning method looks lengthy and complex. They have not suggested any explicit formulae for calculating the input current reference. It is observed that there is a need for a simple and efficient control strategy for the SEPIC converter as it has a wide range of applications. The two degree of freedom internal model control (TDF-IMC) [15] has been recently reported in the literature for the boost converter. It is a plant model-dependent scheme consisting of three control blocks which are tuned using two design parameters. ADRC control technique is a robust control technique, and it doesn't require the exact knowledge of the system to be controlled [4, 13, 24]. ADRC method draws attention owing to its excellent performance in satisfying the aforementioned control objectives [1]. Up to the best of the authors' knowledge, the ADRC method has not been implemented on the SEPIC converter.

Further, it is important to mention here that larger values of the components such as capacitors and inductors of SEPIC cause significant power losses. At higher switching frequencies, these components' size reduces and also the loading effect of external filter components decreases which results in a faster dynamic response. However, designing a converter at higher frequencies such as in the MHz range limits its operating voltage range as the voltage stresses across the switches and diodes are also increased [11]. Therefore, operational voltage ranges at very high frequencies may not be suitable for power converters applications. Thus, for a wide range of operations, a switching frequency close to a few hundred kHz is commonly used.

In the present work, active disturbance rejection control (ADRC) is proposed for the SEPIC converter with high switching frequency. For the effective application of this controller, the order of the converter is reduced to the second-order system using a balanced reduction technique based on the calculation of the Hankel singular value. The tuning parameter has been decided on the basis of the bandwidth parametrization technique described in [8]. Also, the suitable values of the tuning parameters are selected according to the suitable value of maximum sensitivity. The

designed controller has been verified using simulation results. The controller provides good setpoint tracking and disturbance rejection proving its stability robustness. The robustness of the closed-loop system has been proved on the basis of lower values of settling time, overshoot/undershoot voltage, peak inductor current, and integral square error (IAE).

This paper is divided into seven subsections. Section 2 describes the modeling and design of the SEPIC converter. Section 3 explains the complete design of the ADRC controller for the SEPIC converter. Simulation results are presented in Sect. 4. Finally, the conclusion is derived in Sect. 5.

2 SEPIC Converter

Single-ended primary inductor converter (SEPIC) is a buck-boost converter with noninverted output. It has also the unique property of isolating the input–output circuit when no gating signal is provided to the switch. The circuit diagram of the SEPIC is shown in Fig. 1. It consists of a primary inductor (L_1), a coupling capacitor (C_1), a secondary inductor (L_2), a switch (Q), a diode (D) and an output capacitor (C_2). The circuit works as a boost converter if the duty cycle (D) is greater than 0.5 and as a buck converter if the duty cycle is less than 0.5. The output and inputs are equal when the duty cycle is exactly 0.5. Practically the voltage drops of the diode and MOSFET affect the output voltage. The gate terminal of the switch is provided a pulse width modulated (PWM) generated according to the duty cycle. Hence, the operation of the SEPIC can be divided into two modes as described further.

2.1 Switch on Mode

The circuit diagram resembling this mode is shown in Fig. 2. When the switch is ON, it acts like a short circuit and the diode is reverse-biased. Inductor (L_1) charges through
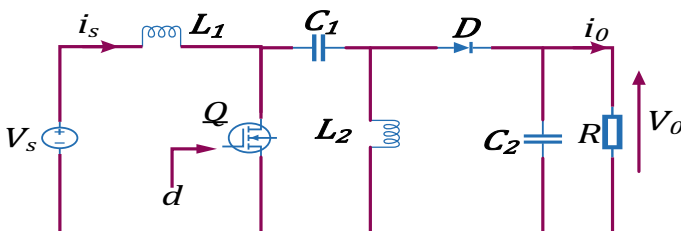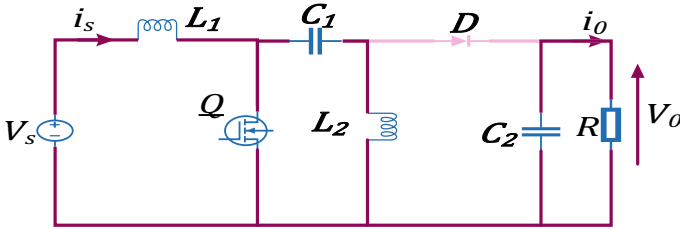

Fig. 1 Schematic diagram of SEPIC converter

Fig. 2 Schematic diagram of SEPIC converter in switch ON mode

the source, while the capacitor supplies the stored energy to the load maintaining the output voltage (V_0) to be constant. Also, the inductor (L_2) is charged by the capacitor (C_1).

The differential equations corresponding to this mode is:

$$\frac{di_{L_1}}{dt} = \frac{v_s}{L_1} \tag{1}$$

$$\frac{di_{L_2}}{dt} = \frac{v_{c_1}}{L_2} \tag{2}$$

$$\frac{dv_{c_1}}{dt} = -\frac{i_{L_2}}{C_1} \tag{3}$$

$$\frac{dv_{c_2}}{dt} = -\frac{v_{c_2}}{C_2 R} \tag{4}$$

The equations in matrix form can be written as:

$$
\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{c_1} \\ \dot{v}_{c_2} \end{bmatrix} =
\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 1/L_2 & 0 \\ 0 & -1/C_1 & 0 & 0 \\ 0 & 0 & 0 & -1/RC_2 \end{bmatrix}
\begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix}
$$

$$
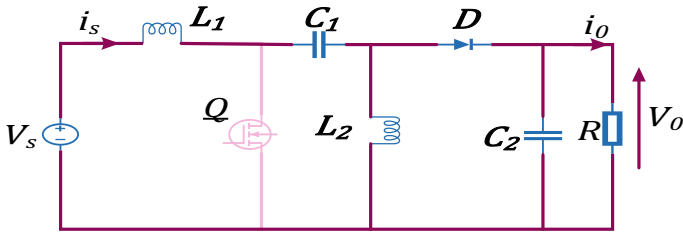+ \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_s] \tag{5}
$$

Fig. 3 Schematic diagram of SEPIC converter in switch OFF mode

2.2 Switch OFF Mode

When the switch is turned off by the means of the PWM signal, then L_1 and L_2 supplies the stored energy toward the load end thereby charging the capacitors C_1 and c_2. The output voltage is still maintained constant when a constant duty ratio is used for the generation of the PWM signals. The circuit diagram defining this mode is shown in Fig. 3.

The differential equations describing this mode are:

$$\frac{di_{L_1}}{dt} = \frac{v_s}{L_1} - \frac{v_{c_1}}{L_1} - \frac{v_{c_2}}{L_1} \tag{6}$$

$$\frac{di_{L_2}}{dt} = \frac{v_{c_2}}{L_2} \tag{7}$$

$$\frac{dv_{c_1}}{dt} = \frac{i_{L_1}}{C_1} \tag{8}$$

$$\frac{dv_{c_2}}{dt} = \frac{(i_{L_1} + i_{L_2})}{C_2} - \frac{v_{c_2}}{C_2 R} \tag{9}$$

These equations can again be written as:

$$\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{c_1} \\ \dot{v}_{c_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1/L_1 & -1/L_1 \\ 0 & 0 & 0 & /-1/L_2 \\ 1/C_1 & 0 & 0 & 0 \\ 1/C_2 & 1/C_2/C_2 & 0 & -1/RC_2 \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix}$$
$$+ \begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_s] \tag{10}$$

The differential equations obtained in ON and OFF modes are combined by multiplying D and $(1 - D)$ respectively using the state-space averaging technique to get the matrices of A, B, C, and D as:

$$A = DA_1 + (1 - D)A_2 \tag{11}$$

$$B = DB_1 + (1 - D)B_2 \tag{12}$$

Now the combined equations in matrix form can be written as:

$$
\begin{bmatrix} \dot{i}_{L_1} \\ \dot{i}_{L_2} \\ \dot{v}_{c_1} \\ \dot{v}_{c_2} \end{bmatrix} =
\begin{bmatrix}
0 & 0 & -D'/L_1 & -D'/L_1 \\
0 & 0 & D/L_2 & -D'/L_2 \\
D'/C_1 & -D/C_1 & 0 & 0 \\
D'/C_2 & D'/C_2 & 0 & -1/RC_2
\end{bmatrix}
$$
$$
\times \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_{c_1} \\ v_{c_2} \end{bmatrix} +
\begin{bmatrix} 1/L_1 \\ 0 \\ 0 \\ 0 \end{bmatrix} [v_s] \tag{13}
$$

where $D' = 1 - D$.

The calculation of the transfer function between the output voltage and duty cycle can be performed by using small signal analysis(SSA). Hence, after performing the SSA, the following state-space equations are obtained:

$$
\begin{bmatrix} \dot{\hat{i}}_{L_1} \\ \dot{\hat{i}}_{L_2} \\ \dot{\hat{v}}_{c_1} \\ \dot{\hat{v}}_{c_2} \end{bmatrix} =
\begin{bmatrix}
0 & 0 & \frac{-D'}{L_1} & \frac{-D'}{L_1} \\
0 & 0 & \frac{D}{L_2} & \frac{-D'}{L_2} \\
\frac{D'}{C_1} & \frac{-D}{C_1} & 0 & 0 \\
\frac{D'}{C_2} & \frac{D'}{C_2} & 0 & \frac{-1}{RC_2}
\end{bmatrix}
\begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{c_1} \\ \hat{v}_{c_2} \end{bmatrix} +
$$
$$
\begin{bmatrix} \frac{(V_{c_1}+V_{c_2})}{L_1} \\ \frac{(V_{c_1}+V_{c_2})}{L_1} \\ \frac{-(I_{L_1}+I_{L_2})}{C_2} \\ \frac{-(I_{L_1}+I_{L_2})}{C_2} \end{bmatrix} [\hat{d}] +
\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} [\hat{v}_s] \tag{14}
$$

and $\hat{v}_0 = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L_1} \\ \hat{i}_{L_2} \\ \hat{v}_{c_1} \\ \hat{v}_{c_2} \end{bmatrix}$

Using the above state-space equations, and neglecting any parasitic resistances, the transfer function is calculated as:

$$\frac{v_0(s)}{d(s)} \approx \frac{\left(1 - s\frac{L_1}{R}\frac{D^2}{D'^2}\right)\left(1 - s\frac{C_1(L_1+L_2)R}{L_1}\frac{D'^2}{D^2} + s^2\frac{L_2C_1}{D}\right)}{D'^2\left(1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{(\omega_{01})^2}\right)\left(1 + \frac{s}{\omega_{02}Q_2} + \frac{s^2}{(\omega_{02})^2}\right)} \quad (15)$$

where

$$\omega_{01} = \frac{1}{\sqrt{L_1\left(C_2\frac{D^2}{D'^2} + C_1\right) + L_2(C_1 + C_2)}} \quad (16)$$

$$\omega_{02} = \sqrt{\frac{1}{L_2\frac{C_1}{D^2} \,\|\, \frac{C_2}{D'^2}} + \frac{1}{L_1C_1\,\|\,C_2}} \quad (17)$$

$$Q_1 = \frac{R}{\omega_{01}\left(L_1\frac{D^2}{D'^2} + L_2\right)} \quad (18)$$

$$Q_2 = \frac{R}{\omega_{02}\,(L_1 + L_2)\,\frac{\omega_{01}^2}{\omega_{02}^2}} \quad (19)$$

The design of the converter is dependent on the frequency of operation at which the switch operates. The higher switching frequency (f_s) allows the selection of reactive components like capacitors and inductors with smaller sizes. In this work, the operating switching frequency of the PWM signal selected is 100 kHz. The selected values of the circuit elements in the present work are listed in Table 1.

Substituting the calculated values for the components in equation (13), the transfer function of the original system is calculated as:

$$G_p(s) = \frac{-980s^3 + 1.9 \times 10^8 s^2 - 6 \times 10^{10}s + 9.6 \times 10^{15}}{s^4 + 20s^3 + 5.3 \times 10^7 s^2 + 1 \times 10^9 s + 3.2 \times 10^{13}} \quad (20)$$

Table 1 Specifications of SEPIC converter

Parameters	Numerical values
Input voltage	48 V
Output voltage	72 V
Duty ratio	0.6
L_1	0.5 mH
L_2	1 mH
C_1	10 μF
C_2	100 μF
Load	100 Ω
f_s	100 KHz

2.3 Reduced Order Model of SEPIC Converter

Being a fourth-order nonminimum phase system, the application of some of the advanced controlling techniques on SEPIC converter leads to complex equations and sluggish response. Hence, a need for the reduction of the order of the system arises. In this work, ADRC control method has been proposed for the converter. The controller design based on the fourth-order system induces greater phase lag that deteriorates the performance of the controller in the case of the transients. To overcome the above-said difficulties and to apply the ADRC method, this converter is reduced to a second-order system. The order of the system is reduced on the basis of a balanced reduction method on the calculations of Hankel singular values. Firstly, a balanced reduction of the system is done to isolate the states whose contribution to the input–output response is negligible[17]. After the reduction of the system, Hankel singular values are calculated which has N small entries. A scientist named Hermann Hankel designed a method to obtain Hankel singular values based on the controllability Gramian, and the observability Gramian[19]. Actually, Hankel singular values provide a measure of energy for each state in a system. Hankel singular values are calculated as the square roots, of the eigenvalues. They are the basis for balanced model reduction, in which high-energy states are retained while low-energy states are discarded. The second-order reduced transfer function is obtained as:

$$G_{\mathrm{pr}}(s) = \frac{299.9s^2 + 146.5\,s + 1.56 \times 10^{10}}{s^2 + 0.009676\,s + 5.203 \times 10^7} \tag{21}$$

The reduced model retains the important features of the original model as its bode plot resembles the original system. The bode plot for these two systems is shown in Fig. 4.
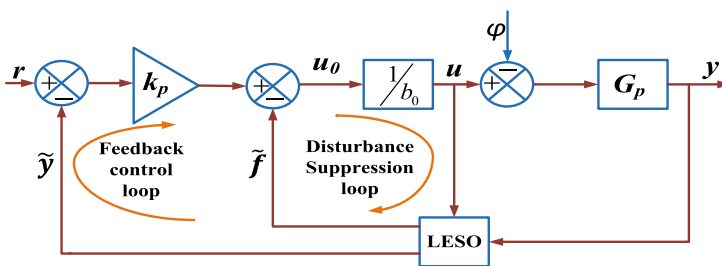

Fig. 4 Schematic block diagram of an ADRC controller

3 Design of ADRC Controller for SEPIC Converter

In the ADRC method, the disturbances whether known or unknown are initially clubbed together in a single variable and further they are estimated in a certain way with the help of an observer. The estimated disturbance is then suppressed with the action of the controller. The block diagram depicting the structure of the ADRC controller is shown by Fig. 4. b_o is defined as the gain of the system, u is considered as the control input and the system's output is denoted by y. Also, k_p is the controller's gain, $\tilde{y}$ is the estimated output, $\tilde{f}$ is the estimated value of disturbance and φ is the external disturbance. The SEPIC converter's reduced order transfer function model is characterized by Eq. (21). By taking the inverse Laplace transform of this transfer function, we get the dynamics of the SEPIC converter in the time domain in the form of a differential equation that relates the output with the input using the following relation:

$$\ddot{y} = (-a_0 y - a_1 \dot{y} + \delta b_o u - b_1 \dot{u} + \delta b_o u + \delta(t)) + b_o u = f(y, \dot{y}, u, \dot{u}, w, \delta) + b_o u \tag{22}$$

where $f(y, \dot{y}, u, \dot{u}, w, \delta)$ has been considered as a generalized form of disturbance comprising of all the internal a well as the external disturbances. Since the system has been reduced to second order hence by the application of basic rules of ADRC method, a third-order observer is designed. The first two states in the observer are formed using the system dynamics while the third state in particular represents the cumulative disturbance. The estimated third state from the observer is canceled by the proper selection of the controller.

Let $x_0 = y$, $x_1 = \dot{y}$, $x_2 = h(.)$, and $\dot{x}_2 = m$ where $h(.)$ is differentiable and m is bounded. Using these assumptions, the state-space model for the system can be derived as:

$$\dot{x}(t) = Ax(t) + Bu(t) + Hm \tag{23}$$
$$y = Cx(t)$$

where

$$\dot{x}(t) = \begin{bmatrix} \dot{x}_0(t) \\ \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix}, A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix}, B = \begin{bmatrix} 0 \\ b_0 \\ 0 \end{bmatrix}, C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \text{ and } H = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}$$

The above state-space model can be used to design an ESO for the system given by:

$$\dot{z} = Az + Bu + L(y - \hat{y}), \tag{24}$$
$$\hat{y} = Cz$$

where $z(t) = \begin{bmatrix} z_0 & z_1 & z_2 \end{bmatrix}^T$ is the estimated states and $L = \begin{bmatrix} \beta_0 & \beta_1 & \beta_2 \end{bmatrix}^T$ is the gain of the observer. A PD controller of the following form is considered:

$$u_0(t) = k_1(r - z_1) - k_2 z_2 \tag{25}$$

The third state of the observer is rejected by the final control law given by:

$$u(t) = \frac{u_0(t) - z_3}{b_o} \tag{26}$$

where $k_p = \begin{bmatrix} k_1 & k_2 & 1 \end{bmatrix}$ is the controller's gain.

The previous works in [7, 12] have proposed some techniques for the selection of bandwidths of the observer (ω_0) and controller (ω_c). The characteristics equation of the controller is compared with the second-order equation tuned in the form of the controller's bandwidth(ω_c) that configures the controller's gain as:

$$\lambda(s) = s^2 + k_1 s + k_2 = (s + \omega_c)^2 \tag{27}$$

From this, the controller's bandwidth is calculated as:
$k_1 = 2\omega_c, k_2 = \omega_c^2$

Similarly, the characteristics equation of the observer is compared with the third-order equation tuned in the form of the observer's bandwidth(ω_0).

$$\psi(s) = s^3 + \beta_0 s^2 + \beta_1 s + \beta_2 = (s + \omega_0)^3 \tag{28}$$

From this equation observer's bandwidth is calculated as:
$\beta_0 = 3\omega_0$, $\beta_1 = 3\omega_0^2$ and $\beta_2 = \omega_0^3$.

The values of ω_c and ω_0 are selected as 900 rad/sec and 12600 rad/sec respectively based on the calculation of maximum sensitivity as 1.4.

4   Simulation Results

The circuit for the converter along with the controller was designed in the MAT-LAB/Simulink environment. The simulation results have been plotted for all three possible cases, i.e., for variation in set point voltage, variation in input voltage, and variation in load resistances. The performance parameters consisting of settling time, overshoot/undershoot, peak inductor current, and integral square error (IAE) has been calculated in each of these cases and listed in Table 2.

4.1   Servo Performance

In this case, the reference tracking capability of the controller is studied. Figures 5 and 6 depict the output voltages, the inductor currents, and the load currents obtained through simulation in boost and buck modes respectively. For the boost mode of operation, the input voltage is fixed to 30 V, while the load resistance is set to 100 Ω. At the time $t = 0.2$ s, the reference is step changed from 48 to 60 V, and again

Table 2 Performance parameters of the proposed method

Types of disturbances	T_s	Overshoot (V)	I_{L_1} (A)	I_{L_2} (A)	IAE
Servo performance (boost mode)	0.01	0	2.6	1.9	0.0402
Input voltage variation (boost-buck mode)	0.02	4	6	4	0.0287
Load variation (boost mode)	0.01	0.2	1.2	0.7	0.0003
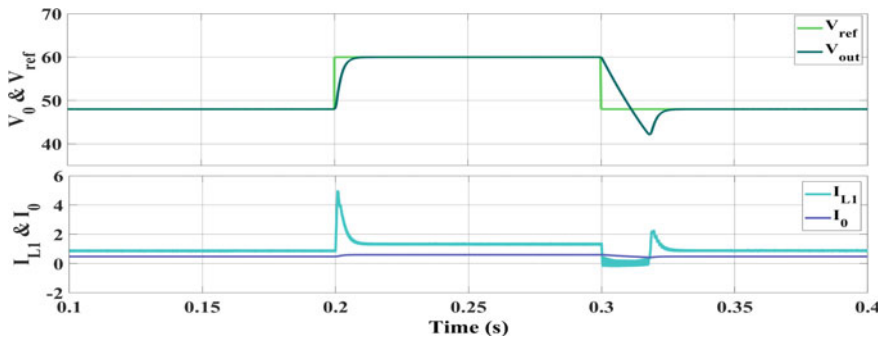
Fig. 5 Responses for change in reference in boost mode
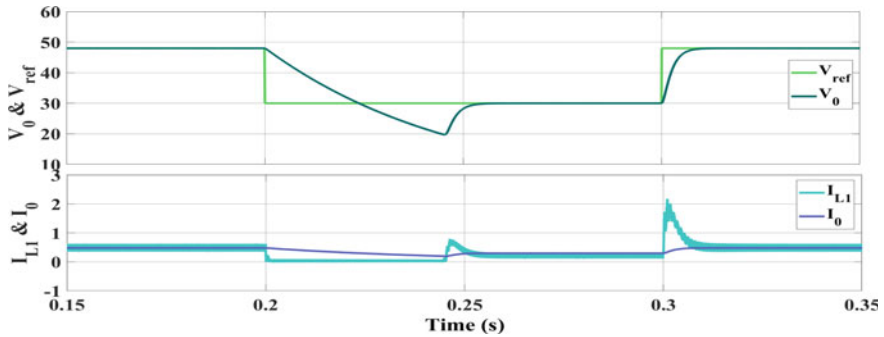
Fig. 6 Responses for change in reference in buck mode

back to 48 V at time $t = 0.3$ s. In the buck mode, the input voltage is set to 60 V, and at time $t = 0.2$ s, the reference voltage is decreased from 48 to 30 V and again to 48 V at time $t = 0.3$ s. The performance parameters have been listed in Table 2. From this, it is observed that the settling time is around 0.01 s when the reference is increased, while the curve settles at around 0.03 s when the reference is decreased.
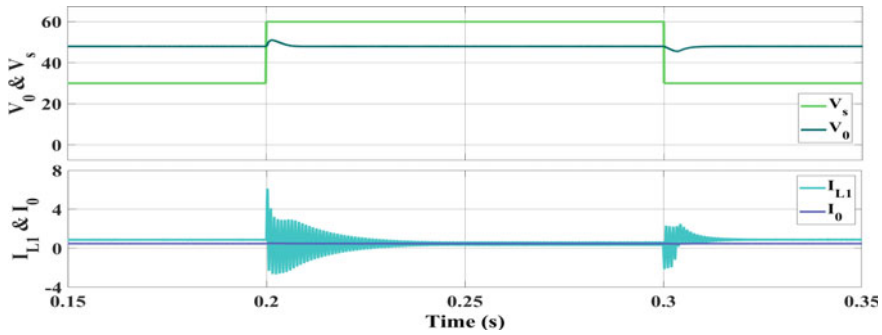
Fig. 7 Responses for change in input voltage

4.2 Regulatory Performance for Variation in Input Voltage

In this case, the effect of varying input was studied by keeping the load resistance and reference voltage fixed to 100 Ω and 48 V respectively. Firstly, the input voltage was changed from 30 to 60 V (boost-buck mode) at time $t = 0.2$ s, and again from 60 to 30 V (buck-boost mode) at time $t = 0.3$ s, keeping the reference constant at 48 V. Figure 7 shows the simulation results under the assumed conditions. Also, the performance parameters are listed in Table 2. It is observed that the output voltage remains settled at 60V with very little overshoot/undershoot at the input voltage transition phase thereby proving a faster disturbance rejection capability.

4.3 Regulatory Performance for Variation in Load Resistance

Here the reference voltage was set to 48 V for observing the effect of varying load. In the buck mode of operation, the input voltage was adjusted to 60 V and the load resistance was varied from 100 to 50 Ω at time $t = 0.1$ s and then back to 100 Ω at time $t = 0.15$ s. For analyzing the boost mode of operation, the input voltage was fixed to 30 V, and at time $t = 0.1$ s, load resistance was varied from 100 Ω to 50 Ω and back to 100 Ω at time $t = 0.15$ s. The corresponding responses are shown in Figs. 8 and 9, and the performance parameters are listed in Table 2. It can be analyzed that a small overshoot/undershoot of around 0.2 V is present. Also, the settling time of around 0.005 s was seen. The load voltage remains settled at the reference voltage, while the load current and primary inductor current changed instantly due to the change in the load as the power demand increased/decreased with increasing/decreasing load resistance.
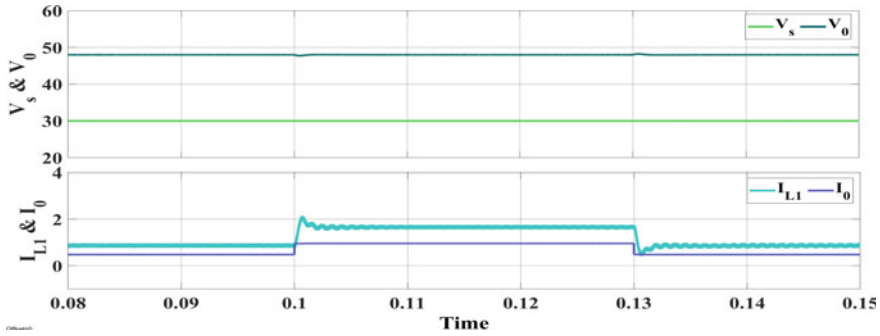
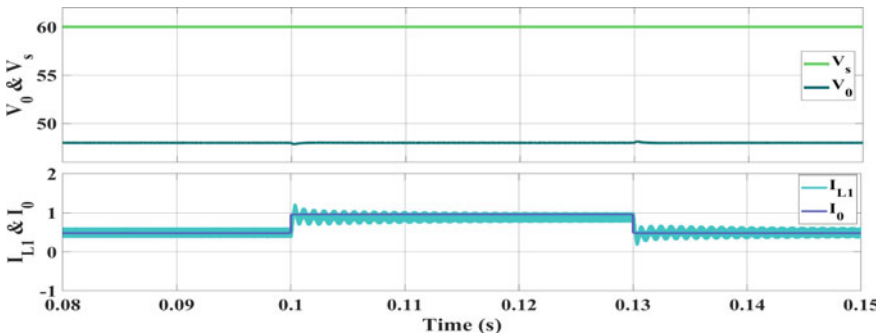**Fig. 8** Responses for change in load resistance in boost mode

Fig. 9 Responses for change in load resistance in buck mode

5 Conclusion

In the present work, active disturbance rejection control (ADRC) is proposed for the SEPIC converter with high switching frequency. Higher switching frequency has allowed the selection of components with lower sizes. An ADRC-based control structure has been proposed for this converter which is derived based on the reduced order model of the SEPIC converter obtained through a balanced reduction technique. The suggested ADRC method results in outstanding performance and satisfactory robustness toward varying input voltages and loading conditions. This SEPIC converter along with suggested ADRC control may be used to achieve constant DC voltage from renewable energy sources like solar PV panels and windmill in varying environmental conditions.

References

1. Ahmad S, Ali A (2019) Active disturbance rejection control of dc-dc boost converter: a review with modifications for improved performance. IET Power Electron 12(8):2095–2107
2. Chennoufi K, Ferfra M, Mokhlis M (2021) Design and implementation of efficient mppt controllers based on sdm and ddm using backstepping control and sepic converter. In: 2021 9th international renewable and sustainable energy conference (IRSEC). IEEE, pp 1–8
3. Chiang S, Shieh HJ, Chen MC (2008) Modeling and control of pv charger system with sepic converter. IEEE Trans Ind Electron 56(11):4344–4353
4. Chu Z, Wu C, Sepehri N (2019) Active disturbance rejection control applied to high-order systems with parametric uncertainties. Int J Cont Automat Syst 17(6):1483–1493
5. Dahale S, Das A, Pindoriya NM, Rajendran S (2017) An overview of dc-dc converter topologies and controls in dc microgrid. In: 2017 7th international conference on power systems (ICPS). IEEE, pp 410–415
6. El Khateb A, Abd Rahim N, Selvaraj J, Uddin MN (2014) Fuzzy-logic-controller-based sepic converter for maximum power point tracking. IEEE Trans Ind Appl 50(4):2349–2358
7. Fu C, Tan W (2021) Analysis and tuning of reduced-order active disturbance rejection control. J Frankl Inst 358(1):339–362
8. Gao Z et al (2003) Scaling and bandwidth-parameterization based controller tuning. In: ACC, pp 4989–4996
9. Gireesh G, Seema P (2015) High frequency sepic converter with pwm integral sliding mode control. In: 2015 International conference on technological advancements in power and energy (TAP Energy). IEEE, pp 393–397
10. Gopi RR, Sreejith S (2018) Converter topologies in photovoltaic applications-a review. Renew Sust Energy Rev 94:1–14
11. Guan Y, Wang Y, Wang W, Xu D (2017) A high-frequency clcl converter based on leakage inductance and variable width winding planar magnetics. IEEE Trans Ind Electron 65(1):280–290
12. He T, Wu Z, Li D, Wang J (2019) A tuning method of active disturbance rejection control for a class of high-order processes. IEEE Trans Ind Electron 67(4):3191–3201
13. Herbst G (2013) A simulative study on active disturbance rejection control (adrc) as a control tool for practitioners. Electronics 2(3):246–279
14. Hwu K, Peng T (2011) A novel buck-boost converter combining ky and buck converters. IEEE Trans Power Electron 27(5):2236–2241
15. Kobaku T, Patwardhan SC, Agarwal V (2017) Experimental evaluation of internal model control scheme on a dc-dc boost converter exhibiting nonminimum phase behavior. IEEE Trans Power Electron 32(11):8880–8891
16. Komurcugil H, Biricik S, Guler N (2019) Indirect sliding mode control for dc-dc sepic converters. IEEE Trans Ind Inf 16(6):4099–4108
17. Laub A, Heath M, Paige C, Ward R (1987) Computation of system balancing transformations and other applications of simultaneous diagonalization algorithms. IEEE Trans Autom Cont 32(2):115–122
18. Luo FL, Ye H (2016) Advanced dc/dc converters. CRC Press
19. Moore B (1981) Principal component analysis in linear systems: controllability, observability, and model reduction. IEEE Trans Autom Cont 26(1):17–32
20. Sel A, Güneş U, Kasnakoğlu C (2020) Design of output feedback sliding mode controller for sepic converter for robustness. Int J Electron 107(2):239–249
21. Smedley KM, Cuk S (1995) Dynamics of one-cycle controlled cuk converters. IEEE Trans Power Electron 10(6):634–639
22. Yao C, Ruan X, Wang X, Chi KT (2011) Isolated buck-boost dc/dc converters suitable for wide input-voltage range. IEEE Trans Power Electron 26(9):2599–2613
23. Zhao Q, Lee FC (2003) High-efficiency, high step-up dc-dc converters. IEEE Trans Power Electron 18(1):65–73
24. Zhou R, Fu C, Tan W (2020) Implementation of linear controllers via active disturbance rejection control structure. IEEE Trans Ind Electron 68(7):6217–6226