

A Comprehensive Review to Investigate the Effect of Read Port Topology on the Performance of Different 7 T SRAM Cells



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Abstract SRAM-based cache memory is an important component for microprocessor-based circuit. The growing demand for portable devices with prolonged battery life has driven designers to report SRAM bit cells with varying topologies. The 7T cell is one of the most popular bit cell topologies. As a consequence, five different 7T cells with a common internal memory core configuration and different read port topologies are reviewed in this paper. The technology node for each cell is 32 nm, while the supply voltage is 0.8 V. The cell topologies are analyzed for static noise margin and time requirement for each operation. It is identified that the 7T4 and 7T5 cells have best read stability at 314 and 324 mV, respectively. In terms of read time requirement, the 7T4 and 7T5 cells are identified to be the best at 5 ps each.

Keywords Read port · SRAM · High integration density · Improved stability · Single port · Dual port

1 Introduction

The increasing popularity of hyper-personalized devices has led to the advent of a world governed by artificial intelligence and applications of Internet of things. The hardware elements essential for implementation of these applications are dependent on cache memories that are fast, have low area footprint, and consume minimal power. Microprocessor memory is composed of static random access memory (SRAM) cells, which occupy 90% of its surface area and consequently dominate the power appetite of the device (Divya and Mittal 2022; Rawat and Mittal 2022a). Thus, it is critical to keep cell area and power in check. The area occupied by an SRAM bit cell can be limited to a smaller value if less transistors are used in designing, whereas, to limit

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power consumption by a bit cell, lowering supply voltage (V_{DD}) is the prevalent and conventional technique. The active power for a cell has a quadratic relation with V_{DD} . Therefore, a small reduction in V_{DD} has a large impact on its active power (Ahlawat et al. 2021). But, decreasing V_{DD} to near-threshold or subthreshold region has severe implications on cell performance (Bharti and Mittal 2021; Calhoun et al. 2005). Also, at lower V_{DD} , the circuit yield decreases due to the greater influence of variation in the threshold voltage (V_{TH}) (Oh et al. 2021). This is an implication of minimally sized transistors to ensure high integration density. A conventional mechanism to uplift the bit cell performance at lower V_{DD} is to increase the bit cell count for the circuit. Consequently, different architectures such as 8T (Giterman et al. 2018; Kushwah and Vishvakarma 2016), 9T (Cho et al. 2020; Shin et al. 2017), 10T (Jiang et al. 2019; Wen et al. 2019) have been reported by designers across the globe. A major challenge for SRAM cells with high transistor count is their lower integration density; as the transistor count for cell increases, its on-chip area also increases. SRAM is formed by an array of bit cells. Thus, a minimal increase in the layout footprint for a cell has drastic impact on the overall area of cache, thus threatening the memory's economic feasibility and commerciality. Consequently, it is essential to design a cell with the capability to demonstrate robust performance at lower V_{DD} and high integration density. Reduction in technology node has been a major contributor to density increment. But, at lower technology node, the conventional single port 6T cell is unable to perform reliably, so the 7T cell has become the next conventional alternative. In this paper, different 7T SRAM cells are reviewed for different performance parameters. This paper is categorized into five sections, including this introduction section. In Sect. 2, the 7T topologies pre-existing in literature, are elaborated upon and their working mechanisms are explained. The cell performance in terms of static margin analysis, time requirement, and their impact on different SRAM topologies is detailed in Sects. 3 and 4, respectively. The results obtained for the different cells are summarized in Sect. 5.

2 Pre-existing 7 T Bit Cell Topologies

Different 7T cell topologies reported in literature are reviewed in this section. The different 7T cells have common memory core design, while they are differentiated based on the read port configuration. The data core for each cell comprises of an inverter pair (P1-N1 and P2-N2). The inverter pair is mutually connected via a positive feedback connection dependent on transistor N3. It is controlled by signal W1, which is used to disable the feedback between the inverter pair. This converts the mutually coupled inverter configuration into a cascaded configuration. Additional to the aforementioned memory core, each cell consists of a read and write port to aid the respective operation. The latter operation for all the cells is single ended and requires the internal core of the memory to be converted into a cascaded inverter configuration. Thus, during write operation, the W1 signal is turned OFF. The nature and mechanism for read operation for each cell are explained individually.

The first 7T cell (7T1) described in the paper was reported by Aly and Bayoumi (Aly and Bayoumi 2007) in 2007. Its write operation is designed to be single ended and the read operation is differential ended. Thus, only bitline (BL) signal is used to perform write operation, whereas both BL and bitline bar (BLB) are employed for read. Its prime highlight is its ability to reduce power dissipation. The schematic for 7T1 is represented in Fig. 1a. Its single ended write topology reduces its activity factor to half (Rawat et al. 2018), thereby resulting in a major power reduction during write mode of the cell. During the read operation, both WL and RL signals are asserted and the cell is accessed via transistors N4 and N5. But, the extra N3 transistor in the read path for the cell introduces an asymmetry in its design causing a lower read stability. Also, the read power consumption is high due to its differential nature.

A second 7T cell (7T2) was described by Rawat and Mittal (Rawat and Mittal 2021a). The transistor-level representation for 7T2 cell is depicted in Fig. 1b. This cell reduces read power consumption by relying only on a single bitline. Thus, this cell has low power appetite for both access (read-write) operations. Its data node lies in the discharge current path for the read operation, making it highly vulnerable to noise. Also, as there are two NMOS transistors N1 and N5 in the read path, the time required to execute the read operation will be high. Thus, this cell suffers due to its noise vulnerability and greater delay for the read operation.

Another cell (7T3) designed by Yang et al. (2016) in 2016 attempts to resolve the challenges encountered by the 7T1 cell. The circuit schematic of 7T3 is presented in Fig. 1c. Its structure is similar to 7T1 with the exception of the N5 transistor. In 7T1 cell, the N5 transistor is used to form the differential read port for the cell whereas for

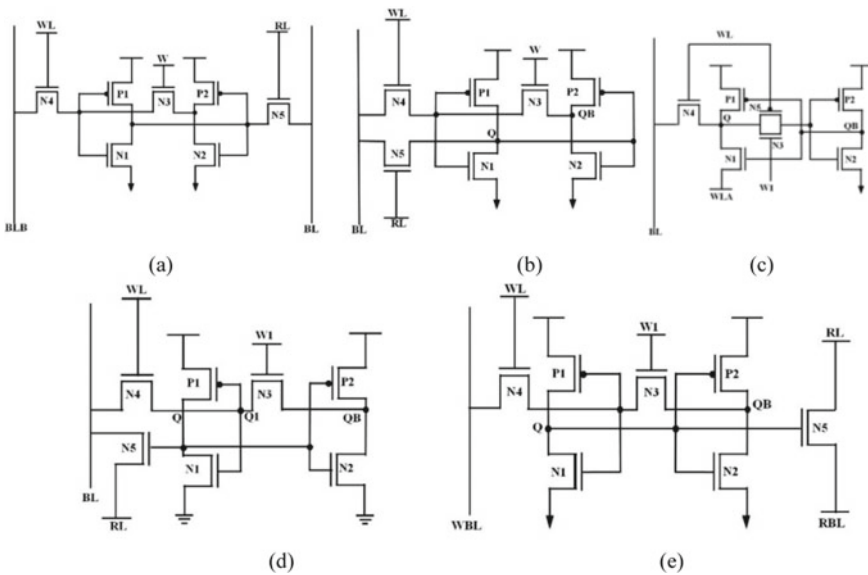


Fig. 1 Schematic diagram for a 7T1, b 7T2, c 7T3, d 7T4, and e 7T5 SRAM bit cells

7T3 cell, it is used to create a transmission gate parallel to N3 transistor. Also, unlike 7T1 and 7T2 cells, the N5 transistor here is of PMOS type. Another modification that is added to the cell topology is the use of additional control signal WLA at the source of the N1 transistor. Due to its single port topology and single ended configuration for operation, it observes a significant reduction in dynamic power consumption. But, the increase in control signal count increases the circuit complexity, decreases its integration density and also increases the peripheral circuitry required for the memory. Thus, the improvement in power consumption for the cell gets overshadowed by the other challenges.

A modification to mend the read noise stability for a cell was reported in Rawat and Mittal (2021b). This 7T (7T4) SRAM cell modifies the read port configuration for 7T2 to make it read SNM free. The transistor-level representation of 7T4 cell is shown in Fig. 1d. An SRAM cell that does not include data node in the read discharge current path is referred to as the read SNM free (Singh et al. 2013). The read port for 7T4 is functional only when $Q = '1'$. The read discharge current passes from BL to RL via N5 transistor, thereby maintaining the integrity of data stored at the node. This cell thus has better power performance along with improved read stability.

Another 7T cell (7T5) with read SNM-free topology is reported in Rawat and Mittal (2022b). This cell differs from the 7T4 cell in terms of its dual-port configuration. This cell isolates the read and write ports, thereby facilitating pipelining for the memory architecture. The transistor-level representation for the 7T5 is shown in Fig. 1e. The single ended nature for the read as well as write operations of the cell facilitates power reduction. The read SNM-free port topology boosts its read stability, and isolated read port for the cell makes its operation faster and pipelining enabled.

3 Static Margin Analysis

A cell irrespective of its topology has to work reliably under three different operational modes—hold, read, and write. A reliable cell should be able to perform each of these operations and withstand noise due to internal or external factors. The resilience of a cell toward noise is estimated in terms of static noise margin (SNM). It is the maximum noise fluctuation that a cell can withstand without resulting in an erroneous data flip for the cell (Kulkarni et al. 2007). It is measured as the side of the largest square that fits inside the smaller lobe of the butterfly curve (Kumar et al. 2014). It is measured individually for hold, read, and write operations in terms of HSNM, RSNM, and WSNM, respectively.

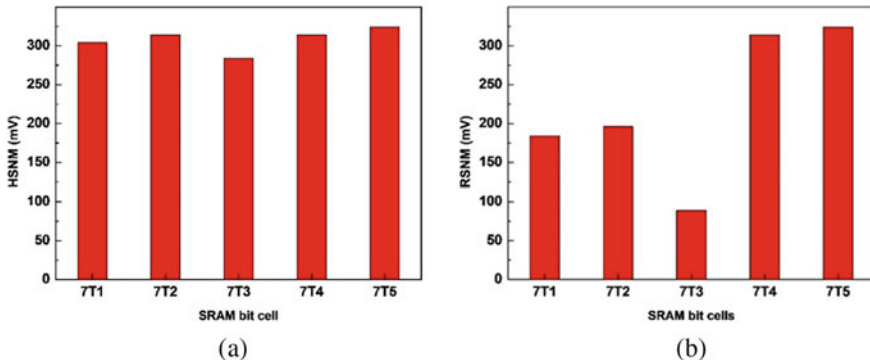


Fig. 2 a Hold and b read SNM values obtained for the different 7 T cells

3.1 HSNM

A cache memory is designed using a large array of cells, but at a given instant only a few cells are accessed. Therefore, an SRAM cell is usually maintained in hold state. Consequently, a cell is required to have high resilience to noise during hold state. The HSNM value obtained for all the 7T cell topologies explained in Sect. 2 is graphically compared in Fig. 2a. Maximum HSNM value is registered for the 7T5 SRAM bit cell at 324 mV. The 7T2 and 7T4 cells have slightly lower values at 314 mV each. They are followed by 7T1 cell which registers an HSNM of 304 mV, whereas the least SNM value for hold operation is recorded for the 7T3 cell at 284 mV.

3.2 RSNM

The read is an access operation for a cell. A crucial aspect of the read operation is maintaining the integrity of the information stored in the cell is to be maintained during the operation. This is largely dependent on the cell's read port configuration. If the read discharge current passes through the data storage nodes, the likeliness for a destructive read operation is high, whereas, if the discharge current path does not include the data node, the likelihood for a destructive read operation is eliminated. Cells that have such a read port configuration are called SNM-free read port. Among the different cells explained in Sect. 2, the only cells with read SNM-free port configuration are 7T4 and 7T5. In these cells, the read current flows through the N5 transistor controlled by node Q.

Therefore, read current will flow only for $Q = '1'$; for $Q = '0'$, no read current is registered by the cell. As the 7T4 and 7T5 cells are read SNM free, their HSNM and RSNM values are identical. The other cells—7T1, 7T2, and 7T3 register an RSNM value of 184, 196, and 89 mV, respectively. The RSNM values obtained for the 7T cells are represented in Fig. 2b.

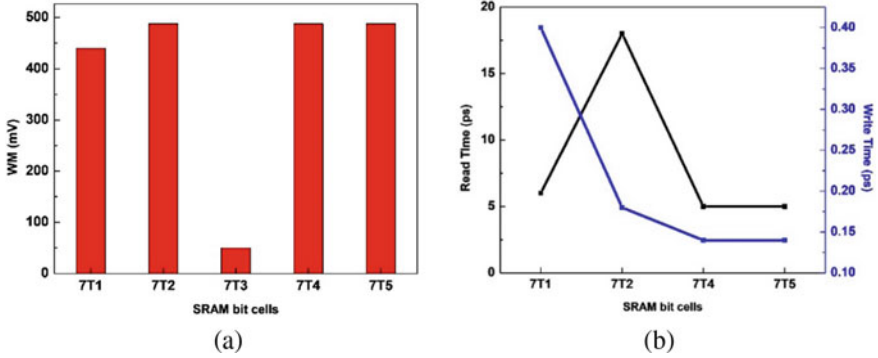


Fig. 3 a WSNM and b read and write time values obtained for different 7T cells

3.3 WSNM

Another access operation that a cell performs is the write operation. During its course, the information retained inside the cell is to be deliberately flipped. A cell's resilience to noise during the write operation is quantified as WSNM. It is calculated as the voltage difference between the wordline and the V_{DD} (Chaturvedi et al. 2021). The WSNM values obtained for all the cells are compared in Fig. 3a. As the write mechanism for all the bit cells is the same, similar values are obtained for all the cells.

4 Delay

During the SNM analysis, each operation for a cell is analyzed irrespective of the time required to complete the operation. But, in real-life application, an SRAM memory is a part of a microprocessor circuit. Consequently, the circuit is driven in keeping with the clock pulse for the setup. Therefore, when designing an SRAM memory, it is crucial to analyze the delay requirement for an individual bit cell. The two access operations (read and write) for a cell are time dependent. Therefore, each cell in the paper is analyzed for both read and write time in the following subsections.

4.1 Read Time

Timing constraint is crucial for the read operation as a longer time pulse may threaten a destructive read operation, whereas an extremely short pulse may result in an insufficient discharge resulting in erroneous read operation. Thus, for an optimal read operation, the read pulse has to be highly optimized. If the read cell topology is

of differential nature, the read time is the time needed to develop a 50 mV differential voltage on the bitline pair, whereas, for a single ended operation, it is the time required to reach the trip voltage for the inverter (Lin et al. 2010). The read time for the different bit cells is depicted in Fig. 3b. The fastest read operation for the 7T4 and 7T5 SRAM cells is at 5 ps each. These two cells have a single ended read SNM-free topology and therefore are faster than their other counterparts. The 7T1 SRAM bit cell also has a similar read time value of 6 ps. It has a differential read operation and therefore performs better than 7T2 cell which relies on a single ended pass transistor configuration for read operation. The timing analysis is not included for the 7T3 cell as it has a two-step process while the other cells have a single step process.

4.2 Write Time

The write operation implies that the data in the cell has to be altered. It is usually the most time-consuming process for a cell. Therefore, an SRAM cell is deemed more reliable and robust if it completes its write operation in least amount of time possible. Consequently, write time is defined as the least time needed to successfully change the values stored in the cell. The write time values recorded for all the 7T cell explained in Sect. 2 are presented in Fig. 3b. The 7T1 cell requires the largest delay for write operation completion of 0.4 ps. This is because the 7T1 cell uses all typical NMOS transistors for inverter implementation, and the cascaded inverter configuration thus makes it slow. But the 7T2, 7T4 and 7T5 SRAM bit cell have modified their inverter core to include a high-performance NMOS transistor to boost the operational speed for the circuit. Therefore, the three cells 7T2, 7T4, and 7T5 are comparatively faster than the 7T1 cell with write delay of only 0.18, 0.14, and 0.14 ps, respectively.

5 Conclusion

In this paper, five different 7T cell topologies are reviewed, and their results are presented. The 7T cells are designed for technology node of 32 nm and simulated at 0.8 V. The 7T cells pre-dominantly differ in implementation of their read port. Thus, the impact of different read port configurations on cell performance is analyzed. Each cell is evaluated for its resilience to noise during the three operations (hold, read, and write) in terms of the static noise margin. The 7T5 cell is most noise resilient during the read operation with RSNM value of 324 mV. Another cell with a slightly lower value for RSNM is 7T4 cell at 314 mV. These two cells also register the least read time requirement of 5 ps. The same is achieved due to the single ended read SNM-free topology of the read port for the bit cells.

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