# Chapter 19
# Design of Low Power 11T SRAM Cell Using CNTFET Technology


**Anitu Atri, Vikram Singh, and Tabassum Khurshid**

**Abstract** With the miniaturization of CMOS technology, the conventional CMOS-based SRAM is facing several challenges, such as increased power consumption, decreased stability, and limited scalability. Carbon nanotube field-effect transistors (CNTFETs) have emerged as a promising alternative to CMOS technology due to their excellent electrical properties, including high electron mobility, low leakage current, and high mechanical strength. This paper presents a low power 11T SRAM cell using CNTFET. The proposed 11T SRAM cell is designed using P-CNTFET as header switch and an N-CNTFET as a footer with separate read circuit and is stimulated using H-Spice tool using 32 nm CNTFET Stanford model. The proposed SRAM cell is operated with the supply voltage of 0.9 V to improve read noise margin of 0.246 V and improved read delay of 0.01627 ns with a write delay of 0.0645 ns. A state of art comparison with existing with CNTFET-based 6T, 7T, 8T and 11T SRAM cells is also presented.

## 19.1 Introduction

Static random access memory (SRAM) is a type of volatile memory that is commonly used in microprocessors, digital signal processors, and other integrated circuits. It is a high-speed memory that uses flip-flops to store data and is often used for cache memory due to its fast read and writes times [1]. Multiple SRAM cells combined together to create larger memory structures that are capable of storing a larger amount of data. The need for faster and energy-efficient electronic devices has resulted in a reduction in the size of transistors in CMOS technology to less than 10 nm. However, this decrease in size has brought about several challenges, such as increased leakage current and reduced reliability, mainly due to the effects of quantum tunneling. To overcome these challenges, researchers have explored the use of CNTFETs as a

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potential replacement for conventional CMOS transistors. CNTFETs have demonstrated superior performance in terms of speed, power consumption, and noise immunity, making them a promising alternative for future electronic devices [2]. The advancement in nanotechnology has led to the development of SRAM cells using CNTFETs [3].

In last few years, researchers have been conducting studies on SRAM cells based on CNTFETs with a focus on enhancing their stability, scalability, and reliability. Some studies have suggested innovative circuit designs for CNTFET-based SRAM cells, while others have examined the use of various fabrication methods and materials to improve their performance [4]. Some commonly used SRAM cell designs include 6T, 7T, 8T, 9T, 10T, and 11T cell, where T stands here for number of transistors used. The total number of transistors used affects the performance and other characteristics of SRAM cell which includes power consumption, read and write speed, and stability. The choice of SRAM cell type hinges on the particular specifications of the device or system that is being developed, given that each type of SRAM cell has advantages and drawbacks of their own [5]. Overall, CNTFET-based SRAM cells have the potential to provide significant improvements in performance and power consumption, making them an alternative option for future memory technologies [6].

## 19.2 Brief Review of CNTFET Technology

CNTFETs have been identified as a potential solution to the limitations of complementary metal–oxide–semiconductor field-effect transistors (CMOSFETs), which have been the cornerstone technology for digital integrated circuits for many years. The ongoing scaling of CMOSFETs has resulted in issues such as power consumption and leakage current, which pose significant challenges. The superior electrical properties of CNTFETs, such as high carrier mobility, low sub threshold swing, and excellent electrostatic control, make them a promising alternative. CNTFETs use carbon nanotubes, which are cylindrical structures made of Graphene sheets as shown in Fig. 19.1, with diameters of a few nanometers, as the channel material in transistors as shown in Fig. 19.2. By utilizing CNTs, it is possible to develop more energy-efficient and high-performance electronic devices that can overcome the limitations of traditional CMOS technology [7].

The chirality of CNTs also plays a crucial role in their properties. Armchair CNTs exhibit metallic behavior, while zigzag CNTs are semiconducting as shown in Fig. 1b. The type of chirality chosen for CNTFETs used in SRAM design can significantly impact the device's performance. For example, zigzag CNTFETs have shown to have better on–off current ratios compared to armchair CNTFETs, leading to better SRAM performance [9]. Therefore, the diameter and chirality of CNTs are critical factors that need to be considered in the design of CNTFETs for SRAM applications. The optimal choice of diameter and chirality can result in better device performance, leading to improved SRAM functionality [7] and can be expressed as

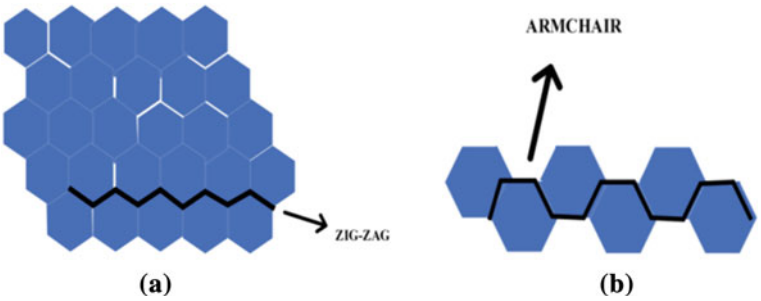
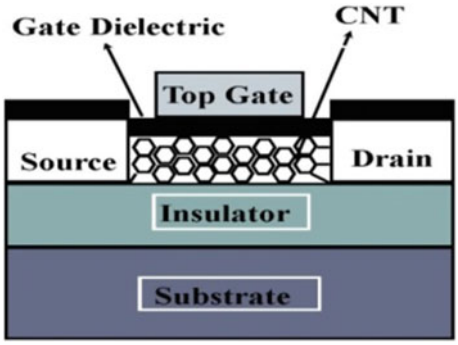



**Fig. 19.1** Graphene sheet **a** Zig-Zag **b** Armchair [9]

**Fig. 19.2** Structure of CNTFET [7]




$$\text{Channel length (L)} = a\sqrt{m^2 + mn + n^2} \tag{19.1}$$

$$\text{Diameter of CNT } (D_{cnt}) = L/\pi \tag{19.2}$$

$$\text{Threshold voltage}(V_{th}) = \frac{a\,V\pi}{\sqrt{3}.q.Dcnt} \tag{19.3}$$

where 'q' is the electron charge, $V\pi = 3.033$ eV , CNT atomic distance (a) = 2.49 Å.

CNTFET sizing can be adjusted by modifying the number of carbon nanotubes used in the channel and to achieve the desired threshold voltage and current drive capability. By increasing the number of tubes, the channel width can be increased, which in turn increases the current carrying capacity of the device. This approach allows for greater flexibility in designing CNTFET-based circuits and can optimize their performance for specific applications.

## 19.3 Related Literature

In recent years, CNTFETs have emerged as a promising technology for developing SRAM cells with superior performance compared to traditional CMOS technology. Several studies have investigated the performance of SRAM cells utilizing CNTFETs, aiming to improve their efficiency and effectiveness. One study proposed a modified 6T structure for a CNTFET-based SRAM cell, which showed its improved write ability, read stability, and read access time when compared with the conventional 6T SRAM cells [10]. Another study proposed an asymmetric CNTFET-based SRAM cell that achieved improvement in write margin and read stability when compared with the symmetric CNTFET-based SRAM cells [11].

A hybrid SRAM cell was also proposed that utilized both CNTFETs and conventional CMOS technology, showing improved read and write performance compared to traditional CMOS-based SRAM cells [12]. Additionally, a dual-Vt CNTFET-based SRAM cell was proposed, which indicates the upgraded write-ability and read-stability when compared with the conventional CNTFET-based SRAM cells [13]. Other studies have focused on design optimizations to improve the performance of CNFET SRAM cells, such as the usage of lightly doped drain/source regions and the optimization of gate length and width [14].

Comparative analyses of different SRAM cells using traditional MOSFET and CNTFET technology have been carried out. The simulation results show that the CNTFET-based SRAM cell has better performance in terms of read signal noise margin (RSNM), write signal noise margin (WSNM), read delay (RD) and write delay (WD), while the MOSFET-based SRAM cell has better performance in terms of RD and WD. Overall, CNTFET-based SRAM cells are a promising candidate for future memory applications due to their superior performance compared to traditional MOSFET-based SRAM cells [15–17].

Furthermore, studies have investigated the impact of various CNTFET parameters such as channel length, channel diameter, and gate oxide thickness on the performance of CNTFET SRAM cells [18–24]. The Table 19.1 shows the technology road map and their advantages. Table 19.1 is illustrating the technology path for transitioning from traditional transistors to carbon nanotube field-effect transistors (CNTFETs), in addition to their benefits and drawbacks.

Therefore, CNTFET-based SRAM cells have demonstrated superior performance compared to traditional CMOS technology, making them a promising candidate for future memory applications.

## 19.4 Proposed 11T SRAM Cell Using CNTFET

A single bit of data can be stored in a memory cell known as a 6T SRAM cell, which is composed of six transistors organized in a certain pattern. The basic operation of a 6T SRAM cell involves using two interconnected inverters, each consisting of

**Table 19.1** Comparison of CNTFET technology with other technologies

| Tech | Advancements | Advantages | Limitations |
|---|---|---|---|
| CMOS | Carried on with reduction of attributes, decreased consumption of power, and enhanced performance | Continued characteristic like decrease utilization of power along with the performance enhancement | Physical barriers hinder scalability, increasing problems with manufacturing at decreased size of features |
| Hybrid Technology | Bringing together the conventional CMOS with CNTs to boost efficiency and reduce consumption of power | Enhanced functionality and decreased power consumption particularly when compared with standard CMOS technology | Concerns with dependability and stability, as well as difficulties with material integration and production |
| CNTFETs | In comparison with CMOS technology, using CNTs improves performance, consumes less power, and produces a lesser impact on the environment | Lowered power requirements, faster switching, increased device density, enhanced low-temperature performance, and reduced vulnerability to radiation-induced malfunctions | High fabrication costs, difficulties in achieving uniformity in device performance, and challenges with material integration and manufacturing |

two transistors (a P-CNFET and an N-CNFET transistor) [7, 23]. The remaining two transistors serve as access transistors, which are used to control read and write operations as shown in Fig. 19.3.

The 6T SRAM works under three mode write, read and hold. In hold operation, the word line is switched off and the pass transistor enters an off state during the hold operation. The latch then safeguards the previous value all throughout this time frame. The write operation begins by setting the bit-lines to the desired values of either 0 or 1, and the word-line is activated to select the corresponding cell. This results in the voltage on one of the access transistors being higher than the voltage

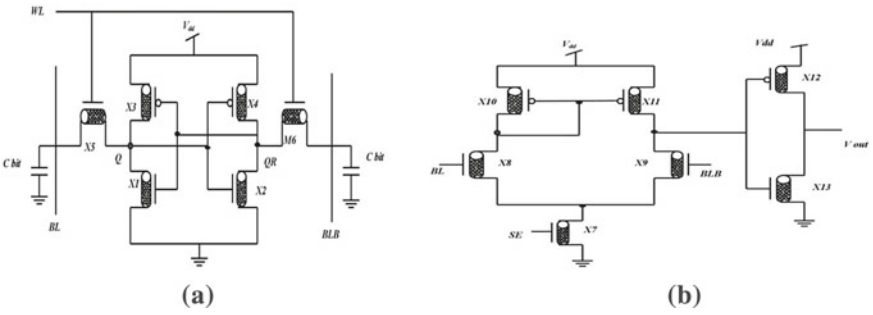



**Fig. 19.3** 6T SRAM using CNTFET; **b** Sense Amplifier [7]

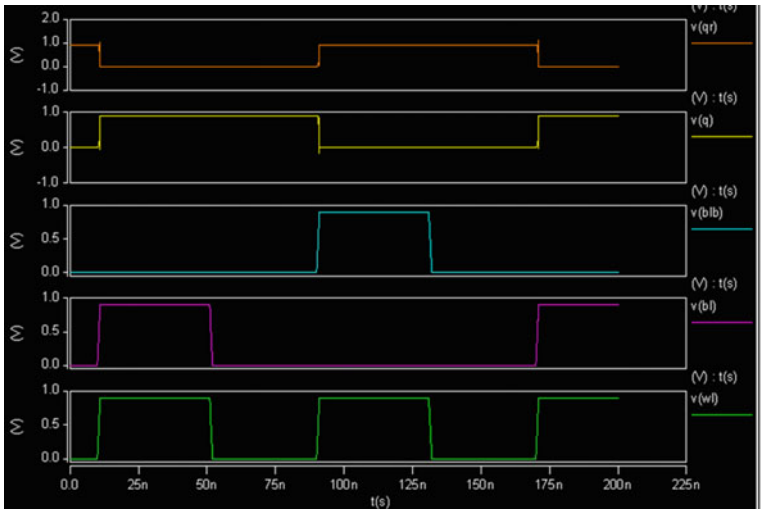



**Fig. 19.4** Write operation in CNTFET based 6T SRAM

on the other access transistor. As a result, the higher voltage transistor enters the ON state, while the other remains in the OFF state. This allows for the transfer of data from the bit-lines to the storage nodes as shown in Fig. 19.4. During the read operation, the word-line is again activated, and the voltages on the bit-lines are compared. If the voltages on the bit-lines match the stored data in the cell, no operation is performed. However, if the voltages on the bit-lines do not match, the sense amplifier is activated to amplify the voltage difference and update the cell with the correct value shown in Fig. 19.5.

When a single P-CNFET or N-CNFET is added as a header switch between the latch and supply in a 6T SRAM cell using CNFETs, it can have a significant impact on the behavior and properties of the cell. A P-CNFET can be used as a switch to connect the supply voltage to the internal storage node during write operations, resulting in faster and more effective writing to the cell. However, this can also increase the write power consumption due to the additional switching activity. Alternatively, an N-CNFET can be utilized as a switch to connect the internal storage node to ground during the read operation, which can enhance read stability and reduce the read disturb issue. Moreover, the elimination of precharge circuitry with a header N-CNFET can reduce the read power consumption of the cell.

The addition of a P-CNFET or N-CNFET can improve write operation or read stability, respectively, compared to a 6T SRAM cell using only CNFETs as shown Fig. 19.6. However, it can also increase the complexity and size of the SRAM cell, which can be problematic in some cases. Furthermore, adding any additional FETs to the SRAM cell can increase the risk of leakage current and other reliability issues. The decision to add a P-CNFET or N-CNFET to a 6T SRAM cell using CNFETs depends on the specific application requirements. If the goal is to improve write operation, a

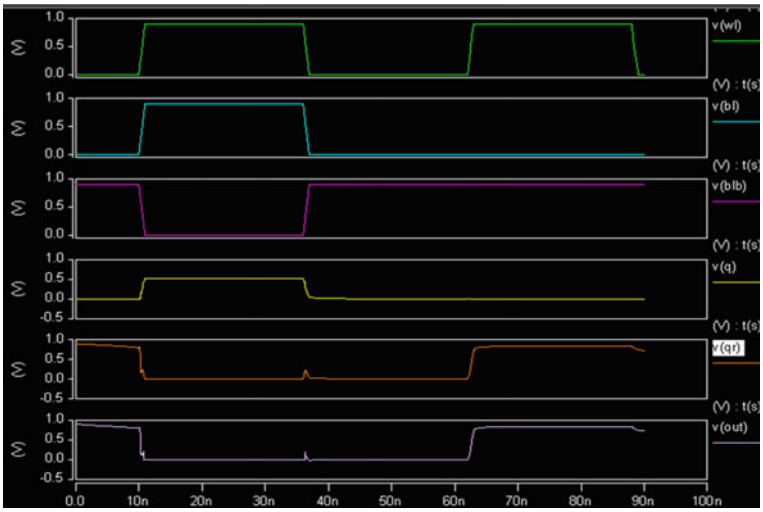



**Fig. 19.5** Read operation in CNTFET based 6T SRAM

P-CNFET can be added. Likewise, if the focus is on read stability enhancement, an N-CNFET can be added. However, careful evaluation of the trade-offs and potential reliability issues are necessary for each application. Adding P-CNFET or N-CNFET between supply and latch of a 6T SRAM cell that uses CNFETs can have a significant impact on the cell's behavior and characteristics.

Reduced write power consumption can be achieved by using the P-CNFET footer as a switch for separating the internal storage node from ground during write operations. However, this may compromise the cell's write margin and reliability. Alternatively, N-CNFET footer can be used to connect the internal storage node to ground during read operations; thereby increasing read margin and reducing the read disturb issue. However, the additional switching activity may lead to an increase in read power consumption [20].

While adding footer P-CNFET or N-CNFET can improve power consumption and operation stability, it may also increase cell complexity and size, and result in leakage current and reliability issues. Choosing to add footer P-CNFET or N-CNFET depends on the specific application requirements. If reducing write power consumption is essential, a P-CNFET can be added, while an N-CNFET can be added to improve read stability. However, careful consideration of the trade-offs and potential reliability concerns are necessary for each application.

When header and footer transistors are added to a 6T SRAM using CNTFET, it becomes an 8T SRAM, which improves the stability of the cell during read and write operations. This improvement is due to reduced voltage swings, better write margin, and lower leakage. However, the use of additional transistors results in increased area, power consumption, and access time, which may not be desirable for some applications. The choice between 6 and 8T SRAM using CNTFET depends on the

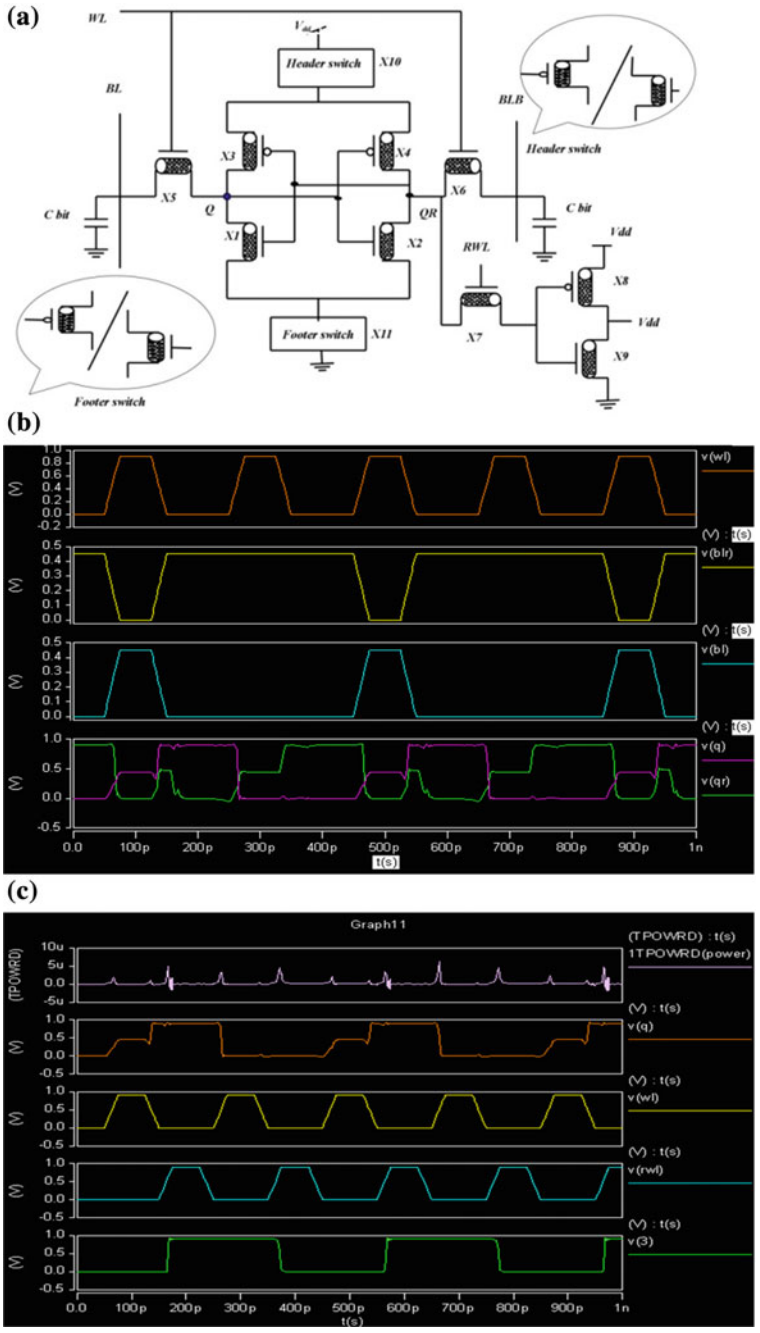



**Fig. 19.6** **a** 11T CNTFET based SRAM; **b** Write operation simulation output; **c** Read operation simulation output

specific requirements of the application, such as density, power consumption, and access time [17].

In proposed SRAM cell a P-CNFET in header while an N-CNFET in footer is used, this will increase the read stability, read delay along with write delay. The 11T SRAM cell has advantages compared to a 6T SRAM cell. The header and footer transistors in the 11T SRAM cell decrease leakage current and improve the cell's stability. Moreover, a separate read circuit allows for efficient read operations without affecting write operations as shown in Fig. 19.6. Nonetheless, the more complex 11T SRAM cell has higher power consumption and larger area requirements compared to the simpler 6T SRAM cell. Ultimately, the choice between using an 11T or 6T SRAM cell using CNTFETs depends on specific design needs, performance requirements, power usage, and area trade-offs. The 11T SRAM cell has benefits like improved stability and reduced read disturb errors, but with the cost of increased complexity and overhead.

## 19.5 Results and Discussion

The proposed 11T SRAM designed and simulated with H-Spice tool at 32 nm technology node with supply voltage of 0.9 V and with the help of CosmoScope software waveforms for the proposed circuit are shown in Fig. 19.6 and 19.7.

It has been observed that CMOS-based 6T SRAM cell offers the lowest read and writes delay times, with values of 1.22 and 2.7 ns, respectively. It also has the lowest write noise margin of 0.07V and hold noise margin of 0.127 V. The CNFET-based 6T SRAM cells offers the lowest read and write delay times among all the CNFET-based SRAM cells, with values of 0.00472 and 0.00721 ns, respectively. It also has the highest read noise margin of 0.17 V and hold noise margin of 0.35 V. The CNFET-based 6T SRAM cell, which contains one footer and one header with a

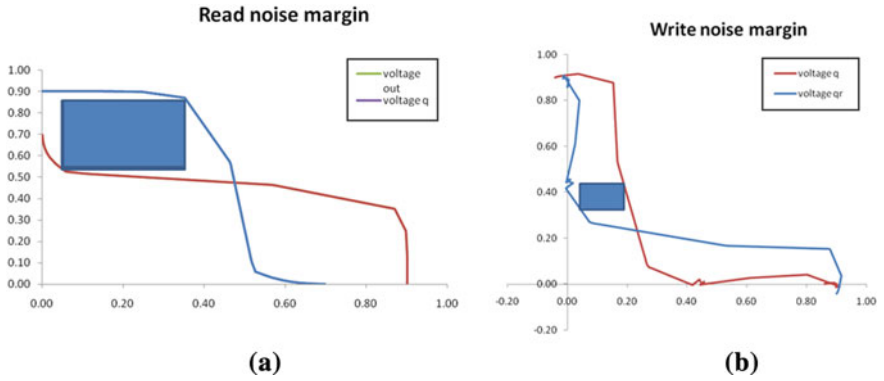



**Fig. 19.7** **a** Read noise margin; **b** Write noise margin

**Table 19.2** Comparison of the proposed 11T CNTFET based SRAM with existing literature

| SRAM Type | RD (ns) | WD (ns) | RNM (V) | WNM (V) | HNM (V) | $V_{DD}$ (V) | Tech (nm) | Ref |
|---|---|---|---|---|---|---|---|---|
| CMOS 6 T | 1.22 | 2.7 | 0.012 | 0.07 | 0.127 | 0.9 | 32 | [7] |
| CNTFET-6 T | 0.00472 | 0.00721 | 0.17 | 0.18 | 0.35 | 0.9 | 32 | [7] |
| CNTFET-6 T | 0.156 | 0.0699 | 0.1473 | 0.143 | 0.140 | 0.33 | 32 | [23] |
| CNTFET-8 T | 0.119 | 6.11 | 0.1564 | 0.156 | 0.130 | 0.3 | 32 | [17] |
| CNTFET-11 T | 3.27 | 6.11 | 0.1562 | 0.1563 | 0.156 | 0.3 | 32 | [25] |
| CNTFET-11 T | 0.01627 | 0.0645 | 0.246 | 0.12 | - | 0.9 | 32 | **This Work** |

separate read circuit, provides the best read delay and noise margin performance. It offers a read delay of 0.156 ns and a read noise margin of 0.1473 V. However, it has the highest write delay of 0.0699 ns and a lower write noise margin and hold noise margin compared to other CNFET-based SRAM cells. The CNFET-based 8T and 11T SRAM cells have higher read and write delays than the 6T SRAM cells, with values ranging from 0.119 to 3.27 ns. However, they offer similar write noise margins and hold noise margins compared to the CNFET-6T SRAM cell. Our proposed model that is 11T SRAM gives us the better stability in read noise margin. In addition to read noise margin of the proposed circuit also improves in term of read and write delay which are presented in Table 19.2.

Therefore, the CMOS-based 6T SRAM cell offers the best read and writes delay performance among all the SRAM cells listed. However, the CNFET-based 6T SRAM cell offers better noise margins. The CNFET-based 6T SRAM cell containing one footer and one header with a separate read circuit provides the best read performance but worse write performance compared to other CNFET-based SRAM cells.

## 19.6 Conclusion

CNTFET based SRAM cell gave better device characteristics from traditional CMOS based SRAM cell. In traditional CMOS there are no separate read circuits but in the proposed 11T SRAM designed using CNTFET have separate read circuit which reduces the leakage current and improve read noise margin because of its high mobility and low leakage property. 11T SRAM CELL Based on CNTFET (6T SRAM cell contains one footer and one header with a separate read circuit). This type of 11T SRAM cell uses a separate read circuit to improve read delay, write delay and enhance stability and provides the highest level of performance and reliability. Hence the proposed 11T SRAM using CNTFET achieved the desired results in terms of reduced read delay and also write delay and improves the read noise margin for which the desired results are shown above when compared with the traditional 6T CMOS based SRAM.

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