An Implementation of Differential Difference Voltage Difference Transconductance Amplifier (DD-VDTA) and Its Application as a Dual Output Integrator

Prerna Rana and Ashish Ranjan

1 Introduction

In recent time, a wide variety of active elements with different characteristics is enriched in the scientific literature based on fundamental active block [1]. These designs are based on the modification of the basic elements like Voltage Feedback Amplifier (VFA) [2], Current Feedback Amplifier (CFA) [3], Operational Transconductance Amplifier (OTA) [4], and Current-Conveyors (CC) [5] which fulfils the modern circuit design speciality like low power consumption, high slew rate, few more [6, 7]. A very popular active element "VDTA" [8] exhibits a simple design approach for the generation of integrators, bi-quad filters, oscillator, inductance, and frequency dependent negative resistor (FDNR) simulator using a single active block with a few passive elements. This design can be compared to the active elements like second generation Current Conveyor (CC-II) [9], third generation Current Conveyor (CC-III) [10], Differential Difference Current Conveyor (DDCC) [11], Differential Voltage Current Conveyor (DVCC) [12], Current Differencing Buffered Amplifier (CDBA) [13], second generation Dual X Current Conveyor (DXCC-II) [14], and offers a better results in comparison to the [9–14]. In addition to this, this VDTA can also be used for transconductance mode applications as its input ports is voltage and output is current. Moreover, integrator design [15–18] and Wave Active Filter (WAF) [19–21] are also available. By keeping in line of the features of VDTA, the authors have made an attempt to design an advance version of VDTA with addition differential difference property and collectively called as "DD-VDTA". This research paper contributes a design for DD-VDTA which enables an extra features of differential

P. Rana (✉) · A. Ranjan
Department of Electronics and Communication, National Institute of Technology, Manipur 795004, India
e-mail: ranaprerna135@gmail.com

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difference property and owes all the good characteristics of VDTA block with its circuit description in Sect. 2. The proposed DD-VDTA design is translated for the active integrator for lossy, lossy subtraction and lossless in Sect. 3. The workability test of DD-VDTA is examined in both DC and AC conditions in Sect. 4. In addition, simulation results of integrator are also verified and ends with a comparative table. Moreover, this proposed block can be used to synthesize integrators having two outputs, i.e. inverting and non-inverting output through the same design and to design WAF with lower number of active and passive elements.

2 Circuit Description of DD-VDTA

The proposed new active element DD-VDTA is a combination of DDA [22] and VDTA [23] which offers the features of DDCC and an OTA in a single circuit design. The CMOS structure of DD-VDTA is shown in Fig. 1.

The characteristics equation of DD-VDTA can be characterized as:

$$I_z = g_{m1}\left(V_p - V_n\right), \tag{1}$$

$$I_{xn} = -g_{m2}V_z, \tag{2}$$

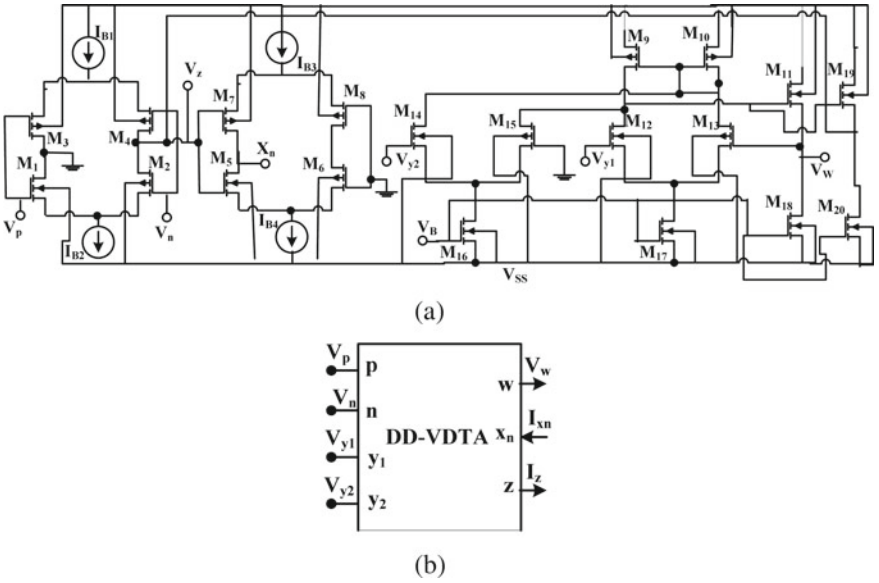

Fig. 1 DD-VDTA **a** CMOS structure **b** block diagram

$$I_w = I_z, \tag{3}$$

$$V_w = V_{y1} - V_{y2}, \tag{4}$$

First stage consists of VDTA having transistors M_1 to M_8, where the output and input stages are made up of floating current sources. It has two input (V_p, V_n) and two output (V_z, I_{xn}) ports of high impedances. Equation 1, indicates the difference of the input voltages of ports p and n with transconductance gain g_{m1} which produces current at port z. The voltage drop at port z with transconductance parameter (g_{m2}) is transformed into output current at port x_n. The first stage of the proposed DD-VDTA block comprises two Arbel–Goldminz transconductance-based OTAs [23] and their transconductance (g_{m1} and g_{m2}) can be mathematically obtained as:

$$g_{m1} = \frac{g_3 + g_4}{2}, \tag{5}$$

$$g_{m1} = \frac{g_7 + g_8}{2}, \tag{6}$$

$$g_i = \sqrt{I_{bi}\mu_i C_{ox}\frac{W_i}{L_i}} \tag{7}$$

where g_i can be defined as the transconductance value of the ith transistor as a function of MOSFET fundamental electrical parameters (μ_i, C_{ox}, W/L) and bias current (I_{bi}). Second stage is DDA that consists of transistors M_9 to M_{20}. It consists of two high impedance input port (Y_1, Y_2) and one low impedance output port (V_w). There are two differential stages (M_{14}, M_{15}) and (M_{12}, M_{13}) with a PMOS (p-type metal oxide semiconductor) current mirror employing M_9 and M_{10}. This current mirror converts the differential current to output voltage (V_w) at the drain terminal of M_{11}. This part gives the difference of input voltages present at ports y_1 and y_2 through the output port z. The transistors M_{19} and M_{20} makes a current mirror pair in which the current flowing through w port and z port are same (Eq. 3). The block diagram of DD-VDTA is given in Fig. 1b.

3 Applications of DD-VDTA

The proposed DD-VDTA is useful for the design of lossy integrator, lossy integration subtraction, and lossless integrator circuit as shown in Fig. 2a–c, respectively. The property of DD-VDTA block supports the differential difference of two voltage inputs with characteristics of a VDTA circuit. Hence, it can be easily used to synthesize integrators with two outputs, i.e. inverting and non-inverting output through the same design. These designs are purely resistor-less and require only one passive capacitor.

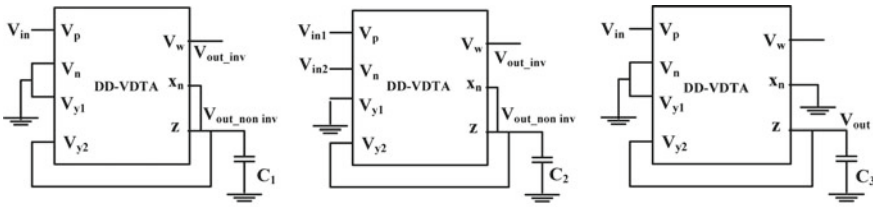

Fig. 2 Integrator designs using DD-VDTA **a** lossy integrator **b** lossy subtraction integrator **c** lossless ntegrator

For lossy integrator circuit, the ports, V_{y2}, z, and x_n are shorted to each other and a grounded capacitor is connected across it. In this circuit, input is given at only one port (V_{p}). The inverted and non-inverted outputs are taken from w and z ports respectively and it yields;

$$v_z = \frac{v_{\mathrm{p}}}{1 + sC/g_m} \tag{8}$$

and,

$$v_{\mathrm{w}} = -\frac{v_{\mathrm{p}}}{1 + sC/g_m} \tag{9}$$

For lossy subtraction integration circuit, the circuit design is similar to the lossy integrator circuit. The only difference is inputs at both the ports V_{p} and $\underline{V}_{\mathrm{n}}$ and the output is differential difference integration output as:

$$v_z = \frac{v_p - v_n}{1 + sC/g_m} \tag{10}$$

and,

$$v_{\mathrm{w}} = -\frac{v_{\mathrm{p}} - v_n}{1 + sC/g_m} \tag{11}$$

For lossless integrator, V_{y2} and z port are shorted together and a grounded capacitor is connected across it. The input is given at port V_{p} and output is taken from V_{z}. It results the following voltage expression for V_{z} and V_{w} respectively as:

$$v_{\mathrm{z}} = \frac{v_{\mathrm{p}}}{sC/g_m} \tag{12}$$

and,

$$v_{\mathrm{w}} = -\frac{v_{\mathrm{p}}}{sC/g_m} \tag{13}$$

4 Simulation Results

To check the working behaviour of DD-VDTA, the CMOS structure of DD-VDTA is simulated in the PSPICE simulator using 0.18 μm technology parameter. The aspect ratios of the transistors are given in Table 1 with supply voltages ± 0.9 V and the bias current (I_{b1}, I_{b2}, $I_{\mathrm{b3,}}$ and $\mathrm{I_{b4}}$ are chosen 150 μA). The transconductance values of g_{m1} and g_{m2} are 627 μA/V.

The DC characteristic of the proposed DD-VDTA is shown in Fig. 3. To plot $\left(I_z = g_{m1}\left(V_{\mathrm{p}} - V_n\right)\right)$, a resistor is connected across the z port and the respective voltages of ports p, n, and z are plotted in Fig. 3a and b. In similar manner Eq. 2 is also plotted and given in Fig. 4c. Equation 3, is represented in Fig. 4d by giving an input current at port z. and in the similar way Eq. 4 is shown in Fig. 4e and f, which are simply plotted by giving an input voltage at y_1 and y_2 port.

In addition to DC characteristics, the AC transfer characteristic of DD-VDTA is also observed in Fig. 4. The frequency response of transconductance gain g_m from port z to v_{p}, from port z to v_n, and from z to v_x is given in Fig. 4a–c respectively followed by V_{y1}/V_w and V_{y2}/V_w is shown in Fig. 4d and e, respectively. The points X and Y in the graphs shows the parasitic gain and the bandwidth of the block.

The performance parameters and their numerical value of the proposed block DD-VDTA is also well observed in Table 2.

Finally, the simulated output of the proposed integrator circuits Fig. 2a–c is shown in Fig. 5a–c, respectively. The capacitor values taken for lossy integrator simulation C_1, C_2 is 250 nF and for lossless integrator simulation C_3 is 180 nF. For the lossy integrator circuit, one square shape input of 200 mV amplitude is applied at the input port and an integrated triangular shape output of 200 mV amplitude is obtained. On the other side, lossy subtractor integrator, uses two square signals of amplitude 300 and 200 mV at two input ports (V_{p} and V_n) which results subtraction integration output of 1 mV output is at V_{w} and V_{z} ports.

Table 1 Aspect ratios (W/L) for DD-VDTA

S. no.	MOSFETs	W/L (in μm)
1	M_1, M_2, M_5, M_6	3.6/0.36
2	M_3, M_4, M_7, M_8	16.64/0.36
3	$M_9, M_{10}, M_{11}, M_{19}$	3.6/0.18
4	$M_{12}, M_{13}, M_{14}, M_{15}$	0.72/1.08
5	$M_{16}, M_{17}, M_{18}, M_{20}$	2.16/1.08

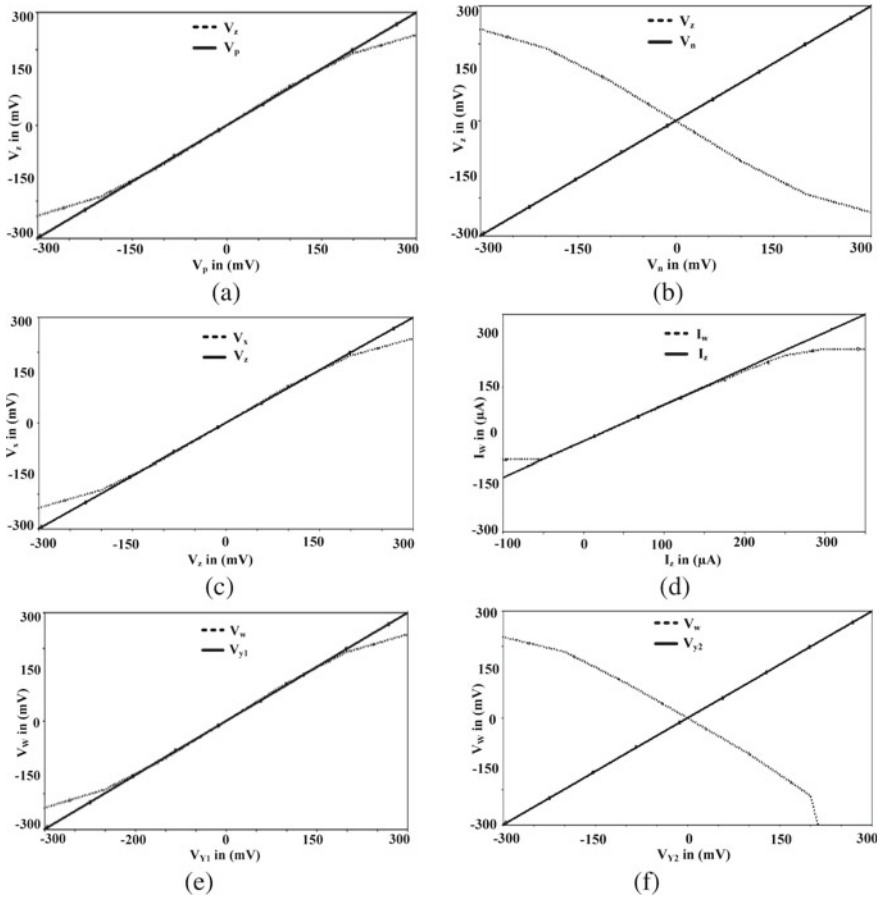

Fig. 3 DC voltage variation behaviour of DD-VDTA at different port **a** voltage z to p **b** voltage z to n **c** voltage x to z **d** current w to z **e** voltage w to y_1 **f** voltage w to y_2

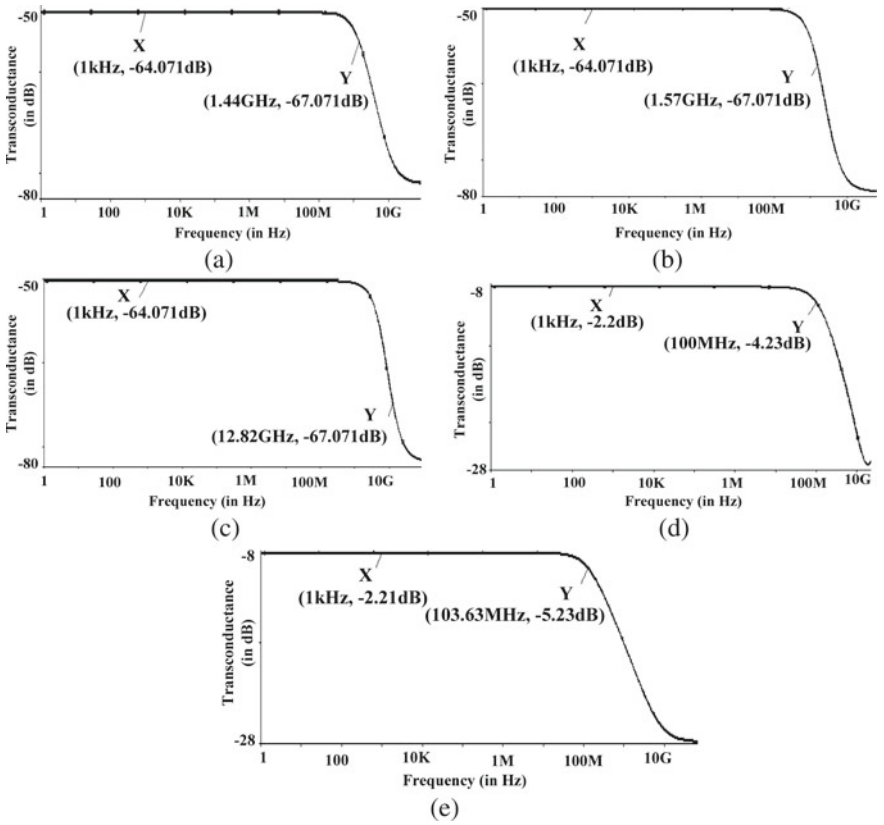

Fig. 4 AC characteristics of DD-VDTA **a** frequency response of g_m from port z to v_p **b** frequency response of g_m from port z to v_n **c** frequency response of g_m from z to v_x **d** frequency response of V_{y1}/V_w **e** frequency response of V_{y2}/V_w

Table 2 Performance parameters of DD-VDTA

S. no.	Parameter	Value
1	Dynamic range of input currents (I_z)	−80 μ to 250 μA
2	Dynamic range of input voltage (V_{y1}, V_{y2})	−250 m to 250 m V
3	Parasitic gain (V_{y1}/V_w, V_{y2}/V_w)	0.77, 0.54
4	Voltage tracking error	0.23, 0.46
5	Transconductance gain (g_m)	627 μA/V
6	Bandwidth (V_{y1}/V_w), (V_{y2}/V_w)	100 and 103.63 MHz
7	Bandwidth (I_z/V_p), (I_z/V_n), (I_x/V_z)	1.44, 1.57, and 12.82 GHz
8	Power dissipation	2.81 mW

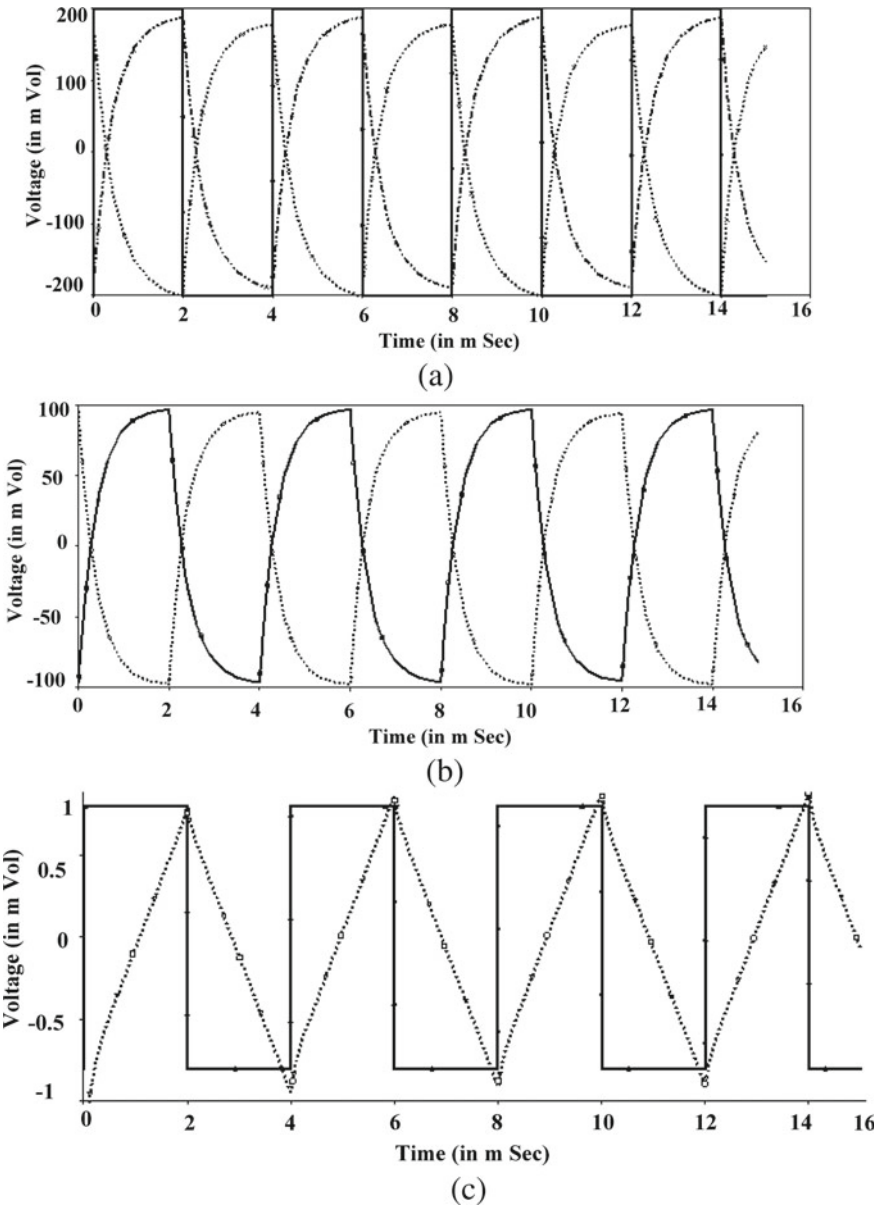

Fig. 5 Output response of integrator circuits **a** lossy integrator **b** lossy subtractor integrator **c** lossless integrator

5 Conclusion

A new active block named Differential Difference VDTA (DD-VDTA, an extension VDTA is proposed. The DC and AC characteristics of this block is done and found that this block can operate for higher frequency range applications. The applications of this block is shown for the lossy integrator, lossy subtractor integrator, and lossless integrator. It is designed using only one DD-VDTA block and one capacitor, having two outputs, viz., inverted and non-inverted at a time. The proposed configurations enjoys advantageous feature like less components are used, dual output at a time, low power dissipation and can be electronically tuned by changing its bias currents and easy design. These applications of proposed block has been proposed and verified. All the mathematical results have been verified by SPICE simulations with TSMC 0.18 μm CMOS process parameters.

References

1. Biolek D, Senani R, Biolkova V, Kolka Z (2008) Active elements for analog signal processing; classification, review and new proposals. Radioengineering 17(4):15–32
2. Moraveji F (1996) A tiny, high-speed, wide-band, voltage-feedback amplifier stable with all capacitive load. IEEE J Solid-State Circuits 31(10):1511–1516
3. Hou CL, Huang CC, Lan YS, Shaw JJ, Chang CM (1999) Current-mode and voltage-mode universal biquads using a single current-feedback amplifier. Int J Electron 86(8):929–932
4. Geiger RL, Sanchez-Sinencio E (1985) Active filter design using operational transconductance amplifiers: a tutorial. IEEE Circ Dev Magazine 1(2):20–32
5. Smith KC, Sedra A (1968) The current conveyor—a new circuit building block. Proc IEEE 56(8):1368–1369
6. Toumazou C, Lidgey FJ, Haigh D (eds) (1990) Analogue IC design: the current-mode approach, vol 2. Presbyterian Publishing Corp
7. Ferri G, Guerrini NC (2003) Low-voltage low-power CMOS current conveyors. Springer Science and Business Media
8. Tangsrirat W, Unhavanich S (2014) Voltage differencing transconductance amplifier-based floating simulators with a single grounded capacitor. IJPAP 52(6):423–428
9. Sedra A, Smith K (1970) A second-generation current conveyor and its applications. IEEE Trans Circ Theory 17(1):132–134
10. Fabre A (1995) Third-generation current conveyor: a new helpful active element. Electron Lett 31(5):338–339
11. Ibrahim MA, Minaei S, Yuce E, Herencsar N, Koton J (2012) Lossy/lossless floating/grounded inductance simulation using one DDCC. Radioengineering 21(1)
12. Elwan HO, Soliman AM (1997) Novel CMOS differential voltage current conveyor and its applications. IEE Proc Circ Dev Syst 144(3):195–200
13. Pathak JK, Singh AK, Senani R (2016) New canonic lossy inductor using a single CDBA and its application. Int J Electron 103(1):1–13
14. Zeki A, Toker A (2003) The dual-X current conveyor (DXCCII): a new active device for tunable continuous-time filters. Int J Electron 89(12):913–923
15. Srivastava M, Chitranshi G, Sengar P, Prasad D (2015) Novel current mode electronically tunable lossless integrator employing VDTA. In: 2015 Annual IEEE India conference (INDICON). IEEE, pp 1–4

16. Santhoshini KM, Musala S, Avireni S (2019) An integrator circuit using voltage difference transconductance amplifier. Solid State Electron Lett 1(1):10–14
17. Kumawat M, Mathur A, Sharma J, Srinivasulu A (2021) An Integrator using voltage differencing transconductance amplifier. In: Proceedings of 6th international conference on recent trends in computing. Springer, Singapore, pp 1–8
18. Kumar P, Pandey N, Paul SK (2017) Operational simulation of LC ladder filter using VDTA. Active Passive Electron Comp
19. Singh H, Arora K, Prasad D (2010) VDTA-based wave active filter. Circ Syst 5:124–131
20. Pandey N, Kumar P, Paul SK (2015) Voltage differencing trans-conductance amplifier based resistorless and electronically tunable wave active filter. Analog Integr Circ Sign Process 84:107–117
21. Singh G (2020) CMOS realization of VDTA based electronically tunable wave active filter with minimum power consumption at low supply voltage ±0.82 V. Circ Syst 11(02):11
22. Rana P, Ranjan A (2021) Odd-and even-order electronically controlled wave active filter employing differential difference trans-conductance amplifier (DDTA). Int J Electron 108(10):1623–1651
23. Rana P, Vista J, Ranjan A (2019) Three-input single-output (TISO) multifunction bi-quad filter implementation using VDTA. In: 2019 3rd international conference on I-SMAC (IoT in social, mobile, analytics and cloud) (I-SMAC). IEEE, pp 431–433