

12-Bit SAR ADC Design in SCL 180 nm for Sensor Interface Applications



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1 Introduction

The modern circuits we see all over the world are digital using which we can measure all the natural signals using sensors. As the responses from these sensors are analog signals (like temperature, speed, weight, etc.), to interpret and operate on them, an ADC is required [1–5]. ADCs could come in various types depending on applications and requirements. High resolution and high sampling speed are difficult to achieve simultaneously and hence needs trade-off in designing. Three types of ADCs are widely used, which are delta-sigma, pipeline, and SAR type ADCs [6]. Here, delta-sigma ADC is used for high resolution and low speed operation, and inversely pipeline ADC is used for low resolution and high speed operation. Amidst lies the SAR ADC which can achieve moderate speed of 10 K to 1 M samples per second and resolution up to 8–16 bits.

From circuits point of view, a delta-sigma ADC contain simple analog circuits such as difference amplifier, comparator, and integrator, but it also contains a complex digital filter requiring large area of implementation. Pipeline ADC has low complexity, but the size is largest. Hence, SAR ADC also provides area advantage over others and makes this more suitable for tiny sensors. The SAR ADC consists of primarily sample and hold circuits, comparator, DAC in feedback loop, and SAR logic circuits.

The presented work contains an assortment of all the sub-circuits in a SAR ADC to achieve high speed of operation and high resolution. To achieve high sampling rate, bootstrapped switch is used in sample and hold circuit. In DAC, differential charge scaling architecture is used to reduce the area compared to weighted resistors

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or capacitors circuits. This ADC also removes even order harmonics and provides common mode rejection [7] which improves SNR. All the sub-circuits designed and integrated using Cadence Virtuoso circuit simulator on SCL 180 nm technology. The ADC circuit thus created can achieve high speed of 1.1 MS/s with resolution of 12 bits.

2 Design of Blocks and Integration

This section discusses the ADC operation, design, and integration of all the circuits in detail.

2.1 ADC Operation

A 12-bit SAR ADC requires minimum 12 clock cycles to convert analog input to digital output. It contains a feedback loop as shown in Fig. 1. During the each clock cycle, a single bit value will be decided in order of MSB to LSB. In first clock cycle, SAR logic sets MSB of DAC to 1, and other bits are 0. This input combination of DAC gives its output as $V_{DAC} = V_{ref}/2$. If sample version of input voltage V_{IN} is greater than V_{DAC} , then comparator gives logic 1 as output, and SAR logic keeps MSB as 1 from next clock cycle during the conversion period, but when V_{IN} is smaller than V_{DAC} , SAR logic sets MSB as 0 from next clock cycle. For second clock cycle, SAR logic sets 2nd MSB as 1 with retaining previous result. Again, we compare V_{IN} and V_{DAC} and repeat the same procedure until we reach to LSB. An algorithm for 12-bit SAR ADC is given below in Table 1. At the end of conversion, DAC output V_{DAC} is approximated to V_{IN} . It means that, at the end the magnitude difference between V_{IN} and V_{DAC} should be less than 1 LSB. The convergence of V_{DAC} towards V_{IN} is shown in Table 1.

Fig. 1 SAR-ADC architecture

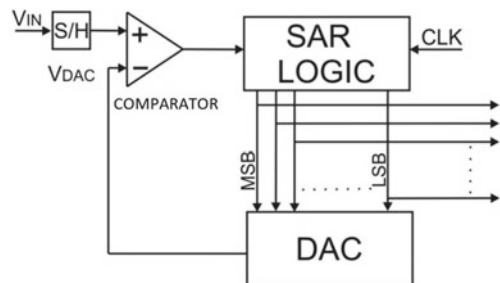


Table 1 V_{DAC} Output for each clock cycle and corresponding bit value

Clock cycle	D11	D10	D9	...	D2	D1	D0	V_{DAC} output	Bit decision
1st	1	0		...	0	0	0	$\frac{V_{ref}}{2}$	B11 = $\begin{cases} 1, & \text{if } V_{IN} > V_{DAC} \\ 0, & \text{if } V_{IN} < V_{DAC} \end{cases}$
2nd	B11	1	0	...	0	0	0	B11 $\frac{V_{ref}}{2} + \frac{V_{ref}}{4}$	B10 = $\begin{cases} 1, & \text{if } V_{IN} > V_{DAC} \\ 0, & \text{if } V_{IN} < V_{DAC} \end{cases}$
3rd	B11	B10	1	...	0	0	0	B11 $\frac{V_{ref}}{2} +$ B10 $\frac{V_{ref}}{4}$ $+ \frac{V_{ref}}{8}$	B9 = $\begin{cases} 1, & \text{if } V_{IN} > V_{DAC} \\ 0, & \text{if } V_{IN} < V_{DAC} \end{cases}$
4th	B11	B10	B9	...	0	0	0	B11 $\frac{V_{ref}}{2} +$ B10 $\frac{V_{ref}}{4} +$ B9 $\frac{V_{ref}}{8} + \frac{V_{ref}}{16}$	B8 = $\begin{cases} 1, & \text{if } V_{IN} > V_{DAC} \\ 0, & \text{if } V_{IN} < V_{DAC} \end{cases}$
...
11th	B11	B10	B9	...	B2	1	0	B11 $\frac{V_{ref}}{2} +$ B10 $\frac{V_{ref}}{4} +$ B9 $\frac{V_{ref}}{8} + B8$ $\frac{V_{ref}}{16} +$ B7 $\frac{V_{ref}}{32} + B6$ $\frac{V_{ref}}{64} +$ B5 $\frac{V_{ref}}{128} + B4$ $\frac{V_{ref}}{256} +$ B3 $\frac{V_{ref}}{512} + B2$ $\frac{V_{ref}}{1024} +$ $\frac{V_{ref}}{2048}$	B1 = $\begin{cases} 1, & \text{if } V_{IN} > V_{DAC} \\ 0, & \text{if } V_{IN} < V_{DAC} \end{cases}$

(continued)

2.2 Digital-To-Analog Converter (DAC)

In SAR ADC, a feedback DAC is required [8] whose output is approximated to analog input signal V_{IN} through an iterative process. The conventional DACs are made of resistors, e.g. R-2R ladder and weighted resistor types, use of which requires larger area in an IC, while also consuming more static power. Generally, in ICs, DAC used in SAR ADC is made of capacitor rather than resistor, which consume power only

Table 1 (continued)

Clock cycle	D11	D10	D9	...	D2	D1	D0	V_{DAC} output	Bit decision
12 th	B11	B10	B9	...	B2	B1	1	$B11 \frac{V_{ref}}{2} +$ $B10 \frac{V_{ref}}{4} +$ $+ B9 \frac{V_{ref}}{8} +$ $B8 \frac{V_{ref}}{16} +$ $B7 \frac{V_{ref}}{32} + B6$ $\frac{V_{ref}}{64} +$ $B5 \frac{V_{ref}}{128} + B4$ $\frac{V_{ref}}{256} +$ $B3 \frac{V_{ref}}{512} + B2$ $\frac{V_{ref}}{1024} +$ $B1 \frac{V_{ref}}{2048} +$ $\frac{V_{ref}}{4096}$	$B0 =$ $\begin{cases} 1, & \text{if } V_{IN} > V_{DAC} \\ 0, & \text{if } V_{IN} < V_{DAC} \end{cases}$

Table 2 Comparison of results

Specifications	[2]	[3]	This work
Technology	180 nm	180 nm	180 nm
Resolution (bits)	10	12	12
Power supply (V)	0.6	1.8	1.8
Sampling frequency (M samples/s)	0.2	0.2	1.1
Maximum DNL/INL	0.29/ - 0.8	NA	0.8/0.3
SNDR (dB)	69.55	71.55	73.54
ENOB (bits)	9.3	11.59	11.92
Power (μ W)	2	336	188
FOM (fJ/conversion step)	15.51	...	44

during charging. There are many examples of capacitive DAC such as C-2C DAC and charge scaling DAC. Some of capacitive DACs also allow to sample on it, and it does not require extra sample and hold circuit. Further, different switching schemes are used, for example, conventional switching and monotonic switching.

An advantage of C-2C DACs is that it has only two types of capacitor, but due to parasitic effect, these C-2C DACs are generally limited to 9-bit applications. For higher bit applications, charge scaling DACs are used with common centroid technique. The major disadvantage of this DAC is that the capacitance ratio increases exponentially with each bit which decreases sampling frequency exponentially. To

increase sampling rate and number of bits simultaneously, one of the solutions is split array DACs. An example of 12-bit split array DAC is shown below. The value of split capacitor C_s is given by following formula.

$$C_s = \frac{\text{sum of LSB array}}{\text{sum of MSB array}} C \quad (1)$$

Ideally output of split array DAC is same as charge scaling DAC for the value of split capacitor C_s . Output equation of this DAC is given as following equation.

$$V_{\text{OUT}} = -V_{\text{IN}} + B(N-1) \frac{V_{\text{ref}}}{2} + B(N-2) \frac{V_{\text{ref}}}{4} + \dots + B0 \frac{V_{\text{ref}}}{2^{N-1}} \quad (2)$$

The Eq. (2) on convergence gives the output as in equation below.

$$V_{\text{OUT}} = -V_{\text{IN}} + V_{\text{DAC}} \quad (2)$$

Other than the above-discussed DACs, which are single input and single output, differential DACs have dual input and output terminals [9]. This architecture has three major advantages, which are (a) input voltage range will double with increase in core power supply, (b) nullification of even order harmonics, and (c) common mode rejection. The 12-bit differential charge scaling DAC is shown in Fig. 2. The value of differential output, V_{OUT} , is given in equation below.

$$V_{\text{OUT}_p} - V_{\text{OUT}_n} = (V_{\text{IN}_p} - V_{\text{IN}_n}) - \text{VDD} + 2 \left\{ B(N-1) \frac{V_{\text{ref}}}{2} + B(N-2) \frac{V_{\text{ref}}}{4} \dots + B0 \frac{V_{\text{ref}}}{2^{N-1}} \right\} \quad (3)$$

From above equation of differential DAC, it can be concluded that power supply is behaving like single DAC whose supply is in range of VDD and (-VDD).

2.3 Comparator

Comparators give binary (digital) output depending on the difference of two analog inputs (Fig. 3a). When voltage at non-inverting terminal V_p is greater than the voltage at inverting terminal V_n , then output of comparator should be high (V_{OH}), but if V_p is smaller than V_n , output of comparator should be low (V_{OL}) for ideal comparator (Fig. 3b). In case of non-ideal ADC, the difference $V_p - V_n$ is in between V_{OH} and V_{OL} making it non-binary state and an undesired value (Fig. 3c). The discrete time comparators used in SAR ADC can mainly be divided into three major parts, namely preamplifier, regenerative latch, and SR flip-flop as shown in Fig. 3d.

The pre-amplifier block contains a fully differential amplifier in cascade with another differential amplifier, which is controlled by a clock signal (CLK) as shown

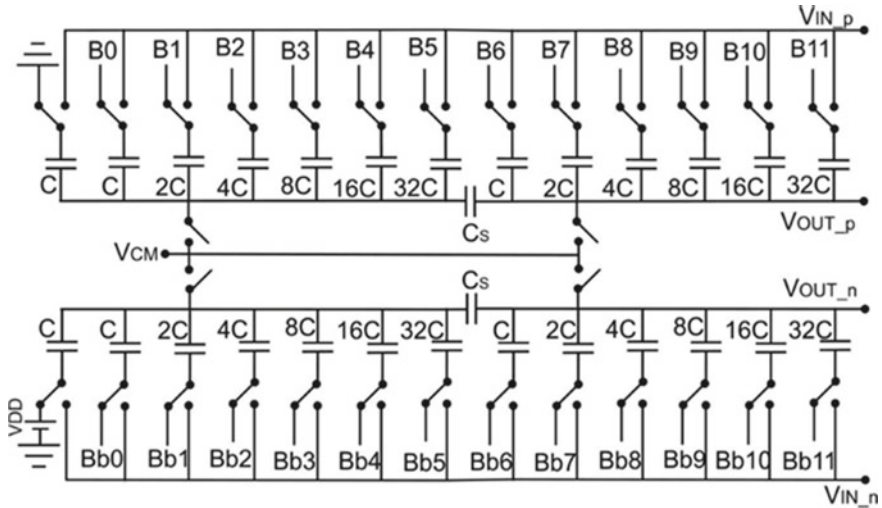


Fig. 2 12-bit differential charge scaling DAC

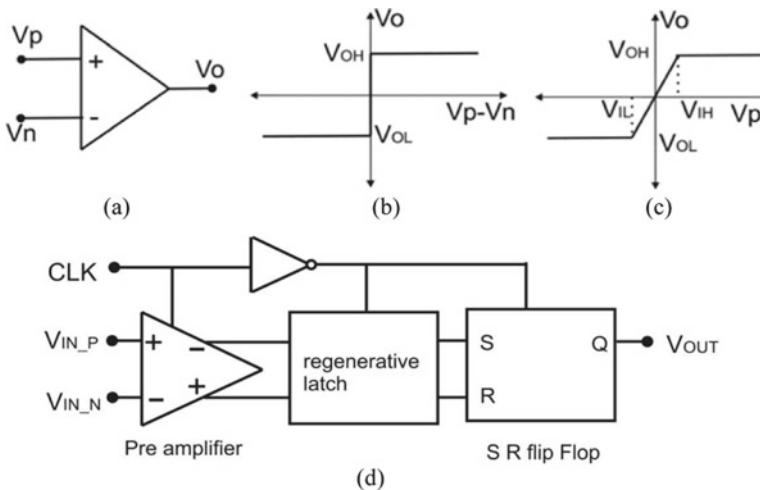


Fig. 3 a Comparator, b ideal comparator output, c non-ideal comparator output, d components of a comparator

in Fig. 4. The size of PMOS M3 and M4 are same and that of NMOS M1 and M2 are same as well to maintain similar sensitivity from high to low and low to high. While gain bandwidth product mainly depends on size of M1 or M2, maximum input common mode rejection ratio (ICMRR) depends on size of M3 or M4, and minimum ICMRR depends on size of M5. The small signal differential gain is given by g_{M1}/g_{M3} .

Fig. 4 Pre-amplifier block

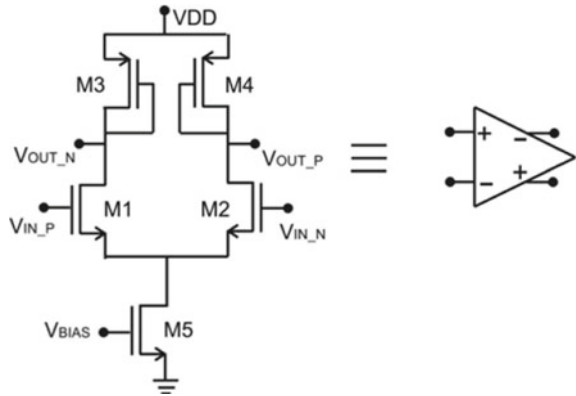
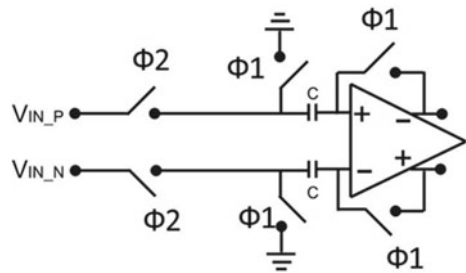


Fig. 5 Auto-zeroing technique for comparators



In the discrete comparator, pre-amplifier block is active only at high clock. This is followed by a regenerative latch which holds the comparison result and further connected to SR flip-flop to hold the result. On low clock, the latch and flip-flop resets their value, which results in no power consumption and discharges all the parasitic capacitances, commonly termed as auto-zeroing [9] technique as shown in Fig. 5. The inverted clock, which is connected to SR flip-flop, gives logic output at positive edge of clock signal.

2.4 Switch

Among basic MOS switches, NMOS as switch can be used for lower analog voltage, and in digital, it can be used to transmit strong zero (logic 0) and weak one (logic 1). Similarly, PMOS switch can be used for higher analog voltage, and in digital, it can be used for strong one (logic 1) and weak zero (logic 0). Even being very small in size, it has huge disadvantage that it cannot allow rail to rail analog signal, and its ON state resistance is dependent on input voltage. The ON state resistance, R_{ON} , for NMOS is given as:

$$R_{ONn} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{Tn})} \quad (4)$$

And, the ON state resistance, R_{ON} , for PMOS is given as:

$$R_{ONp} = \frac{1}{\mu_p C_{ox} \frac{W}{L} (V_{sg} - |V_{Tn}|)} \quad (5)$$

A transmission gate, however, is a parallel combination of both NMOS and PMOS, resulting in direct rail to rail contact in between input to load providing strong one (logic 1) and strong zero (logic 0). Its main disadvantage is that their ON state resistance also depends on input voltage resulting in higher order harmonics terms in transmitted signals. A switch with constant ON state resistance is needed to suppress higher order harmonics terms, which are also known as bootstrapped switch [10].

During the OFF phase in Fig. 6a, capacitor C_B is charged to VDD through the power supply, and gate of NMOS is connected to ground. At the ON phase in Fig. 6b, capacitor is now connected to gate and drain terminal of NMOS while disconnected from previous terminals. This combination keeps the gate overdrive voltage constant, and hence, the ON state resistance of NMOS is constant. It is observable that for implementing this switch the secondary switches are used which can be implemented by NMOS. The ON resistance of bootstrapped switch is given by Eq. (4). NMOS does not turn OFF instantaneously, and then, gate voltage is turned OFF, resulting in charge leakage and short-circuits input with ground. To avoid this, the switch is needed to be disconnected at input terminal when gate is grounded. This can be achieved using a two-phase clock circuit as used in Fig. 6c.

2.5 SAR Logic

The SAR logic block is intended to store, propagate, and output the digital signal. This block mainly contains (a) 14-bit ring counter, (b) array of 12-bit D flip-flop, (c) array of alternatively placed 12-bit NOR and OR gates, and (d) 12-bit parallel-in-parallel-out (PIPO) register [2, 3]. The $N + 2$ (12 + 2)-bit ring counter for N bit SAR ADC and the remaining two bits are required for sampling and holding purpose. In sampling stage, input is sampled by DAC, and at hold stage, the DAC is disconnected from both analog and digital switches. Post the hold stage, all the array in SAR logic is cleared, and then, the conversion phase starts where the capacitors in DAC are connected with digital switches as input terminals. All the 12 LSB outputs of ring counter are connected simultaneously to the respective inputs of array of D flip-flop and at one input of array of OR gates. The other input terminals of array of OR gates are connected with the output of D flip-flop. On the same time, input array of D flip-flop is also connected through output of comparator, where main purpose of D flip-flop is to hold previous comparison result. The output of NOR array is connected to the inverted input of differential DAC. The outputs from OR gates are

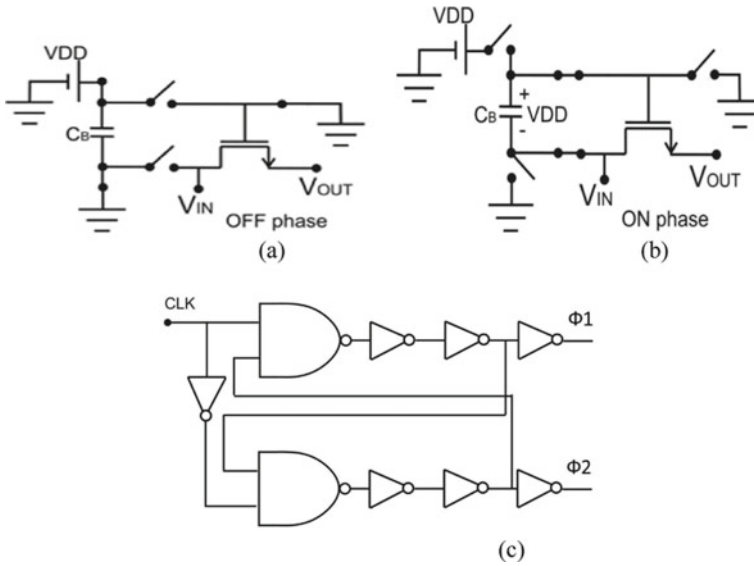


Fig. 6 Bootstrapped switch **a** OFF phase, **b** ON phase **c** Two-phase clock circuit generator

connected with the input terminals of PIPO register which at the end of conversion cycle provides digital output towards external interface.

3 Calculations

3.1 Quantization Noise

In quantization mapping of amplitude of discrete time signal to finite number of level $L = 2^n$ is done. The quantization power P_Q for uniformly distributed quantization noise is given by

$$P_Q = \frac{1}{12} \left(\frac{V_{REF+} - V_{REF-}}{2^n} \right)^2 \tag{6}$$

3.2 Signal to Noise Ratio (SNR)

Ideally the SNR for ADC is given by

$$\text{SNR} = 10 \log \frac{P_{\text{signal}}}{P_Q} \text{ dB} \quad (7)$$

When input has maximum possible amplitude of sinusoidal signal, then SNR is independent of $V_{\text{REF}+}$ and $V_{\text{REF}-}$, and it is given as the following equation.

$$\text{SNR} = 1.763 + 6.02n \text{ dB} \quad (8)$$

3.3 *Signal-to-Noise-and-Distortion Ratio (SDNR)*

SDNR is defined as the logarithmic ratio between input signal to sum of noise signal and harmonic distortion.

$$\text{SDNR} = 10 \log \frac{P_{\text{signal}}}{P_{\text{noise}} + P_{\text{harmonic distortion}}} \quad (9)$$

3.4 *Effective Number of Bits (ENOB)*

This measures the performance of real ADC compared to the ideal ADC. ENOB is measured in terms of SDNR in place of SNR because ideal ADC has only quantisation noise, and it is given by the following equation.

$$\text{ENOB} = \frac{\text{SDNR} - 1.763}{6.02} \quad (10)$$

3.5 *Figure of Merit (FOM)*

FOM is used for energy efficiency measurement of an ADC and is given as

$$\text{FOM} = \frac{P_{\text{total}}}{f_s 2^{\text{ENOB}}} \quad (11)$$

where f_s is sampling frequency, and P_{total} is power consumed by circuit which on physical simulation equals $188 \mu\text{W}$.

4 Results and Discussion

The maximum sampling frequency which indicates speed of operation in terms of bits, without affecting the performance of SAR ADC, calculated as 1.1MS/s for 12 bits, which is around 5.5 times higher than [2, 3]. Higher sampling rate is achieved due to split capacitor C_s which reduces effective capacitance seen by input source. The maximum DNL and INL are 0.8 LSB and 0.3 LSB, respectively, which are less than 1. As magnitude of DNL is less than 1, it can be concluded that there are not any intermediate missing digital counts and compares fairly to [2]. SDNR is calculated to be 73.54 dB. Using the values of SDNR, ENOB is calculated as 11.92. The average power consumption is 188 μ W which is around half of [3] but very high than [2] which focuses more on energy efficiency. Similarly, the FOM calculated to be higher than [2] as 44 fJ for each average conversion step.

5 Conclusion

The presented 12-bit SAR ADC is designed and simulated using Cadence Virtuoso circuit simulator and SCL 180 nm PDK. The designed ADC exhibited better sampling frequency due to bootstrapped switching in sample and hold circuit and auto-zeroing technique in comparator for fast comparison. Also, the differential charge scaling DAC used in this design reduces the harmonic distortion, and the low capacitors size reduces the size of entire circuit.

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