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Trupti Ranjan Lenka
Samar K. Saha
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Micro and Nanoelectronics Devices, Circuits and Systems

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Preface

The book presents state-of-the-art research and developments in micro- and nanoelectronics devices, circuits and systems through selected papers of the **2023 Springer 3rd International Conference on Micro/Nanoelectronics Devices, Circuits and Systems (MNDCS 2023)** held during 29–31 January 2023 through hybrid mode by IEEE EDS NIT Silchar Student Branch Chapter and IEEE Nanotechnology Council Chapter in association with the Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Assam, India. The high-quality contributions cover emerging areas in semiconductor materials, device technology, integrated circuit technology, system-on-chip (SoC), MEMS/NEMS and sensors for emerging applications. The contributed papers from India, Bangladesh, Italy, USA are included in this book.

The micro- and nanoelectronics devices include semiconductor device physics, quantum electronics, heterostructure transport, compact device modelling, LED, MOSFET, OTFT, OFET, FinFET, TFET, HEMT, THz and photonics devices, UWB semiconductor materials, 2D materials, nanotechnology: nanowires, nanostructures, carbon nanotubes, graphene, flexible electronics, high-efficiency solar cells: perovskite, CZTS, kesterite and novel photovoltaic concepts as outlined in various chapters on emerging applications. From micro- and nanoelectronics devices tracks, the Best Paper was awarded to "*Fabrication and Characterization of E-beam Deposited Copper Oxide Thin Film on FTO and Silicon Substrates for Optoelectronic Applications*" and the Honourable Mention Award was awarded to "*Morphological, Structural and Optical Analysis of Chevronic TiO_2 Thin Film Fabricated by Oblique Angle Deposition*".

The micro- and nanoelectronics circuits domain includes analog and digital VLSI circuits, mixed-mode VLSI circuits, bioelectronics circuits, circuit optimization techniques, reconfigurable circuits, HDL-based FPGA design and semiconductor memories: DRAM and SRAM. They are listed in various chapters towards emerging applications such as sensor, 5G/6G technology, IoT and biomedical. From micro- and nanoelectronics circuits tracks, the Best Paper was awarded to "*12-Bit SAR ADC Design in SCL 180 nm for Sensor Interface Applications*" and the Honourable

Mention Award was awarded to "*Resource Efficient TCAM Implementation Using SRAM*".

The micro- and nanoelectronics systems in various chapters include system on chip (SoC), RF-MEMS/NEMS, antennas, sensors, actuators, nanogenerators, energy harvesters (piezoelectric and MEMS), micromachining, microfluidics, lab on-chip, healthcare systems, embedded system design, biomedical systems, IoT and smart systems. From micro- and nanoelectronics systems tracks, the Best Paper was awarded to "*A Modular and Compact RF-MEMS Step Attenuator for Beam forming Applications in the Evolving 5G/6G Scenario*" and the Honourable Mention Award was awarded to "*Insight into 3D Printed Eight Well Electrochemiluminescence Biosensing Platforms with Shared Cathode: Towards Multiplexed Sensing*".

Silchar, Assam, India — Trupti Ranjan Lenka
Milpitas, CA, USA — Samar K. Saha
Canberra, ACT, Australia — Lan Fu

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Micro/Nanoelectronics Devices

A Theoretical Review on Challenges and Solutions of the Free Radical Scavenging Capability of Single-Walled Carbon Nanotubes (SWCNTs)

Meenakshi Malakar

1 Introduction

Carbon nanotubes (CNTs), owing to amazing structural, electrical, chemical and mechanical properties, are known to be the peak interesting materials for applications in various fields including electronics, energy, environment, agriculture, food, textile and so on [1–4]. Nonetheless, the uses of CNTs in biological and biomedical field are noteworthy. CNTs have been used extensively in biosensing applications such as DNA and protein biosensors, glucose sensors, dopamine sensors, immunosensors, biocatalysts and many more [1, 2, 5–13]. CNTs are used as nanocarriers for targeted treatments like drug delivery due to its noninvasive permeation through living membranes [1, 2, 14]. CNTs are also used in the early detection of cancer treatment [1, 2, 15]. Out of abundant applications, the most significant applications of CNTs are that they are extensively used in treating several cardiovascular diseases [2, 16]. CNTs provide a good base for neural growth, and it excites brain circuit action when CNTs and hippocampal cell associates [2, 17]. Owing to the unique features, the CNTs-reinforced composites are versatile candidates when used in bone tissue engineering. The CNTs-based scaffolds have their physical resemblance of collagen fiber as the extraordinary extent of porosity and flexibility of CNT is analogous to the natural extracellular medium [18, 19] (Fig. 1).

Due to the increasing industrial demand, the CNTs worldwide market growth rate is expected to increase from \$4.55 billion in 2018 to \$9.84 billion by 2023 with an annual growth rate (CGAR) of 16.7%. From Fig. 2, the worldwide CNT market growth rate is high in USA, China, India, Australia and parts of Asian countries. The

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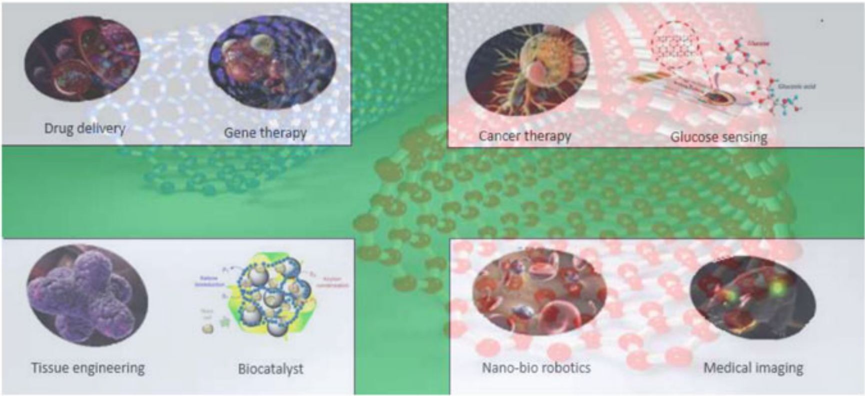


Fig. 1 Uses of CNTs in several fields of medical science [20]

largest manufacturers of CNTs are the USA and China. The OCSiAl, a European-based company, produces the highest (75 tons per annum) amount of SWCNTs [3].

In spite of increasing production and several studies of CNTs in the perspective of medical use, the application of CNTs in the scavenging action of free radicals is still emerging. This is quite surprising especially in the case of the scavenging action of the most devastating free radicals by CNTs. A scavenger is a chemical constituent in chemistry when combined to a mixture removes or de-activates impurities and undesirable reaction by-products, thereby stopping any unfavorable reactions [21]. If CNTs are designed for its application as scavengers, then the major concern of toxicity arises, how much concentration of CNTs would be required, whether CNTs itself would generate free radicals or hinder the biochemical processes of

Fig. 2 Global carbon nanotube market growth rate (2019–2024) with the name of some companies across the world. Adapted from [3] Copyright 2020, Elsevier

our body? However CNTs have proved a good level of biocompatibility because of their good specific surface and cylindrical structure [22]. Among the different CNTs types, SWCNTs are considered biomimetic to physiological molecules as they could permeate through cell crust and disperse along blood. The low charge carrier density of SWCNTs is desired features for developing in biosensing transducer platforms [23]. Moreover, SWCNT's electronic properties can be tuned from a large-gap semiconductor to a conducting metal with a small change in the pitch of helicity known as chiral vector (details are discussed under Sect. 3), which is not possible in case of other type of CNTs like MWCNTs. In an experimental study, Lucente-Schultz et al. [24] found that SWCNTs and ultrashort SWCNT both functionalized with butylated hydroxytoluene (BHT) are good antioxidants. In fact, the oxygen radical absorbance capacity assay shows that the oxygen radical trapping efficiency of the SWCNT is approximately 40 times higher compared to the radio protective dendritic fullerene with very little cytotoxicity on cell viability. Thus, the prospects of SWCNTs for use as free radical scavenger are quite promising.

There are certain experimental studies which have indicated that multi-walled carbon nanotubes (MWCNTs) can be applied as scavenging agents toward free radicals [25–28]. It is reported that the quantity of radicals produced during gamma irradiation procedure is lowered when MWCNTs are infused in ultrahigh molecular weight polyethylene (UHMWPE), an industrially used polymer for orthopedic applications [25]. Nymark et al. have found that MWCNTs are noted to trap hydroxyl radicals in presence or absence of BEAS 2B cell culture medium and bovine serum albumin (BSA) [26]. Cirillo et al. have performed the synthesis of radical embedding of gallic acid to pristine MWCNTs. The functionalized MWCNTs revealed good scavenging features toward hydroxyl, peroxyl and 2,2-diphenyl-1-picrylhydrazyl radicals [27]. Fenoglio et al. have observed that MWCNTs exhibit remarkable scavenging properties toward oxygen radicals (hydroxyl and superoxide radicals), instead of generating them [28].

There are also some research papers which highlights the toxicity issues of MWCNTs [29–32]. It is reported that MWCNTs with smallest diameters induce cytokine release, reactive oxygen species, autophagy dysfunction and activation of endoplasmic reticulum (ER) strain to human umbilical vein endothelial cells [29]. It is further reported that MWCNTs induce oxidative stress on C6 rat glioma cell, thereby making cell cytotoxic [30]. Further, pristine MWCNTs with surface hydrophobicity, metallic impurities and good aspect ratio are noted to make substantial oxidative damage and hepatotoxicity in mice [31]. Lin et al. have reported that MWCNTs' agglomerates are cytotoxic to the Arabidopsis T87 cells, and the toxicity is raised abruptly with the decrease in the diameters of the MWCNTs' agglomerates [32]. Thus, complete use of MWCNTs as free radical scavengers is followed by confusion and dilemma. While the theoretical research world is promising with the prospects of using CNTs especially of SWCNTs as a potent scavenger of free radicals (the details of the studies are discussed under Sect. 4), the rate of exploration or research output per year of CNTs in this research field is low as compared to its exploration or research output in other research fields.

Figure 3 shows that the rate of publication/exploration of CNT per year in the field of biosensing (i.e., 'CNT as DNA/protein/glucose/etc. sensors') is more than twice than that of the rate of publication/exploration of 'CNT as free radical scavengers.' Also, most of these graphical studies on 'CNT as free radical scavengers' are experimental with little theoretical insights. Moreover, these works highlight the use of MWCNTs as radical scavengers rather than SWCNTs. This shows that this valuable property of different types of CNTs is not harnessed extensively and is yet to attain its maximum limit.

Graphene and carbon nanotubes—the two kinds of carbon nanostructures—are used extensively in biomedical applications [33, 34]. However, Fig. 4 shows that in the research field of radical scavenging, the rate of publication/exploration per year is more for graphene than carbon nanotubes since 2018. This is due to more number of theoretical research papers on free radical scavenging capability of graphene have come up recently.

From the above pie diagram (Fig. 5), it is seen that the publication efficiency (in percentage) of 'CNT as free radical scavengers' from period 2015–2022 (till date November 28, 2022) is comparable to that of natural antioxidant (like melatonin/

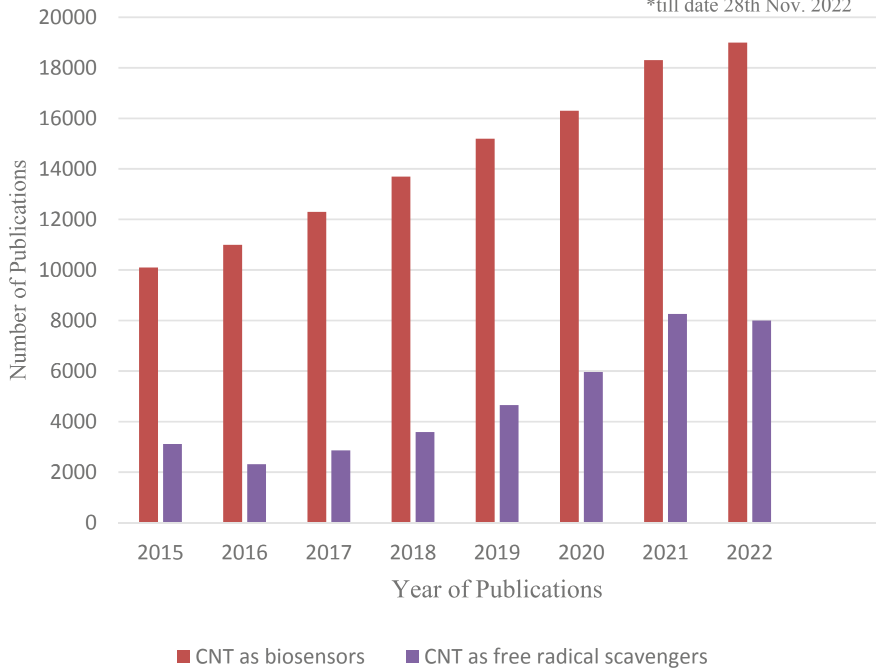


Fig. 3 Publications related to 'CNT as biosensors (including CNT as DNA sensor/protein sensor/glucose sensor/etc.)' are compared to that of 'CNT as radical scavengers' searched using 'Google Scholar.' This data comprises of regular articles, review articles, conference proceedings and book chapters

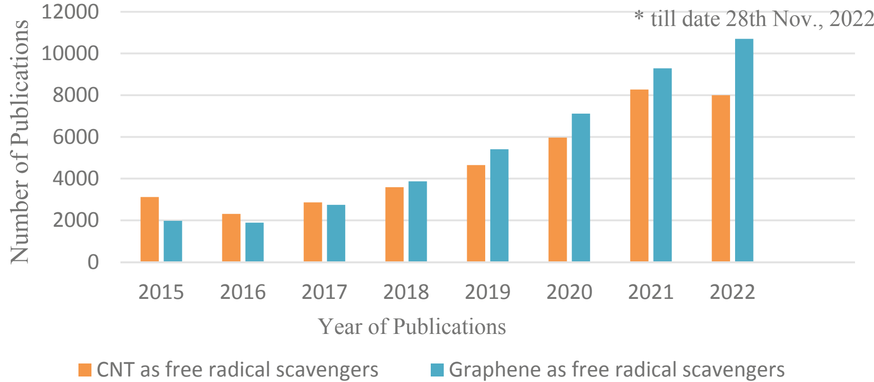


Fig. 4 Publications related to 'CNT as free radical scavengers' are compared to that of 'graphene as free radical scavengers' searched using 'Google Scholar.' This data comprises of regular articles, review articles, conference proceedings and book chapters

carotenoid/glutathione/caffeine/curcumin). This shows that CNTs are as important radical scavengers as that of established biological antioxidants.

The first theoretical research on the capability of SWCNTs to scavenge free radicals is reported in the year 2008 [35]. A decade has passed, and the number of theoretical research papers in this field is very limited (details of the studies are discussed under Sect. 4). This might be due to the improper utilization of the theoretical data, lack of more research in the theoretical field, discrepancies in the theoretical

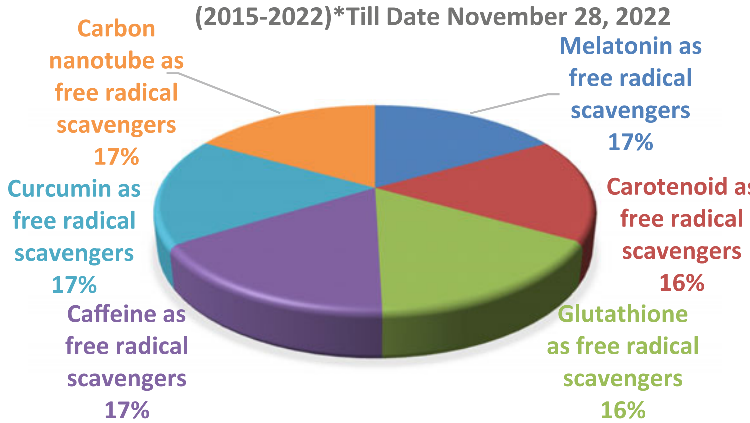


Fig. 5 Publications' percentage (2015–2022) related to 'CNT as free radical scavengers' are compared to that of 'melatonin/carotenoid/glutathione/caffeine/curcumin as free radical scavengers' searched using 'Google Scholar.' This data comprises of regular articles, review articles, conference proceedings and book chapters

model, problems faced by the experimentalists starting from the synthesis and characterization of SWCNTs itself, unexplored theoretical properties needed for practical purposes. Since experimental work is expensive, theoretical studies in this research field must be increased in order to make the graphs of Fig. 3 comparable. Moreover, there is no review paper which could bring forth the pros and cons of the theoretical model as well as the challenges in synthetic procedure, characterization techniques, purification techniques, etc. for the scavenging action of free radicals by SWCNTs. In this review work, we have tried to provide a comparative platform to analyze the discrepancies of the theoretical models as well as the challenges in the experimental field of SWCNTs as free radical scavengers with possible solutions and future directions of development of the scavenger.

2 Free Radicals, Its Types, Properties, Functions, Cell Damaging Properties and Consequent Diseases

A free radical is basically an atom, molecule or ion which can exist independently and has one or more unpaired valence electron. These unpaired electrons are responsible for free radicals' instability and extreme chemical reactivity. At moderate or low levels, free radicals are essential for lifecycle [36]. They take part in numerous biological purposes such as cell signaling processes, immune function, induce mitogenic response, redox regulation [36–38].

Free radicals are of two types—reactive oxygen species (ROS) and reactive nitrogen species (RNS). ROS are oxygen-reactive species including alkoxy radical ($RO^{\cdot}$), hydroxyl radical (OH·), peroxyl radical (ROO·), oxygen radical ($O_2^{\cdot\cdot}$) and superoxides (O_2^-). In biological context, ROS are formed (by mitochondria, endoplasmic reticulum, peroxisomes, phagocytic cells, etc.) as a byproduct of several physiological actions such as in cell signaling and homeostasis. But, at times of environmental strain (e.g., heat or UV contact, pollution, industrial solvents) and changes in habits (e.g., alcohol, tobacco smoke, physical stress, excessive exercise, certain drugs), there is disproportion between the amounts of the antioxidants and oxidants, which causes ROS to accumulate in the cell structures damaging important macromolecules like proteins, DNA, carbohydrates and lipids. This is named as oxidative stress that leads to numerous diseases including neurological disorders, diabetes mellitus, cancer, pulmonary diseases, cardiovascular disorder, arthritis, etc. [36–38].

RNS are chemically reactive species obtained from nitric oxide (NO·) and nitrogen dioxide ($NO^{\cdot}_2$). Both RNS and ROS are collectively responsible to damage cells, referred to as ROS/RNS, causing nitrosative stress [36, 39] (Fig. 6).

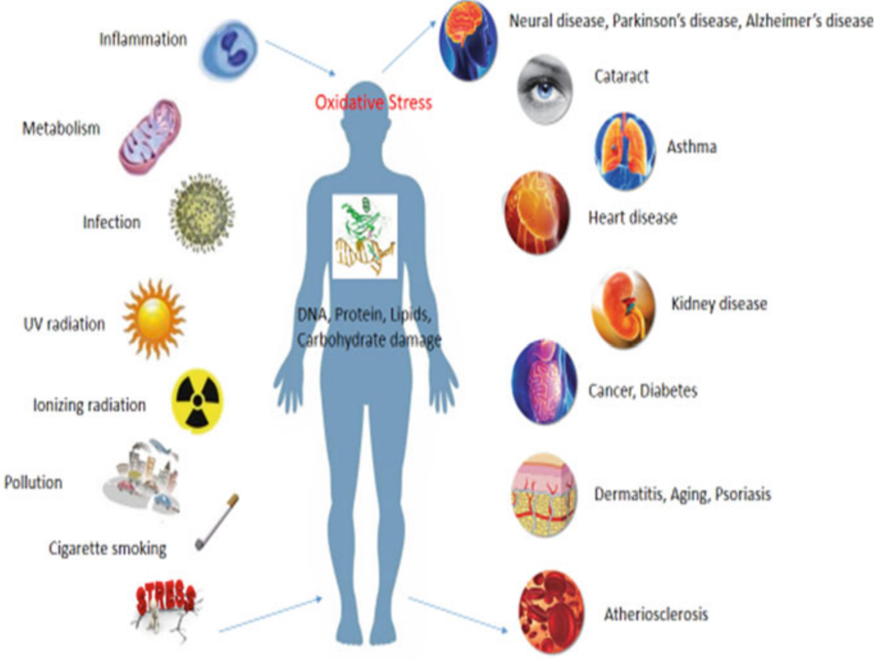


Fig. 6 Some sources of free radicals and consequent diseases [40]

3 Carbon Nanotubes (CNT), Its Types, Structure and Properties

Carbon nanotube (CNT) is a type of allotropes of carbon, having a diameter of nanometer-sized (nearly 50,000 times thinner compared to the thickness of a human hair) and a length of micrometer-sized. The arrangement of C-atoms in carbon nanotubes is same as that in graphene which consists of hexagons of C–C bond like beehive shaped belonging to sp^2 hybridization [1, 41]. In fact, the geometry of CNT is obtained by rolling the graphene sheet to a seamless cylinder with an axis parallel to C–C bonds. Depending on the rolling, there are three kinds of carbon nanotubes—armchair, chiral and zigzag [42], which are as shown in Fig. 7.

3.1 Classification of CNTs

CNTs are categorized mainly as the single-walled and multi-walled.

Single-walled: A single-walled carbon nanotubes (SWCNTs) are obtained by the rolling of a one layer of graphene to a seamless cylinder, making it effectively

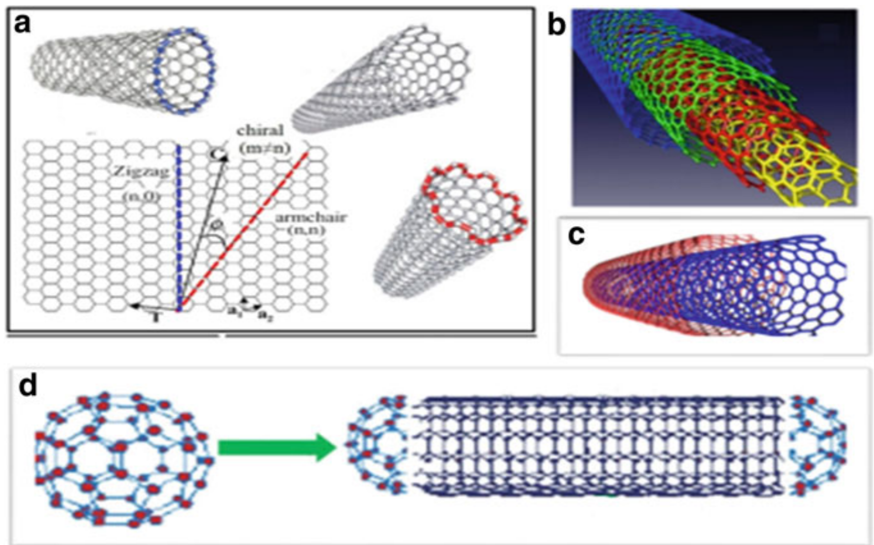


Fig. 7 **a** Different types of single-walled carbon nanotubes—armchair, zigzag and chiral. **b** Multi-walled carbon nanotubes (MWCNT). **c** Double-walled carbon nanotubes (DWCNT). **d** Capping of SWCNT by fullerene. Adapted from [50] Copyright 2015, Frontiers, [51] Copyright 2021, MDPI

a one-dimensional structure called a nanowire. Mostly, SWCNTs are with a diameter ranging from 0.4 to > 3 nm, while the length may spread to a few millions times compared to the diameter [43, 44].

The terminating end of the nanotube can be opened or closed by pentagonal and hexagonal rings of fullerenes. The smallest cap which can match to the SWCNT with diameter of 0.7 nm is the well-known C_{60} hemisphere [45]. However, SWCNTs of diameter with the theoretical maximum of 0.4 nm can be capped with a C_{20} dodecahedron [46, 47].

Multi-walled: Multi-walled carbon nanotubes (MWCNTs) are a collection of several rolled layers of concentric tubes of graphene having varied diameters extending from 1.4 to at least 100 nm. The distance between interlayer in MWCNTs is approximately near to the in between distance of graphene layers which is 3.3 Å [43, 44].

A distinct type of MWCNTs is double-walled carbon nanotubes (DWCNTs) which have very identical structure and properties in comparison to SWCNT [48].

3.2 Structure of SWCNTs

The structure of SWCNTs is represented by a chiral vector defined by the type of rolling of graphene sheet. The chiral vector is determined by two integral values (n,m), where the two integral values resemble to the sum of unit vectors toward the two directions of graphene and are given by:

$$C = \mathrm{na}_1 + \mathrm{ma}_2.$$

The three kinds of SWCNTs are shown by the values:
$m = 0$ for zigzag cylinders with ($\phi = 30°$);
$n = m$ for armchair cylinders with ($\phi = 0°$);
$n \neq m$ for chiral cylinders with ($0° < \phi < 30°$).

The armchair nanotubes are so named due to the edges are armchair-like shaped. They have same chiral indices. Similarly, the zigzag nanotubes are so named due to the edges are like zigzag shaped. They have zero as one of the chiral indices. The zigzag and armchair cylinder configurations have symmetric arrangement of hexagons around the circumference. On the other hand, chiral tubes have different chiral indices and are unsymmetrical [45].

3.3 Properties of SWCNTs

If ($n-m$) be a multiple of 3, the SWCNT behaves as metallic, else the SWCNT is a semiconducting material for all other cases. The armchair SWCNTs are highly desired because of their perfect conductivity, while the zigzag SWCNTs can be semiconductors. Moreover, rotating a graphene sheet simply by 30 degrees can transform armchair SWCNT to zigzag SWCNT and vice versa [45, 49].

4 Computational Studies on Free Radical Scavenging Capability of SWCNTs

On the theoretical front, simulation and modeling studies on SWCNT binding with free radicals have been carried out with varying degrees of exactness and difficulty. Quantum mechanical (QM) methods including semiempirical methods, Hartree–Fock (HF), density functional theory (DFT), etc. are primarily used in these studies' calculations. In attempt to understand these studies, a comprehensive review on the attachment of SWCNT with free radicals is done. The challenges on simulation studies done in this field are highlighted along with some experimental challenges so that comparison can be made to incorporate them in the simulation work. By

reviewing the computational methods, several factors that can contribute to further exploration in this field are identified and discussed.

In the below table, a review is shown chronologically for the simulation studies on the interaction of free radicals with SWCNTs. From Google Scholar surfing, a total of only seven research articles on this topic is found mostly centered around the publication year 2010. The Galano group is the only prominent group which has investigated the free radical scavenging capability of SWCNT theoretically. Table 1 lists the system simulated, method employed, computational details and outcomes for each investigation. Table 1 is a detailed explanation of these research and a comparison of them.

4.1 Studies Based on Reference (I)

The first theoretical research on the capability of SWCNTs to scavenge free radicals is reported in the year 2008 by Galano [35]. In this work, the author has used DFT calculations to model the ability of (5,5) armchair SWCNT nearly 8 Å in length with six varied radicals, namely HO˙,HOO·, ·CH_3, CH_3O·, CH_3OO· and ·CHO radicals. The end-terminals of the SWCNTs are saturated by H-atoms to ignore dangling of bonds due to distortions. Modeling is further increased to four additions for the most reactive and dangerous OH radical. The optimization of the configurations, followed by frequency calculations, is performed by means of the B3LYP hybrid Hartree–Fock density functional with the 3-21G basis set. The stationary energy points are enhanced by the calculations of single point obtained at the B3LYP/6-31G(d,p) level of theory. No imaginary frequency is noted, and the influence of solvent is also incorporated by single-point calculations by means of the polarizable continuum model (PCM) using the B3LYP/6-31G(d,p) level of theory taking benzene as a non-polar solvent. The apparent rate constant ($K_{app\text{-}sol}$) of the studied reactions is determined by Collins-Kimball theory.

The reactions are noted to be spontaneous based on thermodynamic and kinetic (ΔH, ΔG) considerations. The reactions are also noted to be exergonic, excluding those comprising of $OOCH_3$ and OOH radicals, which are reported to be considerably endergonic. The inclusion of non-polar solvents is found to increase the scavenging ability of SWCNT against free radicals in comparison to the gaseous medium.

The distances of the bond formed (forming) in transition states with rate constants at 298.15 K are also noted. It is reported that the scavenging processes take place abruptly; except the case of CH_3OO and OOH radicals, the rate constants are expected to remain in the diffusion range (Fig. 8).

The notable outcomes in this study are that the subsequent addition of OH radical to SWCNT is more favorable. This is suggestive that SWCNTs can be able to behave as free radical sponges. Further, it is noticed that the subsequent additions of OH radicals to the armchair nanotubes give rise to products where the OH groups are ranged in clusters instead of uniformly distributing on nanotubes. This is due to intramolecular interactions between neighboring OH groups.

Table 1 Summary of past simulation work on the interaction of free radicals with SWCNTs

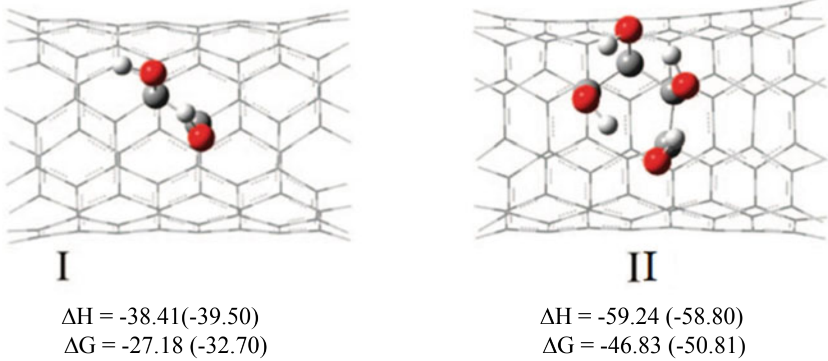
References	System	Method	Computational details	Result
(i) Galano [35]	SWCNT-OH/OOH/CH_3/ CH_3O/CH_3OO/CHO hybrid	B3LYP/ 3-21G for geometry optimization,, B3LYP/ 6-31G(d,p) for solvent effects (PCM) with benzene as solvent	Gibbs free energy, enthalpy, rate constant, global reactivity indexes, DOS	Reactions are spontaneous, SWCNTs act as OH radical sponges
(ii) Galano [52]	SWCNT-OCH_3 hybrid	B3LYP/ 3-21G for geometry optimization, B3LYP/ 6–311+G(d) for solvent effects (PCM) with benzene as solvent	Gibbs free energy, enthalpy	Reactions are spontaneous, zigzag SWCNTs are more efficient for free radical scavenging, the SWCNTs' length has a negligible effect for radical scavenging
(iii) Marquez et al. [53]	Carboxylated SWCNT-OH/ OOH/CH_3O/CH_3 hybrid	B3LYP/ 3-21G for geometry optimization, B3LYP/ 6–311+G(d) for solvent effects (PCM) with benzene and water as solvents	Gibbs free energy, entropy, enthalpy, frequency	Reactions are spontaneous, carboxylated CNT are better free radical scavenger if reactions take place at the most active sites
(iv) Galano et al. [54]	Defective SWCNT-OH hybrid	B3LYP/ 3-21G for geometry optimization, B3LYP/ 6–311+G(d) for solvent effects (PCM) with benzene as solvent	Gibbs free energy, enthalpy, frequency	Reactions are spontaneous, defective SWCNT is better OH radical scavenger

(continued)

Table 1 (continued)

References	System	Method	Computational details	Result
(v) Martinez et al. [55]	Ultrashort (US) SWCNT/ Defective-US-SWCNT/ Carboxylated-US-SWCNT-(20 different radicals) hybrid	B3LYP/ 3-21G for geometry optimization, B3LYP/ 6–311+G(d) for solvent effects (PCM) with benzene and water as solvents	Gibbs free energy, FEDAM graph	Reactions are spontaneous, US zigzag SWCNT is better electron acceptor and donor than US armchair SWCNT
(vi) Martinez et al. [56]	Functionalized SWCNT-OH hybrid	B3LYP/ 3-21G for geometry optimization, B3LYP/6–311 +G(d) for solvent effects (PCM) with water and benzene as solvents	Gibbs free energy, enthalpy, frequency	Reactions are spontaneous, functionalized SWCNT containing C,N,H in the functional groups are better OH radical scavenger
(vii) Shukla et al. [57]	SWCNT/ Defective SWCNT-OH hybrid	PM6 for geometry optimization, B3LYP/ 6-31G(d,p)// PM6 for the calculation of single-point energy	Binding energy	Metallic armchair SWCNTs with diameter in the extend of 0.7 nm or less, single vacancy tubes are better OH radical scavenger, Stone–Wales defective tube is bad OH radical scavenger and binding for two OH radicals takes place at the adjacent C-atoms on zigzag SWCNT

Details on notation: For example, B3LYP/3-21G denotes computation is done by means of B3LYP method with 3-21G basis set



ΔH = -38.41(-39.50)
ΔG = -27.18 (-32.70)

ΔH = -59.24 (-58.80)
ΔG = -46.83 (-50.81)

Fig. 8 Selected geometries of the optimized product of addition of (I) two OH radicals and (II) four OH radicals to (5,5) SWCNT. Energy values are in units of kcal mol^{-1}. Adapted from [35] Copyright 2008, American Chemical Society

The properties of the adducts of OH radical with SWCNT are examined in respect of global reactivity indexes including electrophilicity (ω), electronegativity (χ), hardness (η), chemical potential (μ) and also with density of states (DOS) plots. The calculations show that for two OH groups have reduced hardness values in comparison to pristine SWCNTs, but for four OH groups, η values are increased in comparison to pristine nanotubes. Also, the OH groups increase the electronegativity of SWCNT structures both in gaseous medium and in solvent environment. The largest and lowest values of ω are for SWCNTs attached with two OH groups and four OH groups, respectively.

The DOS spectrum (Fig. 9) shows that the gap near the Fermi level for the finite pristine SWCNT and the adducts of SWCNT with OH radical are transformed into a finite density of electrons at the Fermi level for 1D periodic pristine SWCNT which increases for structure of SWCNT with two OH radicals, whereas decreases for structure of SWCNT with four OH radicals thereby changing the metallic behavior of SWCNT. Thus, the DOS spectrum suggests that by regulating the quantity of OH groups on the SWCNTs, their conductivities can be monitored. However, the conversion of finite fragments of SWCNT to 1D periodic system (infinite nanotubes) for DOS calculations is unclear.

4.2 Studies Based on Reference (II)

In an attempt to understand the effect of length, diameter and chirality on the ability of SWCNTs to scavenge free radicals, Galano [52] choose finite SWCNTs fragments of different armchair and zigzag chiralities (starting from the thinnest tubes of (3,3) and (5,0) to the tubes of (8,8) and (14,0)) extending from 0.4 to 1.1 nm in diameters, while

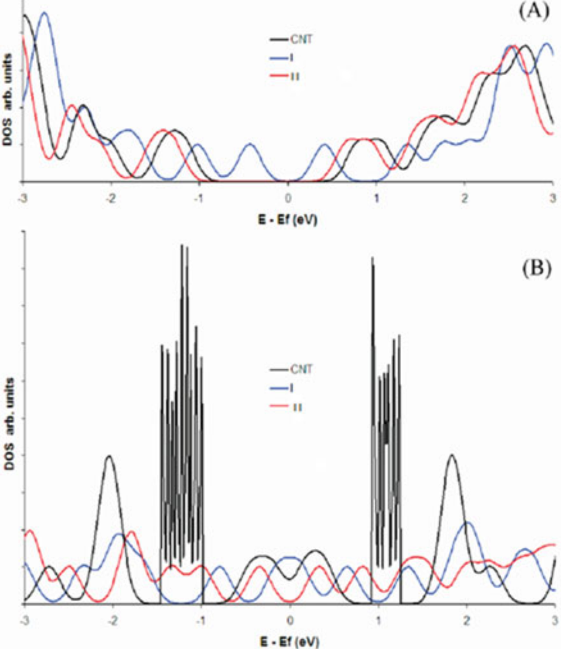


Fig. 9 Density of states (DOS) plots for: **a** SWCNT fragment, **b** SWCNT periodic system. Adapted from [35] Copyright 2008, American Chemical Society

the lengths extend from 0.7 to 2.0 nm. The end-terminals of the SWCNTs are saturated by H-atoms to ignore dangling of bonds due to distortions. These fragments of SWCNTs are then attached to OCH_3 (methoxyl) radical for studying their free radical capturing activity. Similar to the previous work of theoretical steps, the optimizations of the configurations, followed by frequency calculations, are performed by means of the B3LYP hybrid Hartree–Fock density functional with the 3-21G basis set. The stationary energy points are enhanced by the calculations of single point obtained at the B3LYP/6-31G(d,p) level of theory. No imaginary frequency is found, and the influence of the solvent is also incorporated by single-point calculations by means of the polarizable continuum model obtained at the B3LYP/6-31G(d,p) level of theory taking benzene as a non-polar medium. The diameters (D) in nm are calculated using the formula:

$$D = 0 \cdot 0783\sqrt{n^2 + m^2 + \text{nm}}.$$

The studied reactions are noted to be exothermic based on enthalpy data (ΔH), and most of them are found to be exergonic based on Gibb's free energy (ΔG) data. The feasibility of the studied reactions based on enthalpy and Gibb's free energy is noted to be increased when benzene is used as a solvent (Fig. 10).

A graphical analysis (Fig. 11) of the formed (forming) C−O bond with respect to the tube diameter and length reveals that the d(C−O) decrease as the tubes become

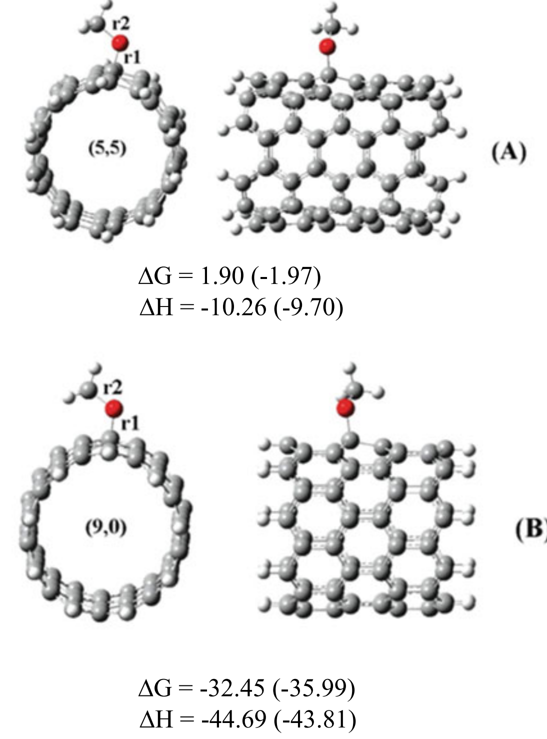


Fig. 10 Selected geometries of the optimized product of addition of OCH_3 radical to **a** (5,5) SWCNT and **b** (9,0) SWCNT. Energy values are in units of kcal mol^{-1}. Adapted from [52] Copyright 2009, American Chemical Society

thinner but increase as the tubes become wider, independent of the length of the tubes. This is the case for both armchair and zigzag tubes.

A similar graphical analysis (Fig. 12) is conducted for Gibbs free energy which reveals that the free radical trapping efficiency of armchair nanotubes decreases with the widening of the tubes. However, zigzag tubes do no show such dependency of tube diameter while reacting toward free radicals. Hence, the zigzag tube is more efficient than armchair one toward free radical scavenging purposes for varied-ranging diameter of SWCNTs. The study also reveals that the length of the tubes has least role on the capturing of free radicals by SWCNTs.

4.3 Studies Based on Reference (III)

Since carboxylated SWCNTs are found to have increased solubility and lowered toxicity [53], Marquez et al. [53] have studied the free radical trapping capability of carboxylated (5,0) zigzag and (3,3) armchair SWCNTs having two –COOH groups placed oppositely at the central hexagons or at the terminal ends for four varied free radicals, namely $\cdot CH_3$, $\cdot OCH_3$, $\cdot OH$ and $\cdot OOH$. The length of all the tubes is 11 Å long.

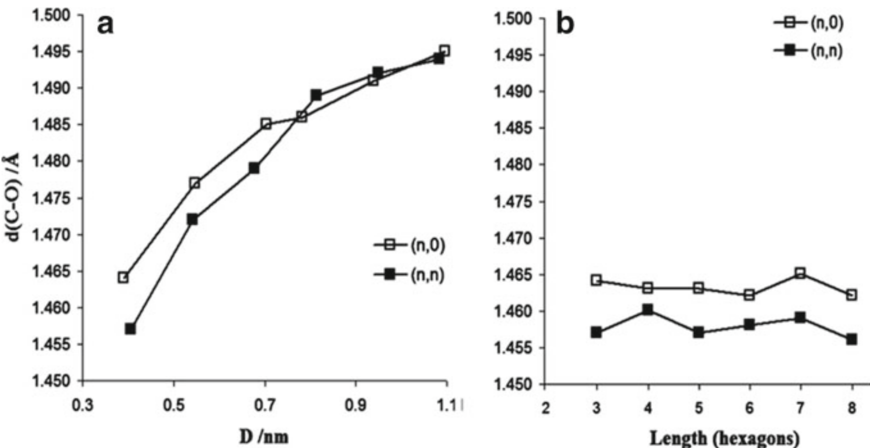


Fig. 11 Graph of d(C−O) in Å as a function of **a** tube diameter and **b** tube length. Adapted from [52] Copyright 2009, American Chemical Society

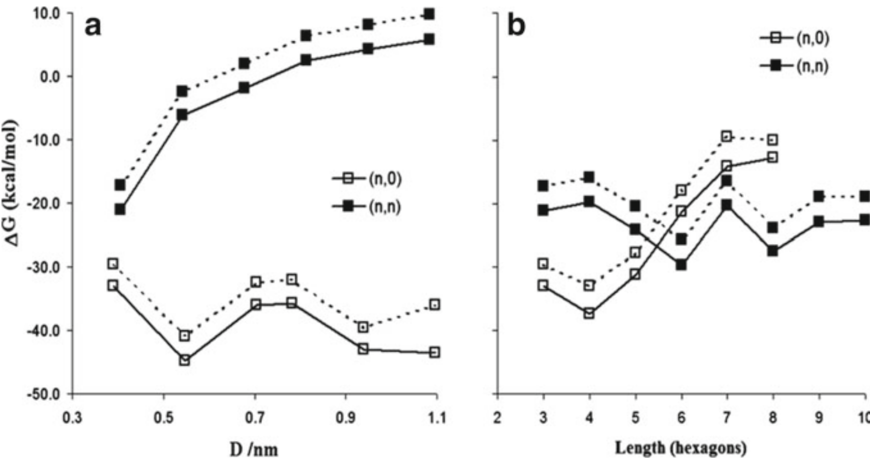


Fig. 12 Graph of Gibbs free energy as a function of **a** tube diameter and **b** tube length, where the continuous lines denote benzene solutions and dotted lines denote gaseous medium. Adapted from [52] Copyright 2009, American Chemical Society

The SWCNTs terminal ends are saturated by H-atoms to ignore dangling of bonds due to distortions. In this work also, the authors have carried out the same theoretical steps, that is, the optimizations of the configurations, followed by frequency calculations, are performed by means of the same B3LYP hybrid of HF density functional with 3-21G basis set. The stationary energy points are enhanced by the calculations of single point obtained at the B3LYP/6-31G(d, p) level of theory. No imaginary frequency is found, and the influence of solvent is also incorporated by single-point calculations

by means of the polarizable continuum model at the B3LYP/6-31G(d, p) level of theory taking water and benzene as solvent media (Fig. 13).

The reactions are noted to be exothermic, mostly exergonic based on enthalpy (ΔH), entropy (TΔS) and Gibbs free energy (ΔG) values of reaction, studied at 298.15 K. The distance of the bond formed between nanotube and radicals is also reported. A new theoretical calculation done in this work is the analysis of infrared (IR) spectra of the functionalized SWCNTs and the products of reaction. The calculated C=O and O–H stretching band frequencies resultant of carboxylic groups are then compared to the experimentally observed values of carboxylated SWCNTs. This comparison is done further for all the studied frequencies of carboxylated SWCNTs with the different radicals. From the calculations, it is found that for the radicals attached nearby to the -COOH groups, interaction between the neighbor functional groups take place as a result the bands analogous to $\nu_{C=O}$ and $\nu_{O\text{-}H}$ vibrations which gets divided into two ranging from about 5–20 cm^{-1}.

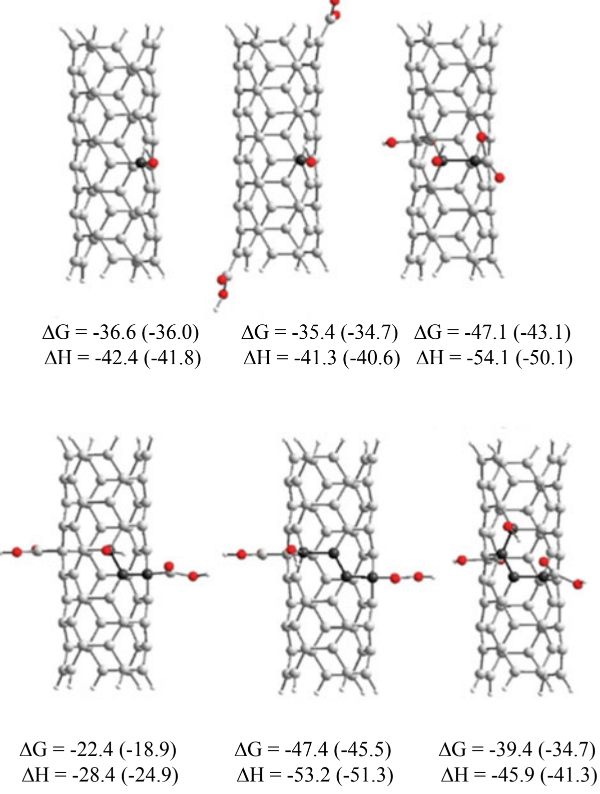


Fig. 13 Selected geometries of the optimized product of addition of OH radical to pristine and COOH-functionalized (3,3) SWCNT. Energy values are in units of kcal mol^{-1}. Adapted from [53] Copyright 2010, American Chemical Society

Further, it is found that the exergonicity (based on Gibbs free energy and enthalpy data) of the explored reactions of the carboxylation of the central hexagons of (3,3) SWCNT is site dependent, and the dependency is similar irrespective of environment and free radicals. The ortho position corresponding to COOH group of carboxylated zigzag fragment (5,0) is the only site which is more exergonic than its corresponding non-functionalized tubes for all studied radicals. The exergonicity corresponding to the pristine SWCNT is noted to be reduced for polar solvents.

4.4 Studies Based on Reference (IV)

In the process of synthesis of CNTs, several kinds of defects appear [59]. With an aim of understanding the effect of these structural defects on the free radical capturing capability of CNTs, Galano et al. [54] have studied the influence of point defects, namely the three kinds of defects, i.e., Stone–Wales (SW), adatom (AA), vacancy (V) defects on the free radical capturing capability of nearly 11 Å long (7,0) zigzag and (4,4) armchair SWCNTs with OH radical using DFT calculations. The end-terminals of the SWCNTs are saturated by H-atoms to ignore dangling of bonds due to distortions. The optimizations of the configurations, followed by frequency calculations, are performed by means of the B3LYP functional with the 3-21G basis set. The stationary energy points are enhanced by the calculations of single point obtained at the B3LYP/6311+G(d) level of theory, and no imaginary frequency is found. The influence of solvent is incorporated by the calculations of single point by means of a polarizable continuum model taking benzene as the solvent at the B3LYP/6–311+G(d) level of theory (Fig. 14).

The formed (forming) bond d(C−O) is also noted. It is found that the C−O distances of the defective tubes are shorter compared to the analogous pristine tube which indicates stronger bonds. The shortest C−O bonds are found when OH radical is attached to the C-atom having dangling bonds of AA and V1 defective SWCNTs.

The stretching vibrations of the C−O and O–H bonds when OH radical is attached to SWCNTs are infrared (IR) frequency analyzed. The IR band resultant of the υ_{O-H} vibration is more prominent near to 3300 cm^{-1} for the adducts studied here. While for the C−O stretching vibrations, an IR spread instead of a distinct band is found extending from ~ 900 to 1100 cm^{-1}.

The reactions are noted to be exergonic and exothermic based on enthalpy (ΔH) and Gibbs free energy (ΔG) data for the OH radical addition reaction to the various defective SWCNTs at 298.15 K.

The enthalpies of the addition of OH radicals to both (4,4) and (7,0) SWCNT fragments are least affected in presence of benzene. The ΔH and ΔG values at equivalent sites of addition reaction of OH radical are more negative for the (7,0) SWCNT than that for the (4,4) SWCNT. The most exergonic and exothermic reactions comprise of OH radical trappings to the positions of C-atoms having dangling bonds in V1 and AA defective SWCNTs respectively. In general, the V1 and AA defective SWCNTs act as better sinks for OH radical in comparison to V2 and Stone–Wales defective

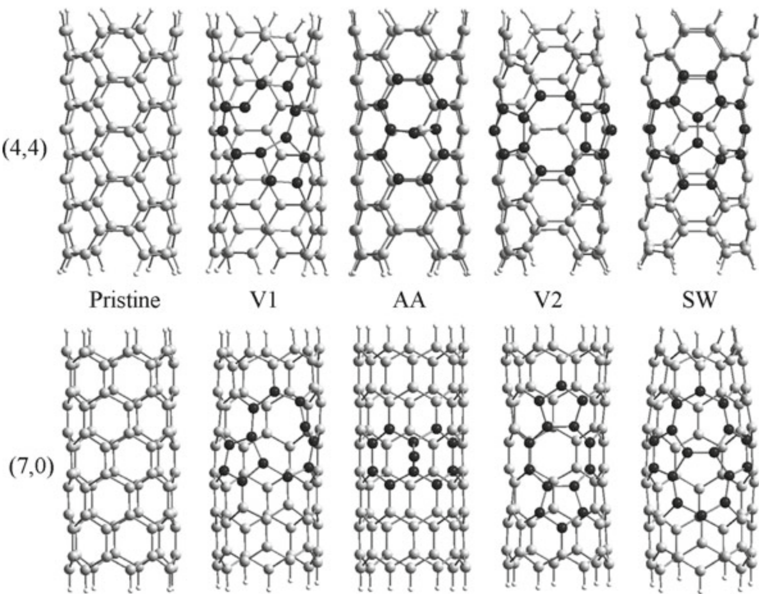


Fig. 14 Studied SWCNT fragments with H-atoms are represented by white color, C-atoms in non-defective regions by gray color and C-atoms in the point defective regions by dark gray color. Adapted from [54] Copyright 2010, American Chemical Society

SWCNTs. However, there is at least one position of increased scavenging activity in defective SWCNTs.

As a concluding remark, it can be said that it is not necessary to filter the various defective SWCNTs from the pristine SWCNTs during the process of synthesis of SWCNTs for its free radical trapping efficiency. In fact, the defective SWCNTs are richer free radical scavengers in comparison to the pristine ones.

4.5 Studies Based on Reference (V)

Inspired by the experimental research of Lucente-Schultz et al. [58] on the antioxidant capability of ultrashort SWCNTs, A. Martinez et al. [55] have studied the free radical trapping efficiency of ultrashort SWCNTs with varying configurations by means of electron transfer (ET) mechanisms. The ET mechanism neutralizes the free radicals by acting as acceptors or donors of electrons. This process occur in two pathways—(i) from US-SWCNTs to free radicals (FR) and (ii) from free radicals (FR) to US-SWCNTs:

$$\mathrm{US-SWCNT + FR\cdot \rightarrow US-SWCNT\,\cdot^{+} + FR^{-}(path\ (i))}$$

$$US - SWCNT + FR\cdot \rightarrow US - SWCNT\cdot^{-} + FR^{+} \text{ (path (ii))}$$

In this work, the authors have used DFT calculations to model the two processes for a range of armchair and zigzag US-SWCNTs, defective US-SWCNTs, carboxylated US-SWCNTs toward a wide-ranging of 20 different free radicals.

The optimizations of configurations, followed by frequency calculations, are performed by means of the B3LYP density functional with the 3-21G basis set. The stationary energy points are enhanced by the calculations of single point obtained at the B3LYP/6–311+G(d) level of theory. The end-terminals of the SWCNTs are saturated by H-atoms to ignore dangling of bonds due to distortions. No imaginary frequency is identified, and the influence of the solvent is incorporated by the calculations of single point by means of a polarizable continuum model obtained at the B3LYP/6–311+G(d) level of theory taking benzene and water as solvent environment.

For the purpose of reducing the simulation expenses of large-sized system, the authors have used an entirely different methods to predict the reaction feasibility by using a donor and acceptor map called as full electron donator acceptor map (FEDAM). It is on the basis of electron affinities and ionization energies, and it distinguishes between antioxidant and antireductant constituents. Hence, DFT calculations are made for several US-SWCNTs and radicals, and relative electron acceptance (REA) and relative electron donation (RIE) are described, taking fluorine and sodium as references (obtained at the same level of theory). A graph of RIE vs REA offers a donator acceptor map (FEDAM, Fig. 9), valuable for categorizing any radical-nanotube pair with respect to its electron donating–accepting ability (Fig. 15).

FEDAM maps can predict the feasibility, and also the reaction path of the electron transfer process is dependent on the behavior and properties of the SWCNTs and free radical. Molecules that are positioned in the upper right portion of the map can act as acceptors by removing electrons from molecules positioned in the lower left

Fig. 15 Full electron donator acceptor map (FEDAM). Adapted from [55] Copyright 2010, American Chemical Society

portion of the map acting as donors. If nanotubes are positioned in the lower left portion of the map (acting as donator) and radicals (R) are positioned in the upper right portion of the map (acting as acceptor), then the nanotube will scavenge the radicals following path I of electron transfer mechanism. If the free radicals are not as good as electron acceptors, then the SWCNTs will scavenge the radicals by acting as electron acceptors and following path II of electron transfer mechanism.

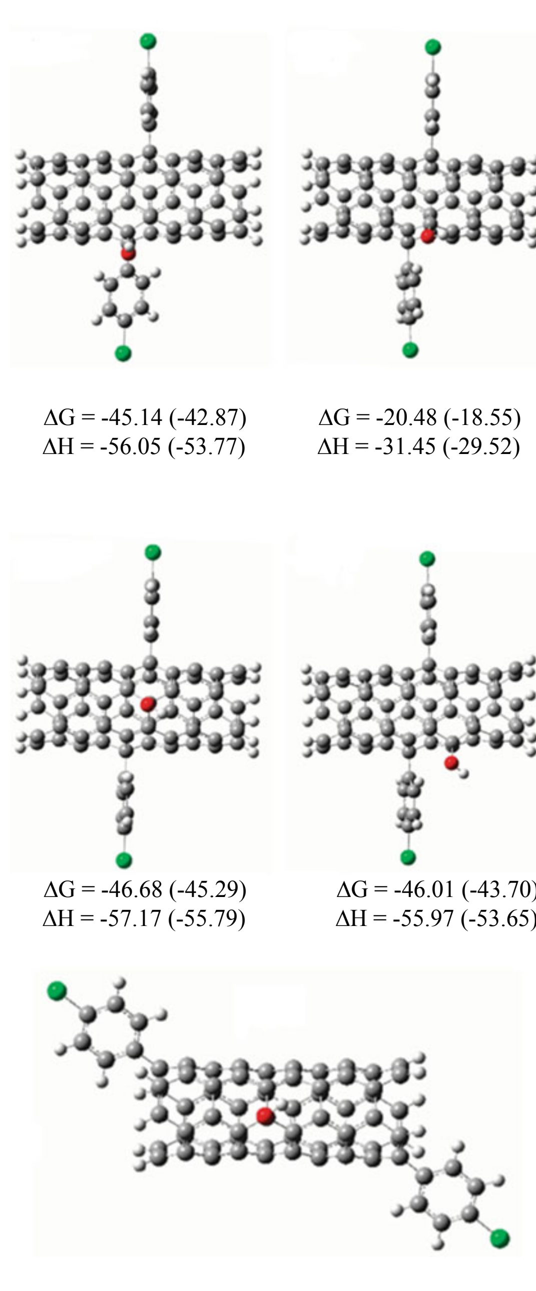
Based on the FEDAM maps which are further verified by Gibb's free energy for a range of armchair and zigzag US-SWCNTs, defective US-SWCNTs, carboxylated US-SWCNTs in water and benzene solvent with a wide-ranging of 20 different free radicals including the most reactive OH radical, the study concludes that ultrashort zigzag SWCNTs are richer electron acceptors or donors in comparison to the analogous armchair SWCNTs. Pristine zigzag SWCNTs are noted to be worse electron acceptors and better electron donors compared to carboxylated US-SWCNTs. The electron donor efficiency of carboxylated SWCNTs is similar to that of the pristine US-SWCNT but richer electron acceptors in comparison to the pristine SWCNTs. Further, the free radical scavenging ability by means of the electron transfer mechanism of the US-SWCNTs has least effect on the length and defects of the SWCNTs.

4.6 Studies Based on Reference (VI)

There may be some functional groups which can increase the solubility and radical trapping capability of SWCNTs. To investigate this, Martinez et al. [56] have noted the effect of different functional groups for the free radical trapping efficiency of SWCNTs. For this purpose, the authors have used DFT calculations to explore the addition reaction of OH radical at different positions of (5,0) and (3,3) SWCNTs nearly 11 Å in length functionalized by eight varying functional groups that have carbon and hydrogen and a combination of either oxygen, nitrogen, chlorine and sulfur. The optimizations of configurations, followed by frequency calculations, are performed by means of the B3LYP hybrid of HF density functional with the 3-21G basis set. The stationary energy points are enhanced by single-point calculations obtained at the B3LYP/6–311+G(d) level of theory. The end-terminals of the SWCNTs are saturated by hydrogen atoms to ignore dangling of bonds due to distortions. There are no imaginary frequencies found, and the influence of solvents is incorporated by the calculations of single point by means of a polarizable continuum model at the B3LYP/6–311+G(d) level of theory taking benzene as non-polar medium and water as polar medium (Fig. 16).

The reactions are noted to be exergonic and exothermic at room temperature based on thermodynamic (ΔH and ΔG) calculations. A comparison of ΔG of the reaction between functionalized SWCNTs and non-functionalized tubes is also reported to compare the free radical scavenging efficiency among them. On comparison, it is seen that there is at least one position in the functionalized SWCNTs where the OH additions are both thermally and chemically more favorable yet there are some

Fig. 16 Selected geometries of the optimized product of addition of OH radical to chlorobenzene functionalized (3,3) SWCNT. Energy values are in units of kcal mol^{-1}. Adapted from [56] Copyright 2010, American Chemical Society



positions of the functionalized SWCNTs which are less exergonic corresponding to that of pristine SWCNTs. Also, the zigzag (5,0) SWCNT has only one position, while the armchair (3,3) SWCNT has two, three or four positions of increased exergonicity. Further, it is noticed that functionalization groups containing nitrogen, oxygen and carbon are noted to be richer OH radical scavengers compared to that comprising of sulfur and chlorine.

4.7 Studies Based on Reference (VII)

Based on semiempirical and DFT studies, Shukla and Mishra have studied the influence of length, diameter, defects and chirality for the radical capturing ability of SWCNTs for OH radicals [57]. In this work, the authors have used binding energies as the only parameter to analyze the reactivities of the various adducts. The structures of both ends opened pristine zigzag (9,0), (10,0) SWCNTs, (5,5), (7,7) armchair SWCNTs, a Stone–Wales and a vacancy defective (5,5) armchair SWCNTs of varying lengths and their complexes with a OH radical added to a centrally positioned C-atom are optimized by means of the semiempirical PM6 approach in a vacuum medium, followed by frequency calculations. The structures of the adducts of (10,0) tube having two OH radicals added to the C-atoms at different centrally located positions are also optimized by means of the semiempirical PM6 approach in vacuum. Further, (5,5), (7,7), (9,0) are metallic nanotubes, while (10,0) is semiconducting nanotube. The end-terminals of the SWCNTs are saturated by H-atoms to ignore dangling of bonds due to distortions. The stationary energy points are enhanced using the calculations of single point obtained at the B3LYP/6-311G (d,p) level of theory in vacuum media. The binding energies (BE) of OH radicals added to different SWCNTs are obtained by means of the formula.

$$\text{BE} = E_{\text{SWCNT}-n\text{OH}} - (E_{\text{SWCNT}} + nE_{\text{OH}}), \tag{1}$$

where $E_{\text{SWCNT}-n\text{OH}}$, E_{OH} and E_{SWCNT} represent total energies of nOH radicals with SWCNT, an OH radical and the SWCNT, respectively.

On the basis of the above formula of BE, it is noticed that when the length of the (5,5) SWCNT increases from 8.7 to 26.0 Å, the BE of the complexes remain unchanged to some extent but when the length of the (7,7) SWCNTs increases from 8.7 to 13.6 Å, the binding energies of the complexes decrease remarkably. It reveals that the BE of the adducts with an OH radical decrease with the increase of the diameters of the longer armchair SWCNTs.

The study also shows that the semiconducting zigzag SWCNT can act as a better OH radical sink compared to the metallic SWCNT, while the presence of a SW defect reduces the OH radical scavenging capability. Further, it shows that the single vacancy defective armchair SWCNTs are richer OH radicals sponges when comparing to that of the SW defective and pristine armchair SWCNTs.

Highest occupied molecular orbital (HOMO) energies of the different SWCNTs have the similar trend as the BE for the case of pristine cylinders but the trend is absent in moving from the armchair pristine SWCNT to the defective SWCNT tubes. However, there is no detailed description of HOMO.

Further, it is energetically feasible of binding of second OH radical in zigzag (10,0) SWCNT, while the attachments of two OH radicals to C-sites placed adjacently are more favorable than the opposite and alternately placed carbon sites. Also, the binding of the two OH radicals having the perpendicular to the tube axis CC bond is better favorable than that along the tube axis.

5 Theoretical Challenges on Free Radical Scavenging Capability of SWCNTs

In spite of the different approaches used and different systems studied, the primary attentions of the past studies have been on the thermodynamic stability and spontaneity (ΔH, ΔG), configuration of the adduct (position of free radical with respect to the SWCNT) and strength of the interaction on the basis of binding energy (BE) values with the least emphasis on the type of the interaction (physisorption or chemisorption). The majority of studies have sought to investigate how system parameters such as the length, diameter, chirality, defects of the SWCNT and the presence of polar or non-polar solvents affect the binding. However, these calculations are limited and short of describing the other important properties.

Usually in all of the studies, SWCNT is modeled as a cylinder with ends are terminated by hydrogen atoms. These structures are then used in calculating the feasibility and binding energies of the complexes of SWCNT toward free radicals. However, a main drawback is that these interactions between the SWCNT supermolecule and radical monomers lead to unphysical energy lowering and consequent changes to geometries and frequencies, due to a phenomenon called as 'basis set superposition error (BSSE).' It is because to the reason that the explanation of the monomer in the supermolecule is better compared to that of the free monomers by using the same basis set. This effect is significant for both weakly/strongly bound systems and also with small/large basis sets. So, it is very important to remove this error [60, 61].

The optimization procedure is dependent on the initial configuration chosen to do the simulation as it is seen that it can vary the BE values or can alter the order of the BE values of various nucleobases with CNTs [62]. On the other hand, most of the past works have used a single initial structure to do the optimization, and the effect of initial configuration is not studied.

Most of the works evaluated the entropy, enthalpy and Gibbs free energy to check the spontaneity of the binding of free radical with SWCNT. However, these thermodynamic calculations are followed by enthalpy–entropy compensation where the

same variables are looked at in different ways. This could be a misleading interpretation of the data obtained from a relatively narrow range of temperature and free energies [63, 64].

Moreover, the simulations lack proper description of SWCNT's electronic response while interacting with the free radicals. Since the nature of the electronic response is an important property which must be known to know the sensing ability of any sensors, the explanation of the electronic response studied is very approximate. There is little understandings about how the SWCNT's electronic response may influence the electric field of the complexes. For the purpose of solving and visualizing the SWCNT's electronic distribution, atoms-in-molecules (AIM) analysis, frontier molecular orbital (FMO) analysis, natural bond orbital (NBO) analysis, molecular electrostatic potential (MEP) maps and density of states (DOS) analysis are mostly used in capturing the electrostatic interactions of the adducts [65–68]. However, a great amount of simulation and time is needed which has limited these computations.

The solution environment is considered in some studies but with a much estimated polarizable continuum models. Due to high computational cost, the optimized structures in gas/vacuum are simply used to do theoretical calculations in solvents, without any further optimization done in solution. Moreover, only water and benzene solution are considered in the past works. The effects of other types of solvents on the free radical capturing action of SWCNTs remain unknown.

Antioxidants can scavenge free radicals through various mechanisms such as electron transfer mechanism using FEDAM maps, quenching singlet oxygen mechanism, radical adduct formation mechanism and hydrogen atom transfer mechanism [69]. However, only Martinez et al. *(reference v)* have studied the scavenging action of SWCNTS toward free radicals through electron transfer mechanism using FEDAM maps. Other mechanisms of free radical scavenging action of SWCNTs are not explored or ignored.

The QM approaches have different methods which includes ab initio methods, DFT and semiempirical methods. Each method is associated with varying degrees of exactness and difficulty [70–72]. Hartree–Fock (HF), also termed self-consistent field (SCF) approach, is the first ab initio approach. In spite of having accurate explanation for the exchange energy, HF disregards correlation between electrons. This can provide a poor depiction of the electronic structure. These ab initio methods have high computational cost and hence are used for treating only small molecules [73]. Semiempirical QM approaches are improved versions of ab initio approaches using empirical parameters for calculations. These are much faster and computationally less expensive than the corresponding ab initio methods [74]. Examples of semiempirical methods are AM1, PM3, PM6 [75–78], etc. Among the QM methods, DFT has made an unparalleled impact in electronic structure calculations because of its comparatively less computational cost and high accuracy compared to ab initio and semiempirical approaches [79].

In the year 1964, Hohenberg–Kohn theorem on DFT shows that an accurate quantum mechanical outcome can be attained by substituting the many electron wave function using the electron density which greatly reduces the sum of variables

[80]. After one year, Kohn–Sham theorem improves it by acquainting with effective potential that includes exchange and correlation interactions, external potential thus connecting DFT to the orbital concept of chemistry [81]. Because of the imprecise behavior of exchange correlation functional, it becomes a challenging step in the development of DFT while constructing it [81]. Local density approximation (LDA) method represents the exchange correlation functional relying merely on the electron density. LDA method gives good prediction for geometries but not for energies as it over binds with the studied molecules [81, 82]. The satisfactorily progress is made when the electron density gradient is incorporated in the exchange and correlation functional, named as generalized gradient approximation (GGA) [81, 83]. This gives rise to a number of functionals whose performances are investigated in many studies. The most popular of all the functionals is B3LYP where a part of Hartree–Fock exact exchange (HF) is included in the functional. B3LYP shows good performance for a varied choice of structures, but its efficacy is challenged in treating π-π stacked systems [81, 84, 85].

6 Experimental Challenges on Free Radical Scavenging Capability of SWCNTs

CNTs, owing to their unique properties, have shown promising agents to behave as free radical scavengers [35, 38, 52–58]. Unlike its potency, the real-time commercial applications for CNT remain the major problem due to the high production and purification costs [3]. Among the CNTs, SWCNTs are much expensive to synthesize. If cheaper and affordable techniques of synthesis of SWCNTs be discovered, then only it would be economically probable for application of this technology to commercial scale uses [86]. During the process of synthesis of CNTs, a combination of tubes with varying length, diameter, defects and chirality is produced. In fact, producing CNTs of definite structures based on the diameter, length, chirality and defects is a major technological challenge [87].

Carbon nanotubes are commonly synthesized by three main processes: chemical vapor deposition (CVD), laser ablation and arc discharge. Each of these processes has its own pros and cons, and the most thrust area of research is to discover better cost-effective processes to synthesize these materials [87] (Fig. 17).

Generally, chemical vapor deposition (CVD) is the mostly applied process, but it produces only MWCNTs or lower quality SWCNTs. The SWCNTs synthesized with CVD have a huge uncontrollable diameter range [42]. CVD normally includes reaction of a carbon comprising source (like acetylene, ethanol, ethylene, etc.) using a metal catalyst (like cobalt, iron, nickel or their mixture) [1]. These catalyst might combine with SWCNTs and can pose threat to life if used for biological purposes [90]. Moreover, this method does not give rise to huge quantities of CNTs and less cost-effective to have any large-scale applications [3].

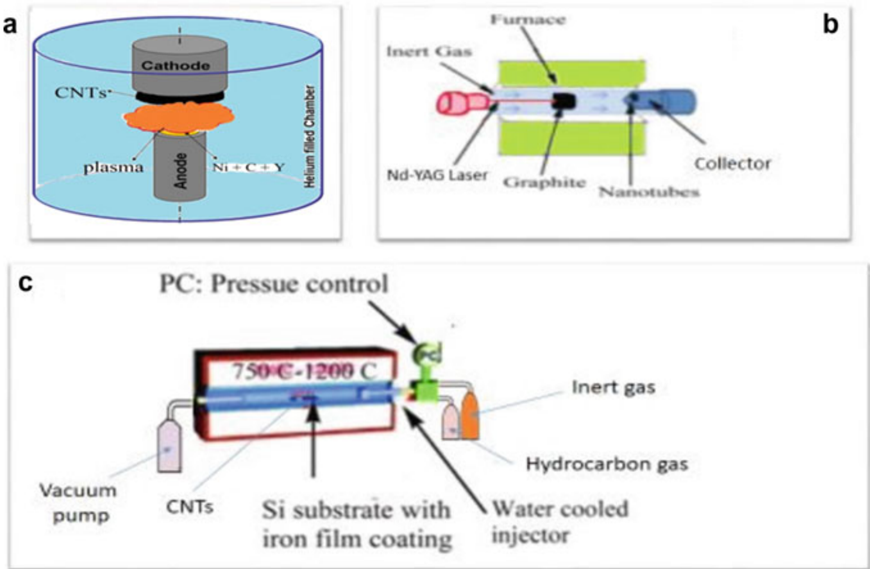


Fig. 17 Different methods of synthesis of CNTs—**a** arc discharge, **b** laser ablation, **c** chemical vapor deposition (CVD) [88, 89]

Laser ablation technique collects soot containing CNTs on the walls of a quartz tube formed due to vaporization of graphite by laser irradiation in a passive environment. This technique may be suitable for the purpose of biological uses of SWCNTs as it is free from harmful catalysts during its preparation [91].

However, all of these methods face difficulty in producing self-aligned CNTs and, aligned CNTs are needed for many basic research and applications of CNTs [92, 93].

The next step of CNT preparation is purification. During synthesis, the CNTs are produced along with impurities whose quantity and nature are influenced by the processes applied. The impurities are generally metals, carbonaceous materials, smaller fullerenes and also other kinds of impurities [94]. These impurities may pose threat to most of the chosen properties of the CNTs. The general industrial processes for purification apply strong acid-refluxing and oxidation processes, thereby modifying the structure of the tubes [95, 96].

The characterization of CNTs is an essential factor determined to identify the properties, feature and amount of the CNTs in the sample. CNTs are characterized by many techniques like transmission electronic microscopy, scanning tunneling microscopy, X-ray and neutron diffraction, X-ray photoelectron spectroscopy, Raman and infrared spectroscopy, etc. [97]. Among all these methods, Raman spectroscopy is a potent established tool to know about the diameter, chirality and length for SWCNTs [98]. However, the sample characterization preparation and its corresponding measurement have an influence on the properties and geometries of CNTs [98] (Fig. 18).

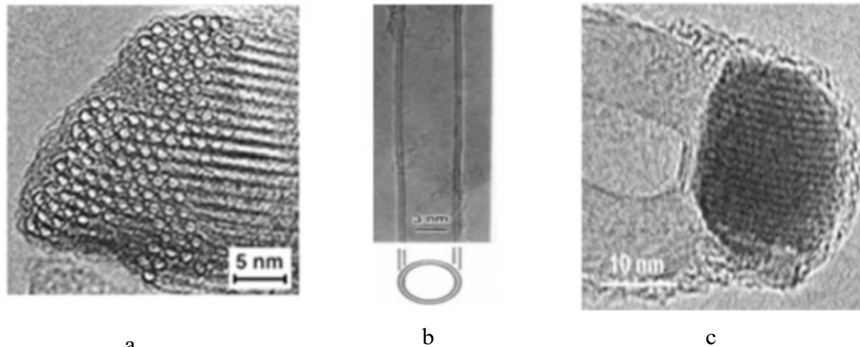


Fig. 18 Electron microscope images of **a** bundle of about 100 SWCNTs **b** DWCNT with a diameter of 3 nm **c** MWCNTs. Adapted from [87] Copyright 2019, Springer Nature

Thus, synthesis, characterization and purification methods have the ill-fated consequence that they alter the physical and chemical structure, electrical and mechanical properties of CNTs. These fascinating features of CNTs should be conserved, and hence, a research for a single and efficient step in producing, purifying and characterizing these structures must be carried out.

7 Toxicity Challenges on Free Radical Scavenging Capability of SWCNTs

The toxicity and biocompatibility of SWCNTs represent the opposite sides of the same coin. In fact, the toxicity of SWCNTs is the game changer for most of the biological applications of SWCNTs. Thus, it is very important to evaluate the toxicity range of SWCNTs before its direct insertion in the body. It is a case of concern if fibrous SWCNTs cause lung inflammation or malignant tumors [99], if SWCNTs interfere with the proteins and cause its denaturation of structure and affect its function, if highly reactive SWCNTs are missed by phagocytic defenses and enters the nearby organs, if non-biodegradable SWCNTs accumulates in the tissue system and cause health hazards [90]? Though the investigation is going on, one cannot conclude that SWCNTs are unsuitable for biological applications. There are numerous studies which strongly support that SWCNTs are biocompatible [100–104] (Fig. 19).

Mutlu et al. [100] have found that nanoscale dispersion of SWCNTs reduces the observed pulmonary toxicity and increases biocompatibility. Gheith et al. [101] have found that SWCNT polyelectrolyte freestanding films and multilayers act as biocompatible platform for neuroprosthetic implants which can significantly advance the diagnostics of neurological problems. The implant prototypes consist of layer-by-layer (LBL) assembly of SWCNTs modified by a polymer. These implants help in the outgrowth of neurites from NG108-15 cells, further supporting cell-to-cell

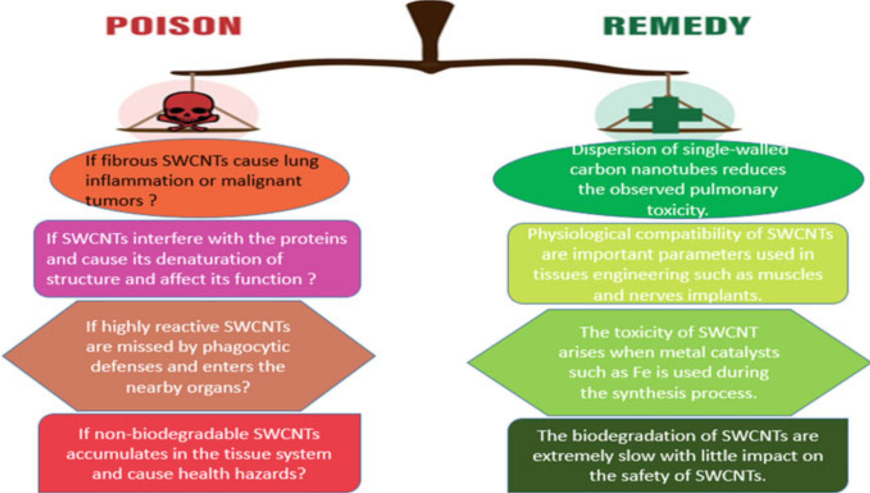


Fig. 19 Schematic representation of CNTs applications vs. their toxicity

communications. The results also prove the flexibility, non-biodegradability, inertness and durability of SWCNTs LBL freestanding films. Liopo et al. [102] have noted the biocompatibility of pristine and functionalized SWCNTs for neural interface. Their study demonstrates that rat primary peripheral neurons and NG108 show extraordinary currents when electrically coupled with conductive SWCNT films. The conductivity, flexibility and physiological compatibility of SWCNTs are important parameters used for excitation of tissues including nerves and muscles. Kim et al. [103] have obtained improved osteogenesis of human mesenchymal cells in chemically treated SWCNTs. This is because of the exceptional properties of SWCNTs like high aspect ratio, biocompatibility, excellent electrocatalytic activity and flexibility. Sitharaman et al. [104] have discussed in vivo biocompatibility of US-SWCNTs reinforced poly(propylene fumarate) nanocomposites in regards to soft and hard tissue response in a rabbit model. The implants help in the production of collagen with favorable bioactive assisting osteoconductivity. The biocompatibility of US-SWCNT/PPF nanocomposites is excellent and can act as a prototype bone tissue engineering scaffold.

Although most of the studies emphasize the biocompatibility of SWCNTs for in vivo applications, the toxicity and safety of SWCNTs still required to be more carefully addressed. It would be better if some computational simulations pertaining the dynamics of SWCNTs in complex cell environment be performed so that its extent of toxicity can be determined beforehand.

The biodegradability of SWCNTs can be initiated by body enzymes and COOH functional groups and defects of SWCNTs act as interaction positions for oxidative agents to initiate the degradation steps. The biodegradation of SWCNTs is extremely slow with little impact on the safety of SWCNTs [90].

The major case of toxicity issues of SWCNT arises when metal catalysts such as Fe are used during the synthesis process resulting in possible carcinogenic effect [105]. Consequently, search of alternative less toxic catalyst must be carried out in this regard.

8 Discussion and Future Direction

The research on free radical scavenging capability by SWCNT is ever-expanding, whether be it in predicting accurate theoretical model or synthesis process or characterization techniques or purification steps or toxicity issues, each part of the research needs further study and more investigation.

In nearly all studies reviewed from the theoretical front, no dispersion treatment is done. CNT and conjugated polymers which have the geometry of aromatic ring display remarkably π-π stacking effect [106]. B3LYP, a generally used functional in most of the tabulated studies, has low performance in considering π-π stacked systems as it does not have any dispersion built-in [85]. In fact, B3LYP is purely repulsive in treating π-π systems [81]. Recent studies using dispersion-corrected DFT with appropriate choice of basis set must be incorporated and be compared with the previous work. For instance, M06-2X function having double the quantity of nonlocal exchange (2X) is used to bring about benchmarking performance in treating of various dispersion-corrected approaches [107, 108]. Other approaches are also being reported; for instance, WB97XD is a range parted version of Becke's 97 functional having added dispersion correction [109]. The inclusion of dispersion correction in the reviewed work is likely to clearly explain the interaction between SWCNT and free radicals and can make more precise outcomes.

BSSE error can be corrected by counterpoise correction (CP) scheme where the monomers in the basis of the entire supermolecule are recalculated for each structural configuration. The difference in the interaction energies between the supermolecule and monomer is calculated in the same supermolecule basis set [60].

The effect of initial configuration can be minimized by performing a potential energy surface (PES) scan. A PES scan obtains the optimal position by tracing out the highest binding energy of the binding of SWCNT and free radical at different relative positions [110–112]. However, this PES scan was not considered in any of the past works.

Molecular dynamics (MD) simulation on the binding of SWCNT with free radical is not studied. As the binding of molecules at room temperature is a dynamic process, studies on dynamics may come up with more information.

Already discussed, both ROS and RNS act together to damage cells. However, in the past works, the efficiency of SWCNT for scavenging ROS is only studied. Moreover, most of the explored free radicals are smaller in size, and the properties may alter for larger in size free radicals because of steric hindrance. Hence, the efficiency of SWCNT for scavenging RNS must be investigated in parallel to its ROS scavenging efficiency.

It would be good if the binding be explored experimentally so that assessment can be done between theoretical and experimental results. Experimental works in both solution environment and vacuum would be beneficial for direct evaluation. Moreover, as it is more feasible to bind free radical with multi-walled carbon nanotube experimentally, theoretical work on free radical binding with MWCNTs in addition to SWCNT would be beneficial.

Finally, previous work showed that checking the spontaneity of the reaction using thermodynamic calculations has been used as the main parameter. Other properties like binding energies and density of states are explored only in one of the mentioned works. Also, studies on the understanding of atomic interaction by the atoms in molecules theory (AIM) analysis, the delocalization of electron density by natural bond orbital (NBO) analysis, the nature of bonding by natural population analysis (NPA) and WIBERG bond index (WBI), stability analysis by using the energy gap between highest occupied molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO) may come up with more information and help in better understanding of the model [65–68, 113, 114]. Molecular electrostatic potential surfaces (MEPS) help to determine the chemical reactivities and 3D charge distributions of molecules [67, 114]. Thus, MEPS can visualize variable charged regions of the hybrid of SWCNT with the free radical, which is used in determining the binding site of SWCNT or to know which region accelerates the electrophilic and nucleophilic reactivity of the designed scavenger [114]. To the best of our knowledge, little analysis has been done till now in this regard. These are good parameters to be explored for in-depth understanding of the theoretical model (Fig. 20).

The HOMO is the highest-energy occupied molecular orbital of electron, and LUMO is the lowest-energy unoccupied molecular orbital of electron in a molecule.

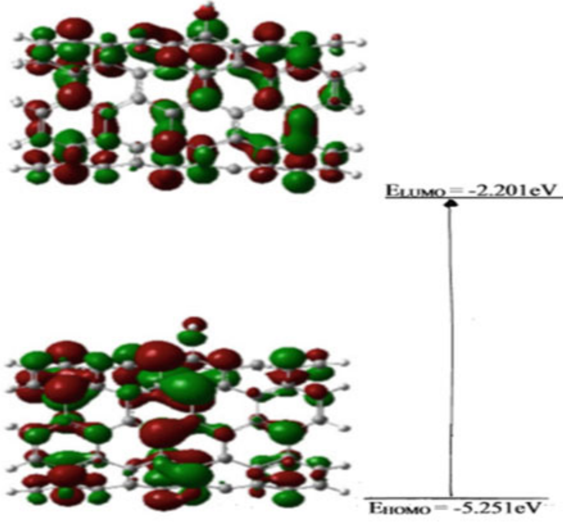


Fig. 20 HOMO and LUMO maps of SWCNT binding with OH radical. Adapted from [114] Copyright 2022, Springer Nature

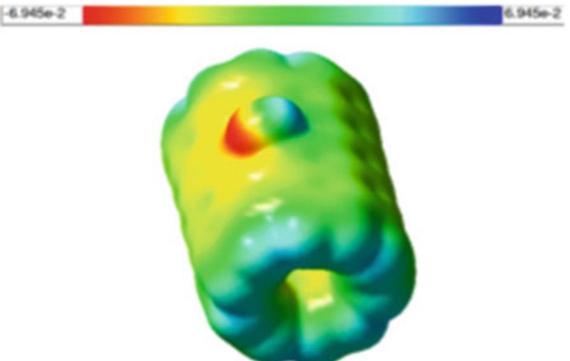


Fig. 21 MEPS graphic representation of SWCNT binding with OH radical. Adapted from [114] Copyright 2022, Springer Nature

The localization of electron density in HOMO and LUMO at a specific location will be regarded as nucleophilic and electrophilic in nature, respectively, describing its chemical reactivity. The electron affinity (A), electronegativity (χ), ionization potential (I), chemical softness (S), electrophilicity index (ω), chemical potential (μ) and other important properties can be determined from HOMO and LUMO [65–68, 113, 114] (Fig. 21).

The molecular electrostatic potential surface (MEPS) is showed by a color spectrum where yellow and red color regions are associated with electrophilic reactivity while blue color region is associated with nucleophilic reactivity. Thus, MEPS will help to determine visually the active electrophilic and nucleophilic sites of the designed scavenger [114].

It is hoped that these limitations on predicting the accurate model of SWCNT as free radical scavenger may be overcome in future with the development of computing facilities, thereby bringing the simulations closer to reality.

Nonetheless, this review work may provide some helpful steps in this regard (the details of the studies are already discussed under Sect. 4). Particularly, the optimum length, diameter and chirality of SWCNTs for OH radical trapping, provided by the work of Shukla et al. [57], give good information for the accurate measurement of diameter, length, chirality, etc., of the synthesized SWCNTs. The information of the various functional groups, which increase or decrease the free radical capturing efficiency of SWCNTs, explored by of Martinez et al. [56] is useful to know the effect of functionalized SWCNTs for the purpose. Since ultrashort SWCNTs are more ideal for in vivo use [115], the work of Martinez et al. [55] provides information about the scavenging activity of ultrashort SWCNTs toward 20 different radicals. During the process of synthesis of SWCNTs, several kinds of defects appear, and it is a troublesome work to obtain defect-free SWCNTs [116]. However, the work of Galano et al. and Shukla et al. [54, 57] showed that the presence of certain point defects can increase the free radical capturing capability of SWCNTs. Thus, the presence of certain defects during the synthesis of SWCNTs may not be a case of concern especially in the case of use of free radical capturing capability of SWCNTs.

The length, diameter and chirality of SWCNTs of the past computational studies are tabulated below (Table 2).

However, there are some aspects which need to be investigated by joining the hands of the theorist and the experimentalists. A review of capping of SWCNT by fullerene has been discussed, but the theoretical work on the free radical capturing efficiency of capped SWCNT must be carried out. As the synthesis of capped SWCNT can be achieved [117], theoretical investigation of this can provide new research grounds (some beneficial properties of capped SWCNT are depicted in Fig. 23). DWCNT has quite similar properties like SWCNT [118], but no theoretical research work based on its free radical capturing efficiency has been devoted in this case. Encapsulation of free radicals by SWCNT must be carried out as this work will be beneficial to the nanomedicine applications [119]. A little experimental research has been done on boron doped CNT as free radical scavengers [120]; however, no theoretical work has been done in this area. Exploring the type of dopants, doping effect, concentration of the dopants on the free radical capturing capability of SWCNTs can bring forth a new research platform both theoretically and experimentally.

As seen from Fig. 22, encapsulation separates and shields the drug from the nearby medium, which is very much helpful for medical uses like targeted drug delivery. For this purpose, SWCNT with large diameter must be chosen so that the molecules can be trapped inside the SWCNT [119]. Consequently, encapsulation of free radicals by SWCNTs will be very much beneficial as the free radicals will be trapped inside the SWCNT without further damaging the surrounding macromolecules. Thus, theoretical work on the binding of free radicals on the inside walls of SWCNTs with large diameter must be investigated. The other important biological application of one end capped and other end opened structure (like a nano-test-tube) of SWCNT is depicted in Fig. 23.

Table 2 Past computational studies based on length, diameter and chirality for free radical scavenging activity of SWCNTs

Computational studies	Length of SWCNT	Diameter of SWCNT	Chirality of SWCNT
Galano [35]	8 Å	–	(5,5)
Galano [52]	0.7–2.0 nm	0.4–1.1 nm	(3,3), (5,0)
Marquez et al. [53]	11 Å	–	(3,3), (5,0)
Shukla et al. [57]	7.1 Å, 8.7 Å, 11.1 Å, 13.6 Å, 26.0 Å	–	(5,5), (7,7), (9,0), (10,0)
Galano et al. [54]	11 Å	–	(4,4), (7,0)
Martinez et al. [55]	0.7–2.0 nm	0.4–1.1 nm	(5,0), (7,0), (9,0), (10,0), (12,0), (14,0), (3,3), (4,4), (5,5), (6,6), (7,7), (8,8)
Martinez et al. [56]	11 Å	–	(3,3), (5,0)

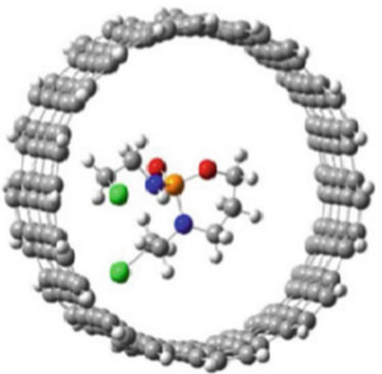


Fig. 22 Encapsulation of ifosfamide anticancer drug by SWCNT. Adapted from [119] Copyright 2019, Elsevier

To meet the increasing global demand, the large-scale synthesis of CNTs should be done such a manner that would not pose any detrimental effects to the life and environment, must be cost-effective and the sources should have abundant availability. This is possible through the sustainable development of environmentally benign and renewable methods of 'green nanotechnology' [3, 122]. The main idea is the choice of a carbon precursor which meets the principle of green chemistry and engineering. Recent studies have suggested hydrocarbons based on plant parts (leaves, stem, seeds and roots), and plant derivatives (camphor, palm oil, turpentine oil, coconut oil, olive oil and sesame oil) can be used as CNT precursors [123]. At present, the conventional approach for CNT production is catalytic chemical vapor deposition (CCVD) adopted by several companies [3, 124]. The greener approaches can be implemented into the existing CCVD technique such as using natural carbon sources, green catalysts and support materials. It is reported that these green processes have the same potential or even better than the conventional methods of synthesis though more research is needed in this case [3].

Further, in 'green nanotechnology,' the toxic metal catalysts are replaced by catalysts of plant extracts such as wallnut, rose, neem and garden grass. These green catalysts are of low-cost, abundantly available and do not pose any threat if used for biological purposes [125].

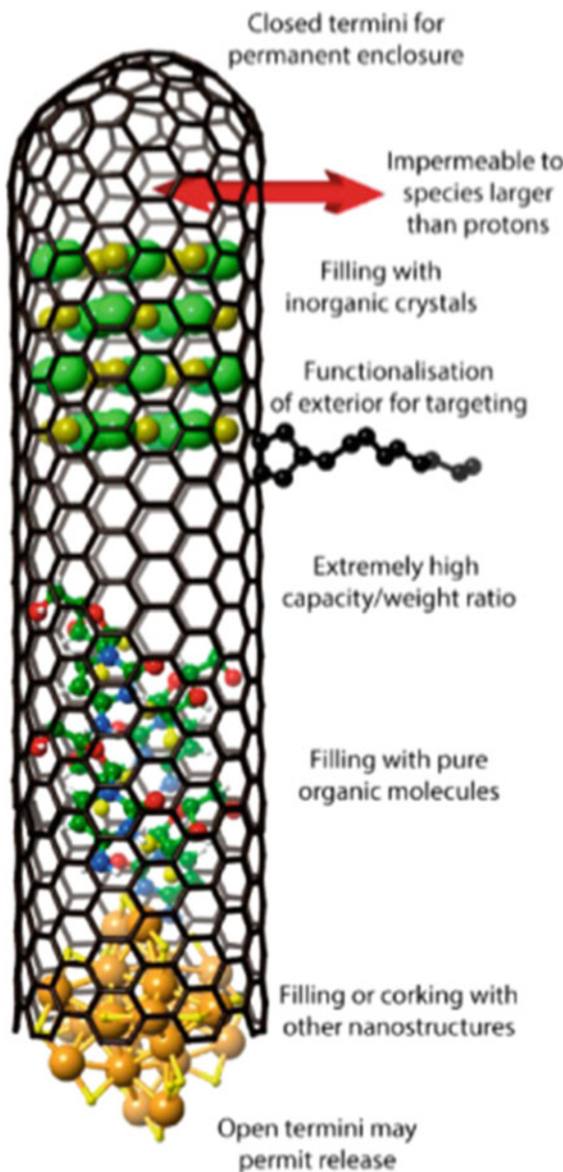


Fig. 23 Encapsulation in SWCNTs for biological applications. Adapted from [121] Copyright 2016, American Chemical Society

9 Conclusion

Nanotechnology is the most important technology in the present world. Its field include biotechnology, electronic, scientific tools, industrial manufacturing processes, etc. The main aspect of the field is to make novel and smart materials, and

CNT is a part of it. CNTs smart and versatile features has an unparalleled influence, particularly, in the field of medical science. CNTs can be used for diagnostic and therapeutic purposes such as they can be loaded with drugs, can detect biomolecules, can act as an implant for neural and muscle growth, can be used as a scaffold for bone tissue regeneration, etc. Theoretically, CNTs, especially SWCNTs are found as promising agents to capture free radicals; however, the research in this field is yet to achieve its exceeding limit. Since free radicals are known to cause several chronic diseases and the theoretical works have sparked about the ability of SWCNTs to act as a potent scavenger of free radicals, it is important to have more investigation on this research topic. The possible areas of further theoretical investigation have been discussed in detail in this review paper including accurate description of the theoretical model, unexplored properties, interaction with other radicals and ways to enhance SWCNT as a free radical scavengers. Though CNTs are encouraged in biomedical applications, there are various practical challenges, which is required to be addressed. For instance, mass production, high purification, real-time commercial applications, etc. are some of the difficulties faced by the industries. Moreover, the basic research of CNTs needs particular size and helicity, which is challenging in the manufacturing process. There must be a standardized protocol for determining the biocompatibility and cytotoxicity range of CNTs for which more investigation is required. All these issues are sought to be resolved, which is possible by joining the hands of material scientists, engineers, doctors and industrialists through discussion and co-operation. This will cause the spirit of these works to be implemented, and the quest for CNT structures with practical applications will then be rapidly passed from the realm of dreams to reality.

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Design and Analysis of T-Shaped Defect-Based Photonic Crystal Waveguide for Application of Optical Interconnect

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1 Introduction

Photonic crystal (PhC) has witnessed an unprecedented research interest since its discovery by Yablonovitch and John in 1987 [1, 2]. PhCs have undergone substantial theoretical and experimental study because of its periodic dielectric structure and ability to guide and manipulate light at the optical wavelength scale. The photonic band gap (PBG), one of the fundamental characteristics of PhCs, restricts the propagation of light within a specific range of frequencies [3, 4]. The PBG property of PhCs opens up enormous opportunities towards envision of wide range of applications like communication, filtering, bio-sensing, interconnector, modulator, polarizer, environmental safety, food processing, etc. [5–8]. However, a peculiar property can be observed when defects are added to PhCs, where the periodicity of this dielectric structure is disrupted, which allows the PhCs to exhibit high electromagnetic field confinement, a little mode volume, and feeble confinement loss. The propagation of light can be altered and engineered by altering the structural characteristics of PhCs or introducing appropriate materials into the air holes of the PhCs.

Optical interconnect serves as a connector between various components in photonic integrated circuits, and it provides certain advantages such as high bandwidth, multiplexing compatibility, and low-power communications. Electrical interconnects suffer from high latency, higher power consumption, and decreased bandwidth as they scale down. Conversely, the optical interconnects have the ability to alleviate the problems in electrical interconnects, since they circumvent the resistive

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loss physics that causes this restriction. Since PhCs demonstrate variations in the refractive index on the order of the light's wavelength, they can be advantageous in photonic integrated circuits. Basically, the efficiency and losses of the light wave circuits are regulated by the interconnects. The losses linked to various devices are directly affected by the interconnects. Therefore, the interconnects are the foundation of the planar light wave circuits.

In the recent decade, different defect-based photonic crystal waveguides have been proposed, including wide-angle bent channel waveguides, Y-shaped branches with wide-angle, L-shaped 90° bend photonic crystal waveguides [9–12]. References [13–15] proposed different bending insensitive, bending orientation insensitive, large mode area-based photonic crystal fibre (PCF) structures with lower confinement and bending loss. However, PCF nonlinearity effect has not been emphasized. Boscolo et al. [16] suggested a power splitter with three photonic crystal waveguides (PCW) intersecting at a 120° angle. In order to explain the reported poor transmission efficiency (43.6%) for each output arm, an analogy between PCWs and the transmission was constructed. The authors utilized tuning holes in the input channels, which allows the efficiency to increase to 49.6%. Fan et al. [17] investigated how well light passed through a T junction power splitter in terms of transmittance performance. Despite the single mode benefit of the waveguide structure, its main limitations were poor vertical confinement and challenging production in the optical realm at wavelength scales. Kabir et al. [18] made an effort to highlight the bending loss, confinement loss, and nonlinearity effect of PCF; the results fell short of expectations. Arif et al. [19] demonstrated how confinement loss and nonlinearity impacted the PCF's ability to operate for cladding that was rotated 90°, but they also acquired a very unfavourable high nonlinearity.

This paper proposes a T-shaped power splitter based on the photonic crystal waveguide formed in a 2D PhC by introducing line defects in T shape. Here, in the proposed photonic crystal structure, the periodic variation of the refractive index causes the photonic band gap (PBG). Because the introduced 2D line defects have the ability to capture photons and keep them from entering the crystal. Therefore, it results in low bending loss and improved optical confinement to the proposed T-shaped power splitter, where the input power is divided into the two output ports. Apart from this, the nonlinear coefficient of the proposed structure is studied.

2 Proposed Design and Methodology

The proposed structure consists of 9 $\times$ 9 circular rods of GaAs. The background is considered to be air as the dielectric. The circular rods are arranged in triangular lattice configuration. T-shaped defect is induced in the structure by removing rows of circular rods along the T shape, hence creating a T-shaped defect-based PCW as illustrated in Fig. 1a. Figure 1b shows the 3D view of the designed structure. A light signal of 2 μm wavelength is impinged in the defect region. Observation points are placed at the input port and each end of the T-shaped structure to record the field

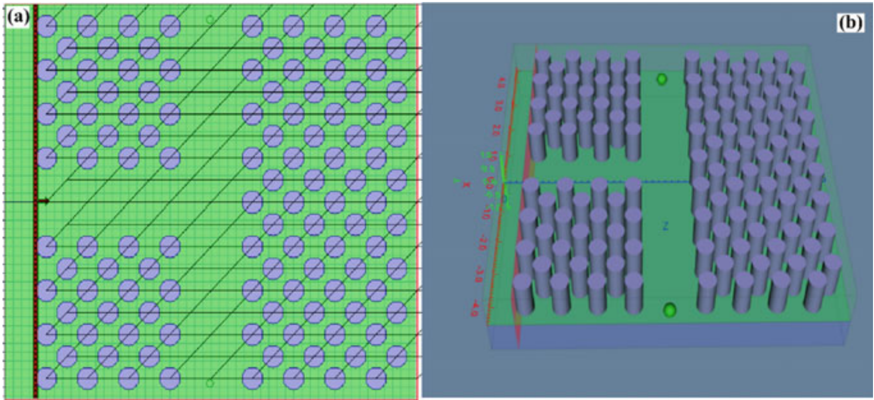

Fig. 1 **a** Proposed designed T-shaped defect structure, **b** 3D view of the design

intensities at these locations. In the design, the radius of each circular rod is taken as 0.25 μm, whereas the lattice constant is selected as 1 μm. These values are selected such that proper photonic band gap characteristics can be realized.

The refractive index (RI) of GaAs is evaluated using Sellmeier equation, which is given as [20],

$$n_{\mathrm{BaTiO_3}}(\lambda) = \sqrt{A + \frac{B}{1 - C^2/\lambda^2}} \quad (1)$$

where the coefficients A, B, and C^2 are taken as 8.950, 2.054, and 0.390, respectively. Photonic crystal-based device properties can be modelled using several computational techniques, including plane wave expansion (PWE), beam propagation, transfer matrices, finite-difference time-domain, finite elements, and effective index approaches. Finite-difference time-domain (FDTD) technique is one of them. Due to its advantages, including the capacity to simulate effects of polarization, reflection, scattering, diffraction, and propagation of light, FDTD is a rigorous and effective way to analyse sub-micron devices with very fine structural details and simulate integrated and diffractive optics devices. FDTD computation methodology is employed for solving the differential equations to find the solutions of electromagnetic field distribution in the waveguide. Entire cross section is meshed into sub-domains, and computation is done for each sub-division simultaneously. Any structure that has the necessary physics described by Maxwell's equations can be simulated using FDTD. Here, OptiFDTD software package is used which is based on FDTD method. FDTD solves Maxwell's curl equations [21, 22]:

$$-\frac{1}{\mu}\nabla \times \vec{E} = \frac{\partial \vec{H}}{\partial t} \quad (2)$$

$$\nabla \times \vec{H} = \varepsilon \frac{\partial \vec{E}}{\partial t} + \vec{J} \tag{3}$$

where H and E denote the magnetic, electric, respectively, and the complex relative dielectric constant $\varepsilon_r(\omega)$ is given by $\varepsilon_r(\omega) = n^2$, where refractive index is given by n. In the proposed structure, we have a 2D PhC considered in the X–Z plane. Since the structure is assumed to be infinite in the Y direction, the fields are said to be independent of Y. Therefore, Maxwell's equations are broken into two (TE and TM) sets of independent of equations, each of 3 vector quantities by eliminating all the $\partial/\partial y$ derivatives, these are termed as TE and TM mode equations [23]. In the proposed work, we have analysed only the TE modes, where the expression for TE mode can be written by putting $H_x = H_z = 0$ and $E_y = 0$.

$$-\mu \frac{\partial H_y}{\partial t} = \frac{\partial E_x}{\partial z} - \frac{\partial E_Z}{\partial x} \tag{4}$$

$$\frac{\partial E_x}{\partial t} = -\frac{1}{\varepsilon} \frac{\partial H_y}{\partial z} \tag{5}$$

$$\frac{\partial E_Z}{\partial t} = \frac{1}{\varepsilon} \frac{\partial H_y}{\partial x} \tag{6}$$

FDTD computes E and H at grid points separated by Δx, Δy, and Δz, with E and H interwoven in all three spatial dimensions in the grid cell (Yee cell). This is achieved by solving the time-dependent Maxwell's equations on a mesh. Each mesh point corresponds to a particular material type and includes details on all of its characteristics, including the dispersion factors and refractive index. The nonlinear coefficient in the PhC waveguide is a vital parameter, which depends upon the effective area of the photonic waveguide. The coefficient of nonlinearity γ is derived by the mathematical expression as given below [24, 25].

$$\gamma = \left(\frac{2\pi}{\lambda}\right)\left(\frac{n_2}{A_{\text{eff}}}\right) \tag{7}$$

In the expression, A_{eff} represents the effective area of the PCW, which portrays the most significant role in estimating the nonlinear property of the fibre, and n_2 relates to material's nonlinear refractive index, which is taken as 3.2×10^{-20} m^2/W.

3 Results and Interpretations

The designed structure is simulated in optiFDTD software platform, which employs FDTD computational technique to solve the Maxwell equations. The simulated structure showing the propagation of electromagnetic signal along the defect is shown in

Fig. 2. It is perceived that light is confined only in the defect area, which is mainly due to the band gap effect. As the light wave experiences band gap, the light is not allowed to enter through the circular rods and forced to move along the defect region. This type of restricted movement of light opens up many important applications. As the light is guided to the two out ports (port 1 and port 2) with feeble loss, this structure can be suitable for optical interconnect application. Figure 3 demonstrates the 3D view of light propagation along the defect region. It is viable to obtain a much stronger mode confinement in photonic crystal waveguides as compared to classical optical fibres, due to reduced effective area and the higher value of difference in indices of core and air-silica fibre cladding.

Figure 4 illustrates the dispersion relation, which shows the photonic band gap (PBG) present in the structure. The PBG is computed and analysed using plane wave expansion (PWE) band solver present in optiFDTD software package. The band gap is marked in blue colour in this figure. It is computed that the PBG exists in the wavelength range 682.38–983.14 nm and 377.23–469.97 nm. The light is restricted in the defect area due to the appearance of band gap.

To the best of our knowledge, in the earlier published articles, the nonlinearity factor has been studied only for photonic crystal fibre (PCF) structures, whereas in this article, we attempt to investigate the nonlinearity factor in photonic crystal waveguide (PCW) structure. To evaluate the nonlinearity, present in the structure, we compute the nonlinear coefficient in relation to various circular rod radius values, which is shown in Fig. 5. We varied the radius from 0.25 μm to 0.29 μm, because light is confined in the T-shaped defect region at these values of these radius range

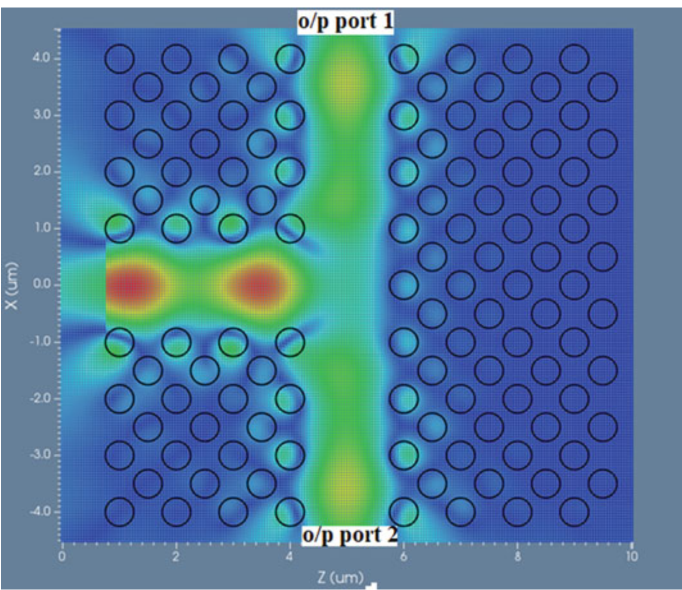

Fig. 2 FDTD simulated output

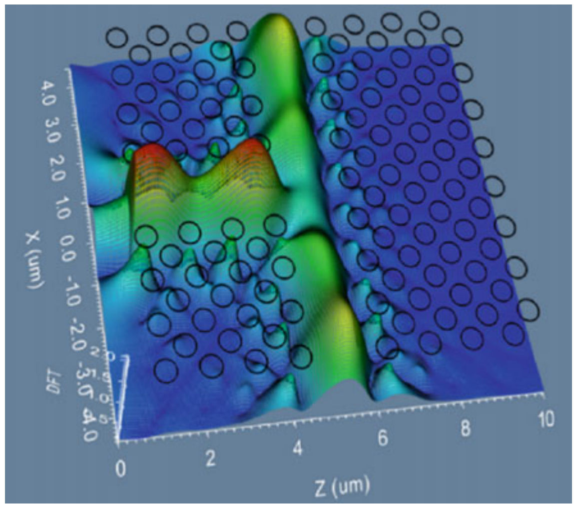

Fig. 3. 3D view of light propagation in the structure

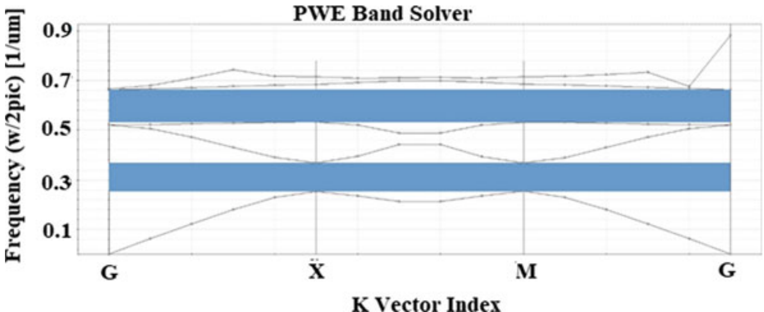

Fig. 4 Analysis of band gap in the proposed structure

only. It has been found that when circular rod radius increases, nonlinear coefficient decreases. Thus, it is concluded that radius of 0.29 nm is the optimized value, where a minimum loss perceived is $3.24 \times 10^{-6}\text{w}^{-1}\mu m^{-1}$.

Further, we computed the power at two output port of the designed T-shaped photonic crystal waveguide at different radius of circular rods, which is illustrated in Fig. 6. The power at the output port 1 is displayed along the primary vertical axis, whereas the power at output port 2 is plotted in reverse order along the secondary vertical axis. It is perceived that with an increase in the radius, the power at the output ports decreases. At a radius of 0.25 μm, a maximum power of 0.1302 mW and 0.146 mW is obtained at the output ports 1 and port 2, respectively.

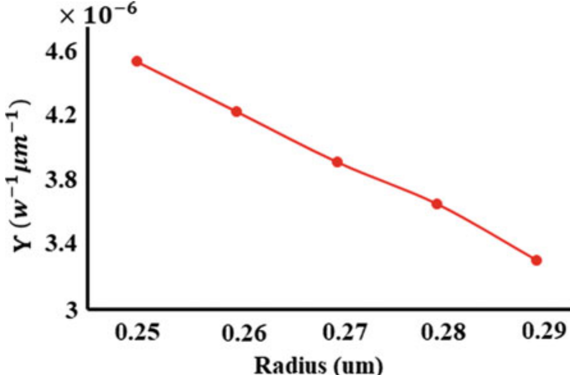

Fig. 5 Analysis of nonlinear coefficient

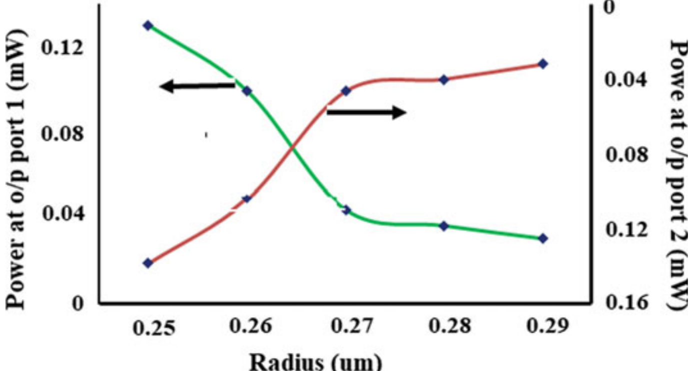

Fig. 6 Analysis of power at the output port of the proposed waveguide

4 Conclusion

In conclusion, we designed a T-shaped photonic crystal waveguide formed in a 2D PhC. The defect is created in the form of T shape. FDTD technique is employed to investigate the TE mode propagation in the defect area. The radius of the circular rods and lattice spacing is properly optimized such that the light is tightly bounded inside the defect region. Further, band gap characteristics in the structure are studied using plane wave expansion method. Apart from this, the nonlinear coefficient of the proposed structure is analysed at different radius of circular rods, and it is observed that a minimum loss of 3.24×10^{-6} $\text{w}^{-1}\mu m^{-1}$ is perceived. At last, it is concluded that a maximum power of 0.1302 mW and 0.146 mW is split at the output ports 1 and 2 of T-shaped PCW, respectively.

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Design and Realization of Logic Gates Using Double Gate Tunnel FET

Arun Kumar Sharma and Chitrakant Sahu

1 Introduction

TFETs are used in energy-efficient applications of the future because they have a good subthreshold swing [1–4]. Digital circuits have been implemented using CMOS technology for decades due to their low cost, reliability, and low power consumption [5–7]. As a result of its constant scaling, CMOS has unfavorable characteristics, such as a high leakage current [8–10]. Moreover, SS cannot be less than 60 mv/decade [2, 11]. As an alternative to CMOS, TFETs have already been recommended due to their low power consumption, high reliability, low cost, and less subthreshold swing. TFETs feature a low off current, steep SS, and are more immune to SCEs. They are also compatible with traditional CMOS, for digital applications like inverters and arithmetic circuits, In addition to that, tunnel FETs with favorable features have been presented [8, 9, 12]. Our paper presents DG-TFET with an independently biased gate. DG-TFET-based logic gates require less transistors compared to CMOS [13, 14]. It is analyzed that the device can be implemented as a two-input Boolean function by making minor alterations to TFET, such as changing the device's thickness, voltage, doping, and selecting the work function appropriately. In this article, Si-based TFET is investigated in detail. Since it is made of silicon, the level of current is lower, which is consistent with the literatures [2, 4, 15]. The basic purpose of this paper is to the realization of logic gates by making slight changes to the parameters of TFETs. The remaining sections of the paper are structured as follows. Section 2 depicts DG-TFET parameters and a simulation model, Sect. 3 shows how to implement logic gates, and

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Table 1 Simulation parameters for the device of DG-TFET-based logic gates

Parameters	OR	NAND	AND	NOR
Input voltage, $V_{DD}(V)$	0.5	0.5	0.5	0.5
t_{si} (nm)	10	10	10	10
Gate WF, ϕ (ev)	4.4	5.13	4.59	4.9
$N_D(atoms/cm^3)$	1×10^{18} (n-type)	1×10^{18} (p-type)	1×10^{18} (n-type)	1×10^{18} (p-type)
t_{ox} (nm)	2	2	2	2
Gate length (nm)	100	100	100	100
$N_S(atoms/cm^3)$	1×10^{20} (p-type)	1×10^{20} (n-type)	1×10^{20} (p-type)	1×10^{20} (n-type)
L_{ov} (nm)			20	20

Sect. 4 shows how to implement an OR gate. The rest of the section discusses how to realize NAND, AND, and NOR gates using a DG-TFET device.

2 Device Parameters and Simulation Model

Table 1 lists the DG-TFET device parameters used in the simulations and is maintained the same throughout this work. "All simulations in this investigation were carried out using Atlas Version 5.0.10 [16]." "The simulation employs the non-local BTBT tunneling model; it computes the tunneling current by taking the spatial profile of the energy bands into account." "Non-local BTBT model is utilized to investigate tunnel FETs and further shows a good match between practical and theoretical data [17–19]." The simulation also employs Fermi Dirac statistics and the Shockley–Read–Hall recombination model. The simulated results in this work have been calibrated with [15, 18, 19].

3 Implementing Logic Gates Using DG-TFET

Figure 1 states the cross-sectional view of the DG-TFET. The upper gate is indicated as V_X, lower gate as V_Y. Both logic gates are biased individually, and the source is overlapped for the AND and NOR gates. In this paper, logic 1 is represented by V_{DD} (0.5 V), and logic 0 is represented by ground (0 V). Two gates, V_X and V_Y, are used in the device. When the input logic of gates is set to the logic X and Y states, denoted by V_{XY}, the output current I_{XY}, reflects the current flowing through the device. If there is a considerable amount of current flowing through the device, the output is deemed to be logic 1, and the output is deemed to be logic 0 when the device is driven by a low current. Nonetheless, a high I_{ON}/I_{OFF} ratio is desired while realizing logic gates. For instance, in the implementation of an AND gate, the output should

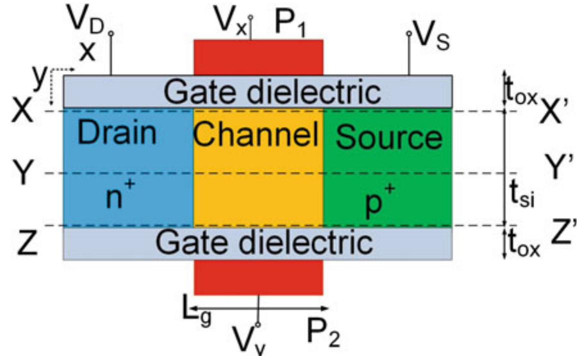

Fig. 1 Cross-sectional view of *n*-type DG-TFET to implement OR logic function

be 0 when both inputs are (00), which is $V_X = 0$ and $V_Y = 0$. In this case, an OFF current (I_{OFF}) 10^{-16} A/μm is obtained. In addition, when both $V_X = 1$ and $V_Y = 1$ input is 1 in an AND gate, an ON-state current (I_{ON}) of 10^{-8} A/μm is achieved.

4 Realization of OR Logic Gate

Figure 1 states a cross-sectional view of an n-type double gate tunnel FET. The upper gate is denoted P_1, whereas the lower gate is denoted P_2. In the DG-TFET-based logic gate design, gates are biased individually, whereas, in conventional MOSFETs, both input gates are joined to enhance the ON-state current. According to what we know about OR gates, tunneling should only take place when either one or both inputs are high. If neither input has a high logic, tunneling should not take place. Figure 2 states the energy band diagram of OR gate realization, the energy band diagram is plotted across XX' cut line, as was to be anticipated, when both gate inputs are grounded (00), no tunneling occurs between the source and channel. Furthermore, the valence band (VB) of the source gets aligned with the conduction band (CB) of the channel in each of the three remaining cases when input is 01, 10, and 11. Because of this, a significant amount of ON-state current flows, as shown by the transfer characteristics in Fig. 3a. When either one of the inputs or both is high, it is possible to obtain a high ON-state current. It is widely known as traditional Si-based tunnel FETs have low ON-state current. Thus, in order to boost the ON-state current, germanium concentration is added to silicon on the source side. For OR gates functionality, it is investigated how much Ge may be incorporated into silicon without compromising functionality. The results in Fig. 3b show that $\mathrm{Si}_{1-x}\,\mathrm{ge}_x$ (x = 0.5) is an appropriate compound without losing functionality. By adding $x = 0.5$ Ge, the ON-state current is raised almost one order of magnitude, from 2.93×10^{-7} A/μm to 3.88×10^{-6} A/μm.

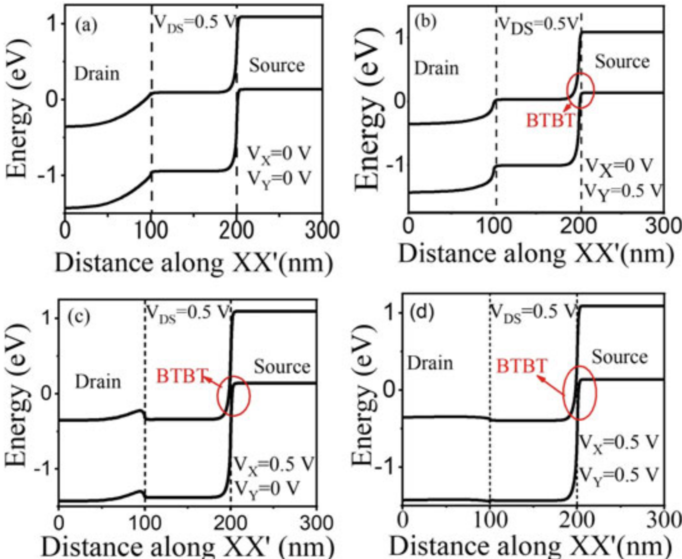

Fig. 2 Band diagram to implement OR function using double gate tunnel FET, across X-axis: "**a** 00, **b** 01, **c** 10, **d** 11," logic inputs

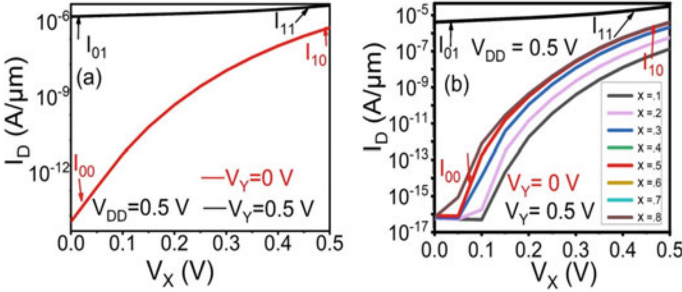

Fig. 3 Transfer characteristics for OR function: **a** Si-based TFET, **b** Si-Ge-based TFET

5 Realization of NAND Logic Gate

Figure 4 states the cross-sectional diagram of DG-TFET for implementing NAND gate. To the realization of the NAND gate, when at least one of the inputs is 0, the output will be 1 or high. P-type DG-tunnel FET is able to realize this functionality. Figure 5 states an energy band diagram across the device length for input logic combinations considering two inputs. BTBT is only allowed when the gate input is 00, 01, or 10, and no tunneling is observed when gate input is at logic 11, and also from Fig. 6, it is noticed that high I_{ON} state current is received in case when gate

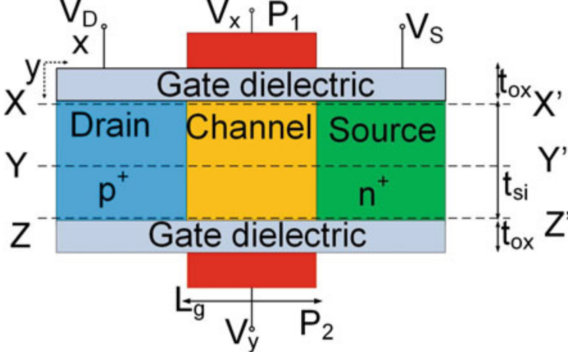

Fig. 4 Cross-sectional view of p-type DG-TFET to implement NAND logic function

input is logic 00, 01, 10 and the device is tuned to OFF-state for input 11. It is also analyzed that a good I_{ON}/I_{OFF} ratio is obtained, which is about 10^{10}.

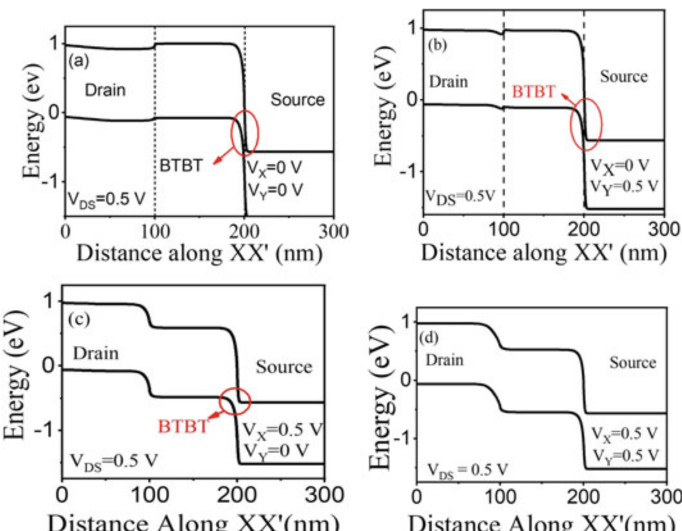

Fig. 5 Band diagram to implement NAND function using double gate tunnel FET, across X-axis "**a** 00, **b** 01, **c** 10, **d** 11," logic inputs

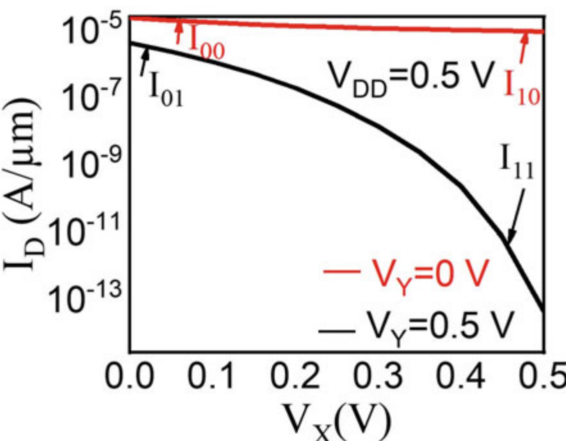

Fig. 6 Transfer characteristics for NAND function

6 Realization of AND Logic Gate

If both gates inputs are at high logic, BTBT should occur to implement AND logic gate. It has already been observed that to realize the OR gate, the BTBT must take place for input combinations of "01," "10," and "11," and BTBT ceases to exist for the input logic combination of 00. "The AND gate is realized using gate-source overlapped n-type DG-TFET such that the BTBT ceases to take place for input logic combinations with at least one of the inputs going low due to misalignment of energy bands [13]." Figure 7 states the energy band structure of double gate tunnel FET without gate-source overlapping and can be seen When a high input is given to both gates, body tunneling takes place along YY'; otherwise, BTBT takes place just near the surface of the gate along the XX' and ZZ' cutlines. In the instance of 01,10, only surface tunneling takes place; hence, if one were to prevent surface tunneling, the device would function as an AND gate. Due to that combination of "01" and "10" is investigated in detail. Figure 8 indicates that the band alignment is changed due to the addition of gate-source overlap, and tunneling of electrons is prevented in cases 01 and 10. This is because the band alignment has been changed. When no overlap exists $L_{ov} = 0$ nm, high OFF-state current (10^{-9} A/μm) flows through the device because the tunneling width is relatively low. When the amount of overlapping is increased to $L_{ov} = 10$ nm, there is an increase in barrier width at the junction between the VB (valence band) of the gate and CB (conduction band) of the channel.

Due to this, a low amount of OFF-state current flow, (10^{-14} A/μm) through the device. The tunneling width at the junction was raised by raising the gate-source overlapping, which led to a decrease in BTBT and, consequently, no current flow at the 01 and 10 inputs. Because an increase in source overlapping greater than $L_{ov} = 20$ nm does not influence the drain current; therefore, $L_{ov} = 20$ nm is selected to achieve the desired output. Figure 9 states the structure of the double gate TFET used to realize an AND gate. Figure 10 shows the band diagram across the device

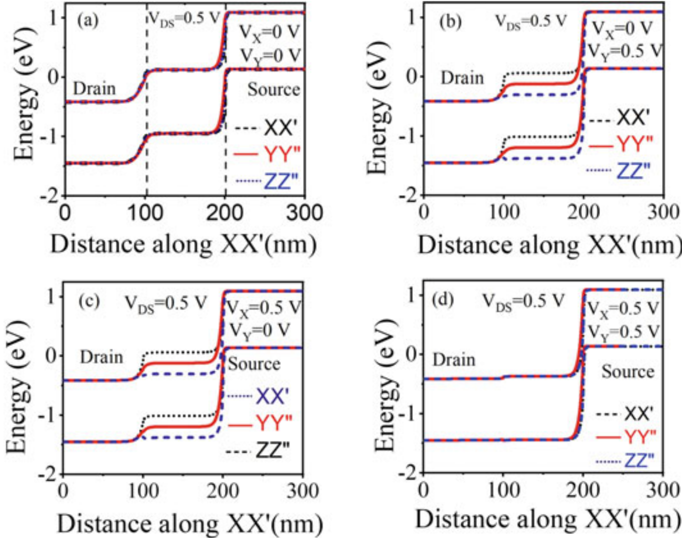

Fig. 7 Band diagram with no gate-source overlap at various cut line XX',YY', and ZZ' "**a** 00, **b** 01, **c** 10, **d** 11" logic inputs

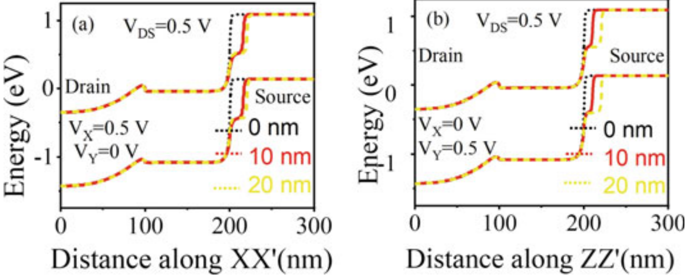

Fig. 8 Band structure to implement AND function using double gate tunnel FET, across X-axis along variable gate-source overlap for logic inputs: **a** 10, **b** 01

lengths XX', YY', and ZZ'. It is observed that when both inputs are high, tunneling of electrons is enabled, and for other logic combinations, band-to-band tunneling is prevented. Table 1 shows a list of all the device parameters which is used in the simulation. Transfer characteristics to realize an AND gate are shown in Fig. 11. When both gate inputs are set to high, a high ON-state current (10^{-8} A/μm) is achieved, and I_{ON}/I_{OFF} ratio 10^6 can be seen at input voltage $V_{DD} = 0.5$ V. Since the working of the AND gate requires source-gate overlapping for the 01 and 10 logic states. In the context of this, it is essential to analyze the thickness of the silicon. Figure 12 indicates that as we raise t_{si}, tunneling width at the junction also increases. Consequently, body tunneling decreases, and less current flows through the device because the impact of gate biasing on the silicon body becomes weaker, and the I_{ON}/

I_{OFF} ratio decreases. So, while implementing an AND gate, a high t_{si} is not favored. Because tunneling ceases in the case of a 01 and 10 due to the silicon body thickness; hence, $t_{si} = 10$ nm is chosen for AND gate implementation to achieve the desired output.

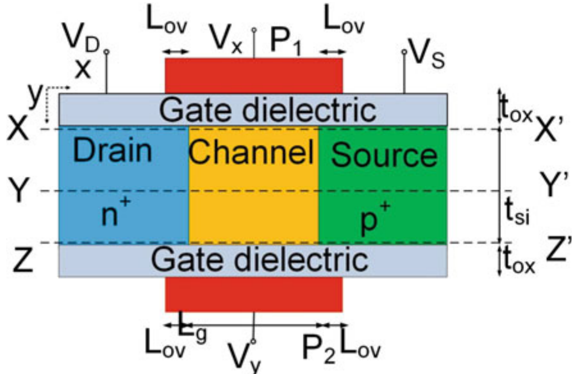

Fig. 9 Cross-sectional view of n-type DG-TFET to implement AND logic function

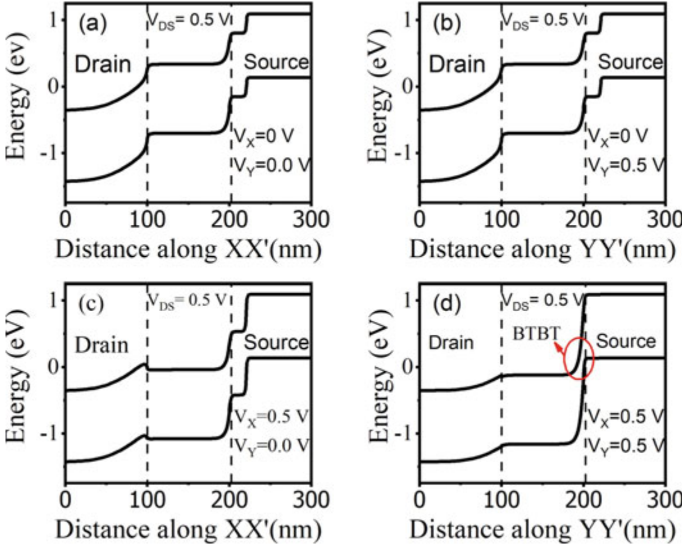

Fig. 10 Band diagram to implement AND function using double gate tunnel FET, across X-axis "**a** 00, **b** 01, **c** 10, **d** 11," logic inputs

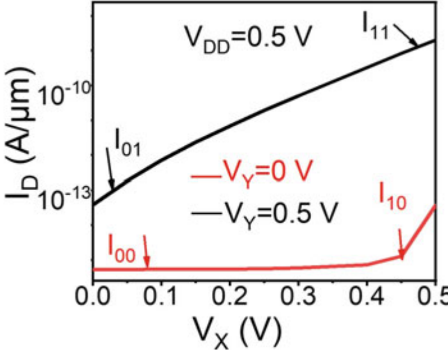

Fig. 11 Transfer characteristics for AND function

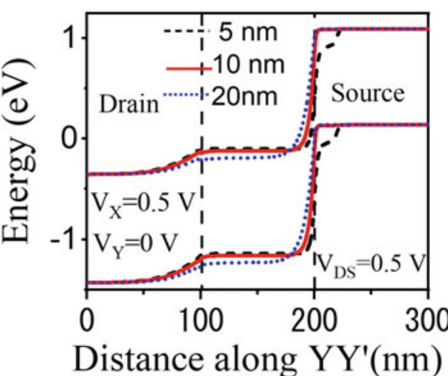

Fig. 12 Band structure for AND logic when V_{DS} is 0.5 V at variable t_{si} for input "11" across X-axis

7 Realization of NOR Logic Gate

For the realization of the NOR gate, BTBT occurs if both the inputs are 00. To cease the tunneling of charge carriers when one of the inputs is high, gate-source overlapping in P-type double gate TFET is used. In Fig. 13, the cross-sectional view for a p-type DG-tunnel FET is shown. The parameters utilized in the simulation are given in Table 1. The band diagram to realize NOR gate is stated in Fig. 14. Figure 14a indicates the band diagram across with the length YY' for 00 input combination where BTBT is enabled, and for other logic combinations, the BTBT does not take place. The transfer characteristics for the realization of NOR gate are stated in Fig. 15, ON-state current (10^{-7} A/μm) is achieved when both gate inputs are low (00), and OFF-state current (10^{-12} A/μm) flows through the device channel for logic combinations other than logic 00.

Performance metrics of implemented double gate tunnel FET are shown in Table 2. "The effect drives current method is used to determine the delay in [20]." The intrinsic delay of the proposed device is very high due to low ON-state current primarily due to the low mobility of silicon besides low ON-state current C_{GD} is also

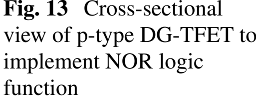

Fig. 13 Cross-sectional view of p-type DG-TFET to implement NOR logic function

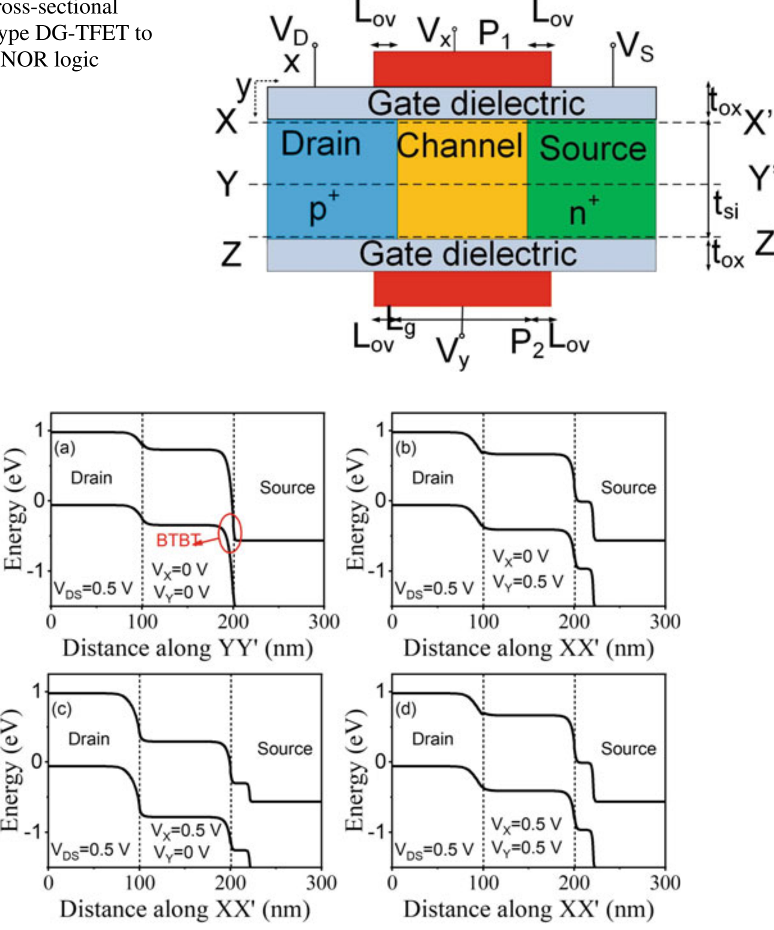

Fig. 14 Band diagram to implement NOR function using double gate tunnel FET, across X-axis "**a** 00, **b** 01, **c** 10, **d** 11," logic inputs

Fig. 15 Transfer characteristics for NOR function

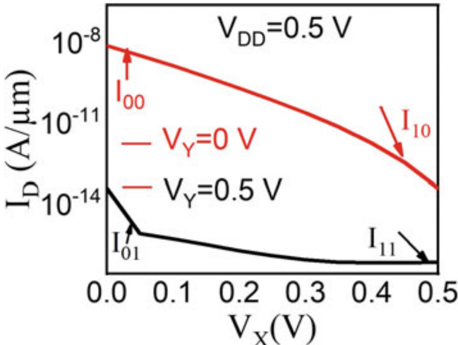

Table 2 Performance metrics of implemented double gate tunnel FET

Function	$V_{DD}(V)$	$I_{ON}(A/\mu m)$	(I_{ON}/I_{OFF})	$C_{gg}(fF/\mu m)$	Delay (ns)
OR	0.5	3.55×10^{-7}	10^{10}	0.96	3.5
NAND	0.5	5.14×10^{-6}	10^{10}	0.96	34
AND	0.5	1.4×10^{-8}	10^{6}	0.63	66
NOR	0.5	2.04×10^{-7}	10^{5}	0.77	166

high. "However, different techniques that include lower bandgap source material, pocket doping, and vertical channel can be used to enhance the ON-state current" [10]. In AND, NOR gate delay is very high as compared to OR and NAND gates because gate and source are overlapped, which further increases C_{GS} and reduces the ON-state current.

Delay is calculated as:

$$\tau_d = \frac{C_{gg} \times V_{DD}}{I_{eff}} \tag{1}$$

I_{eff} is the effective drive current and C_{gg} is total capacitance

$$I_{eff} = \frac{I_H + I_L}{2} \tag{2}$$

I_L is the drain current at $V_{DS} = V_{DD}$, $V_{GS} = V_{DD/2}$, and I_H is the drain current at $V_{DS} = V_{DD/2}$, while $V_{GS} = V_{DD}$.

8 Conclusion

In this article, logic gates OR, NAND, AND, and NOR have been implemented using DG-TFET. The OR gate is realized by an n-type double gate TFET, and by using a P-type double gate, the TFET NAND gate is realized. AND and NOR gates are realized by overlapping of gate-source and choosing the appropriate silicon body thickness. Simulations indicate that the ON-state current is low, and it is generally known that silicon-based TFET devices have a low ON-state current. To increase the ON-state current, $Si_{0.5}Ge_{0.5}$-based TFET is analyzed for OR gate functionality, which shows the ON-state current is raised by almost one order of magnitude. I_{ON} improves from 2.93×10^{-7} A/μm to 3.88×10^{-6} A/μm. Further, Si-Ge-based TFET can be analyzed in detail for other logic gate functionality to increase ON-state current.

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Investigation of Device and Circuit-Level Performances of Dielectric Engineered Dopingless SOI Schottky Barrier MOSFET

Arnab Som and Sanjay Kumar Jana

1 Introduction

Scaling is the most difficult issue for standard CMOS structures in the semiconductor industry. The offensive physical scaling creates numerous challenges, including decreased gate control over the channel, increased gate oxide leakage, and the manifestation of short-channel effects (SCEs) [1]. However, current semiconductor industrial trends focus on low power, low cost, small area, and great performance. This drives the development of novel MOSFET architectures for extremely small dimensions. Schottky barrier MOSFETs are one of the potential candidates to fulfill the industry requirements. It provides numerous benefits, such as an atomically abrupt junction, better control to SCEs, and ease of fabrication [2, 3]. It also offers long-term scalability, no physical doping requirements, and a minimal thermal budget. Regardless of their various benefits, SB-MOSFETs have a high OFF state current due to ambipolar behavior [4–7]. SB-MOSFETs can operate with both negative and positive gate bias. The ambipolar behavior restricts the device's usability in digital circuit applications. As a result, the device's digital operating performance deteriorated. Several works have recently been reported to reduce ambipolar current. Ghoneim et al. first proposed an extra oxide layer in the middle of the metal source/drain regions and the semiconductor interface [8]. Few researchers employed field-induced drain extension between the semiconductor interface and drain regions [9, 10]. Recessed channel design with asymmetric S/D connections was reported to reduce the ambipolar behavior by Zhang [11]. Researchers have proposed different architectures such as underlap gate structure near the drain end [6] and using

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of two asymmetric isolated gates to minimize ambipolar behavior [7]. Recently, Kale et al. [12] reported the dual material gate SB-MOSFET for the reduction of ambipolar current. However, the previously described published methods to reduce the ambipolar current have a number of limitations such as random dopant variations, fabrication complexities, etc. Furthermore, the creation of drain extensions can reduce ambipolar behavior, but it leads to restricted tunability and pitch scaling [13]. So more investigations on ambipolar current suppression and the analysis of its effects on switching performances are required for the Schottky barrier devices.

Another disadvantage of metal source/drain MOS devices is that they exhibit poor ON state performance because of the metal–semiconductor Schottky barrier junction. For source/drain MOS devices, zero Schottky barrier height is essential for achieving improved performance. Few researchers have reported a few structures where the dopant segregation layer (DSL) has been employed in SB-MOSFETs to improve ON current performance by lowering the Schottky barrier height [14]. However, achieving a doped DSL is challenging since it enhances manufacturing complexity and the thermal budget [15–18]. To overcome these difficulties, several device structures like source engineered [19], electrostatically doped DSL SB-MOSFET [20], and floating gate SB-MOSFET [21] have been demonstrated. However, the ON state performance and the subthreshold slope is still needed to be improved for better switching performance.

To address the above-mentioned issues, we have presented a dielectric engineered charge plasma-based Schottky barrier SOI MOSFET where source and drain regions are made by NiSi. To improve the ambipolar behavior, the gate dielectric engineering has been performed. The length of SiO_2 at the drain side has been optimized to decrease the tunneling distance for hole injection near the drain side. Furthermore, to investigate the impact of device-level performance improvements in circuit level, Verilog-A model-based N-MOS inverters of the DE-SOI-SB-MOSFET and conventional SOI SB-MOSFET are developed and simulated in Cadence Virtuoso Tool. The key figure of merits in circuit level like PDP has been analyzed, which has not been reported in earlier published works.

This article is arranged as follows. Different device architectures and different simulation input parameters are discussed in Sect. 2. Several results are analyzed in Sect. 3 where DC, RF, and circuit-level performances are mainly investigated. The conclusion part is described in Sect. 4.

2 Structures of Devices and the Parameters Used for Simulations

The device structures of conventional SOI SB-MOSFET and proposed DE-SOI-SB-MOSFET are presented at Fig. 1.The parameters related to device design are shown in Table 1.

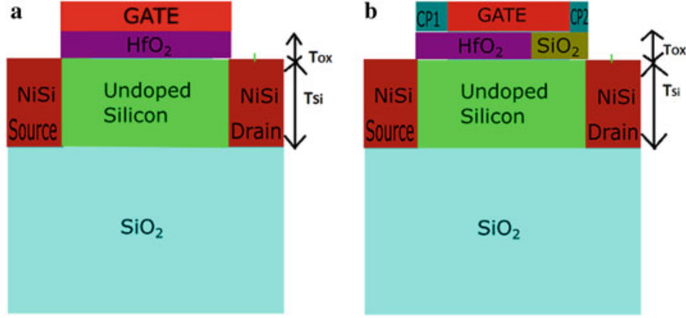

Fig.1 Device structures of **a** conventional SOI SB-MOSFET, **b** proposed DE-SOI-SB-MOSFET

Table 1 Device design parameters

Parameters	DE-SOI-SB-MOSFET	Conventional SOI SB-MOSFET
Channel length (nm)	30	30
Source/Drain length (nm)	10	10
Silicon film thickness (nm)	10	10
Thickness of gate oxide (nm)	2	2
Gate oxide material	$HfO_2 + SiO_2$	HfO_2
Channel doping (cm^{-3})	10^{15}	10^{15}
Source and drain work function	4.85 eV (NiSi)	4.85 eV (NiSi)
Work function of gate	4.45 eV	4.45 eV
Oxide thickness below Si substrate (T_{BOX}) (nm)	45	45

The silicon thickness is considered as 10 nm. The gate oxide thickness is chosen as 2 nm. The WF of the gate metal is considered as 4.45 eV. The length of channel is considered as 30 nm for all devices. The electron SBH of NiSi is considered as 0.65 eV, and hole SBH is considered as 0.47 eV [3]. The channel doping is considered as 10^{15} cm^{-3}. For conventional SOI Schottky barrier MOSFET, one gate dielectric (HfO_2) is used. The width of CP1 is considered as 3 nm, and the width of CP2 is considered as 2 nm for the proposed DE-SOI-SB-MOSFET. The work function of CP2 is considered 3.7 eV (Hafnium). To realize the charge plasma concept, the silicon film thickness is considered as less than the length of debye length (LD) [22]. The metal work functions (CP1 and CP2) near the source and drain side considered in the range of less than (χ_{Si} + Eg/2), where χ_{Si} denotes the electron affinity and Eg denotes the bandgap of the silicon material [22].

The simulations of all the devices have been performed by Silvaco ATLAS [23]. To include the effects of tunneling across the metal–semiconductor junctions, the universal Schottky tunneling model (UST) is used [19]. Two different motility models, field-dependent mobility and concentration-dependent mobility, have been

incorporated in the simulation. The other different models used in the simulations are the band gap narrowing model and Shockley–Read–Hall recombination model. For accurate calibration, the device structures with all parameters and dimensions are kept the same as published in [24]. A good similarity between the experimental I_D-V_{GS} characteristics and simulated characteristics is seen in Fig. 2(a). In this simulation, the electron effective mass is considered as 0.36, and hole effective mass is considered as 0.26 [19]. The other constant values like effective Richardson's constant of holes are considered as 30 A/K-cm^2, and effective Richardson's constant of electrons is considered as 110 A/K-cm^2 [19].

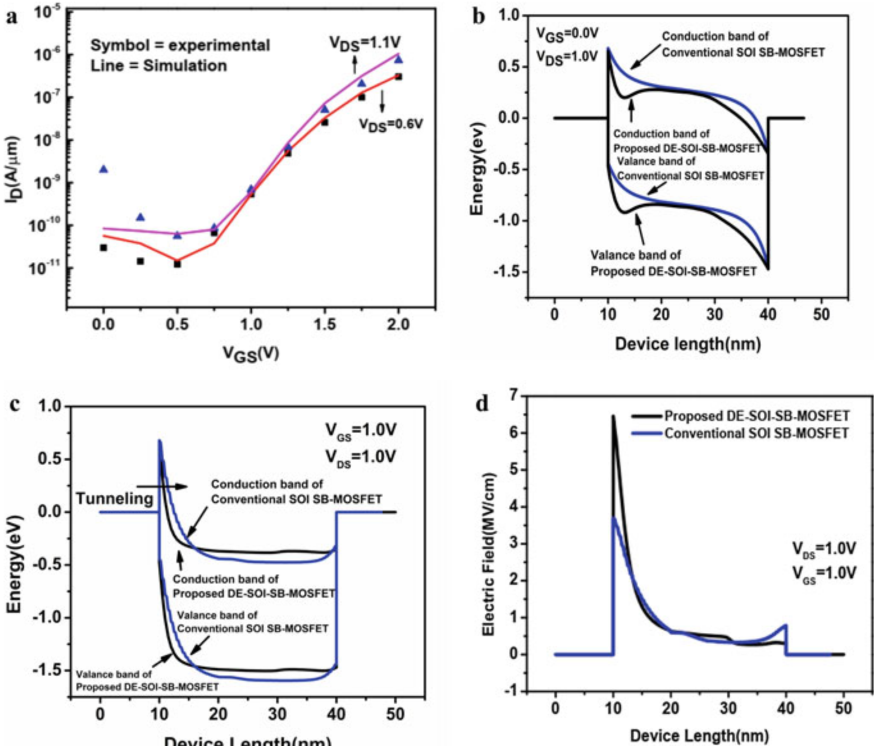

Fig. 2 **a** Calibration of I_D-V_{GS} characteristics against the experimental data [24]. **b** Plot of E-B diagrams for SOI SB-MOSFET and DE-SOI-SB-MOSFET under OFF state. **c** Plot of E-B diagrams for SOI SB-MOSFET and DE-SOI-SB-MOSFET under ON state. **d** Plot of electric field distribution for SOI SB-MOSFET and DE-SOI-SB-MOSFET

3 Results and Discussions

Figure 2b and c indicates the energy band diagrams for both the devices. Figure 2b indicates that the probability of electron injection from the source metal to the channel region is very minimal due to wider energy barrier present at the source-channel junction under OFF state condition (gate voltage = 0.0 V and drain voltage = 1.0 V). Figure 2c indicates the thinner barrier width caused by charge plasma for the proposed DE-SOI-SB-MOSFET under ON state condition (Gate Voltage = 1.0 V and Drain Voltage = 1.0 V). Under ON condition, in the presence of positive gate voltage, larger Schottky barrier thinning causes more tunneling of electrons from the source metal to Si channel region for the proposed DE-SOI-SB-MOSFET. The thinner Schottky barrier in the DE-SOI-SB-MOSFET causes the improved ON state current.

Figure 2d indicates that the proposed DE-SOI-SB-MOSFET shows enhanced electric field near the source-channel interface region than the conventional SOI SB-MOSFET. The gate engineering-induced charge plasma is the reason for the improved electric field for the proposed device. Figure 3a indicates the tunneling rate under ON state with respect to device length for both the conventional SOI SB-MOSFET and the DE-SOI-SB-MOSFET. The enhanced electric field across the source-channel junction induces the larger tunneling rate for the proposed DE-SOI-SB-MOSFET. Figure 3b indicates the electron concentration variations of both the devices. The result shows larger carrier concentration for the proposed DE-SOI-SB-MOSFET. CP1 and CP2-induced charge plasma contributes lager carrier concentration at source end and drain end for the proposed device.

The OFF current variation (Fig. 3c) of the proposed device shows that L_{HfO2} can be either 20 nm or 25 nm to get the better OFF state response. For this reason, the length of the gate dielectric (SiO_2) with low-k dielectric near the drain side is varied from 0 to 10 nm. Figure 3d shows that ambipolar current decreases significantly with the increasing L_{SiO2} of the proposed device while ON current remains same. The reason for that reduction of ambipolar current is presented in Fig. 4a. It has been noticed that as the L_{SiO2} increases, the edge of valance band at drain side widens and the tunneling distance for hole tunneling at the drain side reduces. Due to the above-mentioned reason, the hole tunneling current reduces at drain side and that reduces the ambipolar current.

To enhance the I_{ON}, the work function of CP1 has been varied from 3.5 to 4.1 eV, while L_{SiO2} is kept fixed at 10 nm. The result (Fig. 4b) shows that at 3.5 eV, the proposed CP-based DE-SOI-SB-MOSFET shows maximum ON current where ambipolar current remains same. The reduction of tunneling width is the reason for the ON current improvement of the DE-SOI-SB-MOSFET. Figure 5a indicates that when the WF of the CP1 reduces, the tunneling width of the conduction band decreases. As a result, drain current increases. At 3.5 eV, the drain current reaches maximum value. The improved I_{ON} in the proposed DE-SOI-SB-MOSFET (348 μA/μm) compared to the conventional SOI SB-MOSFET (42 μA/μm) is mainly due to charge plasma-induced n + pockets near drain and source end regions of channel.

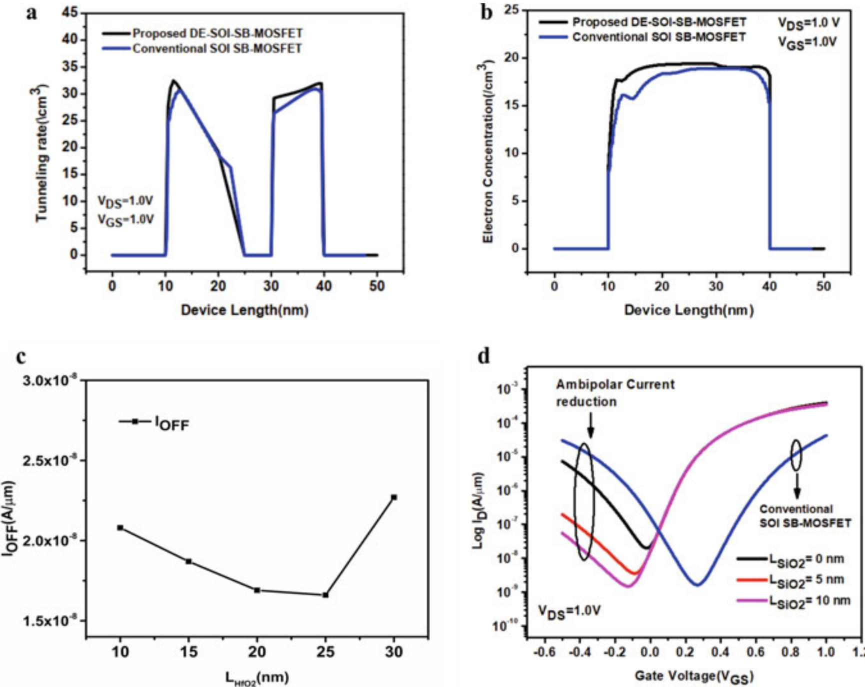

Fig. 3 **a** Plot of tunneling rate for the SOI SB-MOSFET and DE-SOI-SB-MOSFET. **b** Plot of electron concentrations for the SOI SB-MOSFET and DE-SOI-SB-MOSFET. **c** Plot of I_{OFF} variations for different values of L_{HfO2} of the DE-SOI-SB-MOSFET. **d** Drain characteristics for the SOI SB-MOSFET and DE-SOI-SB-MOSFET with different L_{SiO2}(0–10 nm) of the DE-SOI-SB-MOSFET

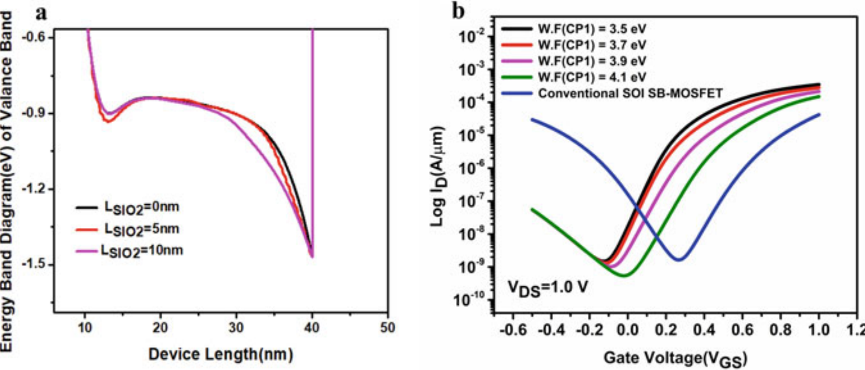

Fig. 4 **a** Plot of valance band diagram under OFF state condition of the DE-SOI-SB-MOSFET for different L_{SiO2}. **b** Drain characteristics for the SOI SB-MOSFET and DE-SOI-SB-MOSFET with different work functions of CP1 of DE-SOI-SB-MOSFET

Figure 5b shows that the peak value of g_m enhances from 4.18×10^{-4}S/μm at WF (CP1) = 4.1 eV to 5.9×10^{-4}S/μm at WF (CP1) = 3.5 eV. The proposed device with 3.5 eV work function of CP1 exhibits the highest transconductance peak and that is due to I_{ON} improvement which can be credited to the thinning of tunneling width across the source-channel junction. The cut-off frequency is the most crucial performance parameter for high-frequency low-power devices. The cut-off frequency is defined as

$$f_T = g_m/(2\pi C_{gg}) \tag{1}$$

The result shows that the proposed DE-SOI-SB-MOSFET provides larger cut-off frequency than the conventional SOI SB-MOSFET. Figure 5c shows that f_T increases significantly with the decreasing WF (CP1) of the DE-SOI-SB-MOSFET. The enhanced transconductance in the proposed device causes improved f_T. Gain bandwidth product (GBP) is the important performance parameter for high-frequency applications. The GBP is defined as

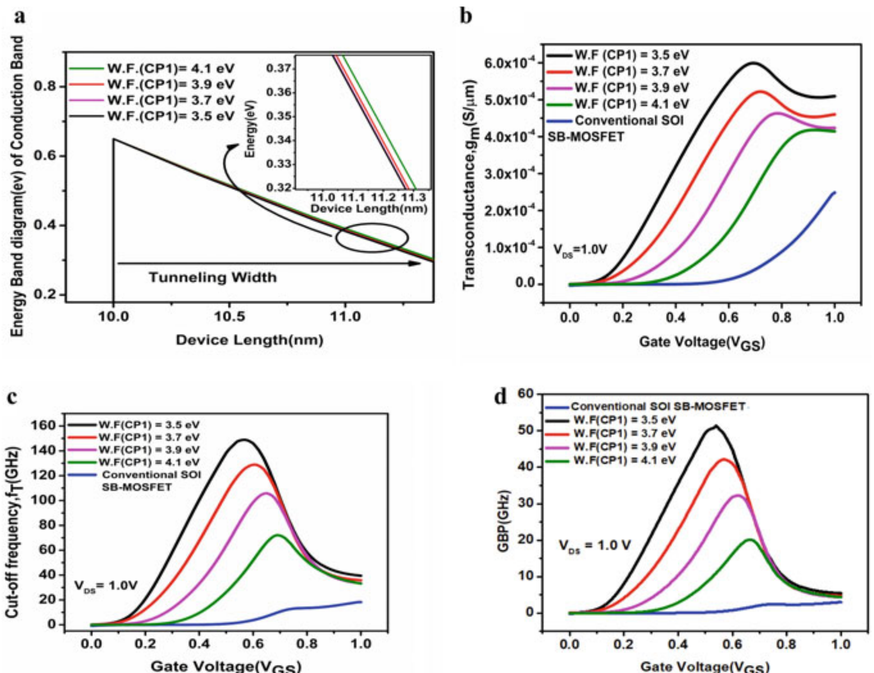

Fig. 5 **a** Plot of conduction band diagram under ON state condition of the DE-SOI-SB-MOSFET for different work functions of CP1. **b** Plot of transconductance with respect to V_{GS} for the SOI SB-MOSFET and DE-SOI-SB-MOSFET with different work functions of CP1 of proposed device. **c** Plot of cut-off frequency with respect to V_{GS} for conventional SOI SB-MOSFET and DE-SOI-SB-MOSFET for various work functions of CP1 of proposed device. **d** Plot of GBP for the SOI SB-MOSFET and DE-SOI-SB-MOSFET for various work functions of CP1 of proposed device

Table 2 Comparison of the device performances

Ref	Applied Voltage(V_{DS}/V_{GS})	Channel length (nm)	I_{ON} (μA/μm)	SS (mV/dec)	f_T (GHz)
[3]	1/1	40	1100	61.7	–
[14]	0.6/1.4	20	2380	96.5	
[14]	0.6/1.4	20	2040	93.3	
[21]	0.5/0.5	20	123.1	83.34	198.8
This work	1/1	30	348	78	149

$$\mathrm{GBP} = g_m/(2\pi 10 C_{\mathrm{gd}}) \tag{2}$$

Figure 5d shows that GBP increases significantly with the decreasing WF (CP1) of the proposed device. Improved current driving capability due to charge plasma-based *n*+ pockets in the proposed DE-SOI-SB-MOSFET causes improved GBP. The device performances have been compared with other reported works at Table 2.The proposed DE-SOI-SB-MOSFET shows better subthreshold slope, and it can be suitable for digital circuit applications.

The circuit-level behavior has been investigated by simulating N-MOS inverters using the conventional SOI SB-MOSFET and DE-SOI-SB-MOSFET. Figure 6a shows simulation framework of TCAD (Silvaco) and Cadence Virtuoso [25]. Figure 6c indicates the comparison of the transient behaviors of two different device-based inverters. Same design parameters have been used for both the device-based circuits. 0.5 V is used as the supply voltage. The DC offset of 0 V is used with the input signal. The pulsed value of 0.5 V, rise time and fall time of 10 ps each, and pulse period of 10 ps have been used in the input of the simulation. To investigate the circuit behavior at high frequency, 100 GHz has been applied as input frequency. To get a clear view of the propagation delay generated by the N-MOS inverters, we calculated the total average delay = [$0.5 \times (\tau_{PLH} + \tau_{PHL})$]. The transient behavior shows that the proposed DE-SOI-SB-MOSFET (42 ps) provides 60 times better result in average delay than conventional SOI SB-MOSFET(2573 ps). An important figure of merit of circuit perspective is the power delay product (PDP). The proposed device-based circuit (1.48 aJ) offers 36% improvement in PDP (Fig. 6d) than the conventional device-based circuit (2.31 aJ). Improved switching performance for the DE-SOI-SB-MOSFET-based circuit can be contributed to the charge plasma-induced higher current driving capability. Transient analysis and power delay product analysis indicate that the DE-SOI-SB-MOSFET is suitable for high-speed circuit applications.

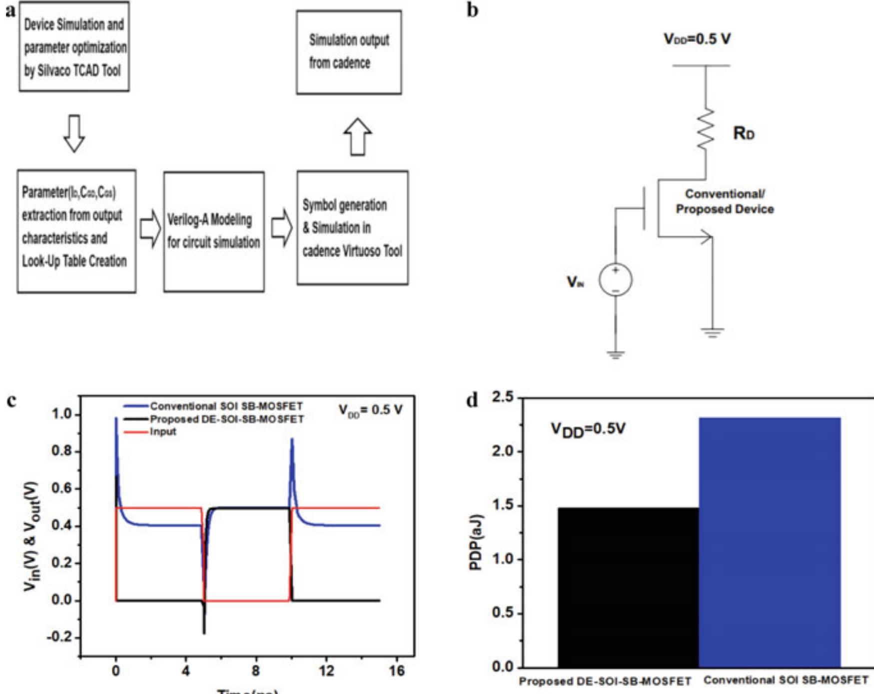

Fig. 6 **a** Simulation framework of TCAD (Silvaco) and Cadence Virtuoso. **b** N-MOS inverter with resistive load of 500KΩ. **c** Plot of transient analysis for the SOI SB-MOSFET and DE-SOI-SB-MOSFET. **d** Plot of PDP for the SOI SB-MOSFET and DE-SOI-SB-MOSFET

4 Conclusion

A precise investigation is made to study the impact of dielectric engineering and gate work function engineering on device and circuit-level performances for the SOI SB-MOSFET devices. The gate work function engineering on the source side charge plasma improves the overall ON state performances of the proposed DE-SOI-SB-MOSFET. It is noticed that the work function engineering of source end metal electrode lowers the tunneling barrier width and enhances the tunneling rate; hence it improves the ON current and the analog/RF performances. The dielectric engineering at the drain end improves the ambipolar behavior of the DE-SOI-SB-MOSFET. Furthermore, the transient analysis shows that the DE-SOI-SB-MOSFET is suitable for low-power high-speed radio frequency applications. In addition to that, fabrication obstacles such as random dopant fluctuations and complexity issues in doping are not present, as the DSL has been created by the gate work function engineering.

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Impact of Dual Gate Material on Performance in Armchair Graphene Nanoribbon Vertical TFET of 1.35 nm Widths

Zohmingliana, Bijit Choudhuri, and Brinda Bhowmick

1 Introduction

The tunnel field-effect transistor (TFET) is quite interesting due to the unique conducting mechanism of band-to-band quantum tunneling that overcomes the thermionic emission of carriers. The advantage of TFET devices has been explored over conventional MOSFETs with exceptional performance at minimal operating voltage situations. TFETs manifest a magnificent low leakage current and an excellent average subthreshold swing (SS_{Avg}). Therefore, it is continuously examined to replace the MOSFETs for low-power devices in the future [1, 2]. Nevertheless, TFETs undergo low ON-state current problems; hence, several techniques have been encouraged by the researcher to enhance the ON-current [3–5]. Besides the device geometry engineering option, lower band gap material significantly improves carriers' tunneling probability [5, 6]. This article has studied the impact of two gate materials at the source and drain sides on the behavior in AGNR DG-VTFET. The device's overall performance, like ON-state current, current leakage, I_{ON}/I_{OFF} current ratio, threshold voltage, and average subthreshold swing, can be optimized by work function engineering [7–9]. However, TFET device is still struggling to explore them in matter-of-fact applications.

It has already been discussed in the other reported works that conventional TFET is facing a challenge in the low ON-state current [3, 4, 10, 11]. The ON-current of conventional DGTFET cannot it bring up to the MOSFET level by only the dual material gate (DMG) technique. Hence, a two-dimensional material with a low band gap and high carrier mobility is introduced in the device's channel region, which inclines the TFET performance [12, 13]. In recent years, two-dimensional materials such as carbon allotropes of carbon nanotubes (CNT) and graphene nanoribbons (GNR) have

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dramatically improved the device's performance. Therefore, we proposed the TFET structure, composed of DMG and a double gate (DG), and includes the benefit of excellent graphene nanoribbon (GNR), so that the performance is acceptable for the practical application. In [4, 14], the impact of high κ dielectric gate material has been depicted, and it enhances the coupling between the tunnel and gate junction, leading to the advancement of device performance. Hence, we employed the interest of high κ dielectric material in our proposed structure to attain high I_{ON} and low average SS and boost the comprehensive achievement. Finally, the TFET is considered to have the potential to work at low power so it can be operated at the drain bias $V_{DS} = 0.5$ V [10].

The remaining part of this letter is arranged in this manner: Sect. 2 demonstrates the proposed device's architecture and dimension and the physics model employed in this investigation. In Sect. 3, detailed analyses have been discussed due to the impact of a two-material gate in the proposed TFET to enhance performance. The finding and results obtained are concluded in the Sect. 4.

2 Device Description and Methodology

The two-dimensional schematic perspective and parameters of the proposed Dual Material Gate Armchair Graphene Nanoribbon DG-VTFET (DMG-AGNR-DG-VTFET) are illustrated in Fig. 1. To improve the results, double-sided gate control has been employed to control the channel better. Both the gate material has two different electrodes with distinct work function (Φ). The electrode to adjacent the source-channel junction is named the tunnel gate (Φ_{Tun}), and the other closest to the drain junction is assigned as the auxiliary gate (Φ_{Aux}). In order to control the gate current leakage, high κ material HfO_2 ($\kappa = 22$) having an oxide thickness 3 nm has been employed in the simulation. An abrupt doping profile is taken for source, drain, and channel doping through the simulation. The doping parameter is as follows: drain doping = 1×10^{20} cm^{-3}, channel doping = 1×10^{18} cm^{-3}, and source doping = 5×10^{17} cm^{-3}. Two-dimensional material of Graphene Nanoribbon (GNR) is used in the channel region instead of conventional silicon material due to the unique and fascinating intrinsic properties of the 2D crystal. GNR is classified into two types based on their chirality: zigzag GNR (Z-GNR) and armchair GNR (AGNR). Z-GNR has metallic (conductor) conducting properties. At the same time, AGNR is familiar with having semiconductor character, energy band gap depending on the width of the ribbon, and band gap is inversely proportional to the width [15]. Armchair Graphene Nanoribbon (AGNR) of 50 nm length is used in the channel region, which has carbon $N = 12$ dimers belonging to the $n = 3p + 1$ family where p is a positive integer. The width of AGNR used in the proposed device is 1.35 nm, corresponding to the band gap of AGNR of approximately 0.7 eV. A schematic sketch of an armchair GNR having edge dimers $N = 12$ is shown on the left side of Fig. 1a. The energy band gap-width relation of GNR is used from [16] for the $3p + 1$ family as follows:

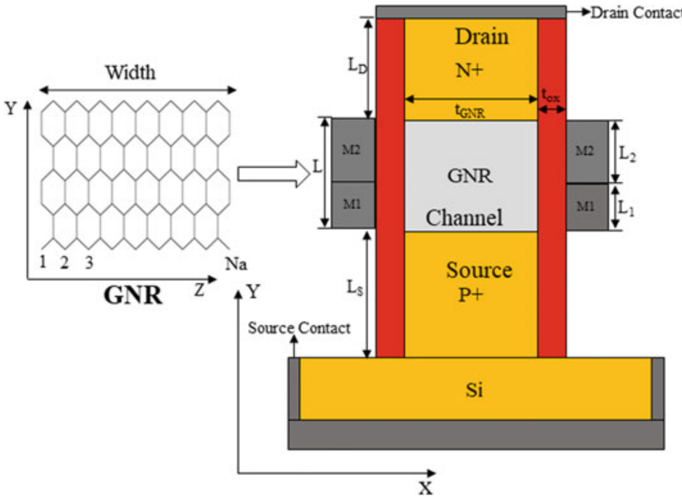

Fig. 1 Schematic cross section of dual material gate-armchair-GNR-DG-vertical TFET

$$E_G = \frac{1.04\ \text{eV}}{W(\text{nm})} \tag{1}$$

$$W(\text{nm}) = \frac{0.236}{2}(N-1) \tag{2}$$

where N represents the number of carbon dimers in the AGNR. The device is operated at a low power supply; drain-source voltage (V_{DS}) and gate-source voltage are set to 0.5 V and 1 V, respectively. The whole simulation uses the Silvaco 2D Atlas tools [17].

The simulation incorporates the following physics models: BBT.NONLOCAL to compute the tunnel occurring at the bands [17], and to examine how temperature and impurities affect the lifetime of electrons, the simulation includes the Shockey-Reed-Hall recombination model (SRH) [17] is integrated into the simulation. In addition, the concentration-mobility model (CONMOB) and band gap-narrowing model (BGN) are also incorporated for low field mobilities of charge carriers and heavily doped, respectively [17]. To estimate the charge carrier movement, the drift–diffusion (DD) model is also employed in the simulation [17] of the proposed TFET-based sensor. The physics models in the simulation are carefully calibrated with the other experiment work [18] to validate the models and tools for the DMG-AGNR-DG-VTFET device. Figure 2 reasonably matches simulated results with the published data [18].

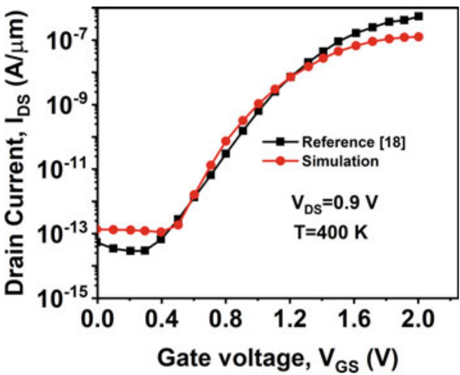

Fig. 2 Calibration of TCAD simulation results against experimental result in [18]

3 Result and Discussion

Firstly, let's analyze the effect of the auxiliary gate (Φ_{Aux}) in the proposed device by fluctuating the work function. Figure 3a, b, and c depicts the alteration in the energy band diagram (ON-state and OFF-state) and transfer characteristic (I_{D}-V_{GS}) of the device as the Φ_{Aux} work function rises and maintains the source sides gate work function (Φ_{Tun}) continual at 4.3 eV. In the OFF-state condition, as the Φ_{Aux} work function is rise, the tunneling gap enlarges, and the band overlapping is reduced at the source-channel junction, ensuing in a significant depletion in the carrier tunneling possibility. Even so, at a higher work function ($\Phi_{\text{Aux}} > 4.4$ eV), the tunneling width is almost constant, OFF-current does not change further. When the device is in ON-state, the auxiliary gate work function variation does not significantly impact the ON-current. Since the energy band diagram does not change as the auxiliary gate Φ_{Aux} increases, the tunneling width is already small in the source-channel junction. Hence, it does not have an impact on the tunneling probability. Figure 3c illustrates the variation in the I_{D}-V_{GS} plot as Φ_{Aux} rises from 4.0 to 4.6 eV. It can be concluded that from the plot, Φ_{Aux} change has no impact on ON-current while OFF-current has an improvement up to 4.4 eV. Figure 4 shows the deviation of the ON/OFF-current ratio and I_{OFF} along the fluctuation of the auxiliary gate work function (Φ_{Aux}). The maximum $I_{\text{ON}}/I_{\text{OFF}}$ current ratio (1.424×10^{14}) and minimum leakage drain current (1.654×10^{18} A/μm) are achieved at $\Phi_{\text{Aux}} = 4.4$ eV; at higher work function ($\Phi_{\text{Aux}} > 4.4$ eV), the flat-band voltage (V_{FB}) is altered, and it shifts the threshold voltage position by some value.

Secondly, the influence of the tunnel gate work function (Φ_{Tun}) has been studied in the proposed device. We keep the auxiliary gate work function constant at $\Phi_{\text{Aux}} = 4.4$ eV while varying the tunnel gate work function in the 4.0–4.8 eV range. The impact of work function (Φ_{Tun}) in the energy band diagram is shown in Fig. 5a and b. Consider the OFF-state, where the conduction band (CB) and valance band (VB), as shown in Fig. 5a, do not overlap. Additionally, there is a clear separation at the tunnel junction, and the work function (Φ_{Tun}) changes with no band coinciding. Therefore, OFF-current is supposed to be relatively low and has the same value. However, in the

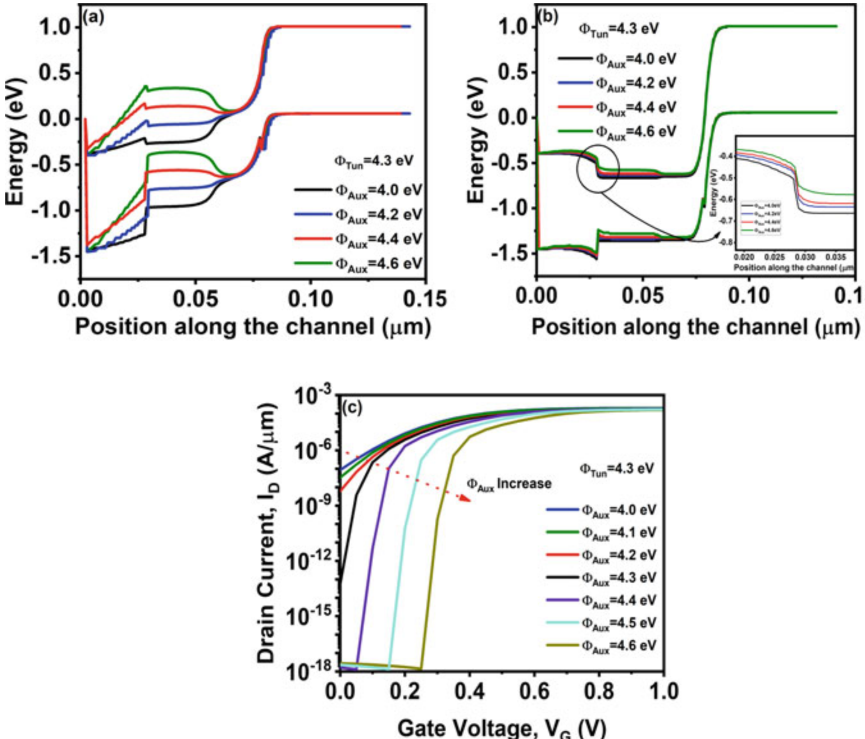

Fig. 3 **a** and **b** Energy band diagram for a different auxiliary gate work functions ($\Delta\Phi_{\mathrm{Aux}}$) in OFF-state and ON-state, respectively, **c** $I_{\mathrm{D}}V_{\mathrm{G}}$ characteristics of the DMG-AGNR-DG-VTFET

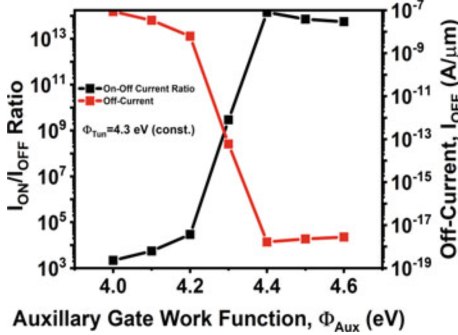

Fig. 4 Auxiliary gate work function (Φ_{Aux}) variation influence on $\mathrm{I_{ON}/I_{OFF}}$ ratio and OFF-current

ON-state, as observed in Fig. 5b, the band overlapping is a minor change, increasing the tunnel gate work function (Φ_{Tun}) and resulting in a small extension in tunneling width. Thus, the tunneling probability of carrier on the tunnel junction is reduced slightly at the ON-current. The fluctuation of transfer characteristics of the DMG-AGNR-DG-VTFET as tunnel gate function Φ_{Tun} varies in the 4.0–4.8 eV range, as illustrated in Fig. 5c. The leakage current has the same magnitude around 1×10^{18} A/μm, but the ON-current decreases by a few orders of magnitude at the higher work function ($\Phi_{\text{Tun}} > 4.6$ eV). Figure 6 indicates the fluctuation of SS_{Avg} and V_T as the function of tunnel gate work function (4.0–4.8 eV), keeping a constant auxiliary gate at 4.4 eV. The increase in the work function (Φ_{Tun}) of tunnel gate material further leads change in flat-band voltage. Thus, it results in overall changes in the threshold voltage, subthreshold swing, and drain current of the device.

The previous analysis shows that fine-tuning auxiliary and tunnel gate work functions can enhance the device's performance. Since the minimum OFF-current and maximum ON-current can be achieved, both the work functions of the gate should be optimized within the range of 4.0–4.8 eV. From Fig. 3c, it can be clearly concluded that to obtain the minimum OFF-current and low threshold voltage, $\Phi_{\text{Aux}} = 4.4$ eV

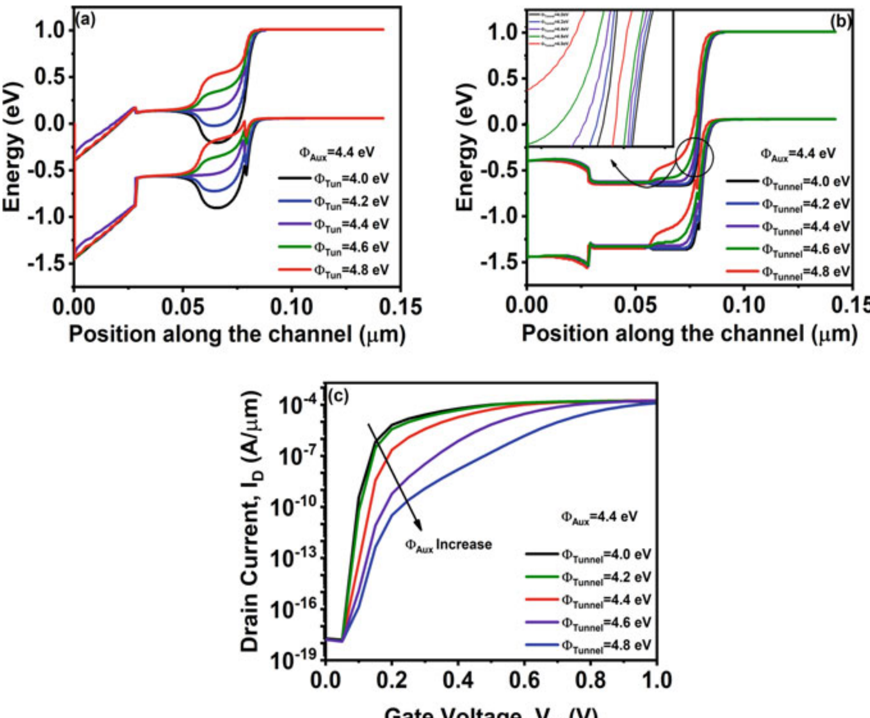

Fig. 5 **a**, **b** Energy band diagram variation with the fluctuation of tunnel gate work function ($\Delta\Phi_{\text{Aux}}$) in $V_{GS} = 0.0$ V and $V_{GS} = 1.0$ V, respectively **c** $I_D V_G$ change with the increase of Φ_{Tun} in the DMG-AGNR-DG-VTFET

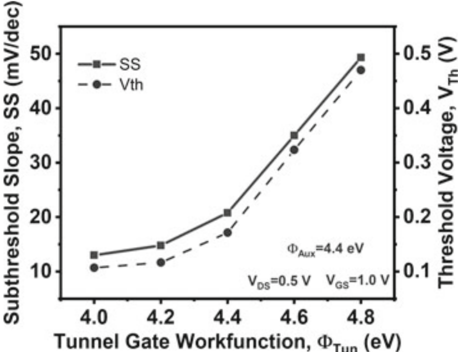

Fig. 6 Impact of tunnel gate work function (Φ_{Tun}) on subthreshold slope and threshold voltage

is picked as the optimum value. Figure 5c shows that ON-current (I_{ON}) and threshold voltage (V_T) are enhanced as the tunnel gate work function decreases. Since the device is desirable to have a high I_{ON} and low V_T parameter, we should select the lowest possible work function ($\Phi_{Tun} = 4.0$ eV). To achieve high I_{ON} and low I_{OFF} current simultaneously, the work functions Φ_{Aux} and Φ_{Tun} are optimized at 4.4 eV and 4.0 eV, respectively.

Lastly, the SMG and DMG of AGNR-DG-TFET have been compared. The $I_D V_G$ characteristics are depicted in Fig. 7. It can be noticed that a higher I_{ON}/I_{OFF} ratio, threshold voltage, and subthreshold swing are achieved in DMG over SMG device. It is noted that at $\Phi_{Aux} = 4.4$ eV and $\Phi_{Tun} = 4.0$ eV, the highest possible value of I_{ON}/I_{OFF} ratio 8.359×10^{13} is achieved in DMG-AGNR-DG-VTFET. The improvement in the I_{ON}/I_{OFF} ratio impacts the subthreshold swing and threshold voltage. The proposed device enhances the average subthreshold swing and threshold voltage from 21 mV/Dec and 0.171 V to 12.79 mV/Dec and 0.104 V, respectively.

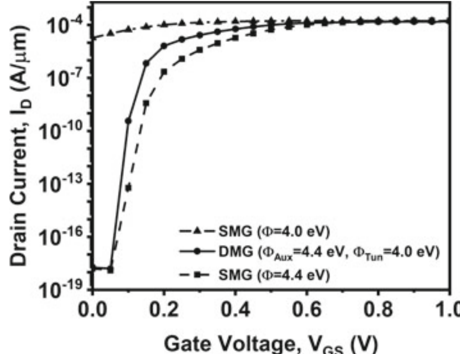

Fig. 7 Comparison of transfer characteristics in the DMG AGNR-DG-VTFET and SMG AGNR-DG-VTFET (Φ = 4.0 eV and Φ = 4.4 eV)

4 Conclusion

In this article, we have investigated the impact of dual gates electrodes in AGNR-DG-VTFET to enhance the device's overall performance concurrently. We have proved that the approach of applied multiple material gate can be used in a proposed device to improve the I_{ON}, I_{OFF}, and threshold voltage, besides an enhancement in average subthreshold swing, improving the behavior of transfer characteristics. We have also manifested that the DMG approach can be used to explore the benefit of both low and high gate work functions (Φ) in a tunnel FET and shows the importance of selecting the work function's accurate value. Moreover, signify the capability of the DMG method to amplify the overall device performance over the single material gate (SMG) of TFET.

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Morphological, Structural and Optical Analysis of Chevronic TiO_2 Thin Film Fabricated by Oblique Angle Deposition

Pinky Khundrakpam, Biraj Shougaijam, and Ashish Ranjan

1 Introduction

Oblique angle deposition (OAD) is a prominent physical vapour deposition method dedicated to fabricating exceedingly functional thin films (TFs) having configurable cylindrical structures. An extensive range of morphologies of thin films, namely S-shapes, slanted columns, chevron/zigzag structures, C-shapes and helices, may be fabricated through the variation of the two fundamental axes of substrate rotation [1, 2]. Normally, these microstructures of columnar morphology results from the deposition flux's shadowing effect during the arrival at the growing film, thereby leading to prevention of deposition shadowed by the tall surface facets. This initiates a combative growth amongst the surface structures, leading to the formation of angled structures slanted towards the approaching deposition flux [3–5]. Lower index of refraction in comparison to denser materials owing to nano porosity of the material and optical anisotropy due to the nanostructure; are shown by the thin films deposited by OAD technique in comparison to other growth techniques. Limited diffusion of adatom and self-shadowing effect are the basis for the high porosity and anisotropic growth which again depends on the material, angle of deposition and deposition conditions. In another extension of OAD technique, known as Glancing Angle Deposition (GLAD) technique, the manipulation of the substrate incline is done during the deposition of film. In contrast to OAD technique where fixed substrate is involved,

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the GLAD method additionally requires active manipulation of both the angle of rotation and substrate incline angle while fabrication of columnar structure growth.

The large assortment of morphologies along with the regulated porosity of the films fabricated through OAD technique usher to innumerable applications, including three-dimensional photonic crystals [6], flat-panel displays [7], graded-index optical filters [8], etc. Additionally, these thin films microstructures formed by the OAD technique incite optical anisotropy [9] that reveals birefringence property [10].

Out of all the potential quantities that represent a cylindrical film microstructure, the relationship of the vapour flux incident angle (α) with the column tilt angle (β), for substrates that do not rotate, is of immense pertinence and has been a topic of deliberation amongst the researchers. The famous tangent rule proposed by Nieuwenhuizen and Haanstra in [11] is represented by

$$\tan\alpha = 2\tan\beta \tag{1}$$

Equation (1) represents sufficiently the relationship of α with β for $\alpha < 60^{\circ}$ but then furnish an inadequate description. The well-known cosine rule was proposed by Tait et al. for $\alpha > 60^{\circ}$ in [12] and is given by

$$\beta = \alpha - \arcsin\left(\frac{1 - 2\cos\alpha}{2}\right), \tag{2}$$

Many other relations have been expressed between α and β in the previous works focusing at a basic explanation of the growth of film. The growth technique directing the columnar structure formation, representing the relation between α and β, has been described to a greater extent by numerical models [13, 14]. A Monte Carlo (MC) ballistic three-dimensional model was proposed by Alvarez et al. [15] to represent the low-temperature physical vapour deposition of TFs at oblique angles. This model expressed the interaction of the film surface and the vapour species at a short range as a source of surface trapping mechanism leading to film growth.

Titanium dioxide (TiO_2), a prominent semiconductor with wide band gap, that is extensively used in varied fields of biosensors [16], optoelectronics [17], UV detectors [18], cancer therapy [19], photocatalysis [20], due to its astounding optical, electrical, and catalytic properties [21, 22]. Many researchers have grown or synthesized TiO_2 nanostructures using a variety of methodologies, including sol–gel [23], hydrothermal [24], glancing angle deposition [25], and chemical vapour deposition [26]. However, the above-mentioned techniques require either a complex fabrication process or is difficult in controlling the growth direction of the nanostructure. In order to overcome such problems, we introduce a simple OAD technique to grow chevronic TiO_2 thin films having a high surface area on a silicon (Si) substrate. TiO_2 thin films grown on silicon substrate at oblique angles through OAD technique has been characterized theoretically and experimentally by Alvarez et al. [15]. Another study reported the fabrication and analysis of TiO_2 thin films on silicon substrate using OAD method [27]. The oblique angle deposition of TiO_2 on glass [28] and silicon [29] substrates forming zig-zag/chevronic TiO_2 thin films have also been

reported. However, most of the above literature discusses the growth mechanisms and morphology of the columnar TF. But, the structure of the TiO_2 TF grown by the OAD is not analysed in any of these literatures.

Therefore, in this work, an attempt has been made to grow chevronic TiO_2 thin film on silicon substrates with the help of a simple OAD technique inside the e-beam chamber. The optical characteristics of the samples were characterized through UV–vis spectroscopy and photoluminescence spectroscopy. Furthermore, the structural and morphological properties were characterized by using X-Ray Diffraction (XRD) and Field Emission Gun-Scanning Electron Microscopy (FEG-SEM).

2 Experimental Details

The Oblique Angle Deposition (OAD) methodology was employed to deposit the chevronic/zig-zag TiO_2 thin films on silicon substrates (1 cm × 1 cm) within the electron beam evaporation system (Smart Coat 3.0, Hind High Vacuum India). The source material used to fabricate the chevronic TiO_2 thin films is 99.999% pure TiO_2 (purchased from Tecnisco Advanced Materials Private Limited, Singapore). The e-beam chamber has an integrated unique OAD unit that ensues the change of the desirable angle with the help of the mechanical axis of the OAD unit. The schematic of simple OAD system is shown in Fig. 1. The e-beam chamber is prepared for deposition by initially cleaning with acetone prior to vacuuming the chamber. The pressure of the e-beam chamber drops to ~ 2×10^{-5} mbar from the initially maintained ~ 6×10^{-6} mbar in the course of the deposition which may owe to the evaporation of the source material releasing oxygen gas. A quartz crystal was employed to track the rate of deposition which was maintained at 1 $Å\ s^{-1}$. The source material to be evaporated and the substrate holder were separated by 20 cm. Initially, a thin film of TiO_2 of 50 nm was deposited on the Si substrate. Subsequently, the substrate holder was then placed at an 85º inclination with the perpendicular axis between the substrate holder and the source material to be evaporated. The fabrication of the 450 nm thick chevronic/zig-zag TiO_2 thin film was achieved by deposition of 150 nm of thick film of the TiO_2 alternately thrice by rotating the substrate 180º azimuthally twice. The schematic representation of the chevronic TiO_2 TF can be observed from Fig. 2. A normal TiO_2 TF of thickness 200 nm was also synthesised by keeping the substrate holder at normal with evaporation material for comparative study with the chevronic TiO_2 TF.

The morphological analysis of the chevronic TiO_2 TF was done through the field emission gun-scanning electron microscopes (FEG-SEM) (JEOL, JSM-7600F). Further, the X-Ray Diffraction (XRD) characterization of the chevronic TiO_2 TF fabricated was accomplished through the X-Pert Pro Pan analytical with Cu K-alpha radiation ($k = 1.54060$ Å). The optical property of absorption was analysed with UV–vis spectrophotometer (UV-1800 Shimadzu, Japan) and the photoluminescence was analysed with UV–Vis spectrophotometer (AN-UV-6500N ANTech) with the use of a 370-nm filter under a wavelength of excitation of 340 nm.

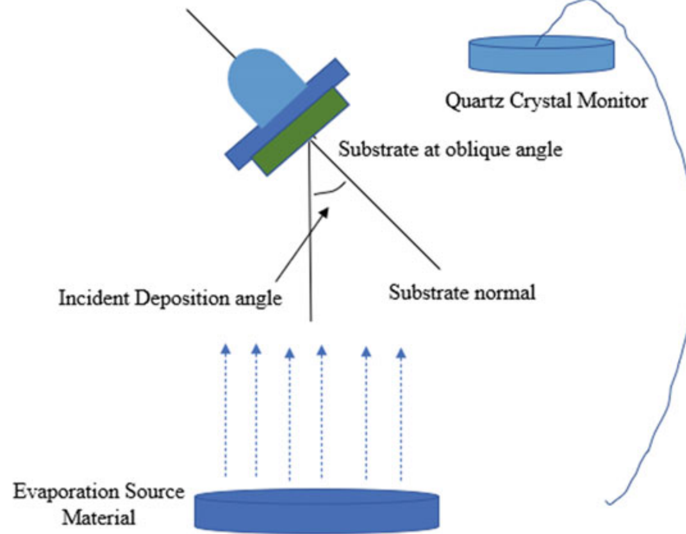

Fig. 1 The schematic of simple Oblique Angle Deposition (OAD) system

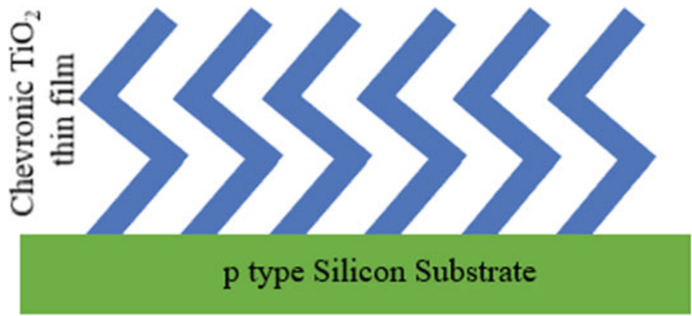

Fig. 2 Schematic representation of the chevronic TiO_2 thin film

3 Results and Discussion

3.1 Morphological Analysis

The sectional view of the FEG-SEM image of the chevronic TiO_2 TF fabricated through OAD at an orientation of 85° is presented in Fig. 3. Top-view of FEGSEM of TiO_2 thin film. The top-view shows the porous nature of the sample, which will enhance the trapping of light. Figure 4 presents the sample's cross-sectional view and clearly depicts the chevronic/zig-zag nanostructure of the TiO_2 TF. A more magnified image showing the chevron/zig-zag nature indicated by blue arrows is

shown in the inset of Fig. 4. The first orientation of the zigzag nanostructure was deposited for the orientation of $\varphi = 0°$ of the substrate position, followed by the second and third orientations with $\varphi = 180°$ and $\varphi = 0°$ respectively. The calculated height of the chevronic TiO_2 structure from the cross-sectional view is ~ 260 nm. The Energy Dispersive X-ray (EDX) analysis shown in Fig. 5. EDS spectrum showing the presence of Ti and O. depicts the existence of titanium (Ti), oxygen (O_2).

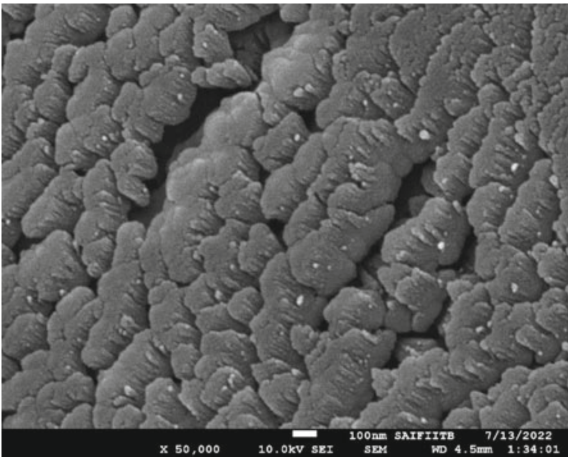

Fig. 3 Top-view of FEGSEM of TiO_2 thin film

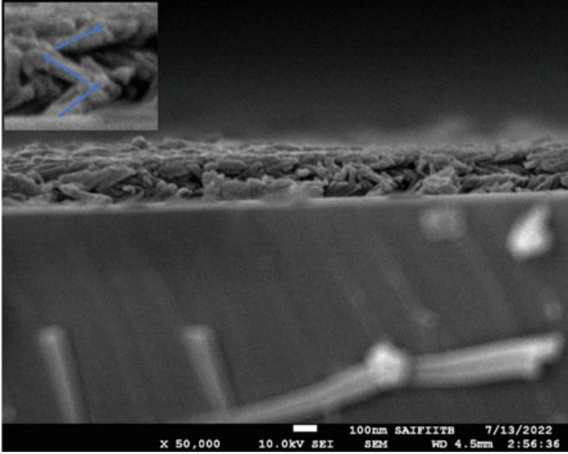

Fig. 4 Cross sectional view of FEGSEM of TiO_2 thin film

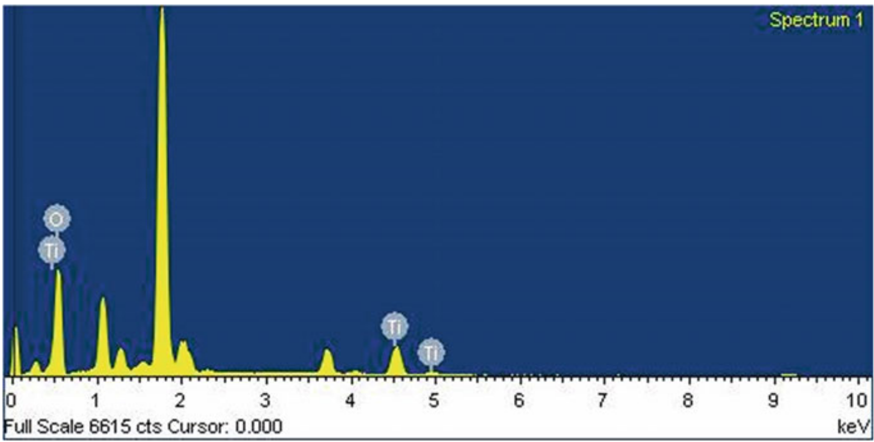

Fig. 5 EDS spectrum showing the presence of Ti and O

3.2 Structural Analysis

The structural properties of the sample were analysed through XRD analysis. The XRD result of the chevronic TiO_2 TF deposited by the OAD technique is presented in Fig. 6. This result presents that the chevronic TiO_2 TF deposited by the OAD technique is mostly amorphous in nature. However, the XRD result shows a very weak peak at ~ 25°. This weak peak at ~ 25° corresponds to the anatase TiO_2 crystal lattice of (101) (JCPDS No. 84-1286). It is reported that the TiO_2 TFs deposited through e-beam are usually amorphous in nature [30]. The structural characteristics of the amorphous TiO_2 TF can be boosted by annealing the sample between 300 and 600 ºC [31].

3.3 Optical Analysis

To analyse the absorption spectra of the TiO_2 TF and the chevronic TiO_2 TF samples, the optical absorption spectra are determined for 310–800 nm wavelengths at room temperature. Figure 7 presents the spectra of absorption of the TiO_2 thin film and the chevronic TiO_2 thin film samples deposited on Si substrate. Greater absorption is shown in the UV range in comparison to the visible range owing to the excited electrons transitioning to conduction band out of the valence band by both the TiO_2 TF and the chevronic TiO_2 TF samples. Further, slightly better absorption is shown by the latter. This may be due to better porosity of the chevronic TiO_2 TF sample as seen from Fig. 3.

Figure 8, Tauc Plot of the absorption spectrum of the chevronic TiO_2 thin film Fig. 8 presents the Tauc plot plotting $(\alpha h\nu)^2$ versus $h\nu$, where $h\nu$ is the incident

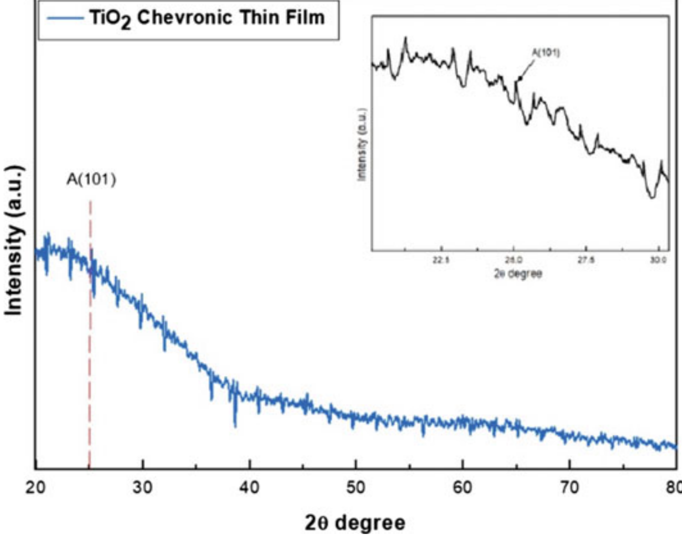

Fig. 6 XRD result of the chevronic TiO_2 thin film

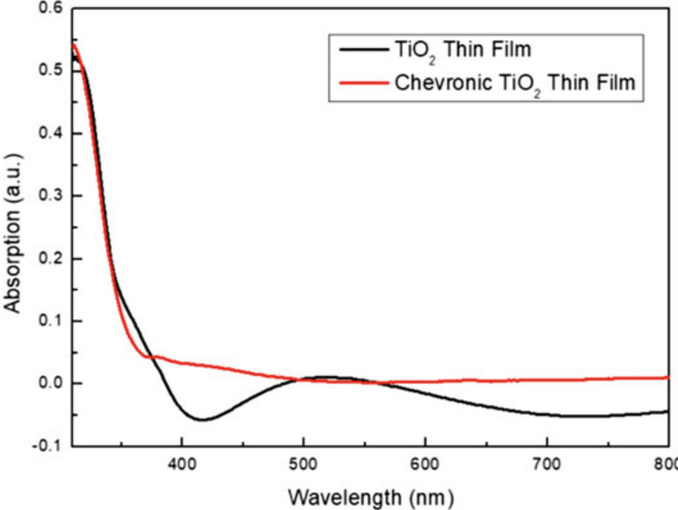

Fig. 7 Absorption spectra of TiO_2 thin film and chevronic TiO_2 thin film

photon energy on the chevronic TiO_2 TF and α is the absorption coefficient. Calculation of the band gap of the chevronic TiO_2 TF so synthesised using OAD technique is achieved through extrapolation of the linear portion of the curve to the energy axis (X axis) and observed to be ~ 3.29 eV as shown in Fig. 8

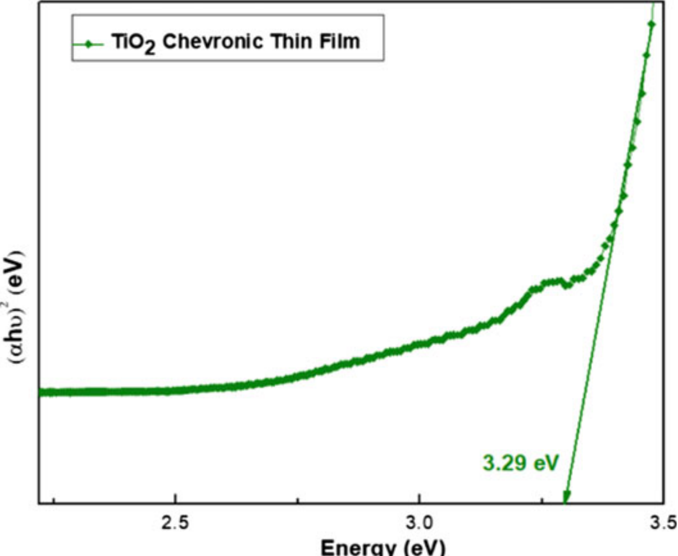

Fig. 8 Tauc Plot of the absorption spectrum of the chevronic TiO_2 thin film

Figure 9 presents the plot of the spectrum of photoluminescence intensity of the chevronic TiO_2 TF fabricated through the OAD which was excited with the use of a 370-nm filter at 340 nm wavelength. The plot shows two peaks, the maximum peak of the chevronic TiO_2 TF at 431 nm corresponding to a near band gap of ~ 2.88 eV and a smaller peak at 413 nm corresponding to a band gap of ~ 3.00 eV. The photoluminescence spectrum is Gaussian fitted and the fitted plot shows a peak at 423 nm corresponding to a bandgap of 2.93 eV. The bandgap from the photoluminescence measurement is faintly lesser than the band gap calculated from the Tauc Plot (~3.29 eV).

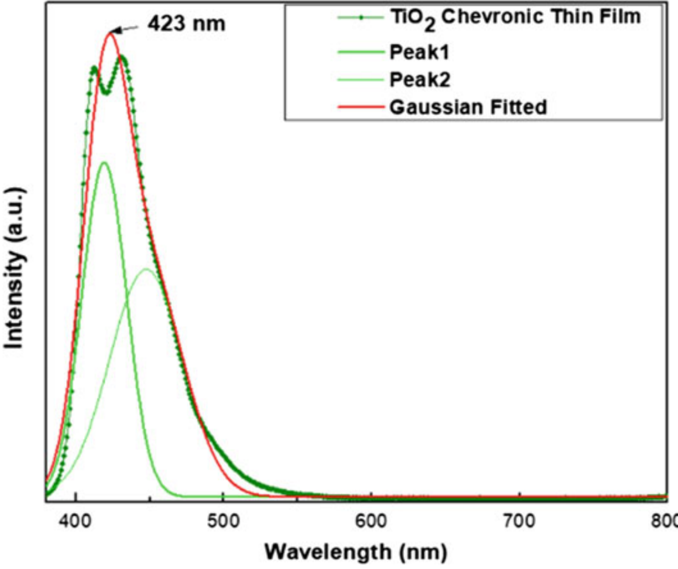

Fig. 9 Photoluminescence spectrum of chevronic TiO_2 thin film

4 Conclusion

The OAD methodology was used to fabricate chevronic/zig-zag TiO_2 TF with the substrate at an inclination of 85° with the perpendicular axis of the evaporation material inside the e-beam evaporation chamber. Morphological, optical and structural analysis of the chevronic TiO_2 TF so fabricated was conducted. The FEG-SEM image of the sample showed successfully grown TiO_2 thin film of chevronic/zig-zag shape on silicon substrate of height ~ 260 nm. The porous nature of the film was also confirmed from the sample's top-view. The existence of titanium and oxygen in the sample was further confirmed by the EDX mapping. A weak peak at ~ 25° belonging to the anatase TiO_2 crystal lattice of (101) was observed from the XRD analysis of the sample. The weak properties of the amorphous TiO_2 may be enhanced through annealing. Enhanced absorption was seen in the ultraviolet (UV) range in comparison to the visible range in the absorption spectra from the UV–vis spectroscopy. Moreover, chevronic TiO_2 thin film sample showed slightly enhanced absorption as compared to the TiO_2 thin film sample. The photoluminescence spectrum is Gaussian fitted and the fitted plot shows a peak at 423 nm corresponding to a bandgap of 2.93 eV which is faintly lesser than the band gap calculated from the Tauc Plot (~3.29 eV). The porous nature of the chevronic TiO_2 thin film may be applicable for efficient harvesting of light.

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Occurrence of Nonlinear Electron Mobility in GaAs/$In_xGa_{1-x}As$ Coupled Double Quantum Well FET

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1 Introduction

The III–V compound semiconductors are used as the channel material in place of Si, since the materials like InAs and GaAs are showing higher mobility and thus higher driving current [1, 2]. $In_xGa_{1-x}As$ heterostructure-based III-V n-channel MOSFETs can be used for low-power (LP) technology. More percentage of In in $In_xGa_{1-x}As$ causes lower energy gap and therefore higher tunneling current, facilitating more precise design for LP applications [3]. The current driving capability of III-V heterostructures with different materials in the channel are examined and it is found that InGaAs possesses the highest electron injection velocity and better performance like high-power gain and low noise [4]. In-rich asymmetric InGaAs MOSFETs shows better performance by analyzing the effect of spacer layer on different device parameters [5]. The III-V compound semiconductors are the key material in logic switching devices [6]. Further, due to better electron transport properties, these can be used for nanometer-scale logic transistors [7]. In case of tunnel FETs (TFETs), advanced III-V compound heterostructures are used to increase energy efficiency and optimized performance. III–V heterostructure TFETs and MOSFETs has been proposed for future CMOS applications [8]. InGaAs/AlGaAs heterostructures are also assuring materials in microwave transistors for high-power application [6].

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Electron mobility is an important parameter for device performance [9, 10]. Studies have been made on μ of two-dimensional electron gas (2DEG) in QW structures [11–18]. High density of 2DEG leads to intersubband transitions which can be controlled by the donor doping profile [19]. Studies of electron mobility in InGaAs/GaAs and InGaAs/InAlAs based strained layer quantum well MODFET structures have been done [12, 13, 15, 19–23]. When more than one subband lies below the Fermi level, the intersubband effects contributes substantially to the subband electron mobility [24–27].

Recently, the DQW structures have been utilized to explore the coupling properties of the electronic states in analyzing the electron mobility [15, 28–30]. Electron mobility at low temperature has been studied in GaAs/AlGaAs DQW structures which includes the effect of coupling of energy states in between the wells. Nonmonotonic oscillatory behaviour of electron mobility which depends on external electric field and different structure parameters have been discussed [16, 17, 31–33]. Also, it has been studied to analyze the mobility in nonsquare structures which exhibits interesting behavior due to their specific shape [34, 35].

In case of asymmetric DQW structure, the potential difference between the quantum wells leads to dissimilar energy states in the wells. The wave functions localize to the related wells. With a variation in the structure parameters, the energy-level difference reduces and with a suitable combination of parameters, the energy states synchronize, that leads to resonance of energy states in the quantum wells. The subband wave functions of the coupled structure at resonance are no longer localized to the respective wells but delocalized forming bonding and antibonding pairs and penetrating almost equally into both the wells. We utilize this type of quantum mechanical variation of wave functions near resonance to study mobility.

In this chapter, we have taken GaAs/$In_xGa_{1-x}As$ pseudomorphic DQW field effect transistor (FET) structure to analyze the electron mobility μ. We consider an asymmetric structure by taking unequal of well widths, $W1 \neq W2$. In the substrate barrier, the doping concentration Nd1 is varied, while Nd2 in the surface barrier is kept fixed. Accordingly, the energy level difference between the wells varies. For a particular value of Nd1, say Nd1r, the levels coincide, thereby exhibiting resonance. Around Nd1r, change in the extension of wave functions in the wells causes substantial variation in the matrix elements of the scattering rates. As an outcome, a sudden nonlinearity in μ is exhibited. This work shows that even though the nonmonotonic μ is based on interface roughness scattering, with increase in well width difference ($W1$–$W2$), the alloy disorder (al-) and ionized impurity (imp-) scatterings also contribute. Further, magnitude depends on al- and imp- scattering mechanisms. Our work, which leads to nonlinearity in μ, can help in studying the fine tuning of the QWFET devices near resonance.

2 Theory

GaAs/In_xGa_{1-x}As DQW structure is considered with Silicon delta doping in the barrier layers having doping widths of D. Nd1 and Nd2 are doping concentrations along substrate side and surface sides respectively. Width of spacer is S. Widths of wells are $W1$ and $W2$ (Fig. 1). Impurity distribution along the direction of z-axis Nd(z) is given as:

$$\mathrm{Nd}(Z) = \begin{cases} \mathrm{Nd1} & -(W1 + D + S + B/2) < z < -(W1 + S + B/2) \\ \mathrm{Nd2} & (W2 + S + B/2) < z < (W2 + D + S + B/2) \\ 0 & \text{Otherwise} \end{cases} \quad (1)$$

Subband electron energy E_n as well as subband wave function η_n are derived self-consistently solving Schrodinger and Poisson's equations. Concentration of electrons can be found out as [24]:

$$N_e(z) = \sum_n N_n |\eta_n(z)|^2 \quad -\infty < z < \infty \quad (2)$$

The 2D electron density N_n for nth subband depends on Fermi energy (E_F) and E_n [24] as:

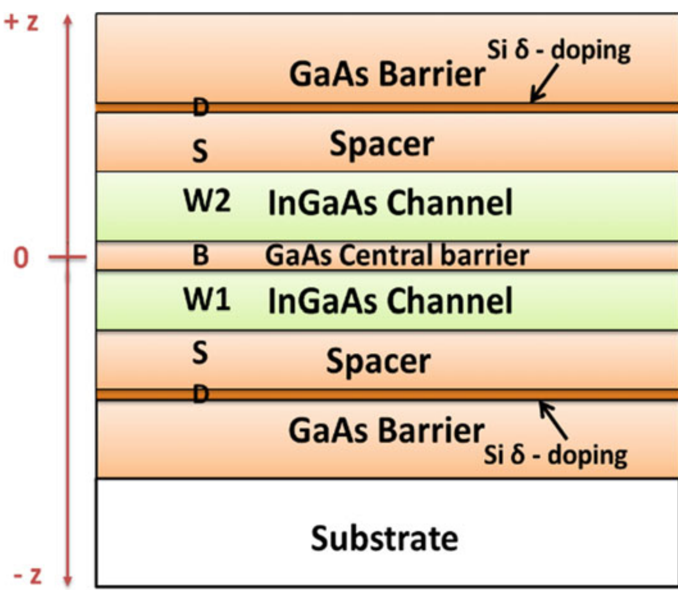

Fig. 1 Graphic Representation of DQWFET

$$N_n = (K_B T m/\pi \hbar^2) \log[\exp(E_F - E_n)/K_B T + 1] \quad (3)$$

Further, N_n and Surface electron density N_s are related with each other [24]. The Boltzmann equation helps in determining the transport life time $\tau_{n,}$ for multi subband occupancy as [24]:

$$\sum_{n=0}^{M} c_{kn}\tau_n = 1 \quad (4)$$

c_{kn} and τ_n are represented as transport matrix and transport life time. Sub-band indices are k and n. For one subband occupied case, n and k both are equals to zero, therefore, $c_{00} = f_{00} = 1/\tau_0$. When more than one subbands are occupied, n and k are having both 0 and 1 values and $\tau_{0,}$ τ_1 are represented below [30]:

$$\tau_0^{(-1)} = \frac{(f_{00} + g_{01})(f_{11} + g_{10}) - h_{01}h_{10}}{(f_{11} + g_{10}) + \{(E_F - E_1)/(E_F - E_0)\}^{1/2} h_0 1} \quad (5)$$

$$\tau_1^{(-1)} = \frac{(f_{00} + g_{01})(f_{11} + g_{10}) - h_{01}h_{10}}{(f_{00} + g_{01}) + \{(E_F - E_0)/(E_F - E_1)\}^{1/2} h_1 0} \quad (6)$$

f_{nn} is termed as intrasubband whereas g_{nm}, h_{nm} are termed as intersubband matrix elements that depend on the scattering potentials $U_{kn}^{\mathrm{eff}}(q)$ [30]. For alloy disorder/interface roughness/ionized impurity (al-/ir-/imp-) scatterings, $U_{kn}^{\mathrm{eff}}(q)$ can be represented as:

$$\left|U_{kn}^{\mathrm{ir}}(q)\right|^2 = U_b^2 \pi \Lambda^2 \Delta^2 \mathrm{e}^{-q^2\Lambda^2/4} \left|\sum_{k'n'} \eta_{k'}^{*}(z)\eta_{n'}(z)|_{z=z_I}\, \varepsilon_{kn,k'n'}^{-1}(q)\right|^2 \quad (7)$$

$$|U_{kn}^{\mathrm{imp}}(q)|^2 = \frac{4\pi^2 e^4}{\varepsilon_0^2 q^2}\left[\mathrm{Nd1}\int_{-(W1+D+S+B/2)}^{-(W1+S+B/2)} \mathrm{d}z_i \left|\sum_{k'n'} \varepsilon_{kn,k'n'}^{-1}(q) J_{k'n'}(q, z_i)\right|^2 + \mathrm{Nd2}\int_{(W2+S+B/2)}^{(W2+D+S+B/2)} \mathrm{d}z_i \left|\sum_{k'n'} \varepsilon_{kn,k'n'}^{-1}(q) J_{k'n'}(q, z_i)\right|^2\right] \quad (8)$$

$$\left|U_{kn}^{\mathrm{al}}(q)\right|^2 = \left[a^3(\delta U)^2 x(1-x)/4\right] \times \int \mathrm{d}z \left|\sum_{k'n'} \eta_{k'}(z)\eta_{n'}(z)\varepsilon_{kn,k'n'}^{-1}(q)\right|^2 \quad (9)$$

where

$$J_{k'n'}(z_i, q) = \int_{-\infty}^{\infty} \mathrm{d}z \eta_{k'}(z) \eta_{n'}(z) \mathrm{e}^{-q|z_i - z|} \quad (10)$$

Parameters like δU, 'a', Δ, x and Λ are related to ir- and al- scattering potentials. For each subband, electron mobility can be found out using the formula $\mu_n(E_F) = (e/m)\tau_n(E_F)$. The mobility is calculated by $\mu^p = \Sigma_n n_n \mu^p{}_n / \Sigma_n n_n$, where p = imp/ir/al for a particular scattering. When more than one scattering are considered, Matthiessen's rule is used for accounting the mobility.

3 Results and Discussion

This chapter describes the impact of Nd1 and Nd2, the uneven doping concentrations on electron mobility μ in GaAs/$In_{0.2}Ga_{0.8}$As strained double quantum well FET structure. Data used here are as follows: barrier potential height U_b = 140 meV, width of spacer, S = 60 Å, width of central barrier, B = 60 Å, doping width D = 20 Å, effective mass of electron $m = 0.62m_0$, ir- scattering parameters, correlation length Λ = 100 Å, mean height Δ = 2.83 Å, δU = 530 meV [25, 30].

We present μ^{ir} in Fig. 2 and μ^{imp} as well as μ^{al} in Fig. 3 as functions of Nd1 for the range 0.5–2.5 (in the unit of 10^{18} cm^{-3}) by considering: Nd2 = 2 (in unit of 10^{18} cm^{-3}) and (a) ($W1$, $W2$) = (160 Å, 140 Å), (b) ($W1$, $W2$) = (220 Å, 80 Å), such that $W1 + W2$ = 300 Å in both the cases. In principle, any set of $W1$ and $W2$ can be considered. For representative purpose, we consider, two sets, say, set (a) of small difference in well widths, from equal values, $W1 = W2$ = 150 Å, and another set of large difference in $W1$ and $W2$ (set (b)). Variation of Nd1 changes the inequality between Nd1 and Nd2 thereby presenting electron mobility versus change in the dissymmetry in the doping concentrations. All through this range of Nd1, two subband levels are seen occupied. It is seen μ^{ir} (Fig. 2) is about one order larger than μ^{imp} and μ^{al} (Fig. 3). For (a): $W1$ = 160 Å, $W2$ = 140 Å, there is clear cut groove like lowering in μ^{ir} at Nd1 = 1.86 (in unit of 10^{18} cm^{-3} (Fig. 2) but no such lowering in μ^{imp} and μ^{al} (Fig. 3). In case of (b): $W1$ = 220 Å, $W2$ = 80 Å, such dip occurs in all the three mobilities, μ^{ir}, μ^{imp} and μ^{al} at Nd1 = 0.8 × 10^{18} cm^{-3}. The substantial dip in μ^{ir} is due to the large turning of subband mobilities ${\mu_0}^{ir}$, ${\mu_1}^{ir}$ around the point of resonance (shown in the subsequent Figs. 4 and 5).

The change in μ^{ir}, μ^{imp} and μ^{al} are realized from ${\mu_0}^{ir}$, ${\mu_0}^{al}$, ${\mu_0}^{imp}$, ${\mu_1}^{ir}$, ${\mu_1}^{al}$, and ${\mu_1}^{imp}$ presented versus Nd1 for (a): ($W1$, $W2$) = (160 Å, 140 Å) and (b): ($W1$, $W2$) = (220 Å, 80 Å) in Figs. 4 and 5, respectively. In case of Fig. 4, only ${\mu_0}^{ir}$ and ${\mu_1}^{ir}$ change prominently at around Nd1 = 1.86 × 10^{18} cm^{-3}, whereas in Fig. 5, there is clear cut turning of all the subband mobilities at around Nd1 = 0.8 × 10^{18} cm^{-3} that gives rise to nonlinearity in mobility in Figs. 2 and 3.

The corresponding mobility μ(160,140) and μ(220,80) are presented in Fig. 6. We note that the position and strength of dip in μ are different in both the cases. In case of μ(220,80), the dip is larger due to the additional effect of nonlinearity in

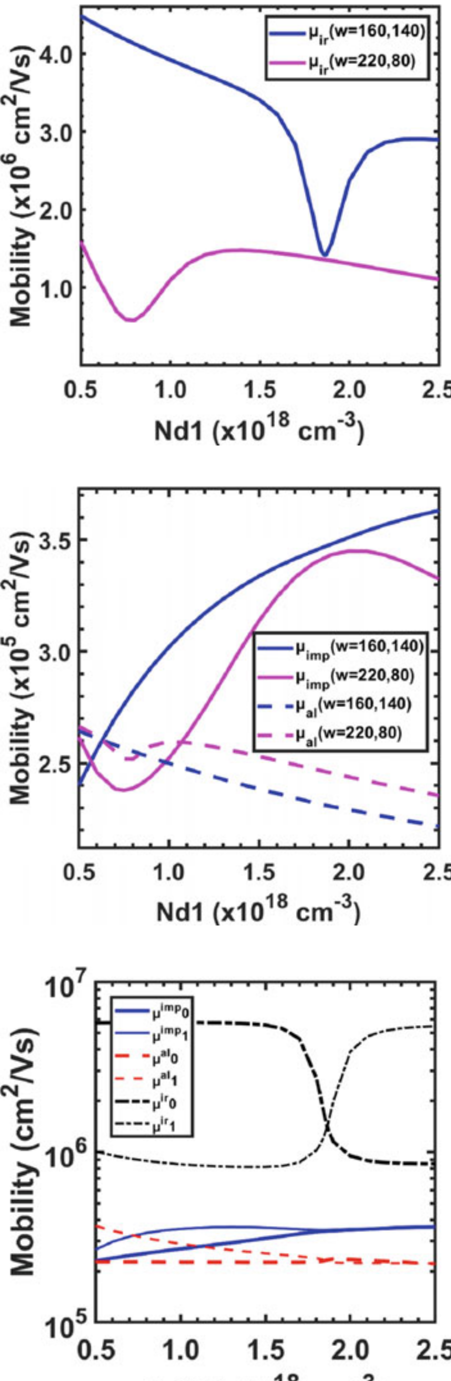

Fig. 2 Mobility μ^{ir} ($W1$, $W2$) versus Nd1 where $B = 60$ Å, $W2 + W1 = 300$ Å, Nd2 = 2 (in unit of 10^{18} cm^{-3})

Fig. 3 Electron mobility μ^{imp} and μ^{al} ($W1$, $W2$) versus Nd1 where $B = 60$ Å, $W2 + W1 = 300$ Å, Nd2 = 2 (in unit of 10^{18} cm^{-3})

Fig. 4 Subband mobilities $\mu_0{}^{\mathrm{ir}}$, $\mu_1{}^{\mathrm{ir}}$, $\mu_0{}^{\mathrm{imp}}$, $\mu_1{}^{\mathrm{imp}}$, $\mu_0{}^{\mathrm{al}}$ and $\mu_1{}^{\mathrm{al}}$ versus Nd1 for B = 60 Å, $W1 = 160$ Å, $W2 = 140$ Å, Nd2 = 2 (in unit of 10^{18} cm^{-3})

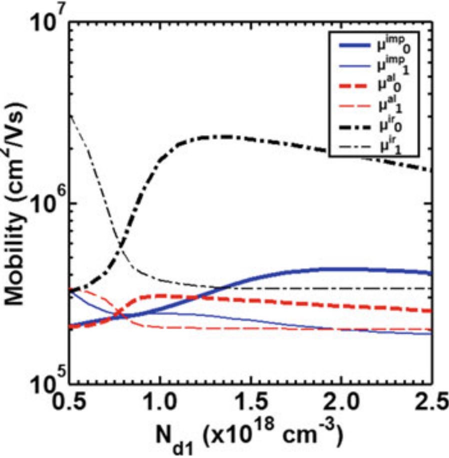

Fig. 5 Subband mobilities $\mu_0{}^{\text{ir}}$, $\mu_1{}^{\text{ir}}$, $\mu_0{}^{\text{imp}}$, $\mu_1{}^{\text{imp}}$, $\mu_0{}^{\text{al}}$ and $\mu_1{}^{\text{al}}$ versus Nd1 for B = 60 Å, $W1 = 220$ Å, $W2 = 80$ Å, Nd2 = 2 (in the unit of 10^{18} cm^{-3})

mobility due to al- and imp-scatterings. Regarding the position of dip in μ, we note that for μ (160, 140), the dip occurs at Nd1 = 1.86×10^{18} cm^{-3} and for μ(220, 80), it occurs at 0.8×10^{18} cm^{-3}, i.e., at different resonance points. To explain this, let us take $W1 = W2 = 150$ Å, where resonance of energy states occurs at Nd1 = 2, Nd2 = 2 (in the unit of 10^{18} cm^{-3}) and the structure potential is symmetric. Subband wave functions of the wells overlap yielding a split in the energy levels. η_0 and η_1, lower- and upper-level wave functions are distributed symmetrically and antisymmetrically in both the wells. Now once $W1 \neq W2$, the symmetry is lost. The wells become asymmetric, which results in different energy levels for each well. To bring them into resonance, the doping concentration Nd1 is varied from Nd2 so that the change in the energy levels due to $W1 \neq W2$ is compensated by a suitable combination of Nd1 $\neq$ Nd2. Therefore, the resonance points in Nd1, that is, say Nd1r is different in case: (a) and (b).

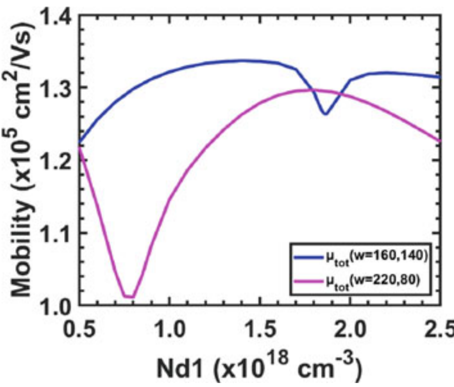

Fig. 6 μ ($W1$, $W2$) versus Nd1 where, $B = 60$ Å, $W2 + W1 = 300$ Å, Nd2 = 2 (in the unit of 10^{18} cm^{-3})

We shall now explain the reason for turning of subband mobilities. We note that near resonance, that is, at Nd1r, the wave functions η_0 and η_1 are distributed equally in both the wells. But a slight variation in Nd1, either Nd1 > or < from Nd1r, there is drastic change in the localization of η_0 and η_1 in the wells. Say, for Nd1 > Nd1r, if η_0 lies mostly in one well, then η_1 lies in the other well. In the other case, Nd1 < Nd1r, vice versa occurs. This is because of quantum mechanical electron distributions in a DQW structure. Since the localization of η_0 and η_1 affects the strength of the scattering potentials, the drastic change in η_0 and η_1 near resonance yields substantial variation in the subband mobilities leading to dip in mobilities.

4 Conclusion

The uneven doping in the barriers induces nonlinear μ in an $In_xGa_{1-x}As$/GaAs QWFET structure. The dissimilar doping concentrations cause the change in the wave function distribution and accordingly that affects the band bending and occupation of subbands. Near resonance the extension of the wave functions in the quantum wells change considerably, which depends on the doping concentration. Consequently, this affects the inter- and intra-subband scattering rates that leads to dip like nonmonotonic variation of mobility. But for $W1 \neq W2$, that is, different well widths, the resonance of energy states arises at Nd1 not equal to Nd2. We show that when well widths differ more, the dip in μ takes place at Nd1 farther away from Nd2. In addition, as the asymmetry in the wells increases, the nonlinearity in mobility μ also increases. We show that even though the nonlinearity is mainly because of ir-scattering, with increase in well width difference, the effect of imp- and al-scattering influence more to enhance the dip in the μ. Furthermore, magnitude of total mobility is mostly depending upon the al- and imp- scatterings. The results of nonmonotonic μ at the point of transition of the structure near resonance, which varies with doping concentration, can help in the tuning and analyzing the channel conductivity characteristics of the p-QWFET devices.

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Investigation of the Temperature Impact on the Performance Characteristics of the Field-Plated Recessed Gate III-Nitride HEMT on β-Ga_2O_3 Substrate

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1 Introduction

High electron mobility transistors (HEMTs) made of AlGaN/GaN have gained a lot of interest for prospective use in next-generation devices for high-power and high-frequency applications [1–3]. AlGaN/GaN HEMTs are 10 times smaller than silicon and gallium arsenide transistors, which lowers material costs while additionally providing a higher power density and greater efficiency for given output power [4]. A variety of high-voltage and high-temperature applications for the industrial and military markets are facilitated by the wide band gap (3.4 eV) [5, 6]. The material has a significant breakdown field, high mobility, and excellent thermal and chemical resilience [7–10]. These HEMT-based systems will be used in a wide variety of military applications, unmanned aerial vehicles, torpedo and ship drive components, high-power satellite communications, sensors, and radar [11, 12].

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Although these transistors have exhibited outstanding results, numerous issues and limitations still need to be fixed in order for this technology to be commercially feasible. AlGaN/GaN HEMTs' high gate leakage, which decreases breakdown voltage, decreased power added increased unwanted noise, self-heating, and kink effect are the primary factors limiting their effectiveness and reliability in high power and RF applications [13–18].

Additionally, lattice mismatch also one of the crucial factor for the cause of leakage current in the HEMT. Therefore, AlGaN/GaN HEMTs necessitated to develop on a substrate that has a reduced lattice mismatch with the GaN material in order to reduce leakage current [19–22]. Sapphire is used as substrate for GaN-based HEMTs, but sapphire exhibited 16% lattice discrepancy with GaN material [23]. Later, SiC utilized as a substrate, but it is exhibited 3.8% lattice mismatch with Buffer material [24]. The β-Ga_2O_3, a recently found UWBG semiconductor, can be employed as a substrate for AlGaN/GaN HEMT due to decreased 2.8% disparity with GaN [25]. β-Ga_2O_3 substrates are highly suitable for power electronics because of their advantages of being inexpensive, feature a superior-quality characteristics material, and having a large bandgap [26, 27].

It is necessary to investigate the performance characteristics over temperature before using AlGaN/GaN HEMT grown on β-Ga_2O_3 substrate for commercial applications. For HEMTs, temperature stability is essential, particularly at higher temperatures where the ohmic and Schottky contacts deteriorate, and the device performance is greatly dependent on the transport characteristics of 2DEG. This article explores how the proposed III-nitride HEMT's output current characteristics are impacted with temperature.

As a preliminary study, in this chapter, we report the novel III-nitride HEMT grown on β-Ga_2O_3 substrate, effect of temperature on drain current characteristics with different thickness of the substrate, performance degradation due to self-heating phenomena, occurrence of kink effect with different temperature, and saturated drain current characteristics deterioration with increment of $R_{ON,sp}$ with the temperature variation is also discussed. The drain source on-resistance ($R_{DS,ON}$) is the resistance between the drain and the source of a MOSFET when a specific gate-to-source voltage (V_{GS}) is applied to bias the device to the ON state. As the V_{GS} increases, the on-resistance generally decreases. If the drain to source on resistance multiplied with active area size, it would be specific on-resistance ($R_{on,sp}$). The primary novelty of the research is that the study of the drain current characteristics of novel III-nitride HEMT grown on β-Ga_2O_3 substrate with temperature variation.

The research article is framed as follows, a brief introduction about importance and limiting factors on the performance characteristics of the AlGaN/GaN-based HEMT and β-Ga_2O_3's useful features are discussed in the Section I. The novel structure of the III-nitride HEMT on β-Ga_2O_3 substrate and models used in simulation framework is given in Sect. 2. The results obtained under various contexts of different temperatures are explained in Sect. 3, and finally conclusion is provided in Sect. 4.

2 Device Structure and Simulation Framework

The schematic cross-section of the simulated 20 nm gate length and 20 nm field-plated novel III-nitride HEMT with a gate recess of 30 nm grown over β-Ga_2O_3 substrate is presented in Fig. 1. The HEMT consists of 20 nm thin Si_3N_4 passivation layer, a 33-nm AlGaN layer, a 22-nm GaN layer. A 2-nm AlN layer as a spacer is utilized in between AlGaN and GaN layers. The Si_3N_4 passivation can enhance the surface state of the AlGaN barrier, which will mitigate the current collapse effect [28]. The AlGaN back barrier facilitates the smoothing of the substrate-to-GaN layer interface and diminishes the short channel impact in HEMT [29–31]. The Al content (x) of AlGaN is set as 0.3 (upper), and back barrier is set to 0.1, respectively.

The charge particles are confined at the interface of AlGaN and GaN layers owing to the dissimilarities between the large bandgap of AlGaN and the narrow bandgap of GaN layer. These charge particles are known as two dimensional electron gases (2DEG), 2DEG is induced mainly due to both on piezoelectric and spontaneous polarization [32]. The barrier layer offers significant carrier confinement in the quantum well at the hetero-interface, and the addition of an AlN spacer layer enhances the 2DEG mobility. A significant amount of n-type impurities are doped in the source and drain regions.

Various physical models are employed in the simulation, such as the fundamental models of Poisson's self-consistency model, drift–diffusion solutions, continuity models, Shockley-Reed-Hall (SRH) model for carrier generation and recombination are used in the simulation deck [33]. Since GaN is a polarized material, the spontaneous polarization model is used to investigate the polarization in GaN portions of the proposed device. Additionally, the piezoelectric models are applied to study the strain induced by the dissimilarities between the AlGaN and GaN layers. The electron mobility models which are dependent on the temperature and field dependent are utilized, and expressed as Eqs. 1 and 2, respectively.

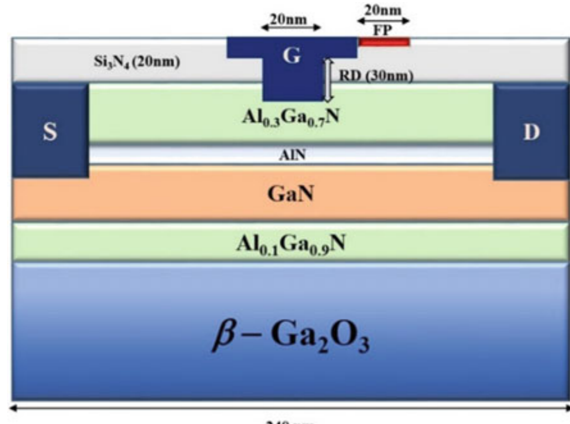

Fig. 1 The cross-sectional view of proposed III-nitride HEMT on β-Ga_2O_3 substrate

$$\mu_{\mathrm{low}} = \mu_0 \left({T}/{300} \right)^{\alpha} \tag{1}$$

$$\mu_n = \frac{\mu_{\mathrm{low}} + v\left({E^{a-1}}/{E_c^a} \right)}{1 + c\left(\frac{E}{E_c} \right)^a + \left(\frac{E}{E_c} \right)^b} \tag{2}$$

where $a = 15{,}951$, $b = 0.7248$ and $c = 2.0984$, and remaining variables are their conventional definitions only [34].

3 Results and Analysis

In this section, the role of temperature on the performance characteristics of the proposed III-nitride HEMT on β-Ga_2O_3 substrate is discussed with the with the help of ATLAS TCAD simulations [33, 35].

Figure 2 illustrates the investigation of the influence on output drain current characteristics of the HEMT with a substrate thickness of 130-nm under different temperatures. In the simulation, the device is supplied the external/ambient temperature by mounting a thermo-contact at the base of the substrate. It is observed that for temperature of 300, 550, and 800 K, respectively, the maximum saturation drain current with 130-nm substrate thickness is 1.2, 0.805, and 0.505 A/mm. It is found that the drain current significantly reduces with increasing temperature.

As the temperature increases, the scattering mechanisms caused by coulomb, lattice vibration, and phonon scatterings will influence the mobility of the charge carriers in the channel [36, 37]. As a result, the output current is declined due to reduction in the channel mobility. It is clearly evident in Fig. 2. Additionally, drain

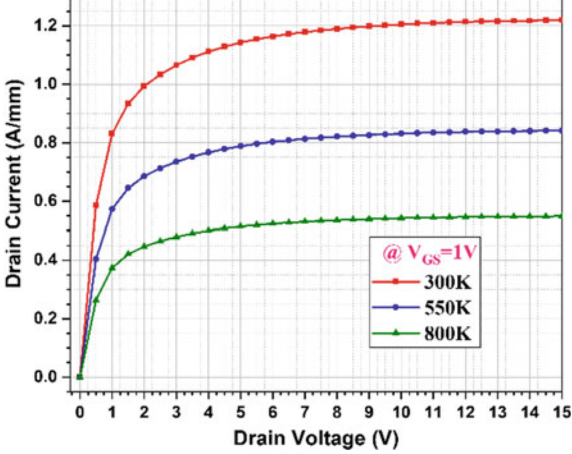

Fig. 2 Illustration of the influence of the temperature in drain current characteristics of the proposed HEMT on β-Ga_2O_3 substrate

characteristics for various temperatures of 300, 550, and 800 K for different substrate thickness is also investigated in Figs. 3, 4, and 5.

The maximum drain saturation current observed with 180 nm (230 nm) substrate thickness are 1.1 (1.06), 0.708 (0.705) and 0.502 (0.499) A/mm for 300, 550 and 800 K, respectively. The influence of substrate layer thickness on drain current is less apparent at a higher temperature, as depicted in Figs. 3, 4, and 5. The analogy between temperature, substrate thickness and maximum saturated drain current are given in Table 1. The I_{DSS} current declined with the substrate thickness raises, but it is not observed for substrate thickness at higher temperature of 800 K. The mobility of the charge carriers is degraded and saturated at 800 K. Therefore, larger substrates could not deliver greater output current, due to deterioration in mobility owing to scattering mechanisms.

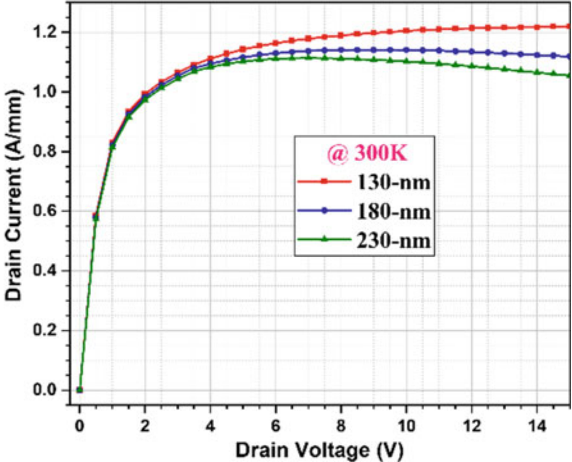

Fig. 3 Illustration of the drain current characteristics for different substrate thickness under temperature @ 300 K

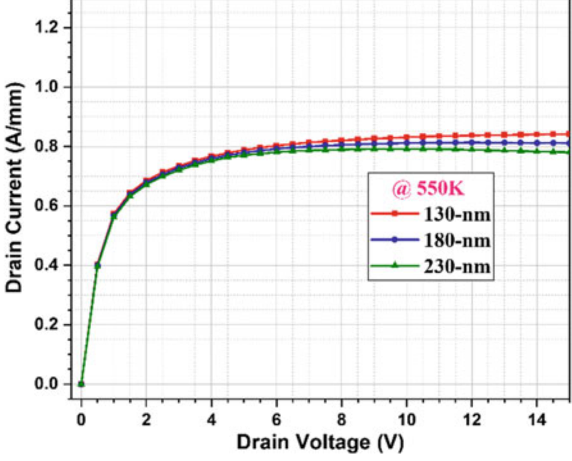

Fig. 4 Illustration of the drain current characteristics for different substrate thickness under temperature @ 550 K

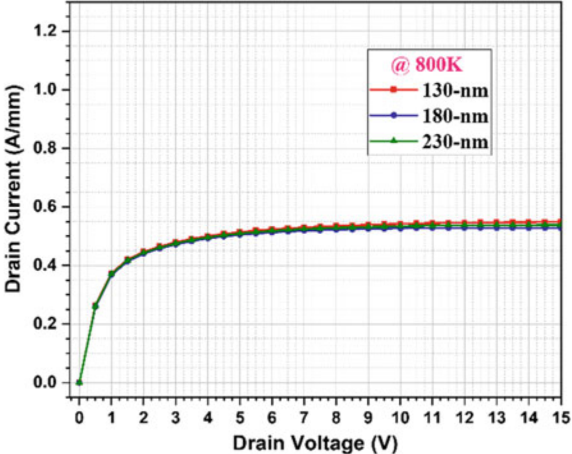

Fig. 5 Illustration of the drain current characteristics for different substrate thickness under temperature @ 800 K

Table 1 Comparison of maximum saturation drain currents at different substrate thickness

Case	Maximum drain current (A/mm)		
	@ 300 K	@ 550 K	@ 800 K
130-nm	1.2	0.805	0.505
180-nm	1.1	0.708	0.502
230-nm	1.06	0.705	0.499

The observations show that the change in substrate thickness has an enormous impact on the drain current at 300 K and a lower influence at 700 K.

The simulated drain current profiles at $V_{GS} = 2$ V under different temperatures with substrate thickness of 130 nm are depicted in Fig. 6.

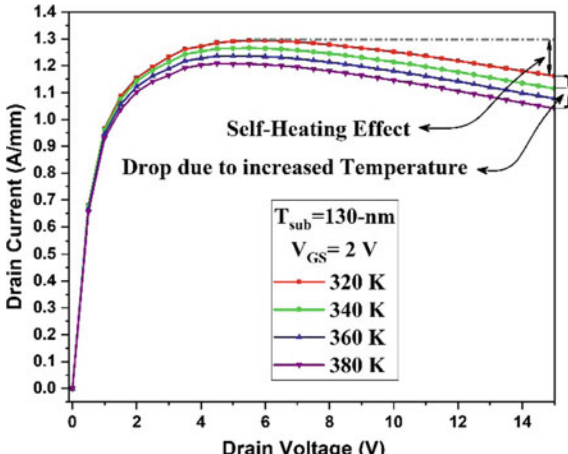

Fig. 6 Illustration of the drain current characteristics at different temperatures

It is evident that both the temperature and the self-heating process cause a decrease in the drain current, as shown in Fig. 6. It is exciting to notice that the HEMT self-heating influences the drain current above the saturation area ($V_{DS} > 6.5$ V). The ambient temperature has an impact on both the linear and saturation sections of drain characteristics.

Figure 7 illustrates the drain current vs. drain voltage for a substrate thickness of 130 nm at different temperatures for $V_{GS} = -1$ V. It's noteworthy to note that at $V_{GS} = -1$ V, the drain characteristics exhibit a kink effect. It is due to acceptor traps caused by dislocations in the GaN buffer. It is found that the drain current demonstrates a more prominent kink effect at $T = 300$ K than at $T = 380$ K. The drain current investigation for a substrate thickness of 130-nm at $V_{GS} = -2$ under different temperature values are carried out, as shown in Fig. 8. It is noted that at $V_{GS} = -2$ V, the drain current is seen to solely be affected by the ambient temperature; there is no discernible self-heating effect at this gate voltage. It is as a result of a reduced drain current at smaller V_{GS}, which could not be adequate to warm up the device.

The following can be inferred from Figs. 6, 7, and 8; (i) At higher gate voltages (above 1 V), both the self-heating and temperature have an impact on the drain current; (ii) The drain current exhibits a kink effect for gate voltage of − 1 V, and is influenced by both self-heating and temperature; (iii) For gate voltages below − 2 V, the sole factor affecting the drain current is only the temperature.

Figure 9 illustrates the impact of temperature on the maximum saturated drain current $I_{d,max}$ and $R_{ON,sp}$. $I_{d,max}$ and $R_{ON,sp}$ exhibited substantial temperature sensitivity in the thermal investigations. As the temperature increased, the device's $I_{d,\max}$ at $V_{GS} = 1$ V, significantly dropped from 1.2 to 0.5 A/mm, while at the same time, a noticeable increase in $R_{ON,sp}$ was observed. The relationship between $I_{d,max}$, and $R_{ON,sp}$ with temperature indicates that the channel resistance is increased under thermal influence. Therefore, the temperature negatively affects the carrier mobility

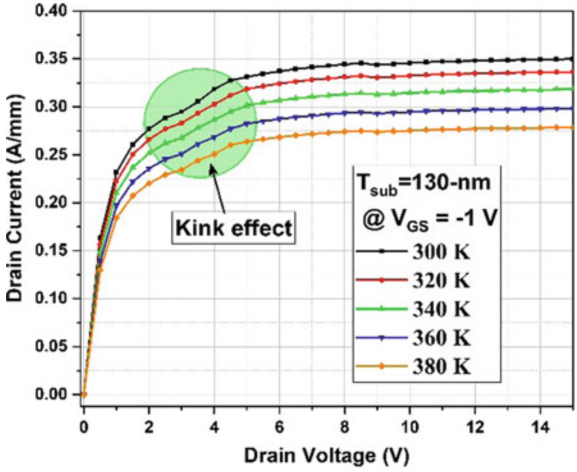

Fig. 7 Illustration of the Kink effect at different temperatures

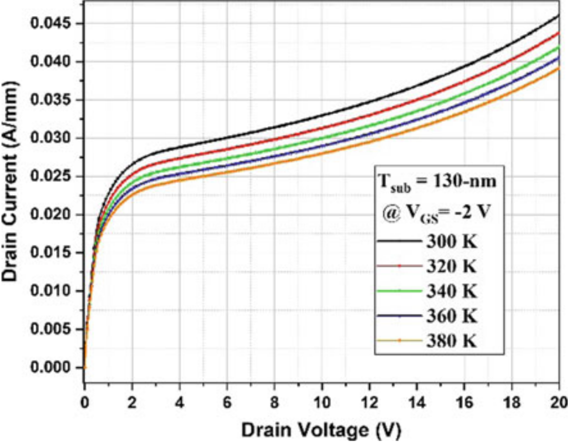

Fig. 8 Illustration of the impact of temperature variation at $V_{GS} = -2$ V for substrate thickness of 130-nm

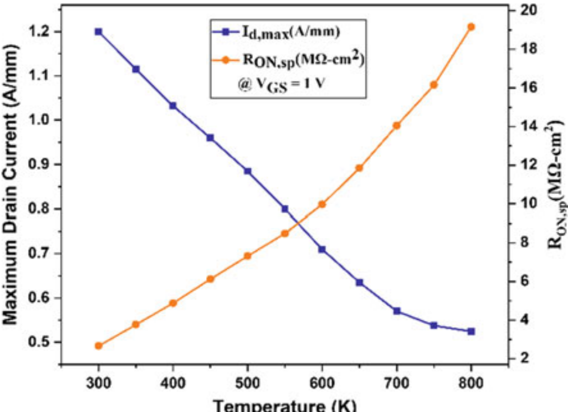

Fig. 9 Illustration of the analogy between maximum saturated drain current and Ron under impact of temperature variation

owing to scattering phenomena, particularly those that are phonon related. The increase of lattice vibration causes an increase in phonon scattering with temperature rises. As a corollary, the movement of the charge carriers in the channel is diminished. Therefore, diminished carrier mobility leads to a reduction in drain current.

4 Conclusion

In this chapter, the effect of temperature which is a primary issue for reliability at device level is investigated. This work is successfully investigated the temperature analysis of proposed field-plated recessed gate III-nitride HEMT grown on β-Ga_2O_3 substrate on drain current performance. It is noticed that, as the temperature increases, the drain current is reduced which further decreases the performance of the device.

This is due to the emergence of scattering mechanisms developed with the temperature rises. Particularly increment in phonon scattering, lattice vibration with the rise in temperature leads to deterioration in 2DEG mobility. Further, the results confirm that the self-heating effect also diminishes the output current along with the temperature impact. So, at 300 K, the substrate thickness has a substantial effect, and as the temperature increases, the impact of the substrate thickness on the output current is insignificant. We concluded that self-heating has a huge impact on drain characteristics at higher gate voltages, but it is not apparent at lower gate voltages. Finally, the investigation presented in this article can be beneficial for developing III-nitride HEMT grown on β-Ga_2O_3 substrates at different temperature values.

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Prospects of III–V Semiconductor-Based High Electron Mobility Transistors (HEMTs) Towards Emerging Applications

E. Raghuveera, G. Purnachandra Rao, and Trupti Ranjan Lenka

1 Introduction

High-speed devices are very much needed in day-to-day life in broad areas like mobile communications, RF technology, Nanoelectronics, etc. This can be achieved by developing a device with high mobility and high speed. Also, the materials used to fabricate these devices for such applications may differ. The invention of such devices is very much needed since the 1980s tremendous research has been carried out towards the development of high-speed devices to achieve such speeds. T. Mimura, a scientist from Fujitsu Laboratories Ltd, Japan involved in the characterization and fabrication of high-frequency, high-speed devices using various compound semiconductors (Group III–V). A device with high speed and high frequency is also used in applications where high power is needed, namely High Electron Mobility Transistor (HEMT), the name given T Mimura at Fujitsu Laboratories, the same device named with different names at different organizations, Modulation-doped FET (MODFET) by the University of Illinois, SDHT (Selectively Doped Hetero Junction Transistor) by AT&T, Bell labs, TEGFET (Two-dimensional Electron Gas FET) by TCSF, this imply that the channel conduction occurs along the channel with in a thin sheet of charge, and also termed as separately doped FET (SDFET) this is to emphasize that the doping occurs in a separate region from the channel. The first HEMT was commercially available in 1985 and is used at NRO (Nobeyama Radio Observatory),

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Nagano, Japan [1] as a low-noise amplifier (cryogenic). The traditional MOSFETs and MESFETs are built with very shot channels (nm) more charge carriers suffer from minimum impurity scattering with degraded performance. The HEMT is a device with a heterojunction and is used for high-speed applications. The need for hetero junctions comes about due to various reasons. The proposed paper is organized as Sect. 2 of the paper discusses the basic concepts of heterostructures and the related work of these heterostructures carried out in Sect. 3, the detailed description of heterojunctions is given in Sect. 4, and the conclusions are discussed in Sect. 5.

2 Basic Concepts

In the case of MESFET, the threshold voltage (V_{T}) shifts in a negative direction when the channel becomes short. The subthreshold slope becomes larger, and the ideality factor n_g shows a higher value. It is become difficult to turn off the device that is guided by a factor n_g. The above-said reasons are due to the 2-D effects in the channel direction. The way to do that increases the field in a particular direction that is larger compared to the field along the channel, this is achieved by raising the doping concentration N_D. The short channel effects are reduced by changing (increasing) doping density N_D of channel and reduction in the thickness of the channel, raising N_{D} in the channel poorly disturbs mobility and velocity overshoot. This problem of mobility getting affected by doping is common for all devices. In the case of GaN MOSFET [2] of Fig. 1a, miniaturization of the length of the channel outcomes in the scattering of the depletion region from drain to source, the depletion region width is reduced by changing the doping concentration to a higher level, increase in doping near channel results in an increase in V_{T}, the increase in V_{T} is controlled by an oxide layer thickness. MESFET is, version of MOSFET without an oxide layer. In either case, an increase in doping is inevitable. Ultimately what we are doing is actually providing a provision for finite channel length and will have a large concentration of electrons. If the doping is high and when the channel is inverted, have high electron concentration in the channel, this results in constant current density even for a lower electric field because current density is comparative to the electron concentration and the field (electric).

The increase in doping concentration also overcomes the problem of channel punch through, the same as in the case of MESFET. The remedy for all these issues and to achieve high-speed and high doping concentration is to use hetero junction transistors so that donors are separated from the region where movement of charge carriers e^- takes place. High concentrations can be achieved using some different transistors called hetero transistors, and with these transistors, we will see that possibility to ensure movement of electrons will be taken place where doping is little. In MOSFET, the electrons transportation takes place in the highly doped regions.

The electrons are confined in the channel due to the notch present at the channel in the energy band diagram of MOSFET [4] (Fig. 2), the e^{-}'s are confined near channel due to barrier even in equilibrium conditions. A similar phenomenon with hetero

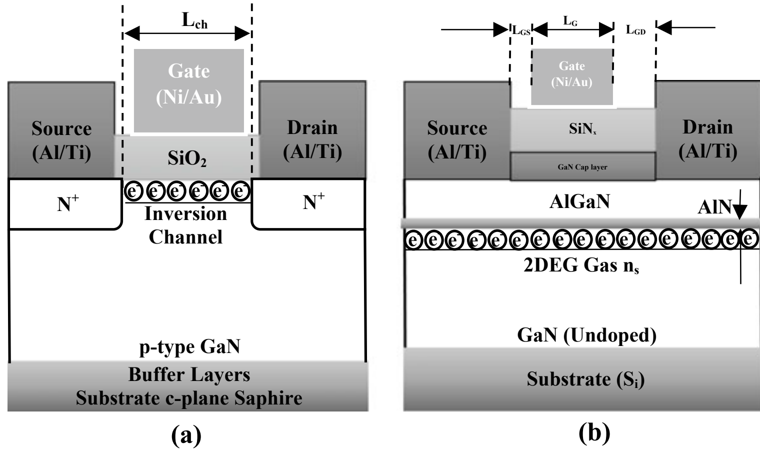
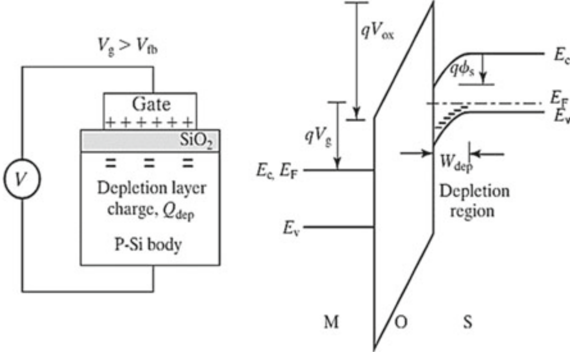


Fig. 1 Schematic of **a** GaN MOSFET, **b** HEMT [2]

junctions, the only difference is that the barrier height is very large (≅ 3.3 eV), and it is very difficult for the electrons to surmount the barrier that exists, these electrons through the barrier when the thickness of the oxide is low, even in OFF state high current tunnelling from channel to the gate results in gate leakage current, power dissipation etc. The remedy is to resolve all these issues to change the device structure.

Similar to the MOSFET energy band structure (Fig. 2), the same band bending is present in the PN junction [5] without any imprisonment of charge carriers e^-'s because of the roll down of charge carriers e^-'s towards n-side and in the same way to the p-side when it is about to reach equilibrium. In the case of MOSFET, there is no movement of charge carriers (electrons) to gate from channel, and all the electrons are accumulated in the channel. Ultimately, it is required to design a structure where the confinement of electrons near the barrier and the problem of tunnelling can be eliminated. The MOS HEMT shown in Fig. 1b, structure HEMT

Fig. 2 Energy band diagram of the MOS capacitor [3]



is similar to GaN MOSFET, the key variance among the two devices is that in the case of GaN MOSFET the electrons are confined in the channel, whereas in the case of MOS HEMT [2] 2DEG gas is developed and the electrons are confined in the notch. Figure 3a shows drain characteristics of GaN MOSFET, it is clear from the graph that, the o/p current is about 1 mA for gate to source potential of 22 V, drain voltage which depends on gate voltage is evaluated at constant drain voltage [2]. The difference of I_D on par with the temperature (Fig. 3b) for a constant V_D is described.

Figure 4 shows the voltage current characteristics at different temperatures. The maximum current density (drain) is obtained at room temperature in Fig. 4b, and is noted that, the significant reduction in drain current with temperature [2].

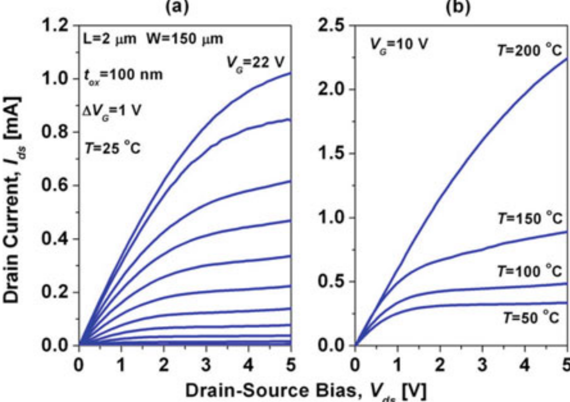


Fig. 3 GaN MOSFET V_{ds} versus I_{ds} characteristics: **a** Gate voltage, **b** Temperature [2]

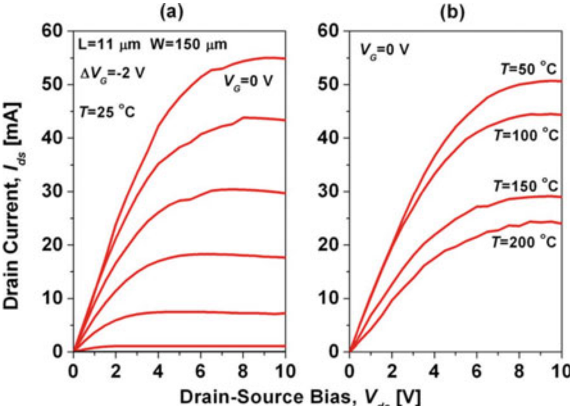


Fig. 4 MOS-HEMT AlGaN/GaN V_{ds} versus I_{ds} characteristics: **a** Gate voltage, **b** Temperature [2]

3 State-of-Art Research

AlGaAs semiconducting material-based devices are the most suitable, and the barrier material GaAs have good lattice match. Hence this heterostructure became most popular and is incorporated in most of the HEMTs. Further, AlGaN/GaN-based devices came into existence with satisfactory performance and are extensively used in current research, the devices made with these materials operate at very high-frequencies, have high-breakdown energy and have high-velocity saturation [6] also these devices are best suitable for biosensing applications [7]. One of the best features of GaN is its strong piezoelectric polarization results in the growth of carriers at AlGaN/GaN edge. The schematic drawing of the various popular structure of HEMTs depicted in Fig. 5 [8, 14, 23–26] application and the device performance discussed in [8] the foremost GaAs material-based heterostructures in Fig. 5a is capable of separating the electrons (majority charge carriers from the impurities, rapid hetero-junction are being created between the narrow and wide bandgap materials GaAs and AlGaAs respectively, the doping concentration of these devices may be around 7×10^{17} cm^{-3}, the channel is being formed between GaAs and AlGaAs heterojunction. One of the limitations of these devices is Columbia scattering which can be eliminated by a layer of thin AlGaAs (undoped) material formed and used as a spacer layer. Further developments of heterostructures carried out with different semiconductor materials, GaN-based heterostructures are developed in Fig. 5b, intentional doping is not required for AlGaN/GaN-based heterostructures, the charge carriers are accumulated from the states of the surface, and a spontaneous polarization may be identified with this structure. Hence intentional doping may not be required and results in development of high carrier concentration two-dimensional electron gas (2DEG) near the interface (AlGaN/GaN), an explicit function at the surface barrier.

The lower electron effective mass of the InGaAs materials in the channel layer is better when compared with the AlGaAs-based devices and has a huge conduction band offset ($\cong$ 0.5 eV) among channel and InAlAs [9], resulting in rise in mobility of e^{-}'s, high velocity saturation of electrons and high concentration of electrons, this device comprises of InGaAs/InAlAs interface, for improved ohmic contact the composite cap layer is being formed, an undoped InAlAs material forms a Schottky barrier for superior electron transportation properties Fig. 5c. The 2DEG is further enhanced for better performance with good lattice match, enhanced charge density of a sheet in channel due to the great impulsive polarization charges that exist, even reduces the short channel effects with AlInN/GaN [10] devices in Fig. 5d. The Polarization effect discussed in [11], the key features of the AlGaN/GaN heterostructures, that these structures can yield 2DEG gas with an undoped material, spontaneous polarization and piezoelectric attributes from Group III nitrides will also be an important feature of AlGaN/GaN heterostructures [12]. Heterostructures made by AlGaN/GaN are extensively used in Microwave and RF applications [13] as GaN with wide-bandgap with enhanced I_d and wide breakdown voltage. GaN is a capable device for MMICs (Monolithic Microwave Integrated Circuits) and radio frequency amplifiers. In the heterostructure shown in Fig. 5e, the substrate material used is β-Ga_2O_3

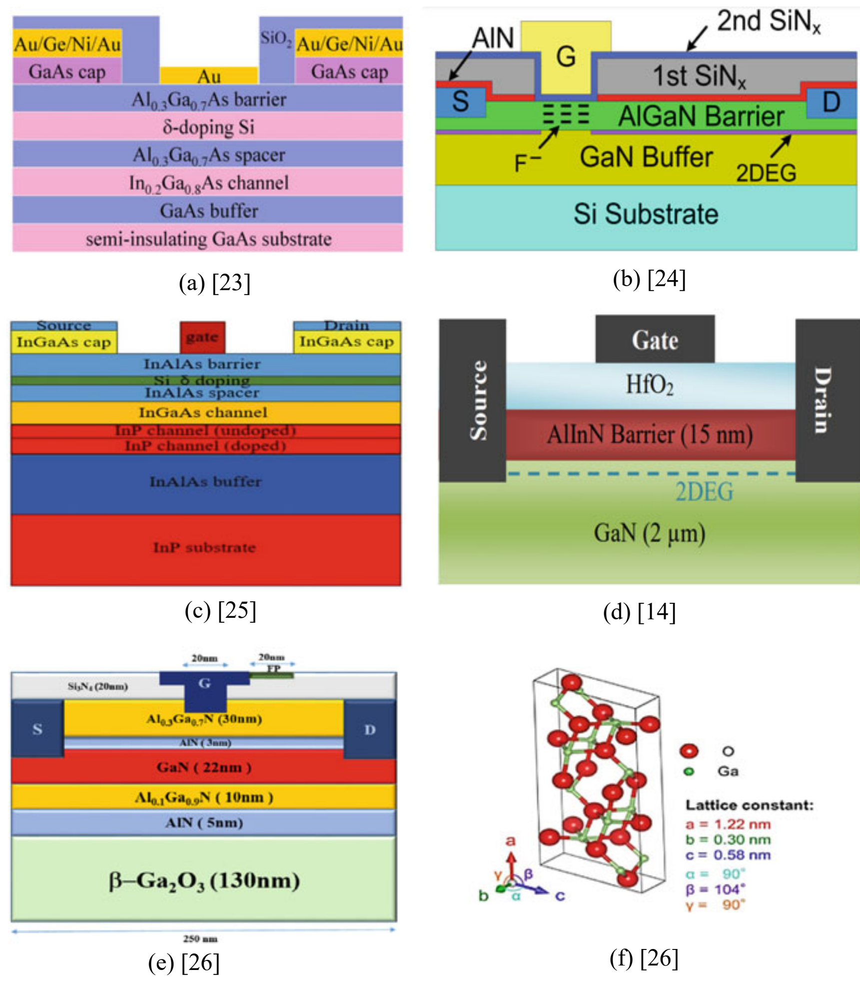


Fig. 5 Schematic of the **a** AlGaAs/GaAs HEMT [37], **b** AlGaN/GaN HEMT [38], **c** InGaAs/InP composite channel InP-based HEMT [39], **d** AlInN/GaN MOSHEMT [14], **e** AlGaN/AlN/GaN with field-plate on β-Ga_2O_3 Substrate [40], **f** The lattice structure of β-Ga_2O_3 [41]

[14] due to its high breakdown voltage and large bandgap (4.6–4.9 eV), hence used for high-power applications; these structures also have excellent transport properties [15]. β-Ga_2O_3 crystal structure, shown in Fig. 5e, consists of five different polymorphs α, β, γ, δ and ε; the lattice constant of these polymorphs is also shown [16] (Fig. 5f). AlGaN/AlN/GaN HEMT (recessed gate) on β-Ga_2O_3 substrate is proposed [14, 17] by incorporating a mechanism called field-plate mechanism and is analysed similarity with AlGaN/AlN/GaN HEMT (recessed gate). The recommended device structure on the chosen β-Ga_2O_3 substrate is good contender for forthcoming high-power nano device applications. A study of III-Nitride [18] Nano-HEMTs on various

substrates stated in [19, 20] used for latest High-Power Nano and millimetre wave applications. The improvement in performance of III-Nitride/β-Ga2O3 Nano-HEMT discussed in [21] is used for the performance enhancement of HEMT. III-Nitride-based HEMTs for THz applications [22] discussed and investigated performance characteristics such as noise power and THz detector response. The GaN HEMT discussed in [23] is used for high-power, reverse injection microwave pulses and duration of the amplitude relations are investigated. A technique called molecular beam epitaxy presented in [24] used improve structural, optical and electrical properties. Organic Field Effect Transistor (OFETs) [25] achieve very high electronic mobility by incorporating a TTC (Tetratetracontane) interfacial layer between C60 and dielectrics. A multi gigahertz AlGaN/GaN RBT (Resonant Body Transistor) reported in [26] is especially meant for extracting electrical modulation and mechanical resonance at the same time. QF (Quality factor) of 250 realized at 4.23 GHz (Resonant Frequency) and in addition to this an acoustic transconductance of 25 μS also achieved. The pseudomorphic HEMT (pHEMTs) discussed in [27] used in microwave applications, the performance metrics line noise, power linearity have been improvised. GaN HEMT-based amplifier for power applications presented in [23], it is observed that a novel interference phenomenon when microwave pulses were injected through the output port. InAlN/GaN HEMTs [28] on substrate (silicon) have been more attractive and pay attention due to the scaling capability and cost-effectiveness of Si substrate. HEMTs [29] designed and demonstrated a review for low-power and low-noise at millimetre wave frequency ranges majorly used to attain better performance. High breakdown voltage HEMT (HB-HEMT) proposed in [30] is used to progress the break-down voltage and Baliga's FOM (Figure of Merit) and shows improved switching characteristics. InGaAs/InP HEMTs [31] used to develop advanced low noise amplifiers governing the charge carrier transportation in association with the noise. GaN electronics in geostationary orbit reported in [32], it is observed the variation in the o/p power of the Colpitts oscillator designed by four GaN transistors. A recess free AlGaN/GaN HEMT (E-mode) [33] with field assemble structure (FAS) has great latent for use in power converters, MMICs, and other applications. the design space for delta-doped β-$(Al_xGa_{1-x})_2O_3/Ga_{\{2\}}O_3$ HEMTs [34] delta-doping effect properties on device V_{TH}, g_m, and breakdown voltages (BVs) were explicated. GaN metal–oxide–semiconductor MOS-HEMT [35] using atomic-layer deposited (ALD) Al_2O_3 as the gate dielectric is analysed the similarities with AlGaN/GaN device, improved in mechanism in interface, reduced leakage current, and observable capacitive potential (C-P) hysteresis being found, the dominance of MOS-HEMT structure with ALD Al_2O_3 as a gate dielectric is revealed.

3.1 Heterojunctions

The accumulation of electrons, like in the case of MOSFET near the channel in Fig. 2, may be carried out by using different materials and device structures, in the case of MOSFET, lightly doped P—substrate is of narrow bandgap (1.1 eV)

material, whereas the oxide layer (S_iO_2) insulator is wide bandgap (8.8 eV) material; hence there is a confinement of electrons near the barrier. Position and charge of 2DEG dependent of gate and drain voltages with respect to source, in the case of HEMT, 2DEG plays a vital role. The HEMT characterized by an corresponding Buried channel (BC) MOSFET discussed [36] may be useful for the purpose of analytical comparison between the BC MOSFET and HEMT. It is clear that to form a heterojunction, use the substrate of a narrow bandgap and the other of the wide bandgap such that the electrons can be confined. The velocity overshoot and high mobility of electrons can be achieved by replacing the P-type substrate of MOSFET with undoped, doped narrow bandgap material G_aAs and joining with wide bandgap material, hence the name "Heterojunction". Hetero junctions are junctions formed by different materials (dissimilar semiconductors), the hetero junctions are of two types, one is of an iso-type heterojunction, and the other is of an aniso type heterojunction. In an iso-type hetero junction, the conducting materials are of the same type, wide bandgap P-type and narrow bandgap p-type or wide bandgap n-type and narrow bandgap n-type. Similarly, in an aniso type, the conducting materials are of the different types, wide bandgap n-type and narrow bandgap n-Type, these junctions are formed with the different crystals.

3.2 *Lattice Constant*

One of the most important properties of hetero junctions is that, to form a junction there must be a lattice match, if there is a lattice mismatch there will be a defective region, even for lattice mismatch in fractions (0.6), there will be a defective region. Ultimately, when they grow on top, we may have a good layer, for the layer thickness, say 0.5 μm or 1 μm or even less, we will have scattering problems, and these layers will be very defective.

$$\text{Lattice constant}\, x = \left[\frac{nM}{\rho N}\right]^{1/3} \tag{1}$$

where M is the molecular weight, N is Avogadro's number, n is the number of atoms per unit cell, and ρ is density. If we want to dope, add a dopant also to gas like hydrogen sulphide gas or sulphur monochloride gas, and we get sulphur doping, or if we use saline, we get silicon-doped AlGaAs. These issues are with the SOS (Silicon of Sapphire) being a single crystal, and at a particular orientation, lattice match is good and is better than other orientations. AlGaAs/GaAs materials have excellent lattice match between the material, when we grow GaAs (Gallium Arsenide) on AlGaAs using a popular and easy method called MOCVD (Metal Organic Chemical Vapour Deposition), $Al_xGa_{(1-x)}As/GaAs$ when we grow gallium arsenide, we have an arsine and trimethyl gallium, after a certain thickness of the GaAs add trimethyl

gallium and trimethyl aluminium together by adjusting the fluorides properly so that lattice constant 'x' can be adjusted (Eq. 1).

The number of dopants that add will decide the doping concentration, we may have undoped $G_aA_{s,}$ and on that, AlGaAs may be grown and can be doped, we will have a layer which is doped and an undoped layer. When we say undoped, it is not doped intentionally, but there is unintentional doping is always present. Generally, it turns out to be P-type due to some of the impurities. We may not get N-type at a lower temperature, if we grow, it is definitely going to be P-type due to carbon concentration. Similarly, there is a carbon concentration of some of the gases, this transfer to the P-type may be $10^3/cm^3$ very lightly doped.

The bandgap may be varied as lattice constant (x) varies from 0 to 1. From Eq. 1, for $x = 1$, AlAs is a wide bandgap material with an indirect bandgap of (2.17 eV), and $x = 0$ gives GaAs as a narrow bandgap material with a direct bandgap (1.43 eV) Fig. 6. The actual bandgap is the gap whichever is minimum, the electrons tend to occupy the lower level at the conduction band edge, if we vary x for $x = 0$, the bandgap is 1.43 eV (GaAs), increase in x will also have linear (not exactly) increase in the bandgap, and it matches with 3.02 eV (AlAs); similarly, 1.87 (GaAs) matches with 2.17 eV (AlAs) Fig. 6.

The direct bandgap of GaAs 1.43 eV directed towards AlAs 3.02 eV direct bandgap is almost linear (not exactly). Similarly, the indirect bandgap of GaAs 1.8 eV drives to directed towards AlAs 2.17 eV indirect bandgap (Figs. 6 and 7). It is clear from Fig. 7 that till the lattice is constant $x = 0.3$, the direct bandgap is smaller than the indirect bandgap up to some levels (1.92 eV) beyond the point (0.3, 1.92), the direct bandgap larger than that of the indirect bandgap, also at $x = 0$ it is direct bandgap, and at $x = 1$ its indirect bandgap, in between there is a transition between direct to indirect. Similarly, for $Ga_xIn_{(1-x)}As$, InAs with the direct bandgap of 0.36 eV at x

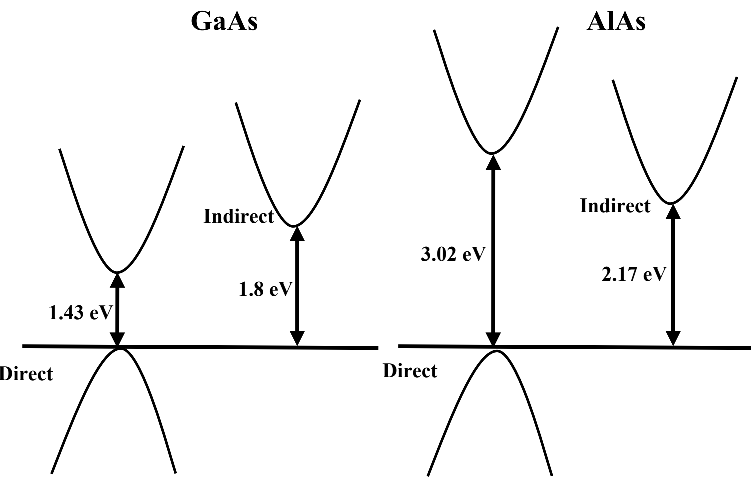


Fig. 6 Energy band diagram of AlAs & GaAs

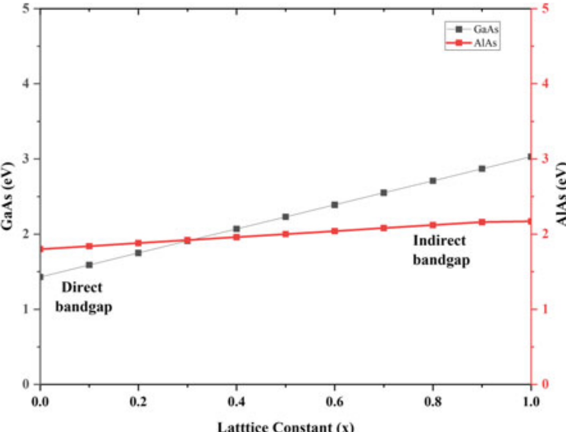


Fig. 7 Bandgap energy and Lattice constant for $Al_xGa_{(1-x)}As$

= 0, GaAs with the direct bandgap of 1.43 eV, here there is no question of indirect band gap (Fig. 8). The key point to remember is on what substrate we may grow gallium indium arsenide, when we mix indium arsenide and gallium arsenide, we get a bandgap which is actually matches with indium phosphide InP. Most popular binary and atomic semiconducting materials [42]. It is noted that, modifying the quantitative study of the products involved and reactants in a chemical reaction not only changes the bandgap energy but also the lattice constant, it can be unstated as in the crystal it is an average distance between the atoms. This is the major complication due to the change in the lattice constant when devices are being designed. If we are using gallium arsenide-based devices, hetero junctions are formed by AlGaAs on GaAs. If we are using an indium phosphide-based substrate, hetero junctions are formed by GaInAs on InP, and that has a good lattice match with gallium (0.47). The important point to remember is that, the material $Ga_xIn_{(1-x)}As$ has good lattice match with InP when $x = 0.47$ i. e. $Ga_{0.47}In_{(0.53)}As$ and is implies to 47% of gallium and 53% of indium is used for good lattice match when we want to grow $Ga_xIn_{(1-x)}As$ on InP. In a similar manner AlAs can be grown on GaAs for any value of x $(0 - 1)$, the bandgap of GaAs 1.43 eV and AlAs is 2.17 eV may have a good lattice match anywhere in the bandgap. In case of InP based devices, heterojunctions are made with GaInAs and GaAs invariably AlGaAs.

4 Comparative Analysis

The parameters like channel length, channel width and substrate doping for both BC MOSFET and HEMT are identical, the representation of BC MOSFET as HEMT which satisfies three criteria, firstly, the total areal 2DEG concentration of HMET is equal to the spatial concentration of doping near channel of the BC MOSFET, secondly, the relation between the gate voltage and depletion charge near channel

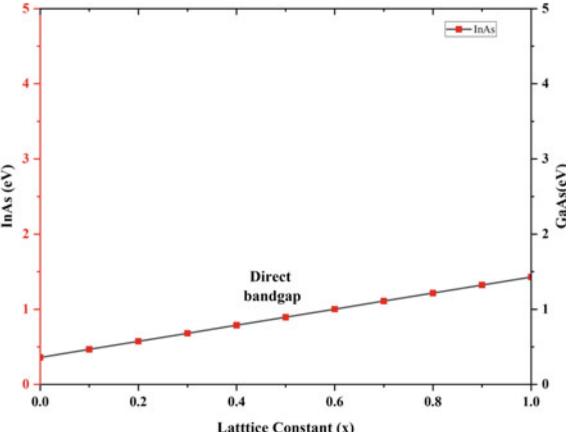


Fig. 8 Bandgap energy and lattice constant for $Ga_xIn_{(1-x)}As$

managed by the device is invertible and integrable, lastly the conduction charge and the depletion edge in the BC MOSFET follow the 2DEG position and the 2DEG in HMET respectively on par with gate voltage [36]. HEMT and MOSFET give in Fig. 1a, b have similar active areas of source and drain dimensions, it is noted clearly that, HEMT devices are proficient to deal with high currents, to assess these properties of the current, the precise on resistance projected with power device (Eq. 2). ON resistance of both MOSFET and HEMT linked to the channel layout (Eqs. 3 and 4) and properties electron mobility by investigative associations for low crosswise fields [43].

$$\frac{1}{R_{\text{on}}} = \frac{\partial I_{\text{ds}}}{\partial V_{\text{ds}}} \frac{1}{\text{WL}_{\text{a}}} \tag{2}$$

where L_a is active area of devices with high power near carrier flow with in device and W is the channel width.

$$R_{\text{on}}(\text{MOSFET}) = \frac{L_{\text{ch}}^2}{\mu_n C_{\text{ox}}(V_{\text{gs}} - V_{\text{th}})} \tag{3}$$

$$R_{\text{on}}(\text{HEMT}) = \frac{L_{\text{ds}}^2}{q\mu_n n_s} \tag{4}$$

Figure 9a shows the specific on resistance for HMET and MOSFET is extracted at various voltage levels and it is observed as the on resistance is above the pinch-off in both the devices (Fig. 9a). At room temperature, the precise ON resistance of the MOSFET is about hundred and twenty times more when it is compared with the equal rated HMET device. From Fig. 9b, the contact resistance is measured from the method TLM and is found that it is at least twice the orders of magnitude below the R_{on} extracted for both MOSFETs and HEMTs. Hence it is assumed that the contact

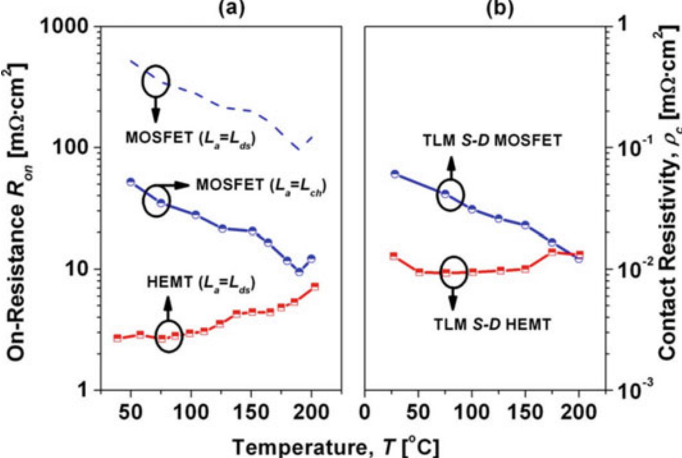


Fig. 9 **a** Transistor on resistance R_{on} versus T of MOSFETs (various active areas) and HEMTs, **b** evaluation of contact resistivity with T [2]

resistance measured TLM is a second order factor when compared with the channel contribution.

5 Conclusion

The past and the future of high-speed devices are purely dependent on the heterostructures; these structures are being modelled, simulated and characterized by compound (Group III–V) semiconducting materials. With a proper selection of materials to form these heterojunctions and the confinement (2DEG) of the majority charge carriers near the junction, a device with better performance and high speed is achieved. The material used to create heterostructures like AlGaAs, AlGaN, and InP have shown the best performance toward high-speed application. The key point to be remembered before we create heterostructures is their lattice constant, it is required to choose materials to form heterojunctions with good lattice match. The comparative analysis between MOSFET and HEMT were analysed and it is concluded that, HEMTs are being used as high-power device when compared with MOSFET. Various structures are also discussed and these structures are used in various applications like RF, Microwave and High-power devices and are also tremendously used in biosensing applications.

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Modulation of Energy Bandgap in Graphene Nanoribbons Using KWANT

Sradhanjali Lenka, Ajit Kumar Sahu, Madhusudan Mishra, and Narayan Sahoo

1 Introduction

Graphene is a two-dimensionally arranged hexagonal honeycomb structure of sp^2-hybridized carbon atoms which have a very high surface to volume ratio, thin, and strong material ever formed [1–3]. It is optically highly transparent and possesses the highest conductivity of heat and electric current among all materials [4]. The band gap, which actively contributes to the conductivity and wavelength of light that is to be emitted from a material (like semiconductor), is ideally zero for prestine graphene. Generation and control of the band gap are needed for the creation of desirable electronic and optical properties [3]. Materials with different band gap ranges are suitable for different activities. The narrow band gap materials like $Hg_xCd_{1-x}Te$, VO_2, InSb, etc. are used as infrared photodetectors and thermo-electronics [4]. The wider band gap materials, that is, Si, GaAs, GaP, GaN are used in electronics, optical devices like light-emitting diodes and solar cells, LASERs, etc. To cater the demand for several device applications, the band gap in graphene is being tuned using different techniques such as chemical doping, application of field, changing the size of width [4–16], applying antidot, and applying strain to the graphene sheet, etc. [9–19].

Owing to their unique structure and properties, the GNRs have additional advantages over graphene sheets and are considered one of the most auspicious materials for future nanoelectronics [13]. According to their edge morphology, they are

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divided into two types, that is, Zigzag (ZNR) and Armchair graphene nanoribbons (AGNR). If the edge is zigzag type, the GNR will show metallic property with zero bandgap but in the case of armchair type, the GNR will show both metallic as well as semiconducting properties as per the number of atoms (N) present in a width [16].

Chen et al. [9] investigated the significance of controlling the electrical bandgap for use in future GNR applications. At the atomic level, they modified the width and edge geometry of GNRs' bandgaps. They have noticed a localized electronic state for $N =$ 13 AGNRs which is related to sp^2-hybridised carbon atom terminated with hydrogen at the zigzag termini. Wang et al. [10] simulated the effects of change in chemical edge on structural and electrical characteristics using tight-binding computations. They found that when edge carbon atoms of GNRs which are attached to various atoms, there are noticeable variations in the C–C bond lengths and bond angles nearby. Zoghi et al. [11] investigated the electrical characteristics of AGNRs and have shown that the band gap could be adjusted by introducing antidotes into the original GNRs and developed antidote super lattice AGNRs. Philipp et al. [12] investigated the effect of edge functionalization on the structure and electrical properties of GNRs. They have used edge-functionalized AGNR, ZNR, and rebuilt Klein-type GNRs with H, F, Cl, Br, S, SH, and OH. They mentioned that a suitable mechanism for adjusting the band gap of AGNRs is the edge-functionalization design.

In this chapter, we have investigated the bandgap of graphene by using a python-based simulation tool KWANT [20]. It is an open source, powerful, and user-friendly Python module for numerical calculations based on tight-binding models with a strong focus on quantum transport. We also tune the bandgap of GNRs by varying its width. We show that in the case of ZNR, even though the width changes from 12 to 22 Å, the bandgap remains zero. It shows the metallic nature of the ZNR. However, in the case of AGNRs, as the width changes, depending upon the number of atoms present within the width, the bandgap varies and it reduces with increase in the width. Our results will be helpful in the study and applications of graphene and its related nanoribbons in the design of optoelectronic devices as well as 2D nanostructure electronic circuits which can be done using KWANT, based on user convenience.

2 Theory

2.1 Graphene: The Wonder Material

Graphene is a single layer of SP^2-hybridized carbon atoms tightly bound in a hexagonal honeycomb lattice, which was discovered by Andre Geim and Konstantin Novoselov, who received the Nobel Prize in Physics for this in 2010 [4]. The sp^2-hybridized carbon atoms in graphene have three hybridized s-orbitals and one unhybridized p-orbitals. Six sp^2 hybridized carbon atoms combine to form a hexagonal lattice structure. The s–s orbitals overlapping form the σ-bond of bond length $a =$

1.42 Å, which represents the plane of the graphene sheet. The sidewise overlapping of p-p orbitals forms π-bond perpendicular to the plane. The p-orbitals overlap to form a filled valence band whereas conduction band is empty with a zero-band gap. The conduction band meet with valence band at Dirac point or known as k-point, forming conical shaped band. Schematics for the sp^2 hybridized carbon atom, six carbon atoms forming σ and π-bond, and an overall graphene sheet are represented in Fig. 1a–c, respectively.

Properties of graphene can be studied depending on the number of layers involved, such as a single layer, bilayer, tri-layer, and multilayer graphene, as shown in Fig. 2. The atoms in a hexagonal cell of a single layer graphene (SLG) are denoted as A and B atoms depending upon their associated σ-bonds (Fig. 2a). In bilayer graphene (BLG), the atoms of the bottom graphene sheet's hexagonal lattice center are directly covered by half of the atoms in the upper layer (Fig. 2b). So, the symmetry between two sub-lattice is broken and such type of stacking is called Bernal stacking [9]. In the case of tri-layer graphene, the layers can be placed in two ways A-B-A or A-B-C, as indicated in Fig. 2c, d, respectively. In the case of BLG, the energy bands are parabolic whereas, for a single graphene sheet, it is conical. Applying an external electric field (E), energy gap in BLG can be created. The schematics for energy band for a SLG, BLG and BLG in presence of E are presented in Fig. 3a–c, respectively. As it can be noticed, the Dirac point vanishes for BLG, while for a BLG under electric field, certain amount of band gap appears, along with a shift in the Fermi level in the direction of applied field.

The facts that lead to graphene being treated as the wonder material include its outstanding electrical, thermal, mechanical, and optical properties. It is 60% more conductive than copper and 200 times harder than steel with a Young's Modulus of 1TPa [4]. It shows thermal conductivity of 5300 Wm^{-1} K^{-1}, and maintains at 600 Wm^{-1} K^{-1} when based on a SiO_2 substrate [2]. Graphene has a carrier concentration of 10^{13} cm^{-2} so the carrier mobility is 0.5×10^6 cm^2/Vs. It is 97.7% transparent to white light with 2.3% of absorbance, with the optical response of $\alpha = e^2/hc = 1/(137.036)$. Owing to $\pi\alpha = 2.3\%$, graphene is visible without a microscope.

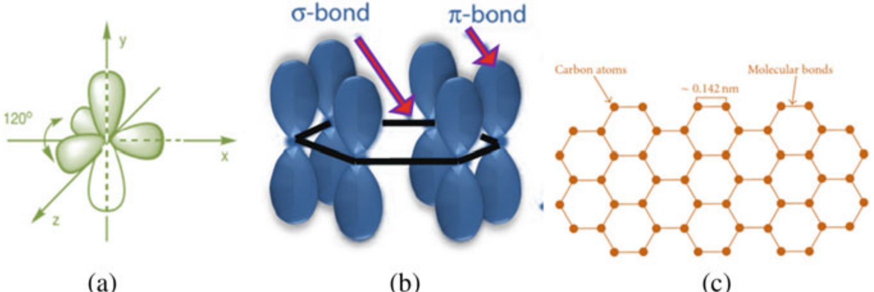

Fig. 1 Schematics for the sp^2-hybridized carbon atom (**a**), six carbons atoms forming σ and π-bond (**b**), and overall graphene sheet (**c**) [4]

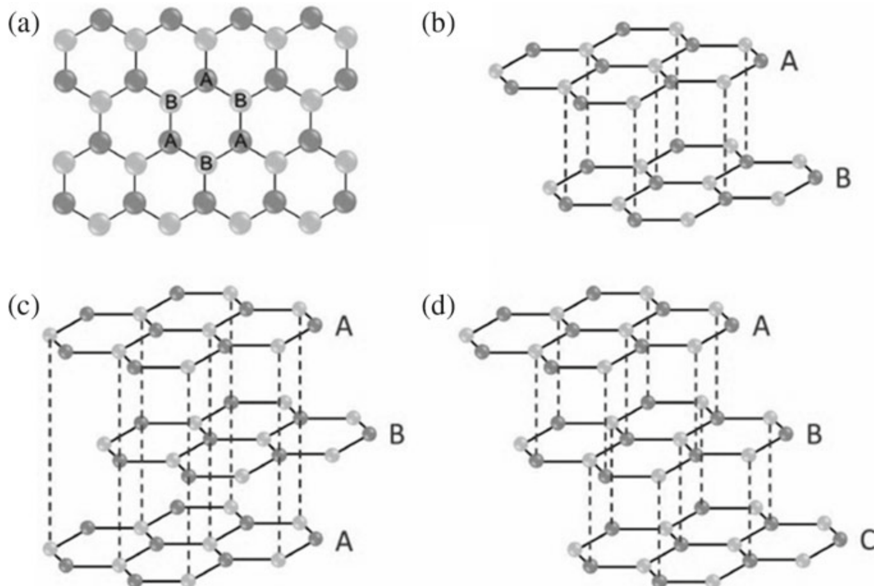

Fig. 2 Schematic representation of single layer (**a**), Bi-layer (**b**), Tri-layer of stack A-B-A (**c**) and stack A-B-C (**d**) graphene [7]

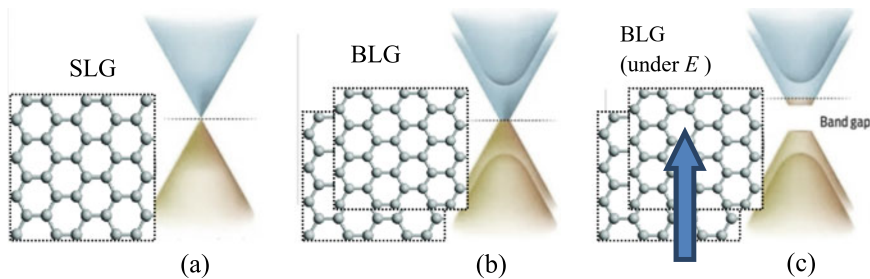

Fig. 3 Schematic of the energy band for a single layer (**a**), double layer (**b**), and double layer in the presence of electric field (**c**) respectively [8]

2.2 Graphene Nanoribbons (GNRs)

Graphene nanoribbons (GNRs) are geometrically terminated single-layer graphite strips of width less than 100 nm [2–4]. These narrow graphene strips are fabricated by cutting graphene sheets or carbon nanotubes through different techniques such as: cutting from graphene using lithography, bottom-up synthesis from polycyclic molecules, unzipping of carbon nanotubes (CNTs), etc. [6]. The electronic structure of GNRs strongly depends upon their edge geometry. This is because the dimension of the material becomes quasi-1D after cutting graphene into GNRs by limiting the

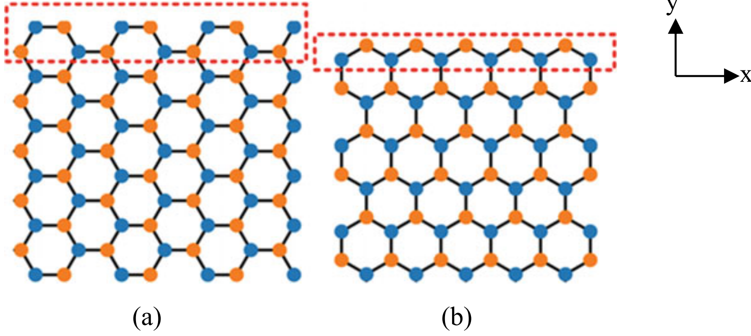

Fig. 4 Schematic of the honeycomb lattice with **a** AGNR and **b** ZNR layout

freedom of electrons in one more direction. As a result, the band structure of GNRs becomes width dependent and the zero-band gap property of graphene is lost. As discussed before, according to the nature of edges, GNRs are divided into two types such Zigzag (ZNR) and Armchair GNRs (AGNR).

In Fig. 4, we show the honeycomb lattice, where, the AGNR and ZNR edges are along *x*-axis. The lengths of both edges continue along *x* and finite in *y*-direction as present in Fig. 4a, b.

There were lots of work on the electronic structure of GNRs in the mid-1990 using tight binding approximation [2–13]. It is known that the ZNRs show metallic properties due to localized edge state fermi level showing zero band gap. The AGNRs show both metallic and semiconducting properties as per its number of atoms in width corresponding to $W = 3P$, $3P + 1$, and $3P + 2$; where P is an integer.

3 Results and Discussions

In this chapter, we have analyzed the band gap energy (E_g) of graphene nanoribbons (GNRs), by tuning width of GNRs, and the effect of external voltage on its energy band. Here, we have obtained *E*-*k* diagram of both ZNR and AGNR by using python-based KWANT tool. We show the lattice arrangements and the energy band structure of ZNR of length 15 Å having different widths i.e., 12, 16, and 20 Å in Fig. 5a–c respectively. Their corresponding *E*-*k* diagrams are also shown in Fig. 5a1–c1 respectively. Here, the atoms present along the width in Fig. 5a–c are 12, 16, and 20 respectively. We note that with an increase in width, there is no change in the bandgap, that is, E_g is always 0 eV. However, the closeness among the subbands decreases, that is, the density of states increases and it is maximum at $k = \pm 3.140$ at energy, $E = \pm 2.64$. Also, we note that closely placed intraband energy levels lead to an increment in conductivity. The band gap in AGNRs depends upon the number of atoms present across the respective GNR width. It shows three sets of configurations

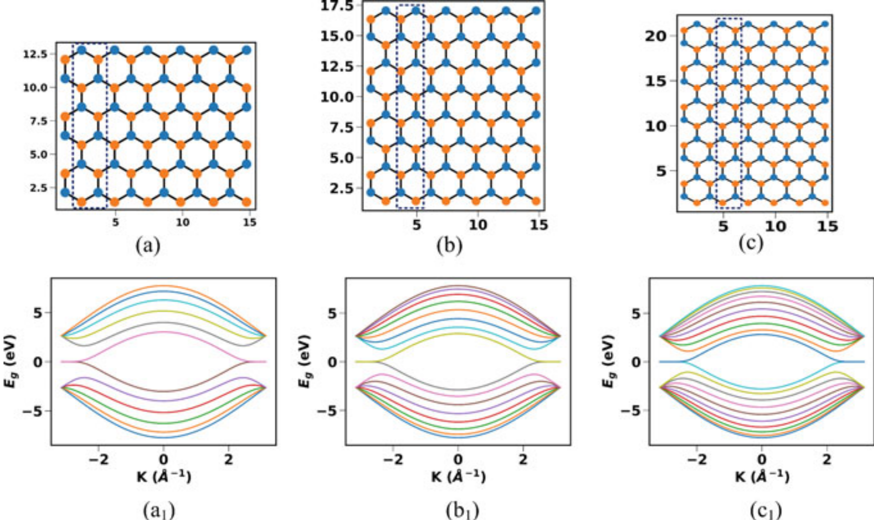

Fig. 5 Lattice arrangement and energy band of a ZNR for length 15 Å and width **a** 12 Å, **b** 16 Å, and **c** 20 Å, respectively. Their corresponding *E-k* diagrams are also shown in $\mathbf{a_1}$, $\mathbf{b_1}$, and $\mathbf{c_1}$, respectively

such as $3P$, $3P + 1$, and $3P + 2$ where P presents an integer. The band structure of different configurations are dissimilar and show both metallic and semiconducting properties.

We show the lattice arrangements and the energy band structure of an AGNR of length 15 Å for different widths, that is, 8, 19, and 30 Å in Fig. 6a–c, respectively. Their corresponding *E-k* diagrams are shown in Fig. 6a1–c1, respectively. Here, the number of atoms as shown in the rectangular boxes are 6, 15, and 24, which satisfies the $3P$ configuration, with $P = 2$, 5, and 8, respectively. We note that E_g changes to 1.304, 0.586, and 0.378 eV for widths of 8, 19, and 30 Å, respectively.

We present the energy band structure of a $3P + 1$ AGNR in Fig. 7, which have a length of 15 Å with different widths, that is, 9, 17 and 28 Å where the number of atoms in the widths are 7, 13, and 22, respectively. They satisfy $3P + 1$ configuration with $P = 2$, 4, and 7 respectively. Here, the number of atoms is 7, that is, $3P + 1$ configuration with $P = 2$. From the above figures, we note that, as the number of atoms increases from 7 to 22, the band gap reduces from 1.238 to 0.421 eV.

To study the impact of width variations in AGNRs with $3P + 2$ configurations, we present the *E-k* diagrams of AGNR having length of 15 Å but with different widths i.e., (a) 14 Å, (b) 18 Å, and (c) 29 Å having 11, 14, and 23 number of atoms along their width respectively. As we increase no. of atoms from 11 to 23, there is no change in the bandgap for $3P + 2$ configuration AGNRs and it remains 0 eV as shown in Fig. 8.

Also, to know the effect of the number of atoms (N) on E_g, we show E_g versus N in a width of AGNR which satisfied the condition of $3P$, $3P + 1$, and $3P +$

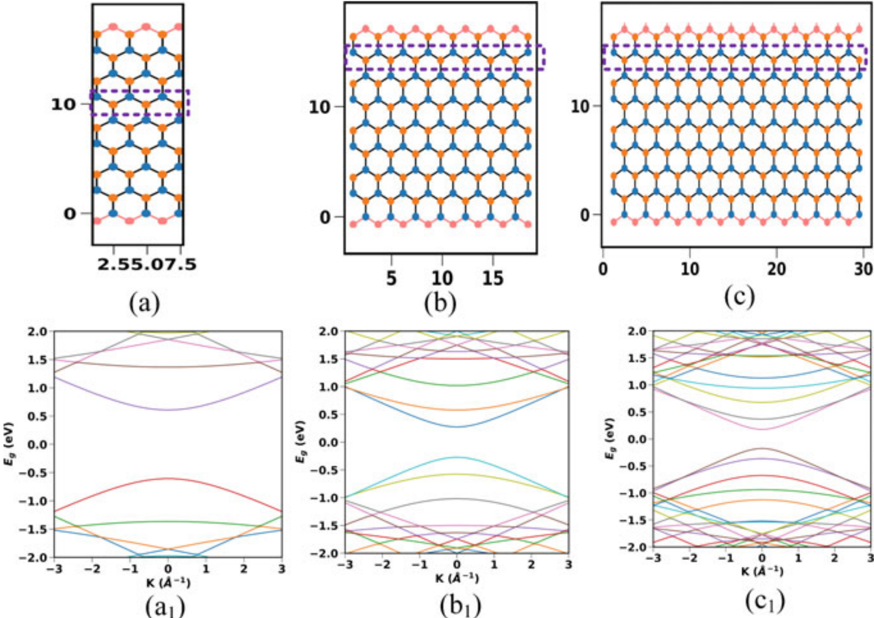

Fig. 6 Lattice arrangement and energy band of AGNR for length 15 Å and width **a** 8 Å, **b** 19 Å, and **c** 30 Å respectively. Their corresponding *E*-*k* diagrams are also shown in $\mathbf{a_1}$, $\mathbf{b_1}$, and $\mathbf{c_1}$ respectively

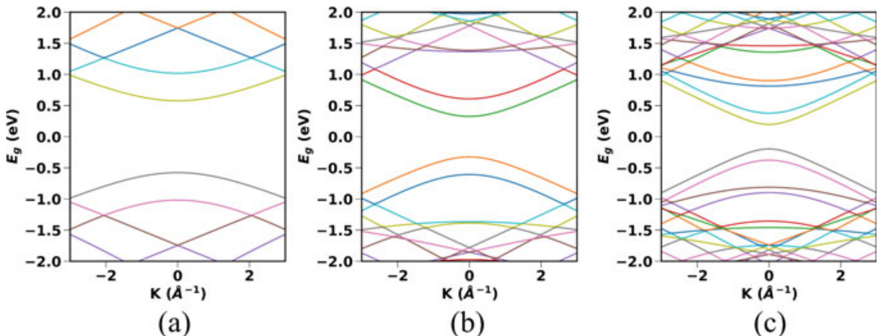

Fig. 7 Energy band structure of AGNR for length 15 Å and width **a** 9 Å, **b** 17 Å, and **c** 28 Å, respectively

2 configurations in Fig. 9a–c respectively. In each configuration, the length of the AGNRs is fixed, that is, 15 Å. We show that as the number of atoms present in that width enhances in $3P$ and $3P + 1$ configuration, there is a reduction in E_g; however, in the case of $3P + 2$, there is no change in the bandgap and it remains 0 eV. However, like in the previous cases, here also as N in the width of the AGNR increases the

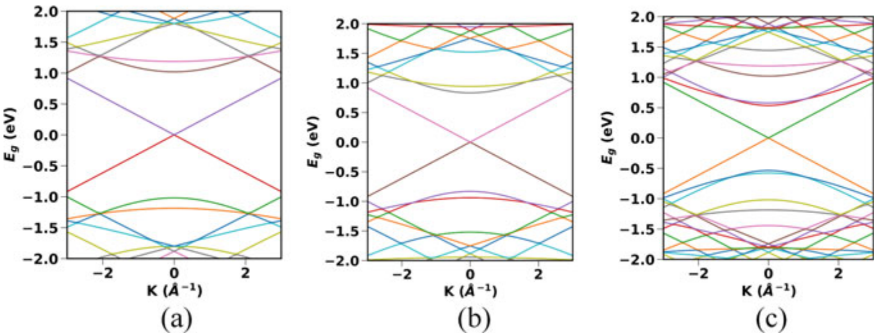

Fig. 8 Energy band diagram of AGNR for length 15 Å and width **a** 14 Å, **b** 18 Å, and **c** 29 Å, respectively

distance between the subbands decreases. It is found that the band structure of ZNRs and AGNRs (3*P* and 3*P* + 1) are parabolic whereas AGNR (3*P* + 2) are conical.

We further investigate the effect of external voltage on the energy band of GNRs. The *E-k* diagram for the ZNR structure of $L = 15$ Å, and $W = 20$ Å with − 2, 0, and 2 V are present in Fig. 10a–c respectively. Also, AGNR having configurations 3*P* ($W = 12$ Å), 3*P* + 1 ($W = 16$ Å), and 3*P* + 2 ($W = 14$ Å) is presented in Fig. 11 for

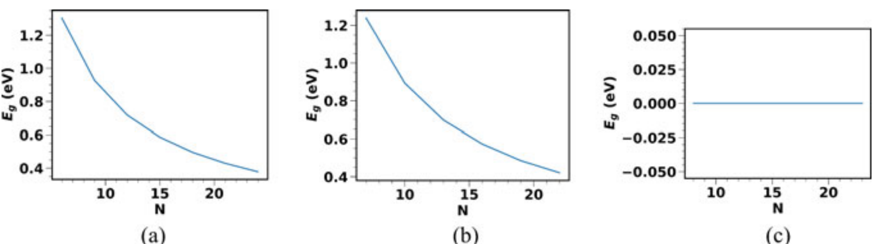

Fig. 9 E_g versus *N* along the width of the AGNR satisfying the configurations **a** 3P, **b** 3P + 1, and **c** 3P + 2 having length 15 Å

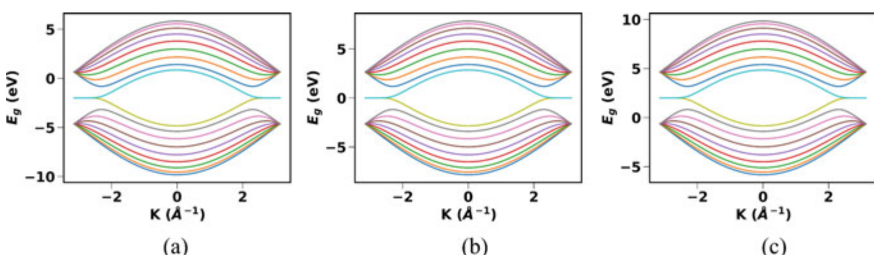

Fig. 10 Application of biasing voltage − 2 V (**a**), 0 V (**b**), and 2 V (**c**) to ZNR structure of $L =$ 15 Å, and $W = 20$ Å

applied voltage − 2, 0, and 2 V, respectively. We found that for all GNRs, the band shifts upward in the energy axis for positive bias voltage and downward for negative bias voltage but there is no change in the bandgap energy.

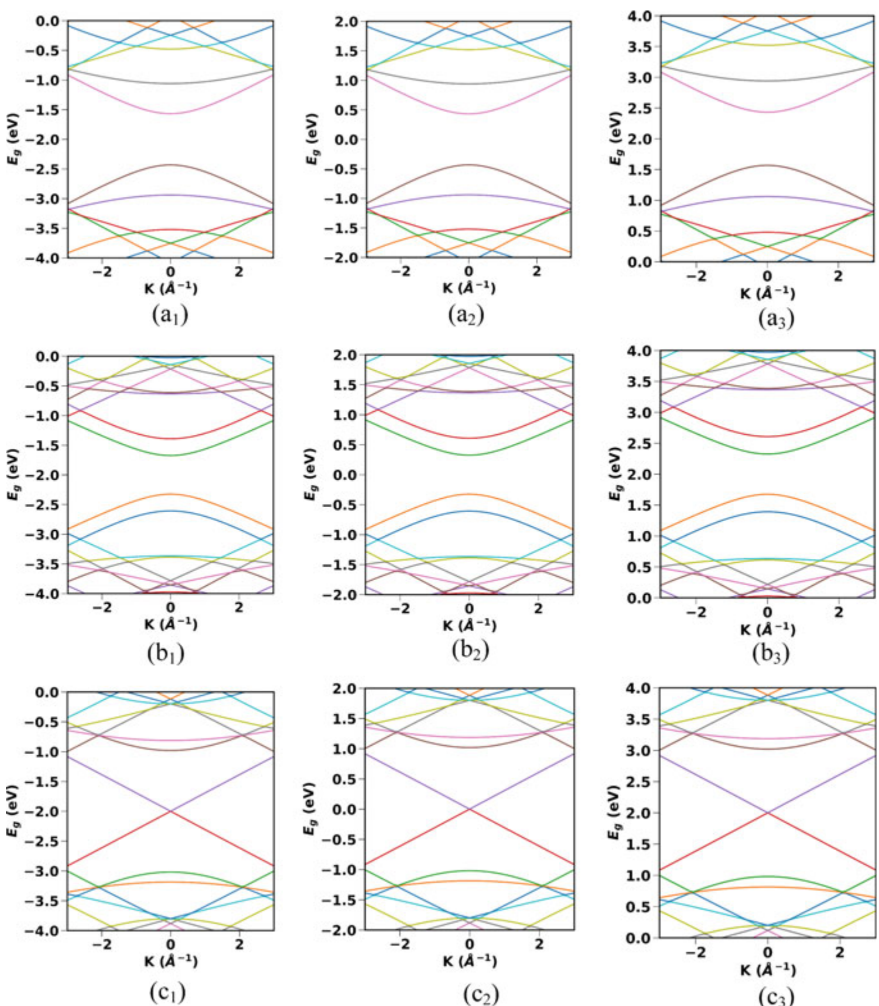

Fig. 11 Application of biasing voltage − 2, 0, and 2 V to AGNR of configurations 3P ($\mathbf{a_1}$, $\mathbf{a_2}$, and $\mathbf{a_3}$), 3P + 1 ($\mathbf{b_1}$, $\mathbf{b_2}$, and $\mathbf{b_3}$), and 3P + 2 ($\mathbf{c_1}$, $\mathbf{c_2}$, and $\mathbf{c_3}$)

4 Conclusion

Here, we investigate and modulate the energy band gap (E_g) in graphene nanoribbons through width variation by using KWANT. It has been found that in ZNRs, with an increase in width, E_g remains unchanged, that is, 0 eV. In AGNRs, it reduces with an increase in width as well as the number of atoms for $3P$ and $3P + 1$ whereas for the $3P + 2$ configurations, E_g remains the same (0 eV). Also, the application of positive and negative voltage, shifts the energy levels to higher and lower values respectively, keeping the band gap unchanged for all GNRs. The current study will be helpful to understand the behavior of the energy band structure of graphene nanoribbons through physical change and the application of external bias. The study also witnesses the ability of KWANT to conveniently perform such tasks.

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Fabrication and Characterization of E-Beam Deposited Copper Oxide Thin Film on FTO and Silicon Substrate for Optoelectronic Applications

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1 Introduction

Transparent conducting oxide (TCO) has received a lot of attention in newly emerging smart devices like transparent displays [1], smart windows [2], DSSCs [3, 4], etc. These devices use different types of substrate and metal oxides having a wide or narrow bandgap depending on the application. FTO is an n-type material with high optical transparency and great electrical conductivity, allowing it to absorb wide bandgap energy. FTO has been employed in a variety of optoelectronic transparent device applications because it is chemically inert, physically durable and has superior thermal stability than other TCO substrates. This substrate can be processed in a higher temperature environment as well. Nowadays, many researchers are interested in studying the narrow wavelength properties of semiconductors with lower bandgaps, such as HgCdTe [5], Ge [6], InSb [7] and others. Copper oxide is of particular interest because to its intriguing physicochemical features, low cost, environmentally acceptable nature, good electrical conductivity and nontoxicity [8, 9]. It is a native *p*-type material with majority of hole conductivity having narrow bandgap that comes in two forms: cuprous oxide (Cu_2O) with bandgap ~ 1.8–2.5 eV having cubic crystal structure and cupric oxide (CuO) with bandgap ~ 1.21–1.51 eV having monoclinic crystal structure [10]. Semiconducting Cu_2O-TF have great scope in the fields of solar cells [11], glucose sensors [12], photocatalyst [13], supercapacitor [14], biosensors [15], solar water splitting [16], gas sensors [17] and lithium-ion batteries

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[18]. Various techniques like sol–gel [19], chemical vapour deposition (CVD) [20], plasma evaporation [21], nebulizer spray pyrolysis [22] and electrodeposition [23] can be used to form copper oxide-TF. Furthermore, it is very crucial to obtain a consistent TF possessing a very porous structure which influence the properties of the film. Again, various properties of the films, including optical and electrical properties, are extremely depended on the deposition process used. E-beam evaporation is another low-cost and simple production approach that can be used to create metal oxide TF. By optimizing the deposition time and current, this fabrication process can be used to create uniform films. Further, post-deposition annealing is one of the factors for improving the TF quality, which will lead to a change in the optical bandgap of the materials. Also, this technique can control the growth mechanism in a simple and catalytic-free process [24]. Accordingly, this study will investigate the film properties formed on FTO and Si substrates as well as the effects of annealing mostly on crystal quality of the film. Moreover, FTO and Si substrates can tolerate higher annealing temperatures as compared to other substrates without increasing the sheet resistance during the coper oxide oxidation process. Moreover, Cu_2O-TF grown on FTO substrates employing E-beam evaporation has not been published before, to the best of our knowledge. As a result, the E-beam technique can be utilized to fabricate a variety of optoelectronic transparent devices.

Hui et al. reported that copper nanoparticles and FTO nanocomposite materials were successfully prepared by hydrothermal method. In addition, the photocatalytic H_2 development under visible light irradiation was studied [25]. Pavan et al. also reported that cuprous oxide-TF is deposited on an FTO glass substrate using the electrodeposition process, which further studies the glucose sensing properties of copper oxide-TF. This experiment was performed with a 1 mM glucose agent using cyclic voltammetry with NaOH as an electrolyte medium [26]. Again, Dolai et al. reported that cupric oxide (CuO) TF was formed using a direct current (DC) sputtering technique that controlled the flow rate of the gases in the plasma which is formed. Also, the substrate temperature is tuned to form the uniform polycrystalline film that will serve as n-type material in the p–n junction solar cell [27].

In this paper, copper oxide-TF is deposited on an FTO glass and Si substrate by using E-beam evaporation. Utilizing an XRD and UV/Vis spectrophotometer, the structural and optical characteristics of the fabricated sample are investigated. Scanning electron microscopy (SEM) is used to investigate morphological features. As-deposited sample exhibits low-quality copper oxide crystal growth formation, which improves with higher temperature annealing. Also, the effect of annealing on the crystal shape and characteristics of TF material, whose properties are temperature-dependent, was also investigated.

2 Experimental Section

Using an E-beam evaporation system Smart Coat 3.0, copper oxide-TF is coated on both the FTO and Si substrates. Before deposition, FTO glass (2 × 2 cm) is consecutively soaked in acetone solvent and de-ionized (DI) water for 2 min each, while the Si wafer (2 × 2 cm) is soaked in acetone solvent, methanol solvent and DI water for 2 min each to eliminate undesirable particles adhered to the substrates surface. The well-cleaned substrate is attached to holder, which placed inside vacuum chamber, after drying for 5 min at room temperature. And, the substrate holder is placed ~ 21 cm from the target material while the chamber is evacuated until the chamber pressure reaches 5×10^{-6} mbar, which takes 1.5 h. Once the desired chamber pressure is reached, the copper oxide-TF is deposited on both the FTO and Si substrates using the 99.999% pure copper oxide source material. Whenever oxygen gas escapes from the source material as it is heated, the vacuum pressure falls during the deposition process. The entire deposition process is observed by the digital thickness monitor (DTM), which is located inside the chamber. By adjusting the current, rate of deposition is regulated at ~ 0.5 s^{-1}, and a thickness of ~ 100 nm copper oxide-TF is attained. Furthermore, fabricated samples are annealed for 1 h at 400 and 500 °C to investigate the impact of annealing on both structural and optical characteristics. XRD is also used to characterize the samples. The absorption spectra of the fabricated sample were evaluated using a UV–Vis spectrophotometer (AN-UV-6500N, ANTech).

3 Results and Discussion

3.1 SEM

The surface morphologies of as-deposited as well as annealed copper oxide-TF deposited using E-beam evaporation are analysed using SEM to study the surface evolution after annealing, which is shown in Fig. 1. This top-view SEM image shows that a uniformly defined and roughly spherical shape of copper oxide particles has developed on the surface of as-deposited film, as illustrated in Fig. 1a. Furthermore, the cross-section image in Fig. 1b and the magnified cross-section image show the formation of a dense and uniform TF with a thickness ~ 100 nm. Moreover, a Cu_2O-TF sample deposited on a Si substrate is heated at 600 °C to investigate the impact of annealing. As a result, spherical shape shown in the top view of as-deposited sample evolved to a semi-cubic shape pattern after annealing Cu_2O-TF at 600 °C, as illustrated in Fig. 1c, d. Thus, annealing temperature rises, phase transformation of Cu_2O to CuO take place, as supported by XRD.

Funda et al. revealed that copper oxide-TF was coated on glass substrate using spin coating process which is annealed at temperatures between 200 and 600 °C in an air environment. Further, it is reported that CuO phase formation is observed at

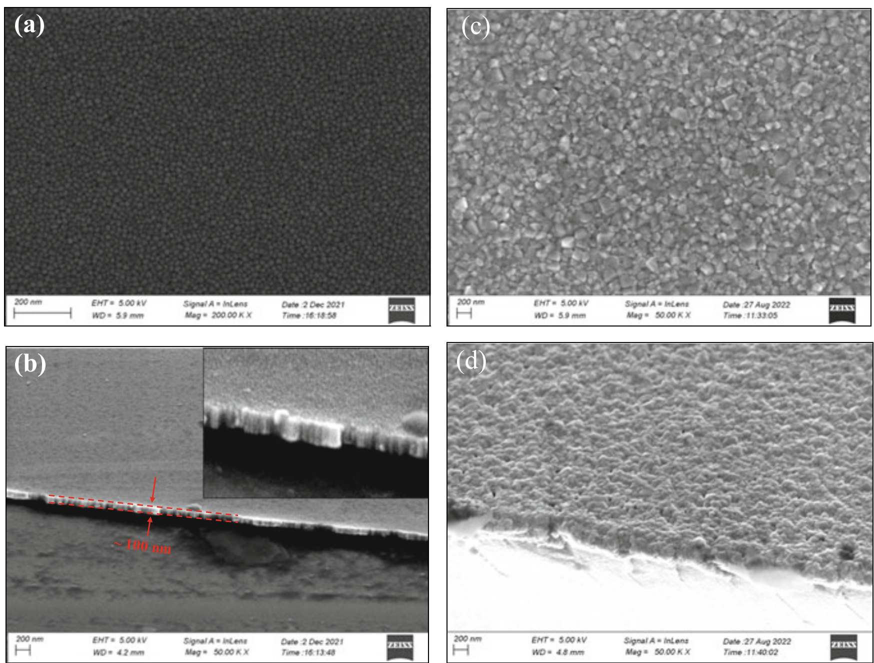

Fig. 1 SEM images of as-deposited Cu_2O-TF, **a** top view and **b** cross-sectional SEM images of CuO-TF annealed at 600 °C, **c** top view and **d** cross-sectional

the higher annealing temperature [28]. Therefore, the post-annealing process may be one way to improve the crystal quality of copper oxide film, which can be used in various optoelectronic devices.

3.2 XRD

XRD was used to characterize as-deposited and annealed copper oxide-TF sample using the X-Pert Pro Pan analyser, which was run at 30 mA and 40 kV. Figure 2 depicts the diffracted pattern of copper oxide samples. For as-deposited sample, diffraction pattern displays single peaks from the cuprous oxide (Cu_2O) crystal at $2\theta = 42.84°$, corresponding to the crystal lattice of (200) (JCPDS Card No. 005-0667). Furthermore, after annealing the Cu_2O-TF film at 400 and 500 °C, more peaks at ~ 34.98 and ~ 38.14, which are assign to (11-1) and (200) of the cupric oxide (CuO) crystal (JCPDS card No. 048-1548), are shown in Fig. 2. As a result of the *X*-ray study, the copper oxide-TF deposited by E-beam evaporation techniques creates Cu_2O crystals, which improves crystal quality and change to CuO crystals following the post-deposition annealing procedure. This change in the copper oxide phase is due to the filling of oxygen vacancies during the heat treatment [29]. Again, Scherrer's equation is used to determine the average crystallite size (D) of samples [30].

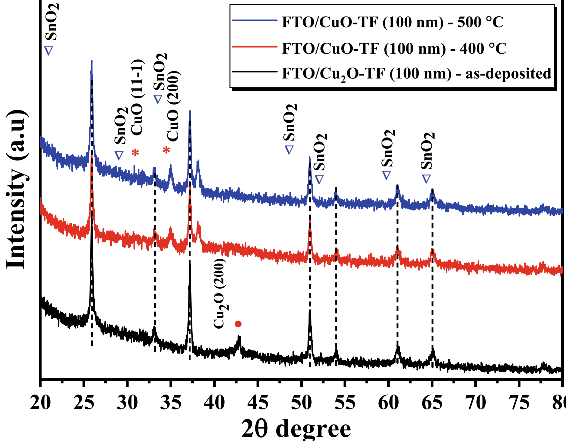

Fig. 2 XRD graph of copper oxide-TF

Table 1 Calculated average crystallite size for as-deposited and annealed samples

S. no.	Temperature (°C)	D (nm)
1	As-deposited	22.96
2	400 °C	22.20
3	500 °C	23.31

$$D = \frac{k\lambda}{\beta \cos\theta}$$

where $k = 0.9$, θ is the Bragg angle, β is the full width half maximum (FWHM) and λ = 1.54 Å. Table 1 shows average crystallite size against annealing temperature. The average crystallite size of the as-deposited Cu_2O-TF is ~ 22.96, which is reduced to ~ 22.20 after annealing at 400 °C. When the annealing temperature increases to 500 °C, the average crystallite size increases to ~ 23.31. This increase in crystallite size is due to the reduction of imperfections in the crystal structure [7].

3.3 *Optical Properties*

The absorption spectra of as-deposited and annealed copper oxide-TF coated FTO substrate is analysed using a UV–Vis spectrophotometer from ~ 400 to ~ 1000 nm. It has been found that the as-deposited copper oxide-TF shows more absorption in near IR than in the visible spectrum. However, the absorption intensity of copper oxide-TF is reduced after annealing, which is shown in Fig. 3a. Usually, Cu_2O is active in the near IR and visible regions, which depends on the annealing time and temperature. As the annealing temperature changes, the phase formation of the copper oxide also changes, which may be due to the filling up of oxygen vacancies during the

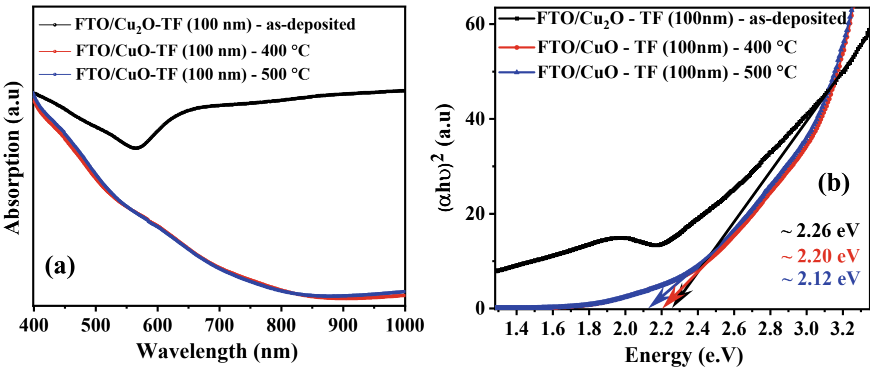

Fig. 3 **a** UV–Visible absorption spectra of copper oxide-TF and **b** Tauc plot of copper oxide-TF

heat treatment. Furthermore, as seen in Fig. 3b, the bandgap of fabricated sample was determined from the Tauc plot by extrapolating the linear component from the graph. According to this graph, the bandgap of the as-deposited Cu_2O-TF is ~ 2.26 eV which decreases to ~ 2.20 eV after annealing at 400 °C. The energy bandgap of the CuO-TF sample is slightly lowered to ~ 2.12 eV when the sample is annealed at 500 °C, though. This bandgap result is comparable to bandgap results that other researchers have reported and that have been deposited using different fabrication techniques [31]. Hence, energy bandgap of copper oxide can be controlled by adjusting the annealing temperature and time.

4 Conclusion

In conclusion, copper oxide-TF has been successfully deposited on an FTO and Si substrate using an E-beam evaporation process. The structural and morphological characterization show the successful deposition of copper oxide-TF on both silicon and FTO glass substrates. The as-deposited copper oxide films show the crystalline character of Cu_2O, which is evidenced from the XRD results. However, post-deposition annealing of the Cu_2O sample shows phase transformation from Cu_2O to CuO, which is observed from XRD. SEM images of the as-deposited copper oxide-TF exhibit morphological changes after annealing, which are caused by annealing effect. From the Tauc plot, the optical bandgap of as-deposited Cu_2O-TF is ~ 2.26 eV, which falls to ~ 2.12 eV after annealing. As a result, the fabricated sample based on copper oxide-TF on Si and FTO substrates using E-beam evaporation technique might be applicable to construct IR based detectors.

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Current Status and Future Perspectives of Tunnel Field Effect Transistors for Low Power Switching Applications

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1 Introduction

The silicon complementary metal oxide semiconductor (CMOS)–based integrated circuits (IC) technology has been scaled down continuously in accordance with Moore's law, for the performance improvement of ICs at reasonable cost since the past half century [1, 2]. However, the supply voltage (V_{DD}) reduces at a slow pace as compared to the scaling of transistor feature size, which hinders the realization of ultra-low power energy efficient switches. A couple of devices are proposed to reduce the V_{DD} further such as impact ionization metal oxide semiconductor (I-MOS) [3, 4], TFET [5], and negative capacitance field-effect transistor (NCFET) [6, 7] and so on [8, 9]. From the aforesaid, TFET has gained significant attention of the scientific community as it is expected to reduce the $V_{DD} < 0.6$ V by attaining sub-threshold swing (S) < 60 mV/dec at 300 K, as presented in Fig. 1. Additionally, TFET offers a small off state current due to asymmetry in doping profile [10], weak temperature dependence due to low energy of conduction carriers in the tunneling region as compared to thermionic emission–based conventional MOSFETs [11]. Hence, TFET has the potential to control the power consumption without the degradation of the device performance and overcomes the Boltzmann's Tyranny or thermal limit of conventional FETs [12].

The conventional MOSFETs operate using the concept of thermionic injection of charge carriers to overcome barrier height such that sub-threshold swing (S) is restricted to greater than 60 mV/dec related using Eq. (1) [13]:

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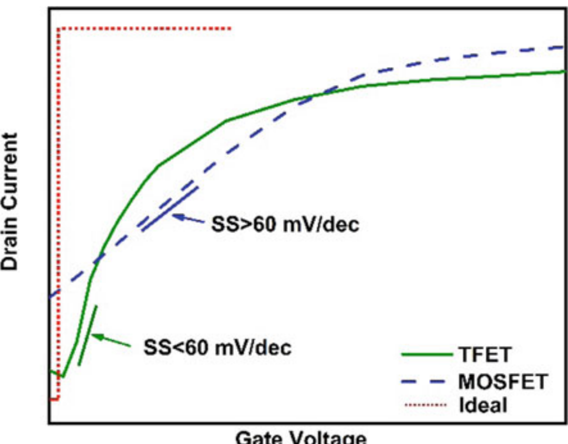

Fig. 1 Typical S value for ideal FET, conventional MOSFET, and TFET devices

$$S = \left(1 + \frac{C_d}{C_{OX}}\right) \ln 10 \frac{KT}{q} \tag{1}$$

where S is the minimum gate voltage (V_{GS}) obligatory to vary the drain current (I_{D}) by at least one decade in the sub-threshold region. C_d, C_{OX}, K, T, and q are the depletion layer capacitance, oxide capacitance, Boltzmann constant, room temperature, and electronic charge, respectively. Since $C_d < C_{OX}$, implies $(1 + (C_d/C_{OX})) \sim 1$ and thus, S $\sim$ $\ln 10(KT/q)$ $\sim$ 60 mV/dec is called the thermal boundary of conventional FETs or Boltzmann's Tyranny.

In the literature, Avci et al. demonstrated an average energy saving of 64% in case a nanowire heterojunction TFET at L_g of 13 nm as compared to conventional Si MOSFET [14]. Alian et al. reported InGaAs homo-junction TFET with I_{ON}, I_{OFF} and S of 4 μA/μm, 100 pA/μm, and 60 mV/dec, respectively, along with superior reliability in terms of g_m and PBTI stress as compared to conventional MOSFET [15]. Convertino et al. reported a comparative analysis of hybrid III-V InGaAs/GaAsSb TFET integrated on cost-effective Si substrates to obtain an exceptional minimum S of 42 mV/dec as compared to InGaAs MOSFET with S of 62 mV/dec [16].

On the other hand, TFET operates according to inter-band tunneling, also called band-to-band tunneling (BTBT) principle, i.e., when applied V_{GS} increases, the channel regions conduction band is brought beneath the source region valence band and enhances the BTBT rate, discussed further in Sect. 2. For TFET, S is related using Eq. (2) as follows:

$$S = \ln 10 \left[\frac{1}{V_{\mathrm{eff}}} \frac{\mathrm{d}V_{\mathrm{eff}}}{\mathrm{d}V_{\mathrm{GS}}} + \frac{\xi + b}{\xi^2} \frac{\mathrm{d}\xi}{\mathrm{d}V_{\mathrm{GS}}} \right]^{-1} \tag{2}$$

where V_{eff}, V_{GS}, and ξ are the tunnel–junction bias, gate–source voltage and applied electric field, respectively. While the coefficient determined as $b = 4\sqrt{m^*}E_g^{3/2}/3q\hbar$, where m^*, E_g, and $\hbar$ are the carrier's effective mass, semiconductor's energy band

gap, and the modified Planck's constant ($h/2\pi$), respectively [17]. In case of TFET, S can be achieved < 60 mV/dec; thus, TFET used in variety of applications such as energy efficient switches for low power circuits [18], analog circuits [19], and biosensors [20]. However, the adoption of TFET in the advanced IC technology is limited by low I_{ON}/I_{OFF} ratio especially low ON current (I_{ON}), because it critically depends on the Wentzel–Kramer–Brillouin (WKB) transmission probability (T_{WKB}) of inter-band tunneling barrier related using Eq. (3) as follows [21]:

$$T_{WKB} \cong \exp\left(-\frac{4\lambda\sqrt{2m^{*}}E_g^{3/2}}{3q\hbar\left(E_g + \Delta\emptyset\right)}\right) \tag{3}$$

where m^{*}, E_g, and $\hbar$ denote effective mass, bandgap, and reduced Planck's constant, respectively, while λ denotes the tunneling length that relates to device geometry, and $\Delta\emptyset$ depicts energy overlap window in the device.

The major challenge for TFET to be a potential contender for next-generation IC technology is to obtain a high $I_{ON} \geq 1$ A/μm and low I_{OFF} <1 μA/μm so as to obtain a practically high I_{ON}/I_{OFF} ratio $\geq 10^6$, steep sub-threshold swing with $S < 60$ mV/dec and $V_{DD} < 0.6$ V. Therefore, numerous approaches are proposed in the literature to improve the I_{ON} such as gate dielectric engineering [22], doping techniques [23], multiple gates [24], heterostructures [25], alternate semiconductor materials (III-V, IV) [26, 27], and so on [28].

In the literature, a couple of review articles on TFET device structure are available that highlight the specific aspects of TFET such as device physics; alternate device structures; integration of alternate materials, e.g., III-V, 2D, and carbon nanotube; and so on [21, 29, 30]. The key aim of this article is to present the recent progress in TFET devices while also covering an overview of TFET structure, device physics, operation, improving I_D, and $S < 60$ mV/dec, along with a comparison of various simulated and experimentally demonstrated TFETs. The rest of the manuscript is structured as follows: Sect. 2 describes TFET structure and device operation, Sect. 3 deliberates the impact of device parameters on performance of TFET, Sect. 4 discusses methodologies to improve the I_{ON} for TFET, Sect. 5 presents challenges and future scope, and Sect. 6 concludes the article.

2 TFET Structure and Operation

In 1958, Esaki introduced the concept of quantum mechanical BTBT based on Zener breakdown concept [31]. The BTBT is the major mechanism responsible for better performance of TFET. In 1978, Quinn et al. presented a gated reverse-biased *p–i–n* structure that forms the typical structure of TFET [32].

The TFET device structure consists of two oppositely doped semiconductor regions (n^+ and p^+) separated by an intrinsic region to form the *p–i–n* device structure. The gated intrinsic region is covered by a gate oxide/insulator. Three electrodes

are designed over the source, drain, and gate regions (Fig. 2a). TFET depicts unique structure because of the opposite type of doping in the source, drain regions, and the need of reverse biased *p–i* and *i–n* junctions for operation. Further, TFET's are classified into two types: (i) p-type TFET: with the *n–i–p* structure where the source is doped with heavily n^+, drain is heavily doped p^+, channel is intrinsic or lightly doped *p*/*n* type, and the tunneling (BTBT) occurs at the source (n^+) and channel interface. Additionally for the operation of *p*-type TFET, drain and gate electrodes are negative biased, while the source is grounded; and (ii) *n*-type TFET represents *p–i–n* structure, strongly doped p^+ source and n^+ drain, while channel is lightly doped (*n*/*p* type) or kept intrinsic in nature, and the tunneling (BTBT) occurs at the source (p^+) and channel interface. For biasing *n*-type TFET, drain and the gate electrode is positive biased while the source is grounded.

Figure 2a and b presents the *n*-type TFET structure and energy band model, respectively. When the gate voltage (V_{GS}) is less than V_{OFF}, the energy barrier at tunneling region is much broader (as depicted using dashed line in Fig. 2b), thus only leakage current flows and TFET is said to be in the "OFF State". Furthermore, when V_{GS} is increased, electric field is enhanced, thus the intrinsic region's energy band shifts down and tunnel width is reduced at the source–channel interface. Hence, the probability of charge carriers tunneling from source's valence band to channel's conduction band increases.

The tunneling between source (p^+) and channel junction in the n-TFET by changing the electrostatic potential with gate bias is defined by the BTBT rate (G_{BTBT}) using Kane's model as [33]:

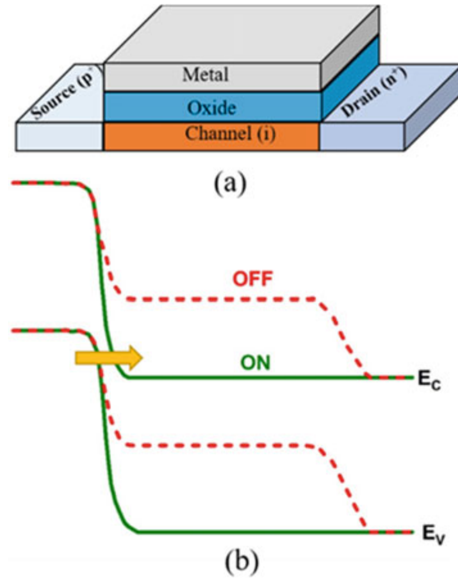

Fig. 2 **a** n-type TFET device structure and **b** Energy band model for the "OFF" and "ON" state denoted by dashed (Red) and solid (Green) lines, respectively

$$G_{\text{BTBT}} = A\frac{\xi^2}{E_g^{1/2}}\exp\left(-B\frac{E_g^{3/2}}{\xi}\right) \quad (4)$$

where E_g and ξ are the energy bandgap of tunneled material and applied electric field, respectively. While A and B are the amendable variables and depend on the material properties, e.g., the value of A and B is ~4 × 10^{14} $\text{cm}^{-1/2}\text{V}^{5/2}$ s^{-1} and ~19 MV/cm for Si and ~8.1 × 10^{18} $\text{cm}^{-1/2}\text{V}^{5/2}$ s^{-1} and ~ 4 MV/cm for InAs, respectively [34].

Further, the I_{D} of TFET can be determined by using the Landauer equation's integration over the energy range that participated in tunneling [35] as:

$$I_D = \frac{4e}{h}\sum T_{\text{tot}}(k_{\text{trans}})\int_0^{\Delta\emptyset} \mathrm{d}E(f_s(e) - f_d(e)) \quad (5)$$

where T_{tot}, f_s, f_d, e, h, and k_{trans} is the total transmission function, the source fermi functions, drain fermi functions, charge of the electron, Planck constant, and the summation over the transverse wave vector, respectively.

Figure 3a depicts transfer characteristics curve for a typical double-gate TFET (DGTFET). Further, for better TFET device understanding, transfer characteristics may be divided into three regions as follows: (i) *OFF State*: When applied gate voltage is less than V_{OFF} ($0 < V_{\text{GS}} < V_{\text{OFF}}$), TFET has extremely low current due to misalignment of the source and channel energy bands. (ii) *Sub-threshold region*: When applied gate voltage increases beyond V_{OFF} ($V_{\text{OFF}} < V_{\text{GS}} < V_{\text{T}}$), the drive current rises exponentially due to alignment of source and channel region energy bands and (iii) *Super-threshold region*: When supplied $V_{\text{GS}} > V_{\text{T}}$, the I_D increases with slow rate. When $V_{\text{GS}} = V_{\text{DS}} = V_{\text{DD}}$, the drain current is recognized as the I_{ON} of the TFET.

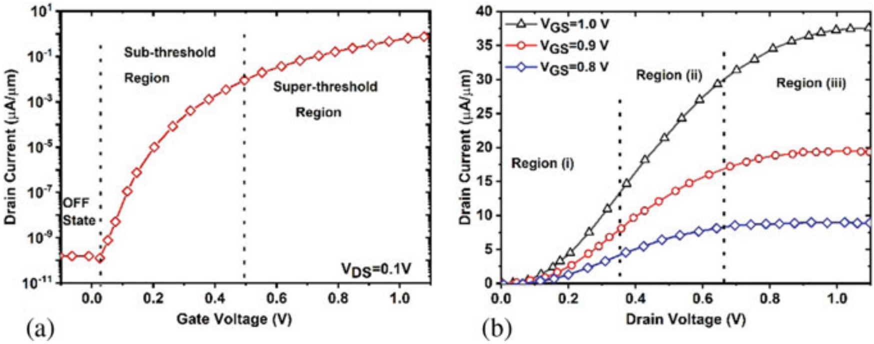

Fig. 3 **a** Transfer characteristics (I_{D}–V_{GS}) and **b** Output characteristic (I_{D}–V_{DS}) of DGTFET

The I_D–V_{DS} characteristics of DGTFET are presented in Fig. 3b and observed three regions are: (i) *Tunnel resistance dominated region:* where I_D increases exponentially with V_{DS} and restricted by the tunnel resistance; (ii) *Channel resistance dominated region* where I_D increases at slow rate with V_{DS}; (iii) *Saturation region* where the I_D saturates, i.e., for applied drain voltage (V_{DS}) > 0.6 V.

Moreover, the TFET behaves as an ambipolar device that means, when electrons dominate the current conduction, TFET shows an n-type behavior, whereas when holes dominate the conduction, TFET shows p-type characteristics. Considering the CMOS application of TFET, ambipolar conduction is undesirable because it leads to higher OFF state current and circuit failure. The ambipolar characteristics of TFET may be minimized by considering several techniques such as dropping the drain doping profile as compared to source, employing a heterojunction, or introducing asymmetry in the TFET device structure [36, 37].

3 Effect of Device Parameters on TFET Performance

This section addresses the TFET device characteristics, including the effect of channel length variation, source doping concentration, body thickness, and gate dielectric material.

3.1 Gate Dielectric

High-κ gate dielectrics with effective dielectric constant greater than SiO_2 (κ ~ 3.9) such as Al_2O_3, Er_2O_3, ZrO_2, HfO_2, TiO_2, and so on [38–42] provide the ability to continue the scaling of gate oxide without compromising the off state static leakage current of CMOS devices. Likewise, in TFETs, integration of high-κ gate dielectric material, increase the gate capacitance, raises the tunneling rate, and thus, drive current can be improved. The tunneling probability $T(E)$ for ultrathin films and gate oxides is related using Eq. (7) [43]:

$$T(E) \propto \left[\left(\frac{-4\sqrt{2m^*}E_g^{*3/2}}{3|e|\hbar\left(E_g^* + \Delta\emptyset\right)}\sqrt{\frac{\in_s}{\in_{ox}}t_{ox}t_s}\right)\right]\Delta\emptyset \tag{7}$$

where m^*, E_g, $\Delta\emptyset$, and $\hbar$ denote the effective mass of carriers, bandgap of semiconductor channel material, the range of energy band where tunneling takes place, and reduced Planck's constant, respectively, while t_{ox}, $\in_{ox}$, and t_s, $\in_s$ are the thickness and dielectric constant of oxide and semiconductor, respectively. In addition, lower EOT attained on integration of high-κ dielectrics is a possible approach to overcome lower I_{ON} problem of TFETs at CMOS compatible voltages.

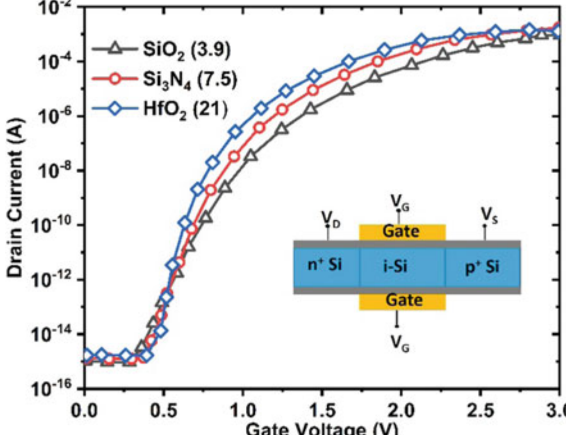

Fig. 4 The drain current–gate voltage (I_D–V_{GS}) characteristics of a double-gate TFET device structure with variation in dielectric materials SiO_2, Si_3N_4, and HfO_2 [44]. The inset of figure shows the corresponding DGTFET device structure

Boucart et al. [22] and Toh et al. [24] have experimentally obtained ~ 2.25 times improved I_D by adopting stronger gate control on integration of high-κ gate dielectric material with reduced thickness. Further, Sandow et al. [45] experimentally observed that I_D was enhanced by six times in SOI-based TFET when t_{ox} reduced ~ 1 nm (from 4.5 nm to 3.5 nm). Additionally, the choice of dielectric material should be such that the device maintains low static leakage current [46, 47]. Figure 4 depicts the behavior of dielectric materials on the TFET performance, where SiO_2, Si_3N_4, and HfO_2 are dielectric materials with dielectric constant of 3.9, 7.5, and 21, respectively. It is generally noticed that the drive current (I_{ON}) improves with increase in gate dielectric constant [44].

3.2 Channel Length

In TFET, the drive current (tunneling current) primarily depends on the applied electric field and energy band orientation near the tunneling junction. Thus, channel length scaling in the TFET device structure does not show extreme changes in device characteristics [48]. However, if the channel region is scaled to a critical length, both the tunneling junctions (source–channel and drain–channel) start to overlap each other. Hence, the effect of gate control over the channel becomes weak; thus, direct source-to-drain leakage called drain-induced barrier thinning (DIBT) occurs. The effective screening length in the channel for tunneling transition (λ_s) is related using Eq. (8) [35]:

$$\lambda_s = \sqrt{\frac{\epsilon_s}{\epsilon_{ox}} d_{ox} d_s} \tag{8}$$

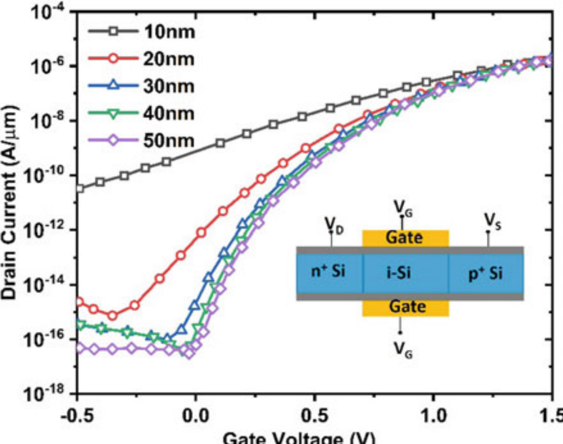

Fig. 5 The transfer characteristics of Si-DGTFET with channel length variation. The inset of figure shows the corresponding DGTFET device structure. Reproduced from Ref. [48]. Copyright 2007 Elsevier

where $\in_s$, $\in_{ox}$, d_{ox}, and d_s are the relative permittivity of semiconductor channel material, relative permittivity of gate dielectric, thickness of the gate dielectric, and thickness of the channel material, respectively.

Figure 5 depicts the effects of channel length variation on transfer characteristics of Si-based DG-TFET. From Fig. 5, it is observed that the drain currents are almost constant with channel length variation from 10 to 50 nm for $V_{GS} > 1$ V. However, I_{OFF} increases with scaling of channel length from 50 nm to 10 nm due to short channel effects, e.g., DIBT. Thus, I_{ON}/I_{OFF} ratio decreases (below six order) with channel length scaling below critical limit ($\lesssim$15 nm) as shown in Fig. 5. For Si-based TFET devices, experimentally critical channel length was reported to be ~ 20 nm [49].

3.3 Body Thickness

In TFET, the drain current depends on two contending effects of body thickness. As body thickness is scaled down, the tunneling volume decreases; thus, I_D (drain current/tunneling current) is also decreased. On the other hand, I_D (drain current/ tunneling current) can be increased, if tunneling volume increases, which is possible by increasing the body thickness. However, increasing the body thickness results in degradation of gate control on channel, i.e., I_{ON}/I_{OFF} ratio is decreased. Thus, optimum body thickness needs to be maintained to achieve reasonable device performance parameters. Toh et al. reported that silicon body thickness between 10 nm and 20 nm for DG-TFET shows maximum drive current [24]. Luisier et al. have experimentally demonstrated S value ~ 60 mV/dec for InAs TFETs by reducing the body thickness < 4 nm and ≤ 7 nm for SG-TFET and DG-TFETs, respectively [26].

3.4 Source/Drain Doping

In TFETs, the bandgap of the source region can be decreased by employing increased source doping concentration; thus, the tunneling distance reduces at the tunneling junction (Fig. 2b). Hence, the I_{ON} can be enhanced with variation in doping level of source. Sandow et al. experimentally verified 2 × improvement in I_{ON} of TFET on doubling the doping concentration of source [45]. Additionally, with higher source doping concentration, the source–channel tunnel junction's doping profile becomes abrupt and I_{ON} increases. Thus, higher tunneling current is achieved for a TFET with heavily doped source as compared to lightly doped source on application of electric field at tunneling junction. However, higher tunneling may lead to increased I_{ON} but lower S value often called the I_{ON}-S trade-off [50].

Furthermore, in TFET device structure, the ambipolar current needs to be reduced so as to achieve a reasonably small off-state leakage current. To achieve reduced ambipolar current, the band bending at tunneling interface should be sharp such that tunneling width can be reduced. To minimize the ambipolarity of the TFET, the source region doping concentration is generally kept higher than the drain region doping concentration [51].

4 Techniques for TFETs Performance Enhancements

TFET is considered as one of the prominent replacements for conventional MOSFET because of its advance performance such as high I_{ON}, low I_{OFF}, and $S < 60$ mV/dec. This section overviews various techniques used for boosting the performance of TFETs such as high I_{ON}, low I_{OFF}, and lower S. Generally, the techniques that can be used to improve the performance of TFET are classified as follows: (1) Gate Engineering (2) Materials Engineering, and (3) Tunneling Junction Engineering.

4.1 Gate Engineering

In TFET, gate controls carrier concentration in intrinsic region, i.e., channel and the orientation of energy band at tunneling junction. Therefore, coupling of gate voltage with channel potential marks noticeable influence on the I_D. Gate engineering can be used to improve the performance of TFET, e.g., multiple gates can increase the I_D due to increased tunneling area because of formation of higher channel region below the multi gates that results in elevated I_{ON}. Toh et al. [24] have presented improved drain current by 2.25 times and excellent S value of ~ 25 mV/dec by adopting double gate structure. Zhaonian et al. proposed the design of an L-shaped gate and U-shaped channel-based TFET device structure to reduce the tunnel width and revealed an S of ~ 38.5 mV/dec [52]. Goswami et al. [53] showed simulation

results for L-shaped gate TFET to achieve S of ~ 22.2 mV/dec, and I_{ON}/I_{OFF} ratio ~ 3.326×10^{11}. Sola et al. presented a trench gate-based source channel covered TFET and observed improved device characteristics with I_{ON}/I_{OFF} of ~ 10^{10} [54]. Vishwa et al. proposed dual metal gate DGTFET to improve the surface potential that results in reduction of tunneling width and optimum I_{ON}/I_{OFF} ratio of ~ 10^5 [55]. Furthermore, gate all around (*GAA*) device structure with wrapped gate around the channel covers more channel area to provide better channel control and hence higher I_{ON}/I_{OFF} ratio. For instance, Chen et al. presented TFETs based on highly scalable vertical silicon nanowires structure that showed high I_{ON}/I_{OFF} ratio and elevated I_{ON} of ~ 10^7 and 53 μA/μm, respectively, due to a strong electrical field at the edge of the channel [56].

4.2 Energy Bandgap (Material) Engineering

Si shows poor BTBT efficiency due to large bandgap (E_G) of ~ 1.12 eV and indirect bandgap. The smaller direct bandgap (0.66 eV) of Ge, makes it a good option to improve the performance of TFET. Additionally, Ge shows higher mobility and more suited for BTBT than the Si. By employing the Ge in entire TFET channel, I_D improved by ~2700 times in Ge-on-insulator (GOI) as compared to silicon on insulator (SOI) [57, 58]. However, major challenge with Ge channel TFET is the smaller bandgap of Ge which is responsible for the ambipolarity and a higher leakage current (I_{OFF}). Kim et al. have presented a TFET structure with Ge source and Si channel to obtain S, I_{ON}, and V_{DD} of ~40 mV/dec, 0.4 μA/μm, and < 0.5 V, respectively [59].

Alternatively, group III–V semiconductors exhibit high tunneling rate, because of smaller bandgap, direct tunneling mechanism, and smaller tunneling mass than the Si, which can be used to attain improved I_{ON} current as compared to Si-based TFETs. Mookerjea et al. [60] introduced InGaAs TFET and obtained I_{ON} and S of ~20 μA/μm and ~250 mV/dec, respectively, while Zhao et al. reported I_{ON} and S of ~50 μA /μm and ~90 mV/dec respectively, for InGaAs TFET [61].

Furthermore, the effective energy barrier for tunneling can be reduced by using heterostructures. Mohata et al. presented a GaAsSb/InGaAs heterojunction TFETs with I_{ON} ~ 13.5×10^{-5} and S ~169 mV/dec [62]. Memisevic et al. demonstrated minimum S of ~48 mV/dec with enhanced I_{ON} ~10.6 μA/μm and I_{OFF} ~1 nA/μm at V_{DS} ~0.3 V for p-GaAsSb/n-InAs nanowire-based TFETs [63]. Table 1 presents the commonly explored heterojunctions for TFET devices.

In addition, carbon nanotubes (CNTs) are also one of the prominent choice of material for TFET devices due to their large carrier mobility, light effective mass, small bandgap, and outstanding electrostatic gate control over channel [21]. Appenzeller et al. [70] demonstrated one of the earliest experimental value for S ~40 mV/dec by using CNT. Recently, Tamersit [71] proposed GAA p–n CNT-TFET structure and achieved S of ~11 mV/dec and I_{ON}/I_{OFF} of ~3.24×10^8 at V_{DD} of ~0.3 V.

Table 1 Some recent experimental and simulation reports on TFET

Source material	Channel material	Gate dielectric	I_{ON} (A/μm)	I_{ON}/I_{OFF}	S (mV/dec)	Ref.
InGaAs	InGaAs	ZrO_2/Al_2O_3	0.12×10^{-5}	$>10^6$	50	[64][a]
InP	InGaAs	Al_2O_3/HfO_2	8.8×10^{-5}	$>10^4$	109	[61][a]
AlGaSb	InAs	Al_2O_3	2.0×10^{-5}	210	830	[65][a]
AlGaSb	GaAsP	HfO_2	1.28×10^{-5}	4.47×10^{12}	19.7	[66][a]
Ge	InGaAs	SiO_2	18.6×10^{-5}	1.4×10^8	10	[67][b]
GaSb	InGaAs	–	22.5×10^{-5}	$>10^7$	>30	[68][b]
GaAsSb	InGaAs	Al_2O_3/HfO_2	13.5×10^{-5}	2.7×10^4	169	[69][b]

[a]Experimental Reports on TFETs; [b]Simulation Reports on TFETs

Moreover, the emerging 2D transition metal dichalcogenides (TMDs) materials such as MoS_2, WSe_2, HfS_2, black phosphorous, and so on [72–74] are another prospective candidate as a channel material for TFETs. TMDs have gained much attention due to their excellent material properties such as ability to fabricate atomically thin layers, low surface roughness, and minimum density of dangling bonds because of feeble van der Waals (vdW) forces amid nearby layers. Hence, 2D TMDs-based TFET devices may show excellent gate control over the channel [75]. Roy et al. has experimentally presented interlayer BTBT in vertical MoS_2/WSe_2 vdW heterostructures using double gate and achieved ~80% of gate coupling efficiency for tuning the interlayer band orientations [76].

Table 2 presents the several heterojunctions TFET device structure by considering various semiconductor materials. From the Table 2, it is evident that III–V materials (such as InAs) have currently demonstrated the best performance among other semiconductor materials used for TFET.

Table 2 Performance evaluation of some experimentally reported TFET devices

TFET	S (mV/dec)	I_{ON} (μA/μm)	I_{ON}/I_{OFF}	Voltage (V)	Refs.
Planar InAs/Si TFETs	21	1	1.0×10^6	1.0	[77]
n-channel Si TFET	52.8	12.1	2.2×10^3	1.0	[5]
GeSn p-TFETs	60	4	1.0×10^7	–	[78]
InAs/InGaAsSb/GaSb nanowire TFET	43	10.4	1.0×10^4	0.3	[63]
InAs/GaSb heterojunction	50	180	6×10^3	0.5	[79]
Graphene source CNT TFET	40	40	1×10^6	0.5	[80]
$SnSe_2/WSe_2$ heterostructure	37	3	10^6	6	[78]
BP-MoS_2 TFET	51	1×10^{-3}	1×10^4	1	[81]

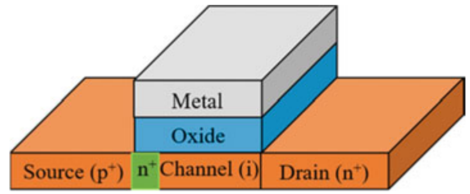

Fig. 6 Schematic diagram for the pocket doping technique

4.3 Tunnel Junction Engineering

In TFET, I_{ON} current dominated by the tunneling junction characteristics, especially on the source side. In particular, the built-in electric field at the tunneling junction increases with higher concentration of source doping profile. Therefore, energy bands alter to decreases the tunnel width at the tunnel junction that leads to enhanced BTBT rate.

The integration of a pocket region (n^+/p^+) in between the source (p/n) and the intrinsic channel regions (as presented in Fig. 6), where pocket region is of different doping type as compared to the source region which is a prevalent method to boost the I_{ON} of TFET. The additional pocket doped region between the source–channel regions provides higher I_{ON} and lower sub-threshold swing enabled energy efficient switching due to reduced tunnel width and boosted lateral electric field [82]. In 2005, Bhuwalka et al. presented a SiGe pocket doped vertical TFET device structure that revealed boosted electrical characteristics and obtained S <60 mV/dec [83]. Later, numerous device structures were investigated using the pocket doped TFET approach to obtain optimum device characteristics. For Instance, Abdi et al. proposed an in-built N^+ Pocket p-n-p-n TFET device structure to obtain improved device characteristics such as 20 × higher I_{ON} and steep S of ~25 mV/dec as compared to conventional TFET. Goswami et al. [53] showed simulation results for pocket doped SOI TFET with L-shaped gate to achieve S of ~22.2 mV/dec and I_{ON}/I_{OFF} ratio ~3.326×10^{11}.

4.4 Work Function Engineering

The metal contacts' work function (ϕ_m) and the metal–semiconductor interface's nature can control the barrier height in the TFET devices. In this regard, TFETs are less resilient to the work function variations as compared to MOSFET in terms of S and threshold voltage [84]. Furthermore, by integrating high work function electrode in the source region, charge plasma (CP) can be introduced in the metallurgical junction (between source electrode and source region) that results in excess charge carriers in source region and hence enhanced device performance. As compared to the physical creation of extra pocket doped region, the CP integration technique eliminates the expensive ion implantation and thermal budget constraint required

for device processing [85]. To create charge plasma at source end, the following conditions must be fulfilled such as (i) the work function of electrode must be different as compared to the sum of semiconductor electron affinity (χ_s) and half of the energy band gap (E_g) related as $\varnothing_m \neq \chi_s + \left(\frac{E_g}{2}\right)$; (ii) thickness of semiconductor (t_s) must be equal to or less than the Debye length (l_d) as $t_s \leq l_d$ [85].

Recently, Anvarifard et al. demonstrated the comparison of conventional TFET (C-TFET); p-n-p-n-TFET; and CP-based SiGe source TFET (CP-SiGe-TFET). The CP-SiGe-TFET device structure revealed good I_{ON}, I_{OFF}, and S of ~ 8.8 × 10^{-6} A/μm, ~ 3.7 × 10^{-18} A/μm, and ~ 57 mV/dec, respectively [86].

Albeit, CP-based TFET technology have several benefits, but the incorporation of charge plasma in source region requires integration of high work function electrode materials that results in more complicated process and low thermal budget constraint that remains an open challenge.

5 Challenges and Future Perspectives

Even though the working concept of the TFET is offered for low power applications, there are still a number of important obstacles to overcome. In recent years, TFET offered prominent performance particularly in Si, Ge, III-V materials, 2D TMD's, and their heterostructures. Yet, limited high performance TFETs are experimentally demonstrated. In the process of heterojunction formation, lattice mismatch is one of the serious issues that needs to be overcome. In general, disorientation and lattice mismatch of 2D materials degrade the switching speed of the device. Furthermore, in the circuit layout, challenges arise due to non-interchangeable TFET source and drain contacts, because they need diverse doping nature and materials such as GaSb, InAs, and so on [29].

In TFETs, ambipolar leakage and low ON state current are another crucial challenge for the device design. With the significant improvement in TFETs' designs and structures, scientific community is focused to design devices with exceptionally low power consumption and input voltage scaling. Therefore, by reducing the V_{DD} collectively with I_{OFF}, the TFET devices have ability to operate with reduced power consumption [11].

Although there are several drawbacks to TFET devices, such as insufficient electrostatic control of channel and concern of manufacturing defect-free channel materials. Thus, new techniques and innovative device design are required to obtain excellent TFET device performance.

6 Conclusions

In Summary, TFET is expected to permit further scaling of IC technology node using BTBT to reduce $S < 60$ mV/dec and $V_{DD} < 0.6$ V. Moreover, TFET can also tackle short channel effects and hot carrier charge effect at smaller channel length. Recent progress in terms of device parameter on the performance of TFETs and strategies to enhance the performance of TFETs using gate engineering (such as multiple gates, GAA TFET, heterostructure), material engineering (such as Group-IV materials, III-V materials, 2D-TMDs, CNT), and tunnel junction engineering (pocket doped) are discussed. Using multiple gates, the tunneling area can be increased that results in improved drive current. Additionally, use of InAs material in the device exhibits excellent experimental results in terms of drive currents and S value. Even if in simulation, high I_{ON}/I_{OFF} ratio of > 6 orders and S value of ~ 1 mV/dec is reported but there are scarce experimental demonstration on TFET devices with CMOS compatible high current ON/OFF ratio of > 6 orders and S value of < 60 mV/dec. This is possibly due to limited gate control of channel and complexity in fabrication of defect-free semiconductor channel materials. There are still some TFET challenges like ambipolar behavior, DIBT, low ON current that need to be resolved in near future. However, one of the most challenging tasks is to achieve high I_{ON} of ~ 100 μA/μm. Additionally, TFET device requires a spotless heterojunction design to obtain high I_{ON} and steep S. Therefore, high performance TFET devices needs to be experimentally demonstrated. Further, the causes behind the variation in experimental and simulation reports are needed to be explored. Therefore, there is a lot of room for research and development on TFET devices. Undoubtedly, TFET is one of the solid possible alternatives for next-generation CMOS logic technology.

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Design and Performance Investigation of Dual-Gate ZnO Nanostructured Thin-Film Transistor

Dasari Srikanya and Chitrakant Sahu

1 Introduction

Thin-film transistors are a subclass of metal oxide semiconductor field-effect transistors (MOSFETs) fabricated with less cost and have a wide variety of applications. They are extensively used in optoelectronic devices, sensors, and driving circuits of liquid–crystal displays, including organic light-emitting diodes [1–4]. In the early years of TFTs, the active channel layer was typically made of amorphous silicon (a-Si) or polycrystalline silicon (poly-Si). However, this silicon (Si)-based TFTs' performance was hampered by their limited field-effect mobility, high leakage currents, and lack of stability. These issues, however, may be addressed by using oxide semiconductor-based TFTs [5–7]. Oxide-based thin-film transistors (TFTs) provide significant carrier concentration tunability under the control of an electric field. Recently, polycrystalline zinc-oxide (Poly-ZnO) semiconductor-based TFTs have been investigated over a-Si and poly-Si-based TFTs due to better electrical properties [8]. The ZnO material has a high mobility when compared with a-Si and a low-processing temperature when compared with poly-Si. ZnO-based TFTs are highly transparent in the visible range, exhibit low-processing temperatures, have high field-effect mobility, and deliver good device performance, making them ideal TFTs for digital display applications [9, 10].

Zinc oxide (ZnO) is a newer II-VI heterostructure semiconductor with a large direct energy band-gap of 3.37 eV and a strong binding excitation energy of 60 meV. It is a preferable material for TFTs because of its excellent piezoelectric, ferroelectric, pyroelectric, optical, and electrical properties [11]. Owing to its excellent properties and applications, extensive research is going on in the domain of ZnO-based TFTs [12–14]. Hence, further investigation is needed to achieve high performance and

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better stability of these devices [15]. The performance of the ZnO TFTs can be further improved by dual-gate (DG) technology [16–20].

In our previous work, the fabrication of back gate ZnO thin-film planar FET was demonstrated and further discussed the electrical characterization for pH sensing applications [21]. This paper demonstrates DG ZnO TFT, which has enhanced electrical performance compared to single-gate devices. The dual-gate configuration can increase the electron density and electric field, together increasing the device's drive current. The DG ZnO TFT also features low leakage current, high field-effect mobility, good electrical stability, and enhanced electrical properties with a simpler fabrication process.

2 Device Structure and Simulation Setup

Figure 1a demonstrates the cross-sectional view of the dual-gate ZnO-based thin-film transistor. The two-dimensional views of top-gate (TG), bottom-gate (BG), and dual-gate (DG) ZnO TFT are represented in Fig. 1b, c and d, respectively. The dimensions for the different layers of the proposed device are ZnO channel thickness = 50 nm, gate length = 5 µm, oxide thickness = 30 nm, gate electrode work-function = 4.6 eV, and source/drain electrode's work-function = 4.33 eV. The width of the proposed device is assumed to be 200 µm. All three device structures have the same source/drain and channel length. The gate oxide thickness for both gates is assumed to be the same. For the TG configuration, the BG electrode is grounded, and for the BG configuration, the TG electrode is grounded. For DG configuration, both gates are shorted together. The proposed structures can be grown on different substrates such as silicon, sapphire, oxide-grown silicon, and glass.

The following physical models are used to carry out the 2-D simulations. Shockley–Read–Hall (SRH) was used for recombination, the Fermi Dirac mel

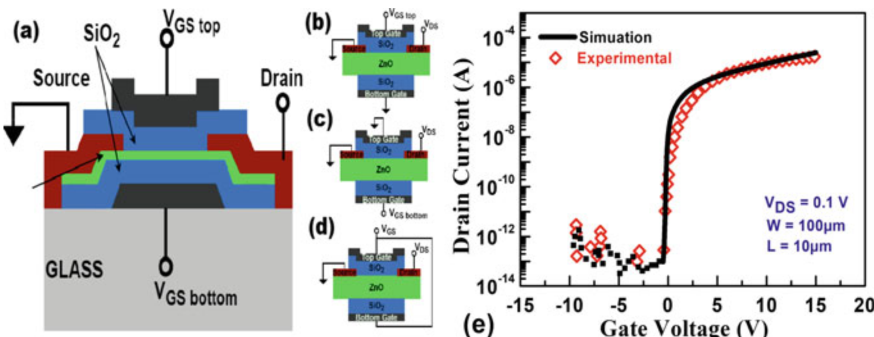

Fig. 1 **a** Cross-sectional view of the DG ZnO TFT. 2-D views of **b** TG configuration, **c** BG configuration, **d** DG configuration. **e** Calibration of simulation models with experimental data [22]

(FERMI) was used for carrier statistics, and for mobility, the CVT model was considered. Planar thin-film devices have defects in the band-gap, due to which charges a tpped. Hence, the defect state's energy distributions must also be defined in the TFT module simulations [23, 24]. An amorphous or polycrystalline TFT can be described as four different components based on the density of defect states (DOS).

$$g_{\mathrm{TA}} = N_{\mathrm{TA}} \times \exp\left[\frac{E - E_C}{W_{\mathrm{TA}}}\right] \tag{1}$$

$$g_{\mathrm{TD}} = N_{\mathrm{TD}} \times \exp\left[\frac{E_V - E}{W_{\mathrm{TD}}}\right] \tag{2}$$

$$g_{\mathrm{GA}} = N_{\mathrm{GA}} \times \exp\left[-\left(\frac{E_{\mathrm{GA}} - E}{W_{\mathrm{GA}}}\right)^2\right] \tag{3}$$

$$g_{\mathrm{GD}} = N_{\mathrm{GD}} \times \exp\left[-\left(\frac{E - E_{\mathrm{GD}}}{W_{\mathrm{GD}}}\right)^2\right] \tag{4}$$

E, E_C, and E_V represent trapped, conduction-band (CB) and valence-band (VB) energies. The subscripts A, D, T, and G, refer to the acceptor, donor (states), tail, and Gaussian levels, respectively. The DOS exponential distribution is defined by CB and VB characteristic decay energies (W_{TA} and W_{TD}) and by their intercept densities (N_{TA} and N_{TD}). Similarly, the DOS for Gaussian distribution is characterized by their total DOS (N_{GA} and N_{GD}), peak energies (E_{GA} and E_{GD}), and characteristic day energies (W_{GA} and W_{GD}). Therefore, $g(E)$ is defined as

$$g(E) = g_{\mathrm{TA}}(E) + g_{\mathrm{TD}}(E) + g_{\mathrm{GA}}(E) + g_{\mathrm{GD}}(E) \tag{5}$$

But ZnO is an n-type oxide semiconductor in this work, and ZnO nanostructured TFTs operate in an n-channel configuration; hence, acceptor-like states only were assumed. Hence, $g(E)$ is redefined as

$$g(E) = g_{\mathrm{TA}}(E) + g_{\mathrm{GA}}(E) \tag{6}$$

Various parameters pertaining to polycrystalline ZnO for 2D simulations are listed in Table 1. It is evident that background physics was properly accounted for in the simulation models after calibration with experimental data, as depicted in Fig. 1e. Calibration device dimensions are assumed to be the same as in [22].

Table 1 List of parameters defined for ZnO during 2-D simulations

Parameter	Symbol	Unit	Value
Electron's mobility	μ_n	cm^2/V-s	100
Hole's mobility	μ_p	cm^2/V-s	25
CB density of states	N_C	$/cm^3$	2.2×10^{18}
VB density of states	N_V	$/cm^3$	1.8×10^{19}
Electron affinity	χ	eV	4.5
Dielectric constant	ε	–	8.49
Energy band-gap	E_g	eV	3.37
Electron's lifetime	τ_n	s	4.2×10^{-6}
Hole's lifetime	τ_p	s	6.58×10^{-6}
–	N_{TA}	$/cm^3$.eV	8×10^{20}
–	W_{TA}	eV	0.025
–	N_{GA}	$/cm^3$.eV	3×10^{17}
–	W_{GA}	eV	0.35
–	E_{GA}	eV	1.4

3 Results and Discussions

We characterized the electrical performance of TG, BG, and DG ZnO TFT using TCAD Silvaco Atlas V5.32.1.R [22]. The transfer and output characteristics of the TG, BG, and DG ZnO TFT are depicted in Fig. 2 for various biasing conditions. The characteristics of a TG and BG are measured by applying a voltage to the respective electrodes while the other electrode is grounded, whereas, for DG configuration, a same voltage is applied to both gates. The DG ZnO TFT exhibits a higher ON-to-OFF current ratio than TG and BG devices. The DG ZnO TFT perceives an ON-to-OFF current ratio of 5.27×10^{10}, while the comparable values of the TG and BG ZnO TFTs are 5.66×10^9 and 5.87×10^9, respectively. The threshold voltages of TG, BG, and DG are −193 mV, −194 mV, and −152 mV, respectively. The measured SS of TG, BG, and DG ZnO TFTs are 142 mV/dec, 140 mV/dec, and 64 mV/dec, respectively. Since the DG ZnO TFT has two gates, a steeper subthreshold swing is attained. The ON current of DG ZnO TFT is 58% higher than the sum of the ON current of TG and BG TFTs. The drain current of ZnO TFT follows the standard MOSFET current equations

$$I_{\text{DS Linear}} = \mu_n C_{\text{OX}} \frac{W}{L} (V_{\text{GS}} - V_T) V_{\text{DS}} \tag{7}$$

$$I_{\text{DS sat}} = \frac{1}{2} \mu_n C_{\text{OX}} \frac{W}{L} (V_{\text{GS}} - V_T)^2 \tag{8}$$

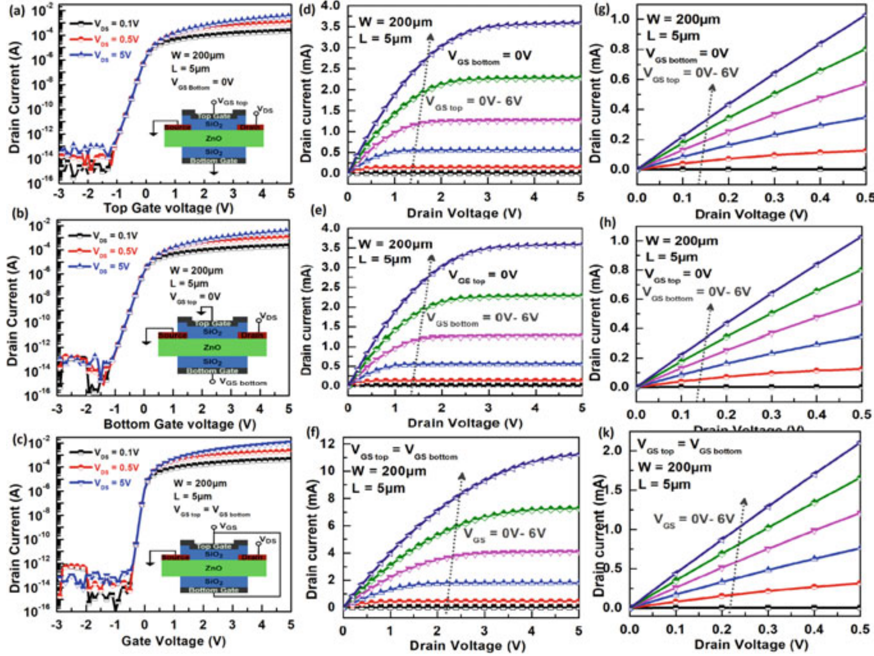

Fig. 2 Transfer characteristics of ZnO nanostructured TFT for **a** TG, **b** BG, **c** DG configurations; output characteristics of ZnO nanostructured TFT for **d** TG, **e** BG, **f** DG configurations; output characteristic details shown for the 0 V ≤ V_{DS} ≤ 0.5 V for **g** TG, **h** BG, **k** DG configurations

The gate oxide capacitances ($C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$) of TG ZnO TFT and BG ZnO TFT can be calculated using the dielectric constant and thickness of the top- and bottom-gate oxides, respectively. But the capacitance of a dual-gate ZnO TFT is not easily defined. Since the same gate voltage is applied on both the electrodes, the oxide capacitors are connected in parallel from the ZnO active layer (channel). Hence, the dual-gate configuration's equivalent gate oxide capacitance is the sum of the top-gate oxide capacitance and bottom-gate oxide capacitance. Since both gate oxide dielectric constant and thickness are the same, the measured gate oxide capacitances of TG configuration and bottom-gate configuration are the same, and it is equal to 0.115 $\mu F/cm^2$. The corresponding value of the dual-gate configuration is twice the single-gate capacitances. In order to make a more quantitative comparison, some figures of merit (FOM) are presented in Table 2. These findings suggest that the DG ZnO TFT has superior electric performance over the SG ZnO TFT.

Figure 3 describes the contour plots of electron carrier concentration and electric field of TG, BG, and DG configurations. From Fig. 3a, it is clear that DG configuration induces high electron concentration compared to TG and BG configurations. Also, we can observe that the total electric field intensity in the channel layer for DG configuration is stronger than TG and BG configurations, as shown in Fig. 3b. As a

Table 2 Comparison of some figure of merits

Parameter	Top-gate	Bottom-gate	Dual-gate
I_{ON} (mA)	3.59	3.53	11.23
I_{OFF} (A)	6.35×10^{-13}	6.01×10^{-13}	2.13×10^{-13}
V_{TH} (V)	−0.193	−0.194	−0.088
C_{OX} (μF/cm^2)	0.115	0.115	0.232
SS (mV/dec)	142	140	64
I_{ON}/I_{OFF}	5.66×10^9	5.87×10^9	5.27×10^{10}

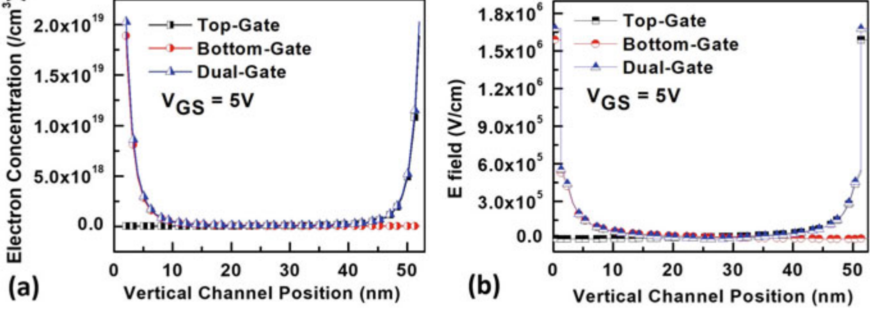

Fig. 3 **a** Electron concentration. **b** The total electric field of TG, BG, and DG configurations at $V_{GS} = 5$ V

consequence of this, the drive current of the DG ZnO is much larger than single-gate ZnO TFTs due to the high electric field.

Figure 4 depicts the impact of different gate oxides on the electrical performance of the proposed DG ZnO TFT. Different gate oxides such as SiO_2, Si_3N_4, Al_2O_3, HfO_2, Ta_2O_5, and TiO_2 were considered for the analysis. Among all gate oxides, SiO_2 has the lowest dielectric constant, and TiO_2 has the highest dielectric constant. Figure 4a and b depicts the device's transfer and output characteristics for different gate oxides. The DG ZnO TFT with TiO_2 dielectric exhibits a greater output drain current than the DG ZnO TFT with other dielectrics. It is observed that optimized DG ZnO TFT showed good electrical performance at the gate oxide with a high electric constant (TiO_2). Figure 4c describes the effect of different gate oxides on the drive-ON current (I_{ON}) of DG ZnO TFT. A high dielectric constant enhances the gate capacitance, which improves the drive-ON current for the same gate biasing. The DG ZnO TFT with TiO_2 oxide layer provides high I_{ON} compared to all other oxides since it has the highest dielectric constant.

Figure 5 illustrates the electrical performance of DG ZnO nanostructured TFTs depending on channel thickness. In this analysis, SiO_2 and TiO_2 dielectrics are assumed for both the proposed device's bottom- and top-gate dielectrics. The channel thickness of the device was systematically increased from 10 nm to 100 nm. Figure 5a, b, and c shows the device's transfer curves, output characteristics, and drive-ON

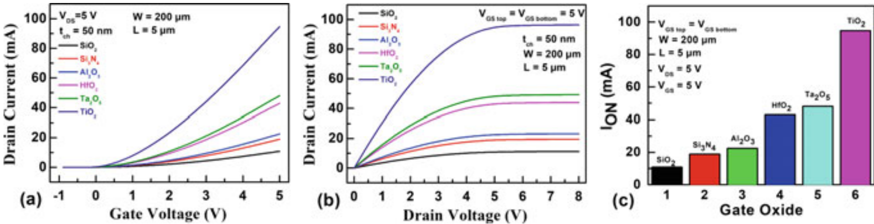

Fig. 4 **a** Transfer characteristics, **b** output characteristics, **c** drive-ON current of the DG ZnO Nanostructured TFT at different gate oxide layers

current while considering both the top and bottom dielectric of the device as SiO_2. Similarly, the corresponding plots for TiO_2 dielectric are depicted in Fig. 5d, e, and f. Transfer curves of the device for different channel thicknesses observed at the gate biasing (V_{GS}) varied from -1 V to 5 V, and the drain voltage (V_{DS}) was fixed at 5 V. The carrier concentration in the channel increases with the channel thickness, resulting in the device's V_{th} shifting negatively. The DG ZnO TFT with TiO_2 dielectric exhibits a higher drain current (178.14 mA) which is 15× greater than the corresponding value (11.88 mA) of the DG ZnO TFT with SiO_2 dielectric aannel thickness of 10 nm.

The output characteristics depend on the channel thickness at a fixed V_{GS} of 5 V and are observed for both SiO_2 and TiO_2 dielectrics. However, the drain voltage varies from 0 V to 8 V to include saturation effects in the drain current. Reducing the channel's thickness improves the proposed device's electrical properties in terms of

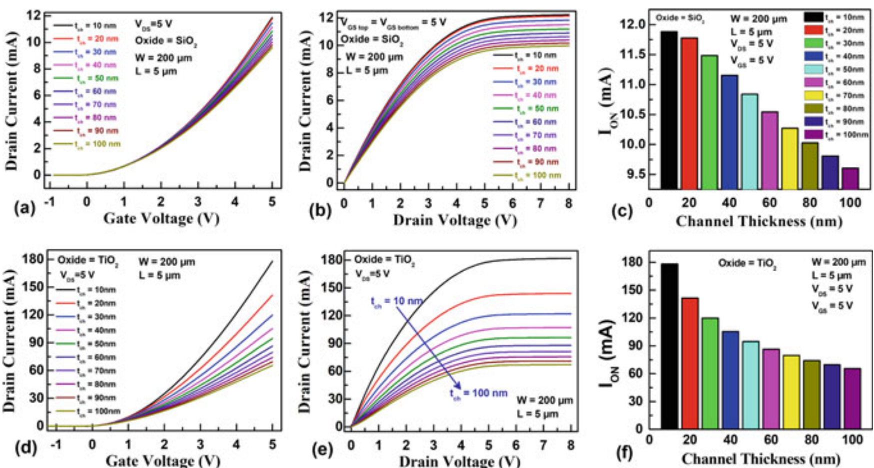

Fig. 5 **a** Transfer characteristics, **b** output characteristics, **c** Drive-ON curent of the DG ZnO nanostructured TFT at different channel thicknesses at SiO_2 gate dielectric **d** Transfer characteristics, **e** output characteristics, **f** Drive-ON current of the DG ZnO nanostructured TFT at different channel thicknesses at TiO_2 gate dielectric

ON-current, output drain current, I_{ON}/I_{OFF} ratio, and mobility. The impact of channel thickness on the drive-ON current (I_{ON}) of DG ZnO TFT is also analyzed for both dielectrics. A decrease in channel thickness results in an increase in I_{ON} of the device. When the channel thickness decreases, the total electric field strength in the center of the channel layer also increases with edges, which improves effective channel conduction, leads to an increase of ON current of the device. For SiO_2 gate, dielectric I_{ON} of the device is increased from 9.61 mA to 11.88 mA, respectively, when channel thickness decreases from 100 nm to 10 nm. Similarly, the corresponding increment in the I_{ON} for TiO_2 dielectric is noted from 65.56 mA (at $t_{ch} = 100$ nm) to 178.14 mA (at $t_{ch} = 10$ nm). This superior characteristic makes DG ZnO TFT a potential device for optoelectronics, sensors, and liquid–crystal displays.

4 Conclusion

In summary, simulations of the DG ZnO TFT have been performed, and its electrical properties are described and compared with those of the TG and BG ZnO TFTs. Under dual-gate biasing, the top-gate and bottom-gate electrodes generate two conduction layers at the channel's top and bottom interfaces, improving total channel conductivity. A high I_{ON} of 11.23 mA and a steeper subthreshold swing of 64 mV/dec are achieved without affecting I_{OFF}. The I_{ON}/I_{OFF} ratio was also calculated and found to be higher compared to the rest of the two devices. The lower subthreshold swing of DG ZnO TFT can switch the device faster from OFF-state condition to ON-state condition. The impact of the channel thickness on the I_{ON} is analyzed, and I_{ON} increases as the channel thickness decreases. The influence of gate oxide dielectric on I_{ON} is also inspected, and I_{ON} increases with the dielectric constant. Therefore, the high mobility dual-gate ZnO nanostructured TFT has enhanced electrical performance, and that makes it a suitable candidate for optoelectronic devices, sensors, and liquid–crystal displays.

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Investigation of Normally-Off β-Ga_2O_3 Power MOSFET Using Ferroelectric Gate

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1 Introduction

Gallium oxide (Ga_2O_3) is currently fast emerging as a favorable material for futuristic electronic power devices. Among its five known polymers, the β-phase is the most stable one and widely reported. In addition to its ultrawide bandgap of ~ 4.9 eV which enables a high breakdown electric field up to 8 MV/cm [1], it has a wide variety of n-type dopants such as Si or Sn and can achieve very controllable doping in the range of 10^{15}–10^{20} cm^{-3} [2–4]. Recently, electron velocity of ~ 1.1×10^7 cm/s is measured in Ga_2O_3 modulation-doped field-effect transistors (MODFETs) [5]. Apart from its excellent physical and material properties, sustained progress of bulk crystal growth and availability of inexpensive native substrate are proved to be the real growth drivers for the β-Ga_2O_3 devices.

To date, various Ga_2O_3 power devices have been developed such as Schottky barrier diodes (SBDs) having forward current of 1 A [6], and reverse breakdown voltage of 3 kV [7], metal–oxide–semiconductor field-effect-transistors (MOSFETs) with high output currents of 650 mA/mm [8], and modulation-doped β-$(Al_XGa_{1-X})O_3/Ga_2O_3$ heterostructure or high-electron-mobility-transistors

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(HEMTs) [9–11]. These devices have demonstrated promising dc and RF performance suitable for power applications. However, due to the unavailability of reliable p-type dopants, most of the reported devices essentially operate in the depletion-mode (D-mode). Despite this inherent challenge and considering the importance of off-state power mitigation, a fairly enough number of enhancement-mode (E-mode) β-Ga_2O_3 MOSFETs have been already reported. The different structures include gate-recess [12], wrap-gate fin-array [13], Si-doped access regions [14], and vertical FinFETs [15]. However, the E-mode 'status' of all these devices was obtained at the cost of complicated designs and regularity issues [13], low on-current [14], poor gate control due to the thick gate dielectric [14, 15], among others. Taking cues from gate charge storage in GaN HEMTs metal–insulator–semiconductor (MIS) structures, some of the recent reports [16–18] have successfully demonstrated β-Ga_2O_3 MOSFETs E-mode operation using ferroelectric gate (FeG). The underlying technique is found to be simple yet effective way to achieve E-mode operation without degrading channel conductivity. Since large bandgap of ultrawide bandgap (UWB) semiconductors enables lower value of intrinsic carrier concentration (n_i), these semiconductors find useful application in harsh atmospheric conditions and at high temperature. Utilizing this property of Ga_2O_3, Noh et al. [19] demonstrated ferroelectric β-Ga_2O_3 FET operations up to 400 °C. These β-Ga_2O_3 devices utilized either single or multiple layers of FE material along with Al_2O_3 as gate dielectric to trap gate charges at the interface of FE and Al_2O_3. Subsequently, these trap charges enable depletion of the channel charge to achieve E-mode operations. However, these devices find it difficult to achieve both high breakdown voltage (V_{BR}) and low on-resistance (R_{ON}), simultaneously. Although, thicker drift region facilitates higher V_{BR} but at the cost high R_{ON}.

Here, this work proposes HfO_2/β-Ga_2O_3 ferroelectric FET and investigates the effect of back barrier layer on the various electrical parameters related to E-mode operations. The gate stack for the proposed β-Ga_2O_3 ferroelectric MOSFET (FE-MOSFET) utilizes HfO_2 and Al_2O_3 of thickness 17 nm and 5 nm, respectively, as given in [17]. Ferroelectric hysteresis loop for HfO_2 is analyzed to estimate the value of initialization gate pulse voltage and time duration. Furthermore, thickness of unintentional doped (UID) β-Ga_2O_3 back barrier layer is varied to assess the resulting effect on threshold voltage (V_{TH}) shift. Furthermore, the effect of UID β-Ga_2O_3 back barrier layer on drain leakage current is also analyzed. After achieving the normally off-state operation of the β-Ga_2O_3 FE-MOSFET, rigorous simulation cycles were performed to achieve high-power figure of merit (PFoM) by optimizing the values of both V_{BR} and R_{ON}.

2 Device Structure and Simulation Framework

The cross sections of the analyzed devices are shown in Fig. 1. The device cross section structure shown in Fig. 1a is kept similar to the device given in [17], and Fig. 1b shows the device with UID β-Ga_2O_3 back barrier layer. The back barrier

layer alleviates leakage current and is in sync with the earlier findings reported in [20]. Apart from back barrier layer, both of the analyzed devices have common device dimensions and same values of other parameters, including layer thickness, doping, and type of concentration. The epitaxial layer sequence contains Sn-doped (n-type in β-Ga_2O_3) drift layer of 150-nm thickness on a semi-insulating β-Ga_2O_3 substrate which is unintentionally doped with Fe. These n-type impurities stem from crucible and usually incorporated during growth of β-Ga_2O_3 single crystal substrates using melt growth techniques. Various experimental evidences, reported earlier, had already established about unintentional doping in β-Ga_2O_3 substrates. β-Ga_2O_3 channel layer is followed by 17-nm hafnium-oxide and 5-nm aluminum-oxide (HfO_2-Al_2O_3) as gate dielectrics. The access areas under source and drain contacts are heavily doped (n-type, 10^{19} cm^{-3}) to obtain low contact resistance of these ohmic contacts. Gate contact is kept as Schottky type, and work function of the gate material is set as 4.7 eV. Finally, outer surface of the devices is passivated using Si_3N_4 to alleviate environment contaminants. All other fabrication related details are given in [17].

Physics-based 2-D device simulator—ATLAS Silvaco is used to analyze the electrical characteristics of the device. The simulation framework includes different physical models like Shockley–Read–Hall (SRH) for recombination, Fermi–Dirac for carrier statistics, and low-field mobility model for electron mobility. β-Ga_2O_3 material parameters are taken from [21], while other required parameters are used as default values given in [22]. Since lattice thermal conductivity of β-Ga_2O_3 is quite low and affect electron mobility at the higher temperatures, thermal model LAT. TEMP is included to account for lattice heat flow and associated effect on electron mobility in the simulated device. The low-field default mobility model as given in [22] is used, given as:

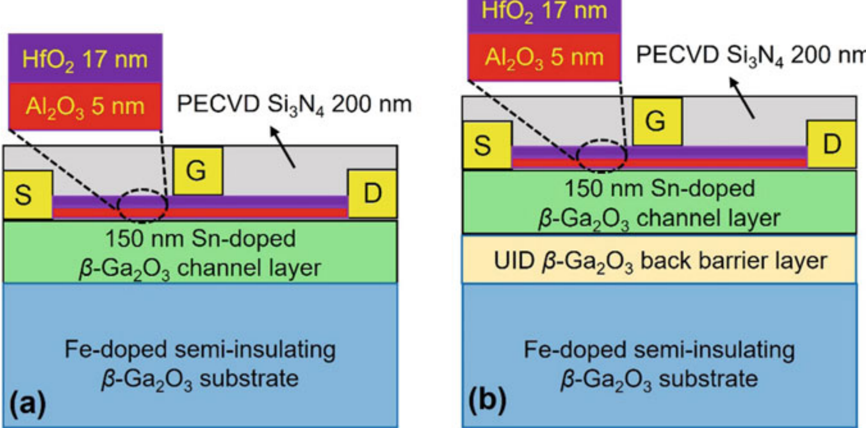

Fig. 1 Schematic cross section of β-Ga_2O_3 FE MOSFET showing **a** HfO_2/Al_2O_3 gate stack and **b** with UID β-Ga_2O_3 back layer

$$\mu_{n0} = \text{MUN}\left(\frac{T_L}{300}\right)^{-\text{TMUN}} \quad (1)$$

where T_L is the lattice temperature, and mobility values for electron and holes MUN/MUP = 140/50 cm^2/Vs, temperature-dependent coefficients TMUN/TMUP = 2/1.5 are updated for β-Ga_2O_3 channel in the mobility model statements.

3 Results and Discussion

As discussed in previous section, the proposed device uses ferroelectric gate charge storage to achieve enhancement mode in β-Ga_2O_3 MOSFET, and ferroelectric characteristics of HfO_2 of is analyzed first and shown in Fig. 2. Polarization–electric field (P–E curve) and capacitor-electric field (C–E curve) are plotted for 5, 12, 17-nm, and 17-nm thick HfO_2, respectively. As the thickness decreases polarization value increases, and for 5-nm thick HfO_2, polarization value of 12 μC/cm^2 is obtained. Hysteresis in the P–E curve is also evident for all three thickness of HfO_2. This confirms the ferroelectric property of the 17-nm thick HfO_2.

The E-mode operation in proposed β-Ga_2O_3 is achieved using gate charge trapping as elaborated in [17]. A transient gate pulse of amplitude 5 V and pulse width of 1 ms is applied in the steady state of the device. The pulse amplitude is derived on the basis of P-E curve shown in Fig. 2a. Due to strong polarization charge of the HfO_2 material, charges are trapped at the HfO_2-Al_2O_3 interface. These charges are modeled by interface charge in the simulation. A fixed negative charge of 1×10^{12} cm^{-2} at the HfO_2-Al_2O_3 interface is used to deplete the channel charges and achieve E-mode operation in the β-Ga_2O_3 FE-MOSFET. The following formulas are used to calculate the electron concentration in the channel (N_e) to achieve E-mode operation.

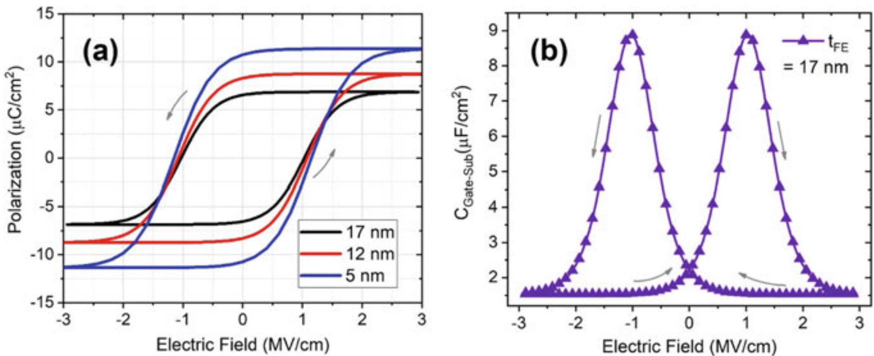

Fig. 2 P–E hysteresis curve (**a**), and C–E curve (**b**) of metal-HfO_2-metal capacitor

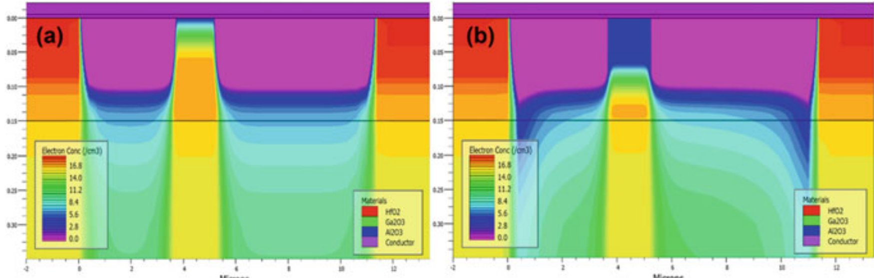

Fig. 3 Gate pulse application and effect on channel charges **a** before pulse application, charge depletion occurs due to the negative fixed interface charge; **b** after gate pulse application, charge depletion also happens under the gate

$$E_F - E_c = k_0 T \ln\left(\frac{N_e}{N_c}\right) \tag{2}$$

$$\Delta E_C = E_g^{\text{dielctric}} - E_g^{\text{Ga}_2\text{O}_3} - \Delta E_V \tag{3}$$

where the constants are k_0 (Boltzmann constant), T (temperature), and N_C (conduction band state density of 3.72×10^{18} cm^{-3}) [23]. The estimated value of electron concentration, before and after the application of gate pulse, in the channel is analyzed and shown in Fig. 3. Both results are extracted from device structures biased in steady state. During the initialization process, gate pulse is absent; however, due to interface charge at HfO_2-Al_2O_3 boundary, charge carriers are depleted from source–gate and gate–drain access regions, as shown in Fig. 3a. After the application of gate pulse charges under the gate are also depleted apart from strong depletion from source and drain access regions. Effectively, the channel is depleted from the electrons, and E-mode operation is achieved. It is worth to mention that, here, highly-doped ohmic-contacts access regions help to achieve similar amount of current in E-mode as compared to D-mode β-Ga_2O_3 FE-MOSFET. Furthermore, strong polarization charge of HfO_2 is quite sufficient to deplete the channel charges, however, less than as reported for HZO dielectric in [17]. Therefore, use of HfO_2 may not achieve full channel depletion in devices having thick drift region.

The electrical characteristics including I_D–V_G and I_D–V_{DS} curves of the analyzed device are shown in Figs. 4, 5 and 6. The plots also include characteristics curves those for D-mode. This will help to analyze both the operations simultaneously and provide an easy assessment of device parameters.

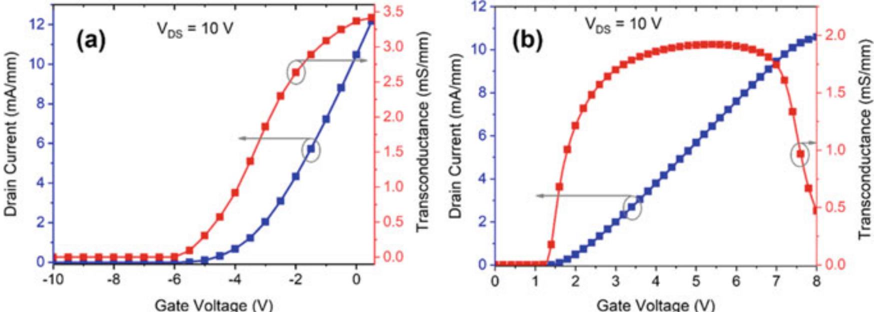

Fig. 4 Transfer characteristics of the analyzed devices, **a** D-mode operation showing V_{TH} of—5.45 V; **b** E-mode operation showing V_{TH} of 1.4 V

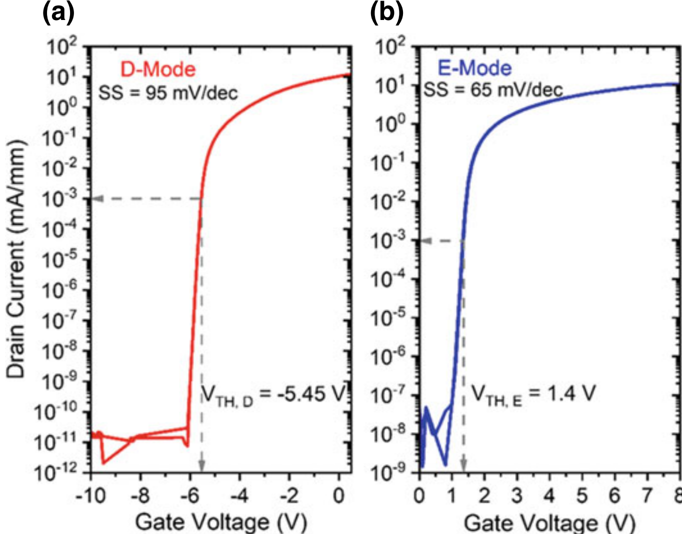

Fig. 5 Transfer characteristics of the analyzed devices on log scale showing I_{ON}/I_{OFF} and subthreshold slope for **a** D-mode operation and **b** E-mode operation of the β-Ga_2O_3 FE-MOSFETs

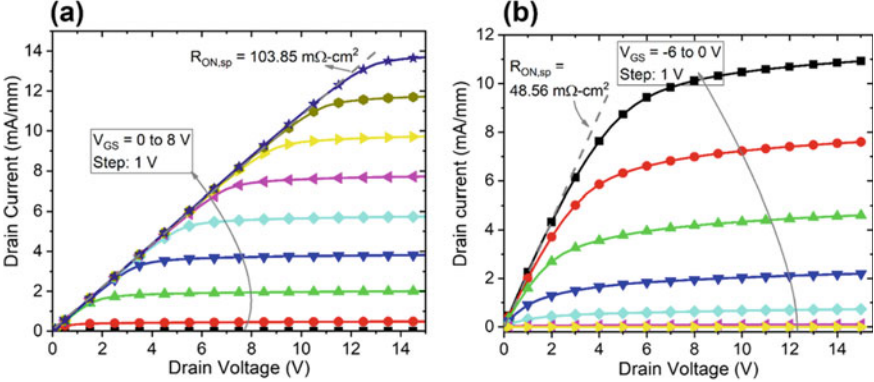

Fig. 6 Output drain characteristics of the β-Ga_2O_3 FE-MOSFETs in **a** D-mode operation with $R_{ON\text{-}sp}$ of 103.85 mΩ-cm^2, and **b** E-mode operation with $R_{ON\text{-}sp}$ of 48.56 mΩ-cm^2

4 Conclusion

Normally-off operation in β-Ga_2O_3 MOSFET is achieved using ferroelectric gate oxide. The high polarization charge of the HfO_2 is trapped at the interface of HfO_2-Al_2O_3 interface which caused depletion of channel charge from the device. The trapped charges are modeled as fixed interface charges during the simulation, and the operation of charge depletion is demonstrated showing electron concentration in the device at steady state. Results show that there is a negligible degradation of peak current in E-mode as compared to D-mode operations. Nevertheless, highly-doped ohmic-contacts access regions help to achieve rather flat transconductance curve and lower values of sub-thresholds slope and specific on-resistance. Furthermore, E-mode β-Ga_2O_3 MOSFET achieves a high breakdown voltage (V_{BR}) of 2250 V (not shown in results), when combined with $R_{ON,sp}$ brings in a figure of merit ($V_{BR}{}^2$/$R_{ON,sp}$) of 49 MW/cm^2. The results indicate effectiveness of the ferroelectric gate and resulting trap charges to achieve E-mode operations in always-on β-Ga_2O_3 device, over other methodologies.

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Micro/Nanoelectronics Circuits

Resource-Efficient TCAM Implementation Using SRAM

Madhu Ennampelli and Kuruvilla Varghese

1 Introduction

Memories are broadly divided into three types, namely random access memories, serial access memories, and content addressable memories (CAM). Random access memories gives the content of the specific memory location when the address of the memory location is provided; CAM operation is exactly opposite to these memories, finding address of the given data stored in memory. CAM is also called binary CAM, since it is used to match a '0' or a '1'. As an extension to CAM memories, ternary content-addressable memories (TCAM) have the additional feature of 'don't care' bit that can match a '0' or a '1'. There are two types of TCAMs, global masked and local masked. TCAM operation can be inferred in two ways: storing the 'don't care' bit in a direct CAM table, this is called locally masked TCAM, and another way is searching the address with content that has 'don't care' bits; this is called globally masked TCAM.

A typical TCAM has SRAM cells and a complex comparison circuit to store the data. In the SRAM cell conceptually, '0', '1', and 'X' (don't care) will be stored.

In most of the TCAM implementations, SRAMs are used as original address table address (OATA) memories. Addresses corresponding to the TCAM table will be stored in OATA memories, and the size of each OATA memory is $2^w \times w$, where **w** is the number of bits in the input subword.

There has been demand for a computer memory that can do what human memory does naturally. Specifically, such memory should be associative. In order to be practical, such a memory would also need to be fast, stored in a high-density medium,

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and inexpensive. CAM is one such memory that is fast and intuitive. CAMs are preferred in most applications involving fast searches like buffer memory organization, pattern recognition, communications networking, artificial intelligence, disk/database Caching, IP routing, and parallel data processing.

1.1 Related Work

The work on RAM-based TCAMs is limited. TCAM-based RAM are discussed in many publications, but most of them have the problem that the required memory increases exponentially with respect to the increase in the word length of the TCAM table. This problem causes inefficient utilization of memory in designs. For example, 36 bits of TCAM word requires 64 GB of RAM to emulate TCAM functionality.

Most of the existing RAM-based TCAM operates at lower frequencies. This is because of the complex circuitry between RAM and decoding logic. These types of TCAM designs utilize complex high order priority encoders and excessively utilize RAMs, causing increase in the critical path delay.

The work in [1] introduces the hybrid partitioning of TCAM to reduce this exponential relation between TCAM word and RAM required, and validation memory is implemented as $2^{w-b} \times 2^b$ array, and because of 2^b bits in each location, power consumption and decoding output of bit is complex. In [2], design is improved by using $2^w \times 1$ size for each validation memory and design uses their Original Address Table (OAT) memory address stored in OATA memory. But this TCAM functionality can be emulated by bypassing this OATA memory resulting in effective design of TCAM using RAMs. This design introduces OATA less TCAM design, which improving memory utilization compared to previous work in [3], and as a consequence of this, power consumption and combinational logic delay will also reduce.

1.2 Paper Organization

The rest of the report is organized to give the details regarding the design of TCAM. Section 2 describes our hybrid partitioning algorithm. Section 3 elaborates description of TCAM architecture. Section 4 explains the data mapping and search operation TCAM. Section 5 discusses results and optimization comparison tables. Section 6 concludes the design brief.

2 TCAM Table Hybrid Partitioning

A given TCAM table is divided into vertical and horizontal partitions using hybrid partitioning. As shown in Fig. 1, these partitions are called TCAM subtables, and each of these subtables are mapped to their corresponding SRAM cells. Based on the entries of the TCAM table, corresponding SRAM cells data will be stored with their respective data. This data mapping is explained in Sect. 5. In TCAM partitioning, the input TCAM word of C bits is divided vertically into N subwords of each w bits, and vertical partition will reduce the memory utilization of TCAM, as the exponential relation between the number of bits and required memory is relaxed to a linear relationship. TCAM's original address range is divided into L address ranges by horizontal partition, and each vertical partition subword is divided into L horizontal partitions. Horizontal partitioning alone will increase the number of memory units required. Hence, it will be power, cost, and area hungry. But horizontal partitioning makes a good layering structure for TCAM. Hence, it is easily scalable. Therefore, by combining vertical partitioning and horizontal partitioning optimization, a resource-efficient TCAM can be designed. After partitioning, the TCAM table will be divided into total $L \times N$ hybrid partitions. It should be understood that number of horizontal and vertical partitionings is equal to the number of layers and number of subwords, respectively. An example of 4×4 TCAM with hybrid partitioning sizes of $L = 2$ and $N = 2$ is shown in Fig. 2.

The size of each hybrid partitioning will be $K \times w$ bits, where K is a subset of the original address range, and each subword will have w bits. Subtables with the same address ranges will span the same layer.

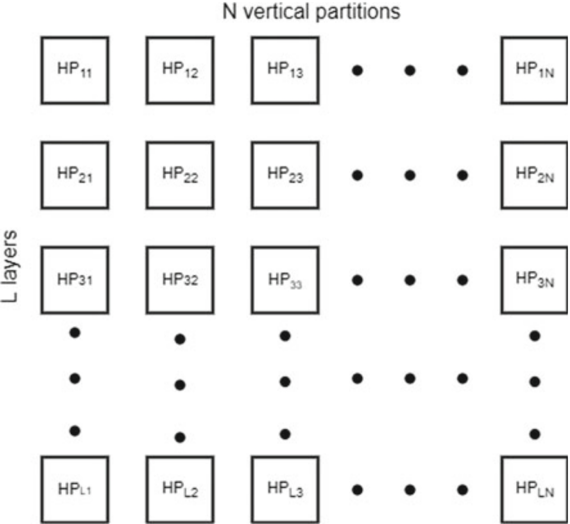

Fig. 1 Simplified diagram of hybrid partitioning

Address	Hybrid partitions				Layer
0	00		11		
1	01	HP_{11}	01	HP_{12}	1
2	0x		11		
3	11	HP_{21}	1x	HP_{22}	2

Fig. 2 TCAM table of size 4 × 4

3 Overall Architecture

In resource-efficient TCAM implementation, the overall architecture has one TCAM priority encoder and *L* layering blocks for each layer, which is shown in Fig. 3. In search operation, input word of *N* subwords is applied to each layer of the architecture, and each layer will generate its corresponding potential match address (PMA). These generated PMAs from each layer are further fed to the TCAM priority encoder to select one matched address (MA) which has the highest priority.

As shown in Fig. 4, the layered architecture of resource-efficient TCAM has the input of *N* subwords with each of *w* bits. These N subwords are fed to N validation memories (VMs) and *N* original address tables (OATs) as addresses. In addition to these memories, layer priority encoder (LPE) selects one highest priority matched output in each layer. The 1-bit AND operation will confirm the presence of all subwords in each layer, and *K*-bit AND operation is for finding the exact location

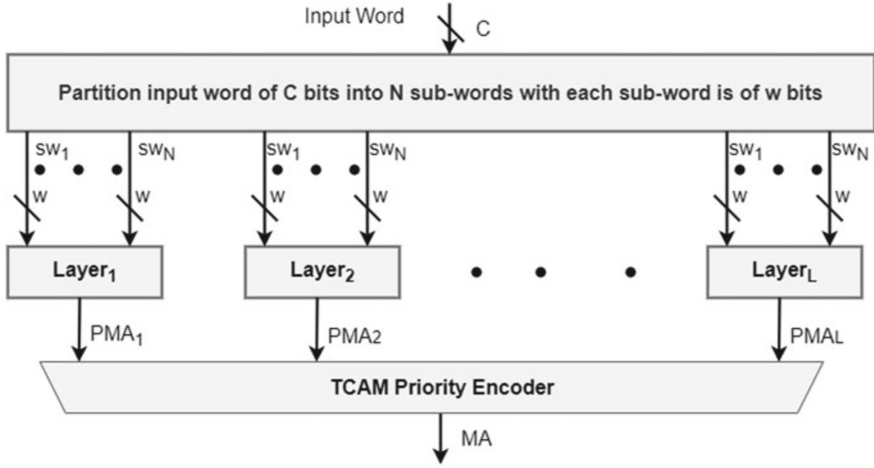

Fig. 3 Overall architecture of resource-efficient TCAM

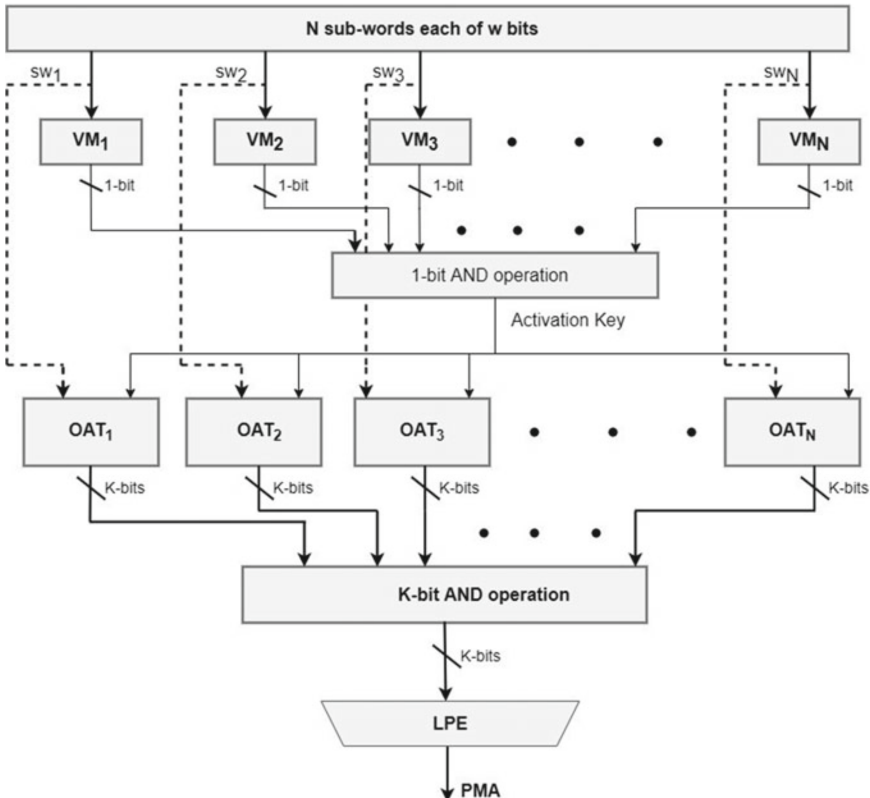

Fig. 4 Layer architecture of resource-Efficient TCAM

of the input word in each layer. In the final stage, TCAM priority encoder selects matched address from highest priority layer.

Each VM has a size of $2^w \times 1$ bits, where w denotes the subword's bit count, and 2^w denotes the number of rows in each VM.

OAT has the following dimensions: $2^w \times K$, where w is the number of bits in a subword, 2^w is the number of rows, and K is the number of bits in each row, each of which represents an original address. K is a subset of the original addresses in the traditional TCAM table in this instance. The outputs of VMs are used as enabling signals to lower the power consumption of OAT memories, which effectively lowers the switching activity of the OAT memories. This 1-bit AND operation performs AND operation on outputs of the VMs. This result decides the flow of the search operation. If the ANDed output is high, the search operation continues; otherwise, it does not.

This K-bit AND operation is used for performing bitwise AND operation of output data from OATs. These ANDed K-bits are further fed to layer priority encoder (LPE), which generates the corresponding PMA output from each layer.

Since in a TCAM, more than one matches are possible, to select one address in each layer when multiple matches occur, the LPE is used. This PE is used to select one PMA when multiple PMAs from layers are matched.

4 Data Mapping and Searching

The TCAM table is intelligently divided into hybrid parts. Being a TCAM, the table might have a 'don't care' bit. Since SRAM cannot store 'don't care' bits, 'don't care' bit extended into paired bits (0 and 1). For instance, assuming that a ternary expression of 01X0 is available in a TCAM table, then, at that point, it is first expanded into 0100 and 0110. Then, the data of these two words are stored in their corresponding VMs and OATs.

Figure 4 illustrates how each subword acts as an address to access a particular memory location in the memory blocks. Each subword is applied to the VM that corresponds to it, and a high logic value is stored there to signify the presence of that subword in the layer. The corresponding OAT is additionally addressed using the comparable subword, and *K*-bits are saved in that memory region. In these *K*-bits, if a TCAM table has a subword in a layer, then the corresponding bit in these *K*-bits are made high. In this way, VMs and OATs are initialized. For the example in Sect. 2, HP_{11} has two subwords 00 and 01; it belongs to layer 1. Hence, the corresponding VM will be VM_{11} with the size of 4×1. In this, at 00 and 01 locations, logic high value will be stored, in the remaining location, the logic low will be stored, it is shown in Fig. 5, and for this example, for HP_{22} corresponding OAT will be OAT_{22}. In this hybrid partition subword, 11 present at the second and third addresses and 10 are present only at the third address. In OAT_{22}, in addresses 0 and 1, zeros will be stored because 00 and 01 are not in HP_{22}. At address 2 in OAT_{22}, 0 and 1 will be stored because 10 present only at address 3 in the TCAM table, and at address 3 in OAT_{22}, 1 and 1 will be stored because 11 present in both 2 and 3 locations in the TCAM table. Layer 1 and layer 2 OATs are shown in Fig. 6.

In the resource-efficient TCAM's search procedure, N subwords are simultaneously applied to each layer, which are subsequently fed to the corresponding VMs

Address	Layer1		Layer2	
	VM_{11}	VM_{12}	VM_{21}	VM_{22}
0	1	0	1	0
1	1	1	1	0
2	0	0	0	1
3	0	1	1	1

Fig. 5 Data mapping of layer 1 and layer 2 VMs

Address	Original addresses							
	Layer1				Layer2			
	OAT_{11}		OAT_{12}		OAT_{21}		OAT_{22}	
	0	1	0	1	2	3	2	3
0	1	0	0	0	1	0	0	0
1	0	1	0	1	1	0	0	0
2	0	0	0	0	0	0	0	1
3	0	0	1	0	0	1	1	1

Fig. 6 Data mapping of layer 1 and layer 2 OATs

and OATs. All N subwords are read out as addresses from their respective VMs in the associated memory locations. VMs' output is logic high, if the corresponding subword is present; otherwise, a logic low. If all VMs outputs are logic high, that indicates all subwords are present in the layer, and if all the subwords are in single row, then there is a chance that the input word will be matched. Hence, to confirm that, AND operation done on VMs outputs, and this output is the activation-key. Therefore, if the activation-key is logic high, then the search operation will continue; otherwise not. This activation-key acts as enable signal for subsequent stage memories OATs.

Input subwords are also applied to corresponding OATs as addresses, and if the activation-key for that corresponding OAT is high, then corresponding OAT K-bits are output; otherwise, these output K-bits will be zero. These K-bits from each OAT are fed to K-bit bitwise AND operator. In output K-bits, each logic high bit indicates that all subwords are in single row which confirms the matched address. This ANDed output is fed to LPE, by which highest priority matched address is selected. Output of the LPE is potential matched address (PMA). Then, these layer outputs PMAs fed to TCAM priority encoder by which highest priority layer output will be selected from all layer outputs which is final matched address (MA).

An information word mismatch during a search activity in a layer can occur at two different locations. When a 1-bit AND operation in the first level yields a logic zero, it means that at least the input subword is absent from the corresponding layer. Therefore, a match of the address in the appropriate layer is not possible.

If the activation-key from ANDed output is high, it is possible that not all of the subwords come from the same word. After K-bit AND operation, none of the bits in this situation are high. The whole search process has a throughput of one clock cycle and a delay of four clock cycles.

Table 1 FPGA implementation results of resource-efficient TCAM of size 64 × 32

Implementation	BRAM (18 K)	FFs	LUTs	Speed (MHz)	Power (mW)
Z-TCAM	32	198	447	190	35.69
Efficient TCAM	26	164	233	210	33.00

5 TCAM Implementation and Results

The resource-efficient TCAM is implemented with a size of 64 × 32 with $L = 4$ and $N = 4$ using Verilog HDL on Xillinx FPGA xc7z030sbg485-3. Different test vectors are applied to verify the functionality of the design. Maximum frequency, resource utilization, and power consumption of the example design comparisons are shown in Table 1. Design parameters were improved in all corners like speed by 10.52%, power by 7.62%, and resource utilization by 50% compared to performance in [3].

To accurately measure the power consumption of the design on FPGA, the switching activity interchange format file was generated. In Xilinx Xpower Analyzer using SAIF file, total dynamic power consumption was estimated with 1.0 V core voltage and 100 MHz operating frequency.

An ASIC design for the same architecture is implemented using Cadence tool with Generic Process Design Kit (GPDK) library on 45-nm CMOS technology node. In this tool, the total placement and route of the design is automated using the Innovus tool; this will confirm the technical feasibility of the design on a chip. Layout of ASIC implementation is shown in Fig. 7. At the end of the ASIC flow, graphic database system (GDS) file has been generated. ASIC design performance is compared with performance in [3], and it is shown in Table 2. Design parameters were improved in all corners like speed by 121.10%, power by 70.12%, and area uses reduced by 18.7 times compared to performance in [3]. In the GPDK library, standard hard intellectual property (IP) are not there for memories. Hence, for memory blocks in our design, synthesis tool generated it using flipflop along with required combinational circuitry. With in-built hard IPs, use area, power, and speed performance of the design can be enhanced. Latency of resource-efficient TCAM implementation is four clock cycles, and throughput is one clock cycle per word.

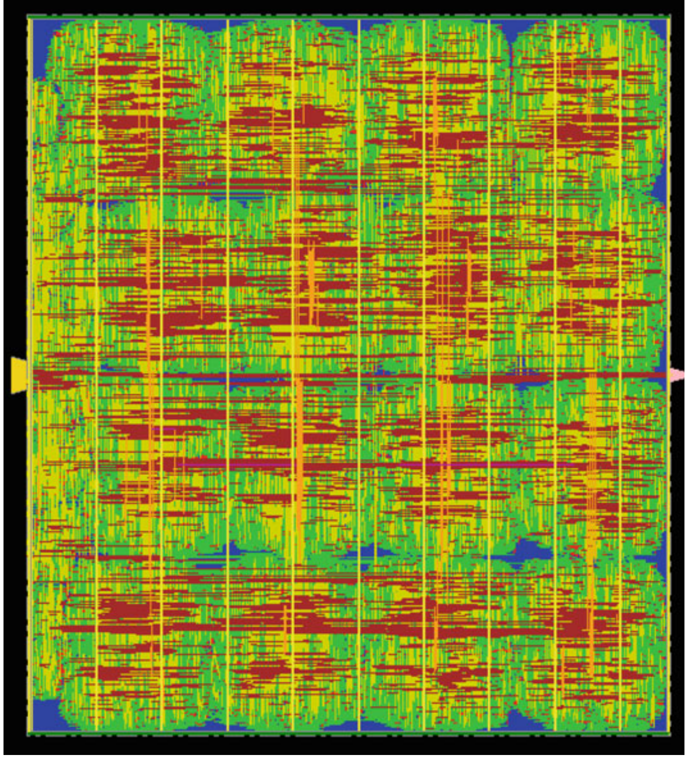

Fig. 7 Layout of 64 × 32 resource-efficient TCAM

Table 2 ASIC implementation results of resource-efficient TCAM of size 64 × 32

Implementation	Area (μm^2)	Speed (MHz)	Power (W)
Z-TCAM	18,707,925	223.00	0.376
Efficient TCAM	1,000,000	493.82	0.112

6 Conclusion

This paper has implemented a novel TCAM architecture using SRAM cells. On the Xilinx FPGA, we have implemented a 64 × 32 efficient TCAM example design. Additionally, we created a 64 by 32 efficient TCAM for 45-nm technology using the GPDK library, demonstrating the feasibility of our ASIC design. Both FPGA- and ASIC-based designs achieved performance increases in speed and reduce resource and power consumption. This implemented TCAM is simple in structure, easily scalable and designed to have deterministic throughput.

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Implementation of Vending Machine to Offer and Recycle Products

Apurba Mondal, Gauri Kumari, and Kavicharan Mummaneni

1 Introduction

A vending machine is an electronic machine that dispenses products such as cold drinks, books, newspapers, journals, magazines and chocolates to customers/users after cash, a credit card, or another kind of payment is entered into the machine or otherwise done [1]. The first modern vending machine was designed in England in the early 1880s and offered postcards. There are vending machines in many nations, and more recently, specialist vending machines have been developed that deliver less typical stuff than conventional vending machine. Previously, vending machines were used to collect old/used products also. This type of vending machine is called reverse vending machine. Numerous studies have been done in order to design vending machines. Vending machines are used near ATM, railway stations, shopping mall, movie theatre, etc. It is easily operated by the user/customer, and it is movable [2]. Microcontroller-based automatic paper vending machine has been designed. It accepts coins as an input and dispenses sheets as an output [3]. Vending machine using radio frequency identification has been designed [4, 5]. Vending machine has been designed to recycle bottle. Microcontroller-based vending machines are comparatively slower [6]. In [7], FSM-based vending machine has been implemented, and power consumption is reduced. Reverse vending machine based on fraud detection sensors has been designed that accepts only plastic waste as input and provides reward as coin in output [8]. Design of vending machine using Automata theory, and Visual

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Automata simulator is done [9]. Implementation of high-tech vending machine using fingerprint sensor has been done [10]. We have seen vending machine that offers products or reverse vending machine that recycles the old/used products. In this paper, we will be implementing a vending machine that covers both the features of vending machine and reverse vending machine. So, it will offer multiple products and recycle old/used products. Consumption of power will be less so that it can run in low power.

2 Implementation

(i) The user needs to select whether want to deposit newspaper, journal, and magazine or not.
(ii) The user selects the product to be purchased.
(iii) If the coin inserted matches the product selection, then the selected product will be served.

This vending machine offers three products (i) Newspaper (ii) Journal (iii) Magazine. The price list of products with and without discount is shown in Table 1. The inputs and outputs of proposed vending machine is shown in Table 2 and Table 3. If the customer/user submits old newspaper or journal or magazine, then discount will be given to the customer/user in that purchase. Coins of Rs. 5, Rs. 10 are accepted. Four states have been used, namely S0, S5, S10 and S15. S0 is the starting state followed by S5, S10 and S15. If the customer/user selects newspaper and does not have any newspaper or journal or magazine to recycle and enters coin Rs. 5, then newspaper will be served. If the customer/user selects journal and does not have any newspaper or journal or magazine to recycle and enters coin Rs. 10, then journal will be served. If the customer/user selects magazine and does not have any newspaper or journal or magazine to recycle and enters coin Rs. 10 and Rs. 5 or Rs. 5 and Rs. 10 or Rs. 5 and Rs. 5 and Rs. 5 (it has to be sum of Rs. 15), then magazine will be served. If the customer/user selects newspaper and has newspaper or journal or magazine to recycle, then newspaper will be served for free (does not need to enter coin). If the customer/user selects journal and has newspaper or journal or magazine to recycle and enters coin Rs. 5, then journal will be served. If the customer/user selects magazine and has newspaper or journal or magazine to recycle and enters coin Rs. 10, then magazine will be served. Block diagram of vending machine is shown in Fig. 1. State diagrams of vending machine are shown in Figs. 2, 3, 4, 5, 6 and 7.

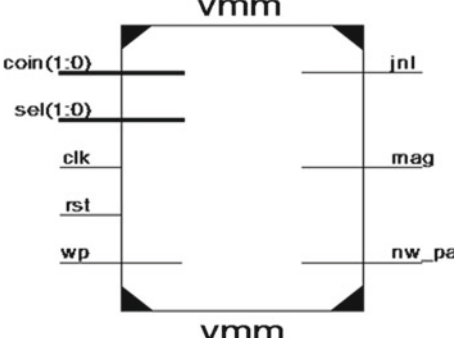

Fig. 1 Block diagram

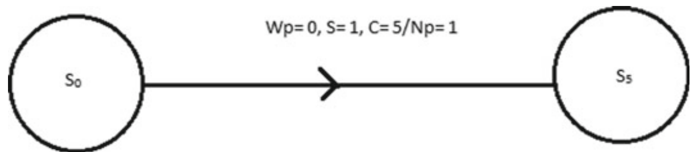

Fig. 2 FSM for newspaper without recycle product

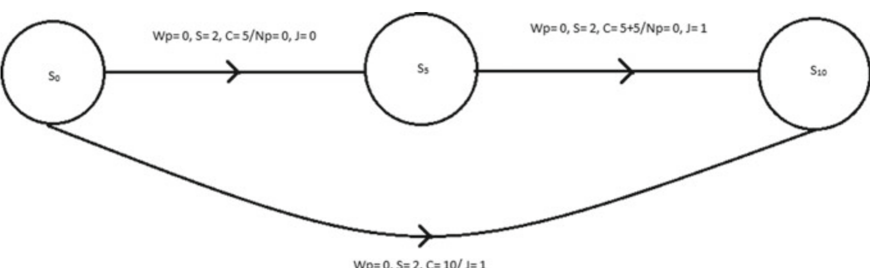

Fig. 3 FSM for journal without recycle product

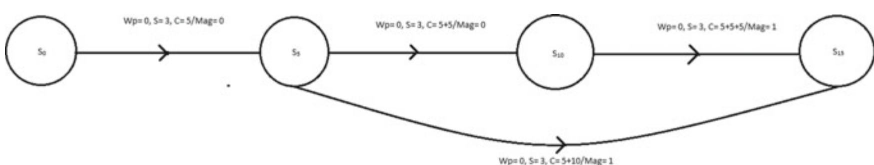

Fig. 4 FSM for magazine without recycle product

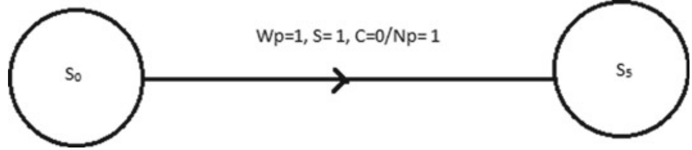

Fig. 5 FSM for newspaper with recycle product

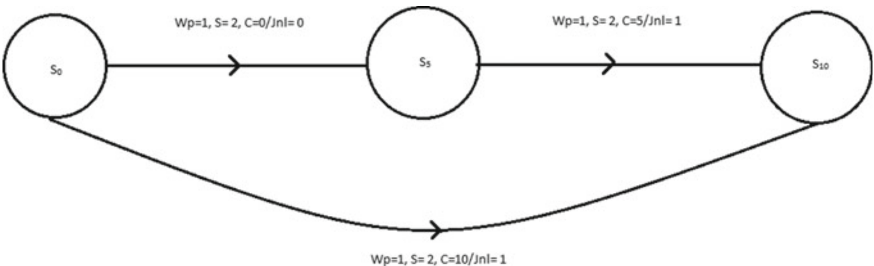

Fig. 6 FSM for journal with recycle product

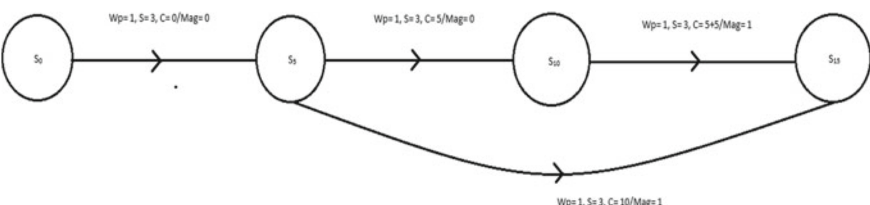

Fig. 7 FSM for magazine with recycle product

Table 1 Price list of products

Products	Price list without discount (Rs)	Price list with discount (Rs)
Newspaper	5	Free
Journal	10	5
Magazine	15	10

Table 2 Inputs

S. No.	Input notations	Description
1	Coin	Coin
2	Clk	Clock
3	Sel	Select
4	Wp	Notation to select whether has any product to deposit
5	Rst	Reset

Table 3 Outputs

S. No.	Output notations	Description
1	Nw_pa	Newspaper
2	Jnl	Journal
3	Mag	Magazine

3 Results

Synthesizable codes were compiled in order to design the intended vending machine system. It is simulated on Xilinx ISE 14.7. The RTL schematic of proposed vending machine is shown in Fig. 8. The simulation result and respective output waveforms are shown in Fig. 9 for the different inputs like select, coin, reset and Wp (notation to select whether has any recycle product). From simulation results, we can see when Wp (notation to select whether has any recycle product) is selected (by '1'), then the user gets a discount on products. But when Wp (notation to select whether has any recycle product) is not selected (by '0'), then the user does not get a discount. Thus, the intended operation has been performed. From Table 4: Power Analysis, we can conclude, out of all these FPGA Boards, Spartan 6 lower power consumes less power, whereas Virtex 5 consumes maximum power. Thus, the manufacturer should consider this point while designing the product to make it power efficient. We have compared our results with the previous one [7] that consumes 81 mW, the proposed design consumes less power, i.e. 34 mW using Spartan 3E family.

Table 4 Power analysis using different FPGA boards

S. No.	FPGA boards	Power (mW)
1	Spartan 6 lower power	11
2	Spartan 6	14
3	Spartan 3E	34
4	Kintex 7	80
5	Artix 7	82
6	Virtex 5	321
7	Virtex 7	177

Fig. 8 RTL schematic of proposed vending machine

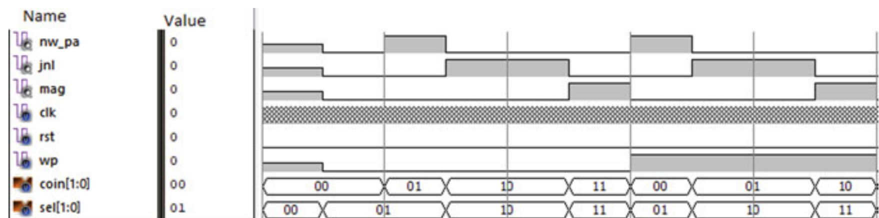

Fig. 9 Simulated waveforms

4 Conclusion

In this paper, we have presented a FSM-based vending machine that dispenses products and accepts old or waste product to recycle. The proposed vending machine consumes less power. It accepts two coins, i.e. Rs. 5 and Rs. 10, and offers three products. It also offers discounts if the customer wishes to deposit any old or waste products. Its algorithm is very flexible and reliable as the vendor can easily enhance the algorithm for large number of products. It reduces human efforts. It is designed in Xilinx ISE 14.7.

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Using the Cell-Based Design, Employ a Contrivance Analysis on a Quadrature Phase Shift Keying Modulator

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1 Introduction

Compared to digital systems, analogue communication has more downsides. This decade has seen an upsurge in demand the demand for digital techniques and devices due to several number of problems with security, accuracy, reliability, speed, etc. Transmission of the information to sites remote from the source requires an additional rapid, secure medium. The design and analysis of digital systems are the crucial factors that require agonizing. The primary developed feature of advanced data communication systems is the distribution of all data through a single channel or gear mechanism. Shift keying, time and frequency division multiple access, and other advanced digital modulation techniques can be employed to boost the rate of transmission [1].

Compared to lower modulation techniques, greater modulation approaches will result in a doubling of the band dimensions. The QPSK has a bandwidth that is twice as large as BINARY-PSK's [2]. PAM, PWM, PCM, ASK, PSK, FSK, and many other different digital modulation algorithms are just a few examples. In this paper, the quadrature phase shift key modulator section shift keying theme has been constructed and performance evaluated. In contrast to other modulators [3], this one uses a Booth's multiplier [1], a multiplier, to produce the correct output of modulation.

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Lecture Notes in Electrical Engineering 1067,
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IP core design is a specific technology that processes the entire design in a semi-custom manner. Intellectual property is known as IP. It is a cell-based system with a semi-custom design in which each planning module is reincarnated into a cell and then integrated using a block integrator [3, 4].

1.1 QPSK

Depending on the modulating signal, the carrier phase changes. Two bits of data are transmitted across a single channel in QPSK [4]. Compared to the earlier BINARY-PSK method, it has larger bandwidth, allowing for the transmission of more data via channel. Two bits that are modulated at one are transmitted by the modulator. It can go through four distinct phases which would include, 0, π/2, π, 3π/2, etc. Using the same bandwidth, it enables the signal to convey twice as much information as regular PSK [5] (Fig. 1).

The input is divided into even- and odd-bit data by the modulator's serial-in-parallel-out shift register, which also serves as a bit divider [6]. The event data is sent over the BINARY-PSK I channel, while the odd data is sent over the BINARY-PSK Q channel. The carrier signal is produced by the modulator's local oscillator, or LO, and delivered straight to the BINARY-PSK I channel together with the data that was phase-shifted by 90° angle. The output signal of the quadrature-PSK is then obtained by computing the data from the I and Q channels once the two signals reach adders. There will not be any shift in the phase of output carrier signal if the input is 00. If the output is 1, a 90-phase shift will take place. There will be a phase shift of 180° and 270°, correspondingly if the input is 10 and 11.

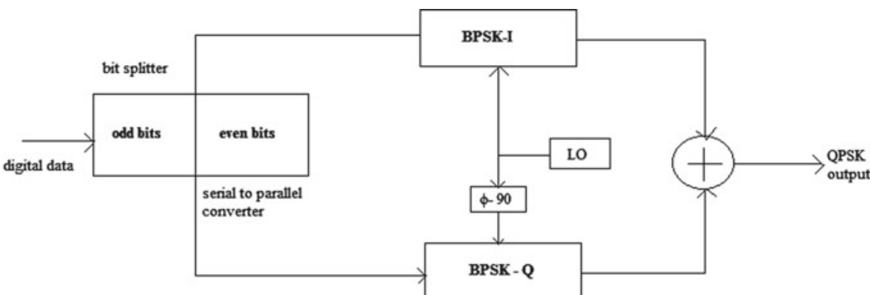

Fig. 1 Conventional QPSK modulator block

1.2 Booth Multiplier

A multiplication procedure that might multiply two signed binary values in two's complement notation is Booth's encryption or Booth's multiplication rule. Compared to the conventional multiplication rule, Booth's rule can do fewer additions and subtractions. A multiplication technique might be used with an encryption method to reduce the number of the partial product. It is mostly based on the equation $2 * n = (2n-1-2n)$ [7] (Table 1 and Fig. 2).

Booth's Algorithm for Multiplication

The technique's stages are carried out algorithmically:

- Look through the input for carrier information and 8-bit data.

Table 1 Booth's multiplication sequence [1]

$Q(n)$	$Q(n+1)$	Observed bits @ output	Action to be performed
0	0	0	Shift operation
0	1	+ve 1	M to be added
1	0	−ve 1	M to be subtracted
1	1	0	Shift operation

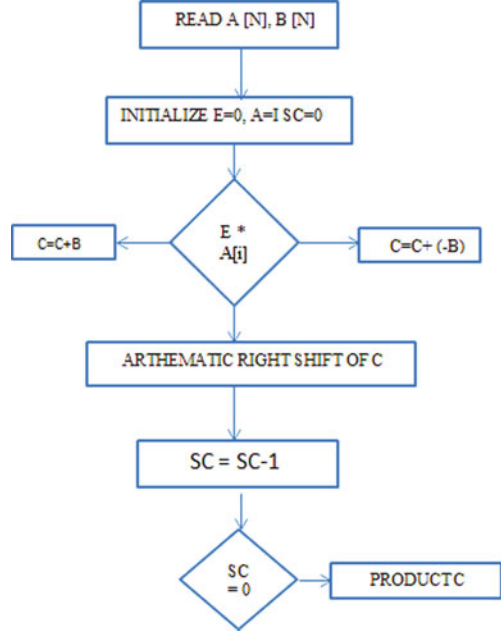

Fig. 2 Booth multiplication algorithm [1]

- Important to set the one-bit transition detector's initialization parameters to $E = 0$, $I = 0$, and $A =$ I. By initializing the sequence counter SC = 0, you can transmittance for carrier information for 1-bit and 8-bit information (multiplicator-$A(n)$).
- Combine E with A. If 10, extrapolate output C to get B. Add B to output C if 01.
- Else execute an arithmetical right shift operation on output 'C' and twice the value of $A[i]$ to E if 00 or 11 is the result.
- Decrement the sequence counter (SC) by unity, such that it becomes SC = SC−1.
- If the process is complete, the outcome will be stored in the C-register.

1.3 Cell-Based Design for Intellectual Property-Core [2]

The entire depiction has been put into implemented or simulated using a semi-customized pattern that can be referred to as a standard-cell-based design. This can be accomplished by combining the entire project or architecture into a single IP cell, also known as a standard-cell design, and referred to as the IP-core architecture. The procedures for transforming a hardware description language module into a standard-cell design of IP-core are listed below.

- Behavioral modelling (HDL) of the module.
- Creating an intellectual property (IP).
- Modifying the definition of intellectual property (IP)
- Including a module guide that details the intellectual property (IP) module features in the cell.
- Reviewing and packaging an intellectual property (IP) module.
- Validating the new IP location
- Adding of the repository path to add the IP in the catalogue of the IP.
- Making use of the new IP cell that is included in the intellectual property (IP) catalogue in a more complex design/architecture that is also a single-cell packaging.

The definition [8] indicates, write about how an IP module might be a reusable core information in building a block for an application-specific-IC or field programmable gate array for a product. The expanding commercial electronic trend of electronic style automation (EDA) toward the ongoing use of already built components includes IP core area units. The accompanying IP core should generally be highly adaptable. That is easily included in any merchandiser or styling approach. Universal asynchronous receiver/transmitters (UARTs), central process units (CPUs), LAN controllers, and peripheral component interconnect interfaces connect complete IP core samples [9]. There are three types of IP cores: soft, firm, and hard.

2 Architectural Overview

The architecture shown in Fig. 3 is a QPSK modulator with a multiplier and change_registry operating in serial-in-parallel-output mechanism. This multiplier was discussed in previous section. In serial in parallel mechanism, register data can be serially loaded and retrieved simultaneously.

The SIPO shift register's even-bit and odd-bit data to be received [10], and the modulator has two multipliers in this instance. A closer examination at the construction reveals that the digital input data is provided to the SIPO register, and the parallel output serves as both a message signal and one of the inputs to the Booth's multiplier. The carrier signal, which we provide separately, is the Booth's multiplier's second input. We will therefore aggregate the outputs of both multipliers using the output of an adder, whose output is the modulated output. The following is the QPSK modulator output.

2.1 *SIPO*

Serial-in-parallel-out shift registers [10]—abbreviated SIPO—are shift registers in which data is input serially and shifted out in parallel form. Once the data bits have been stored, they all appear on their individual output lines and are all available at once rather than serial output's bit-by-bit. If the last flip flop's Q net serves as the serial-in-parallel-out shift register's output, the shift register can also be utilized as a serial-in-serial-out shift register (Fig. 4).

Even data will go to one multiplier as an input, and odd data will go to one multiplier after the SIPO splits the output into even and odd parallel data. The second input to the multiplier is carrier data. Both will be processed, and the results will be given

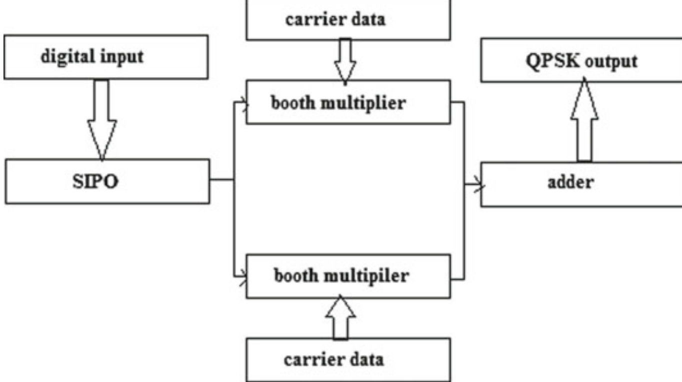

Fig. 3 Architecture of QPSK modulator [1]

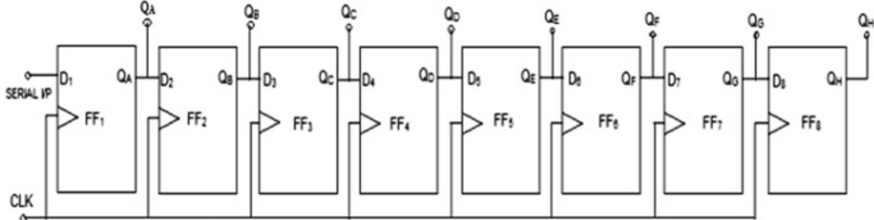

Fig. 4 8-bit serial-in-parallel-out shift register

to the adder. The adder will then combine the output data from the two multipliers to provide quadrature-PSK. It is a ripple carry adder that is being employed here [11].

3 Inference and Responses

The area analysis of the prior [1] and new QPSK modulator designs is shown in the graph above. The prior QPSK modulator requires 62 flip flips, while the new one only needs 58 (Figs. 5, 6, 7 and 8).

The number of LUTs (look-up tables) needed for the proposed QPSK modulator design is 97 as opposed to 114 for the prior [1] design, which suggests there will be refinement in the low area utilization (Fig. 9).

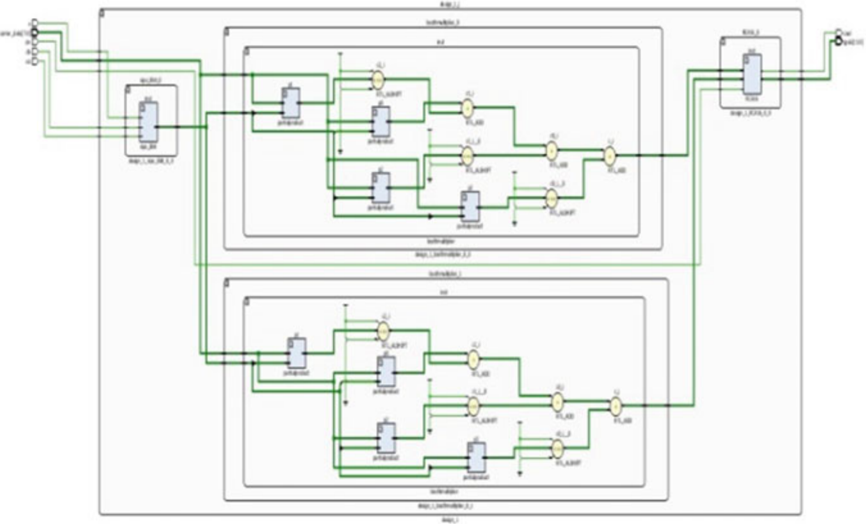

Fig. 5 RTL schematic of QPSK module

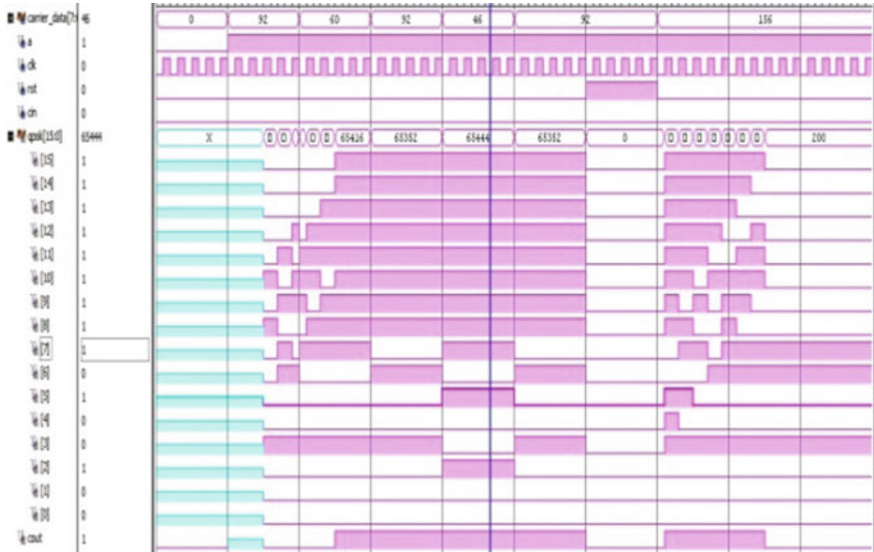

Fig. 6 Simulation waveforms of QPSK modulator

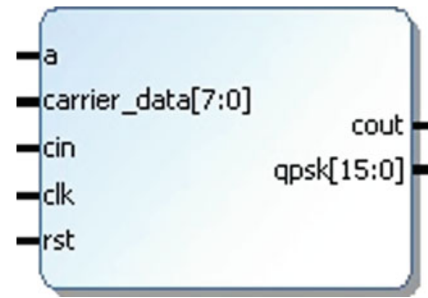

Fig. 7 IP core module design of QPSK modulator

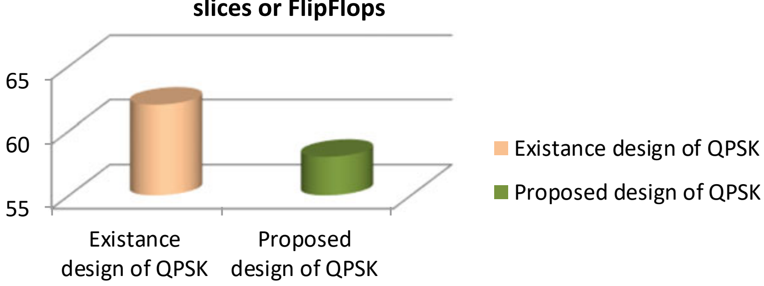

Fig. 8 Comparative inference (flip flops) of QPSK modulator in terms of area

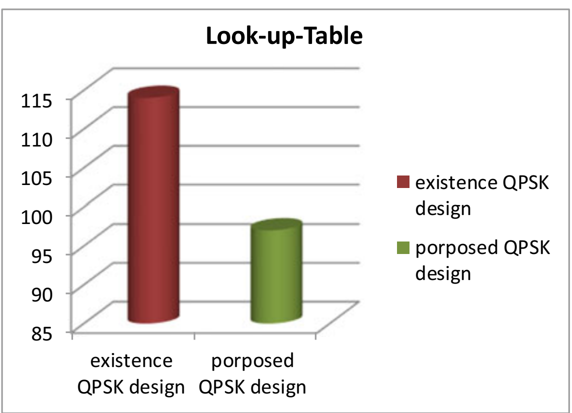

Fig. 9 Comparative inference (look-up tables) of QPSK modulator in terms of area

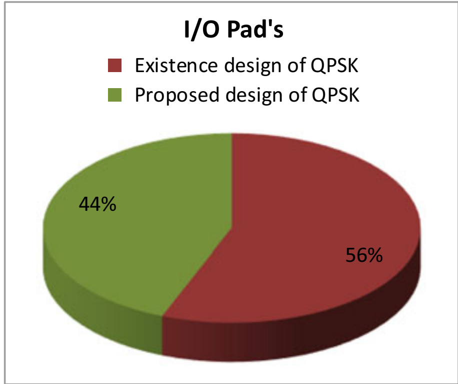

Fig. 10 Pie chart for comparative inference of I/O Pads for QPSK module

The number of input and output blocks needed for the existence [1] and proposed designs of quadrature-PSK modulators are shown in the pie diagram above. The earlier design [1] required 12% more area for I/O blocks, or 56%, against 44% for the new design. This suggests that, in terms of cell sizing, the new approach might be superior to the old one (Fig. 10).

Here, power, a new parameter, must be considered. The comparison between the old and new QPSK modulator designs revealed that the space occupation had decreased, and therefore, it was assumed that this was the case in this instance.

4 Conclusion

A feasible IP core standard-cell architecture of a Quadrature-PSK modulator can be created from this modulator design by using various packaged IP cells that are needed in an intellectual property (IP) integrator; the efficiency parameters will then

be compared to those of earlier iterations in order to produce a better outcome than the earlier one. The communication system is created for a variety of wireless applications; by utilizing this QPSK module architecture, the time required to create and re-enact the code without error can be reduced.

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12-Bit SAR ADC Design in SCL 180 nm for Sensor Interface Applications

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1 Introduction

The modern circuits we see all over the world are digital using which we can measure all the natural signals using sensors. As the responses from these sensors are analog signals (like temperature, speed, weight, etc.), to interpret and operate on them, an ADC is required [1–5]. ADCs could come in various types depending on applications and requirements. High resolution and high sampling speed are difficult to achieve simultaneously and hence needs trade-off in designing. Three types of ADCs are widely used, which are delta-sigma, pipeline, and SAR type ADCs [6]. Here, delta-sigma ADC is used for high resolution and low speed operation, and inversely pipeline ADC is used for low resolution and high speed operation. Amidst lies the SAR ADC which can achieve moderate speed of 10 K to 1 M samples per second and resolution up to 8–16 bits.

From circuits point of view, a delta-sigma ADC contain simple analog circuits such as difference amplifier, comparator, and integrator, but it also contains a complex digital filter requiring large area of implementation. Pipeline ADC has low complexity, but the size is largest. Hence, SAR ADC also provides area advantage over others and makes this more suitable for tiny sensors. The SAR ADC consists of primarily sample and hold circuits, comparator, DAC in feedback loop, and SAR logic circuits.

The presented work contains an assortment of all the sub-circuits in a SAR ADC to achieve high speed of operation and high resolution. To achieve high sampling rate, bootstrapped switch is used in sample and hold circuit. In DAC, differential charge scaling architecture is used to reduce the area compared to weighted resistors

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or capacitors circuits. This ADC also removes even order harmonics and provides common mode rejection [7] which improves SNR. All the sub-circuits designed and integrated using Cadence Virtuoso circuit simulator on SCL 180 nm technology. The ADC circuit thus created can achieve high speed of 1.1 MS/s with resolution of 12 bits.

2 Design of Blocks and Integration

This section discusses the ADC operation, design, and integration of all the circuits in detail.

2.1 ADC Operation

A 12-bit SAR ADC requires minimum 12 clock cycles to convert analog input to digital output. It contains a feedback loop as shown in Fig. 1. During the each clock cycle, a single bit value will be decided in order of MSB to LSB. In first clock cycle, SAR logic sets MSB of DAC to 1, and other bits are 0. This input combination of DAC gives its output as $V_{\mathrm{DAC}} = V_{\mathrm{ref}}/2$. If sample version of input voltage V_{IN} is greater than V_{DAC}, then comparator gives logic 1 as output, and SAR logic keeps MSB as 1 from next clock cycle during the conversion period, but when V_{IN} is smaller than V_{DAC}, SAR logic sets MSB as 0 from next clock cycle. For second clock cycle, SAR logic sets 2nd MSB as 1 with retaining previous result. Again, we compare V_{IN} and V_{DAC} and repeat the same procedure until we reach to LSB. An algorithm for 12-bit SAR ADC is given below in Table 1. At the end of conversion, DAC output V_{DAC} is approximated to V_{IN}. It means that, at the end the magnitude difference between V_{IN} and V_{DAC} should be less than 1 LSB. The convergence of V_{DAC} towards V_{IN} is shown in Table 1.

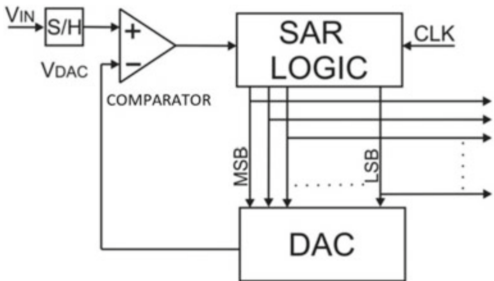

Fig. 1 SAR-ADC architecture

Table 1 V_{DAC} Output for each clock cycle and corresponding bit value

Clock cycle	D11	D10	D9	…	D2	D1	D0	V_{DAC} output	Bit decision
1st	1	0		…	0	0	0	$\frac{V_{ref}}{2}$	B11 = $\begin{cases} 1, \text{ if } V_{IN} > V_{DAC} \\ 0, \text{ if } V_{IN} < V_{DAC} \end{cases}$
2nd	B11	1	0	…	0	0	0	B11 $\frac{V_{ref}}{2} + \frac{V_{ref}}{4}$	B10 = $\begin{cases} 1, \text{ if } V_{IN} > V_{DAC} \\ 0, \text{ if } V_{IN} < V_{DAC} \end{cases}$
3rd	B11	B10	1	…	0	0	0	B11 $\frac{V_{ref}}{2}$ + B10 $\frac{V_{ref}}{4}$ + $\frac{V_{ref}}{8}$	B9 = $\begin{cases} 1, \text{ if } V_{IN} > V_{DAC} \\ 0, \text{ if } V_{IN} < V_{DAC} \end{cases}$
4th	B11	B10	B9	…	0	0	0	B11 $\frac{V_{ref}}{2}$ + B10 $\frac{V_{ref}}{4}$ + B9 $\frac{V_{ref}}{8} + \frac{V_{ref}}{16}$	B8 = $\begin{cases} 1, \text{ if } V_{IN} > V_{DAC} \\ 0, \text{ if } V_{IN} < V_{DAC} \end{cases}$
…	…	…	…	…	…	…	…	…	…
11th	B11	B10	B9	…	B2	1	0	B11 $\frac{V_{ref}}{2}$ + B10 $\frac{V_{ref}}{4}$ + B9 $\frac{V_{ref}}{8}$ + B8 $\frac{V_{ref}}{16}$ + B7 $\frac{V_{ref}}{32}$ + B6 $\frac{V_{ref}}{64}$ + B5 $\frac{V_{ref}}{128}$ + B4 $\frac{V_{ref}}{256}$ + B3 $\frac{V_{ref}}{512}$ + B2 $\frac{V_{ref}}{1024}$ + $\frac{V_{ref}}{2048}$	B1 = $\begin{cases} 1, if\, V_{IN} > V_{DAC} \\ 0, if\, V_{IN} < V_{DAC} \end{cases}$

(continued)

2.2 *Digital-To-Analog Converter (DAC)*

In SAR ADC, a feedback DAC is required [8] whose output is approximated to analog input signal V_{IN} through an iterative process. The conventional DACs are made of resistors, e.g. R-2R ladder and weighted resistor types, use of which requires larger area in an IC, while also consuming more static power. Generally, in ICs, DAC used in SAR ADC is made of capacitor rather than resistor, which consume power only

Table 1 (continued)

Clock cycle	D11	D10	D9	…	D2	D1	D0	V_{DAC} output	Bit decision
12th	B11	B10	B9	…	B2	B1	1	B11 $\frac{V_{ref}}{2}$ + B10 $\frac{V_{ref}}{4}$ + B9 $\frac{V_{ref}}{8}$ + B8 $\frac{V_{ref}}{16}$ + B7 $\frac{V_{ref}}{32}$ + B6 $\frac{V_{ref}}{64}$ + $B5\frac{V_{ref}}{128}$ + B4 $\frac{V_{ref}}{256}$ + B3 $\frac{V_{ref}}{512}$ + B2 $\frac{V_{ref}}{1024}$ + B1 $\frac{V_{ref}}{2048}$ + $\frac{V_{ref}}{4096}$	B0 = $\begin{cases} 1, if\, V_{IN} > V_{DAC} \\ 0, if\, V_{IN} < V_{DAC} \end{cases}$

Table 2 Comparison of results

Specifications	[2]	[3]	This work
Technology	180 nm	180 nm	180 nm
Resolution (bits)	10	12	12
Power supply (V)	0.6	1.8	1.8
Sampling frequency (M samples/s)	0.2	0.2	1.1
Maximum DNL/INL	0.29/ − 0.8	NA	0.8/0.3
SNDR (dB)	69.55	71.55	73.54
ENOB (bits)	9.3	11.59	11.92
Power (μW)	2	336	188
FOM (fJ/conversion step)	15.51	…	44

during charging. There are many examples of capacitive DAC such as C-2C DAC and charge scaling DAC. Some of capacitive DACs also allow to sample on it, and it does not require extra sample and hold circuit. Further, different switching schemes are used, for example, conventional switching and monotonic switching.

An advantage of C-2C DACs is that it has only two types of capacitor, but due to parasitic effect, these C-2C DACs are generally limited to 9-bit applications. For higher bit applications, charge scaling DACs are used with common centroid technique. The major disadvantage of this DAC is that the capacitance ratio increases exponentially with each bit which decreases sampling frequency exponentially. To

increase sampling rate and number of bits simultaneously, one of the solutions is split array DACs. An example of 12-bit split array DAC is shown below. The value of split capacitor C_s is given by following formula.

$$C_s = \frac{\text{sum of LSB array}}{sum \text{ of MSB array}} C \tag{1}$$

Ideally output of split array DAC is same as charge scaling DAC for the value of split capacitor C_s. Output equation of this DAC is given as following equation.

$$V_{\text{OUT}} = -V_{\text{IN}} + B(N-1)\frac{V_{\text{ref}}}{2} + B(N-2)\frac{V_{\text{ref}}}{4} + \cdots + B0\frac{V_{\text{ref}}}{2^{N-1}} \tag{2}$$

The Eq. (2) on convergence gives the output as in equation below.

$$V_{\text{OUT}} = -V_{\text{IN}} + V_{\text{DAC}} \tag{2}$$

Other than the above-discussed DACs, which are single input and single output, differential DACs have dual input and output terminals [9]. This architecture has three major advantages, which are (a) input voltage range will double with increase in core power supply, (b) nullification of even order harmonics, and (c) common mode rejection. The 12-bit differential charge scaling DAC is shown in Fig. 2. The value of differential output, V_{OUT}, is given in equation below.

$$\begin{aligned} V_{\text{OUT_}p} - V_{\text{OUT}_n} &= \left(V_{\text{IN}_P} - V_{\text{IN}_N}\right) - \text{VDD} \\ &\quad + 2\left\{B(N-1)\frac{V_{\text{ref}}}{2} + B(N-2)\frac{V_{\text{ref}}}{4} \ldots + B0\frac{V_{\text{ref}}}{2^{N-1}}\right\} \end{aligned} \tag{3}$$

From above equation of differential DAC, it can be concluded that power supply is behaving like single DAC whose supply is in range of VDD and (−VDD).

2.3 Comparator

Comparators give binary (digital) output depending on the difference of two analog inputs (Fig. 3a). When voltage at non-inverting terminal V_p is greater than the voltage at inverting terminal V_n, then output of comparator should be high (V_{OH}), but if V_p is smaller than V_n, output of comparator should be low (V_{OL}) for ideal comparator (Fig. 3b). In case of non-ideal ADC, the difference $V_p - V_n$ is in between V_{OH} and V_{OL} making it non-binary state and an undesired value (Fig. 3c). The discrete time comparators used in SAR ADC can mainly be divided into three major parts, namely preamplifier, regenerative latch, and SR flip-flop as shown in Fig. 3d.

The pre-amplifier block contains a fully differential amplifier in cascade with another differential amplifier, which is controlled by a clock signal (CLK) as shown

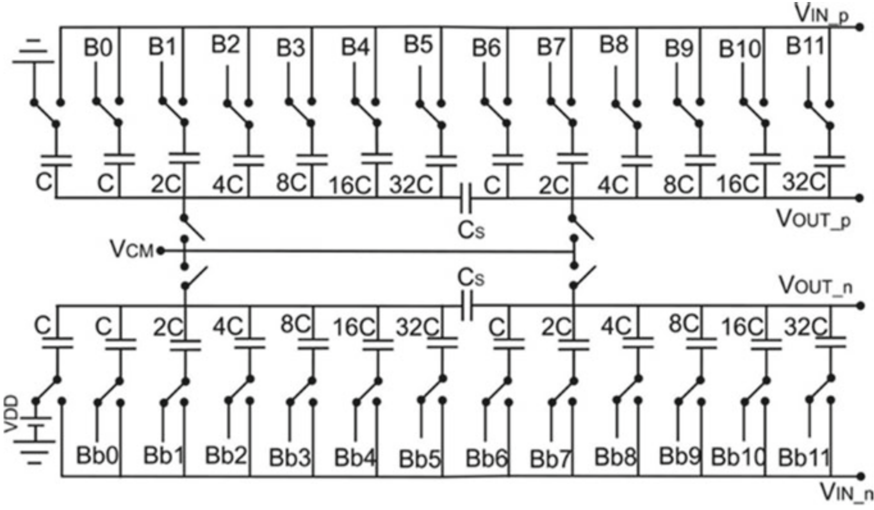

Fig. 2 12-bit differential charge scaling DAC

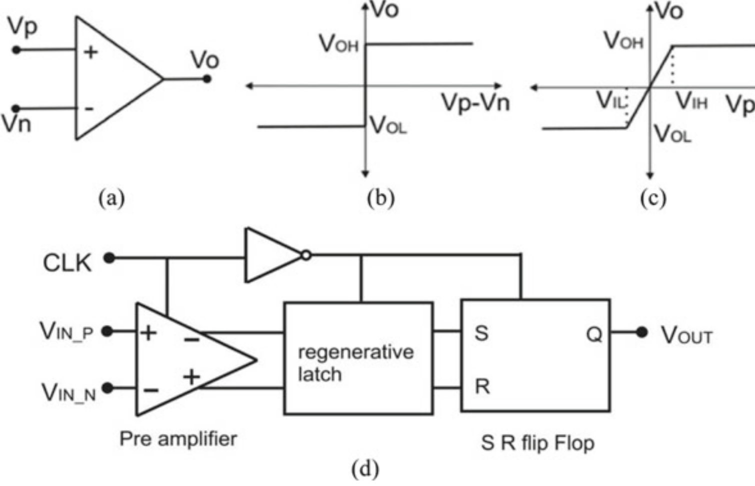

Fig. 3 **a** Comparator, **b** ideal comparator output, **c** non-ideal comparator output, **d** components of a comparator

in Fig. 4. The size of PMOS M3 and M4 are same and that of NMOS M1 and M2 are same as well to maintain similar sensitivity from high to low and low to high. While gain bandwidth product mainly depends on size of M1 or M2, maximum input common mode rejection ratio (ICMRR) depends on size of M3 or M4, and minimum ICMRR depends on size of M5. The small signal differential gain is given by g_{M1}/g_{M3}.

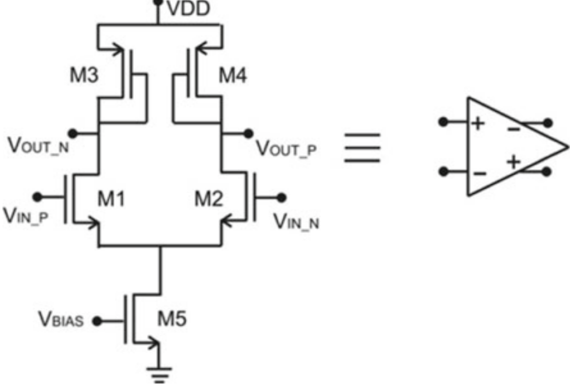

Fig. 4 Pre-amplifier block

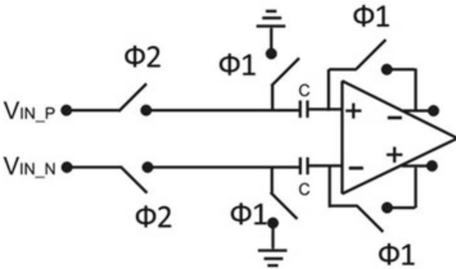

Fig. 5 Auto-zeroing technique for comparators

In the discrete comparator, pre-amplifier block is active only at high clock. This is followed by a regenerative latch which holds the comparison result and further connected to SR flip-flop to hold the result. On low clock, the latch and flip-flop resets their value, which results in no power consumption and discharges all the parasitic capacitances, commonly termed as auto-zeroing [9] technique as shown in Fig. 5. The inverted clock, which is connected to SR flip-flop, gives logic output at positive edge of clock signal.

2.4 Switch

Among basic MOS switches, NMOS as switch can be used for lower analog voltage, and in digital, it can be used to transmit strong zero (logic 0) and weak one (logic 1). Similarly, PMOS switch can be used for higher analog voltage, and in digital, it can be used for strong one (logic 1) and weak zero (logic 0). Even being very small in size, it has huge disadvantage that it cannot allow rail to rail analog signal, and its ON state resistance is dependent on input voltage. The ON state resistance, R_{ON}, for NMOS is given as:

$$R_{\mathrm{ON}n} = \frac{1}{\mu_n C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{Tn}})} \tag{4}$$

And, the ON state resistance, R_{ON}, for PMOS is given as:

$$R_{\mathrm{ON}p} = \frac{1}{\mu_p C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{sg}} - |V_{\mathrm{Tn}}|)} \tag{5}$$

A transmission gate, however, is a parallel combination of both NMOS and PMOS, resulting in direct rail to rail contact in between input to load providing strong one (logic 1) and strong zero (logic 0). Its main disadvantage is that their ON state resistance also depends on input voltage resulting in higher order harmonics terms in transmitted signals. A switch with constant ON state resistance is needed to suppress higher order harmonics terms, which are also known as bootstrapped switch [10].

During the OFF phase in Fig. 6a, capacitor C_B is charged to VDD through the power supply, and gate of NMOS is connected to ground. At the ON phase in Fig. 6b, capacitor is now connected to gate and drain terminal of NMOS while disconnected from previous terminals. This combination keeps the gate overdrive voltage constant, and hence, the ON state resistance of NMOS is constant. It is observable that for implementing this switch the secondary switches are used which can be implemented by NMOS. The ON resistance of bootstrapped switch is given by Eq. (4).NMOS does not turn OFF instantaneously, and then, gate voltage is turned OFF, resulting in charge leakage and short-circuits input with ground. To avoid this, the switch is needed to be disconnected at input terminal when gate is grounded. This can be achieved using a two-phase clock circuit as used in Fig. 6c.

2.5 SAR Logic

The SAR logic block is intended to store, propagate, and output the digital signal. This block mainly contains (a) 14-bit ring counter, (b) array of 12-bit D flip-flop, (c) array of alternatively placed 12-bit NOR and OR gates, and (d) 12-bit parallel-in-parallel-out (PIPO) register [2, 3]. The $N + 2$ (12 + 2)-bit ring counter for N bit SAR ADC and the remaining two bits are required for sampling and holding purpose. In sampling stage, input is sampled by DAC, and at hold stage, the DAC is disconnected from both analog and digital switches. Post the hold stage, all the array in SAR logic is cleared, and then, the conversion phase starts where the capacitors in DAC are connected with digital switches as input terminals. All the 12 LSB outputs of ring counter are connected simultaneously to the respective inputs of array of D flip-flop and at one input of array of OR gates. The other input terminals of array of OR gates are connected with the output of D flip-flop. On the same time, input array of D flip-flop is also connected through output of comparator, where main purpose of D flip-flop is to hold previous comparison result. The output of NOR array is connected to the inverted input of differential DAC. The outputs from OR gates are

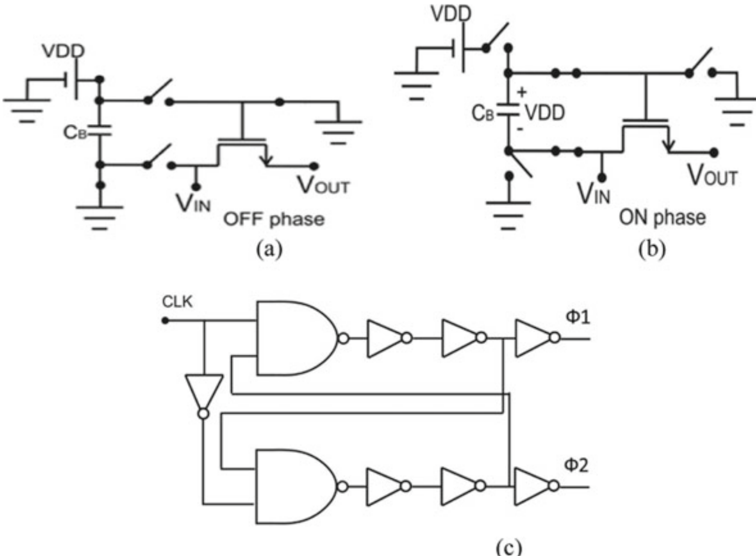

Fig. 6 Bootstrapped switch **a** OFF phase, **b** ON phase **c** Two-phase clock circuit generator

connected with the input terminals of PIPO register which at the end of conversion cycle provides digital output towards external interface.

3 Calculations

3.1 Quantization Noise

In quantization mapping of amplitude of discrete time signal to finite number of level $L = 2^n$ is done. The quantization power P_Q for uniformly distributed quantization noise is given by

$$P_Q = \frac{1}{12}\left(\frac{V_{\text{REF+}} - V_{\text{REF}-}}{2^n}\right)^2 \tag{6}$$

3.2 Signal to Noise Ratio (SNR)

Ideally the SNR for ADC is given by

$$\mathrm{SNR} = 10 \log \frac{P_{\mathrm{signal}}}{P_Q} \, dB \tag{7}$$

When input has maximum possible amplitude of sinusoidal signal, then SNR is independent of $V_{\mathrm{REF}+}$ and $V_{\mathrm{REF}-}$, and it is given as the following equation.

$$\mathrm{SNR} = 1.763 + 6.02n \, \mathrm{dB} \tag{8}$$

3.3 Signal-to-Noise-and-Distortion Ratio (SDNR)

SNDR is defined as the logarithmic ratio between input signal to sum of noise signal and harmonic distortion.

$$\mathrm{SNDR} = 10 \log \frac{P_{\mathrm{signal}}}{P_{\mathrm{noise}} + P_{\mathrm{harmonic\,distortion}}} \tag{9}$$

3.4 Effective Number of Bits (ENOB)

This measures the performance of real ADC compared to the ideal ADC. ENOB is measured in terms of SDNR in place of SNR because ideal ADC has only quantisation noise, and it is given by the following equation.

$$\mathrm{ENOB} = \frac{\mathrm{SDNR} - 1.763}{6.02} \tag{10}$$

3.5 Figure of Merit (FOM)

FOM is used for energy efficiency measurement of an ADC and is given as

$$\mathrm{FOM} = \frac{P_{\mathrm{total}}}{f_s 2^{\mathrm{ENOB}}} \tag{11}$$

where f_s is sampling frequency, and P_{total} is power consumed by circuit which on physical simulation equals 188 μW.

4 Results and Discussion

The maximum sampling frequency which indicates speed of operation in terms of bits, without affecting the performance of SAR ADC, calculated as 1.1MS/s for 12 bits, which is around 5.5 times higher than [2, 3]. Higher sampling rate is achieved due to split capacitor C_s which reduces effective capacitance seen by input source. The maximum DNL and INL are 0.8 LSB and 0.3 LSB, respectively, which are less than 1. As magnitude of DNL is less than 1, it can be concluded that there are not any intermediate missing digital counts and compares fairly to [2]. SDNR is calculated to be 73.54 dB. Using the values of SDNR, ENOB is calculated as 11.92. The average power consumption is 188 μW which is around half of [3] but very high than [2] which focuses more on energy efficiency. Similarly, the FOM calculated to be higher than [2] as 44 fJ for each average conversion step.

5 Conclusion

The presented 12-bit SAR ADC is designed and simulated using Cadence Virtuoso circuit simulator and SCL 180 nm PDK. The designed ADC exhibited better sampling frequency due to bootstrapped switching in sample and hold circuit and auto-zeroing technique in comparator for fast comparison. Also, the differential charge scaling DAC used in this design reduces the harmonic distortion, and the low capacitors size reduces the size of entire circuit.

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Fabrication of Blue Laser-Induced Graphene Electrodes and Evaluation of Their Electroanalytical Performance

Raghavv Raghavender Suresh, Sampratikshya Das, Amlan Ashish, and Gorachand Dutta

1 Introduction

Biosensors are employed for numerous purposes like disease diagnosis and monitoring [8] and plenary of other arenas. Of the many transduction principles, the electrochemical methodology enjoys immense advantages such as conferring ultra-sensitivity for detection, which are mass producible, portable, being subjectable to rapid miniaturization and easily integrable with electronics [12]. On a lab scale, researchers employ conventional electrodes to demonstrate the proof-of-concept applications. However, the conventional electrodes pose problems in terms of portability which poses problems for their real-time sensing applications. Furthermore, the rigorous cleaning procedures such as mechanical polishing, chemical and electrochemical activation activities render the time consuming and tedious [6, 14]. Also, the requirement of high volumes of analyte shall also render them resource consuming. Thus, utilization of printed electrodes, which do not demand such rigorous cleaning procedures and also consume very less sample volume, is extremely desirable for POC experiments. In this regard, screen-printed and laser-printed electrodes are being used in the present day to address these problems. Furthermore, the results thus obtained are more reliably convertible/employable outside the lab. While screen printing offers advantages of rapid-mass production, the resultant electrodes do demand some kind of pre-treatment before their utilization. This may be attributed to the presence of polymeric binder content in their inks, which albeit impedes the electrochemical activity is necessary to render printable characteristics [21]. On the other

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hand, the recent laser-based manufacturing strategy [17] that employs a computer-controllable laser head tool for electrode fabrication is devoid of such binder/additives and hence are readily usable. Furthermore, the 3D porous architecture, active edge sites, containing higher density of electronic states and electrochemical activity, these electrodes are more advantageous for electroanalytical applications [4].

Albeit many works based on CO_2 lasers have been reported, the CO_2 lasers posses certain limitations such as poor spatial resolution and overheating of substrates. On the other hand, the blue laser diodes have improved spatial resolution and avoid overheating of substrates. Considering the pre-mentioned advantages of blue laser diodes, electrodes, in this work, we have fabricated blue laser-induced graphene (LIG) electrodes at an optimum power/lasing speed and have performed a preliminary investigation into their material characteristics (mainly structural). Apart from this, electroanalytical performance was evaluated using inner-sphere redox couple $[Fe(CN)_6]^{3-}$. A popular disc type electrode design was chosen and the electroanalytical performance was assessed at a particular fabrication parameter. Such a study design was rapidly executable owing to the inherent customizable property of laser printing thus vindicating the fabrication process. The XRD and Raman spectroscopy ($I_D/I_G \sim 0.9$) results revealed graphene formation with excellent crystallinity (98%) and sp^2 hybridization characteristics thus vindicating the fabrication parameters. Furthermore, the SEM micrographs revealed sheets like structures, which are interconnected to form 3D porous structures. While, the main focus of this work is to report the structural information from XRD and Raman spectroscopy, we also evaluated the electroanalytical performance, where the latter did not exhibit near-Nernstian/reversible response, which we attribute to the electrode design, hence, the future works shall focus on optimizing the electrode design and evaluating the electrochemical performance.

2 Materials and Method

Potassium ferricyanide ($K_3[Fe(CN)_6]$) and potassium chloride (KCl) were purchased from Sigma-Aldrich (St. Louis, MO). Deionized (DI) water (18.3 $M\Omega\text{-cm}^{-1}$) was generated using water purification system. Polyimide (PI) sheet (10 mil thickness) was purchased from Dali Electronics, Mumbai, India, Insulating PI tapes was purchased from local vendor. The electrode designs were created using Inkscape software (Version 1.1) (Fig. 1). The design was imported to voxelizer software, (scaled down to about 0.26 according to address scaling issues in Voxelizer software). Lasing parameters were, vertical distance—5 mm, hatching angle—90°, hatching distance—0.05 mm, work speed—20 mms^{-1}, travel speed—20 mms^{-1} and lasing power—25% (100% power—2.8 W). The electrodes of pre-mentioned design were lased onto polyimide sheet. An insulating tape was used to cover the conducting paths in order to restrict the flow of analyte to the working region of the electrode. Thereafter, Ag paste was applied to the surface to form a quasi-reference electrode. Finally, copper strips (4 × 4 mm) were pasted on the conducting pads to avoid discrepancies

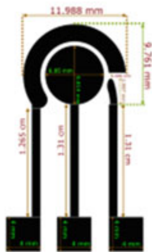

Fig. 1 LIG electrode with dimensions and lased electrode pattern on PI film

in connections. Electrochemical characterization was performed using 5 mM Fe^{3+} solution, prepared 0.1 M KCl and 350 μL of solution was dropcasted onto working regions. Cyclic voltammetry with following parameters was set, $V_{initial} = 0.6$ V, $V_{final} = -0.4$ V, 2 sweeps. Scans rate optimization studies from 100 mVs^{-1} to 10 mVs^{-1} were performed. The analyte solution was thoroughly pipetted in and out to disturb the diffusion layer formed during the previous measurements. Furthermore, analysis was done from higher scan rate to lower scan rate, which also ensures the diffusion layer formed during last iteration is of minimal thickness.

3 Results and Discussions

3.1 XRD and Raman Analysis

$$D = \frac{K\lambda}{\beta \cos\theta} \tag{1}$$

$$K = 0.9,\ \lambda = 0.15406\,\text{nm},\ \beta\ \text{is FWHM of peak},\ \theta\ \text{is diffraction angle}$$

$$\%\text{Crystallinity} = \frac{\text{Area of crystalline Peak}}{\text{Area of all peaks, crystalline + amorphous}} \times 100 \tag{2}$$

$$d = \frac{n\lambda}{2\sin\theta} \tag{3}$$

$$\delta^2 = \frac{1}{D^2} \tag{4}$$

$$\varepsilon = \frac{\beta}{4\tan\theta} \tag{5}$$

$$L_a = 2.4 * 10^{-10} * \frac{\lambda^4}{\frac{I_D}{I_G}} \quad \text{where } \lambda = 514\,\text{nm} \tag{6}$$

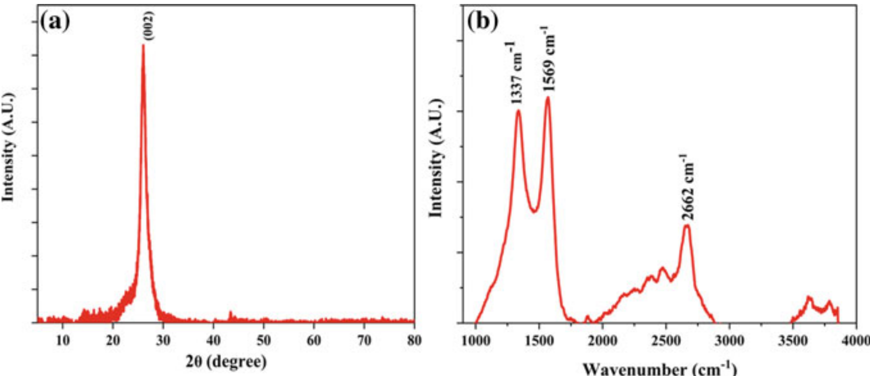

Fig. 2 (**a**) XRD spectrum of LIG (**b**) Raman spectrum of LIG

XRD analysis (Fig. 2a) revealed a very sharp peak at $2\theta = 26.9$ degree, with a preferential plane orientation (002), and the d spacing indicative of graphene structures and is in accordance with LIGs reported by Nayak et al. [19]. The LIG exhibited excellent crystalline characteristics as indicated by the crystalline percentage. Apart from these, the dislocation density and micro strain are reported in Table 1. Figure 2b shows the Raman spectrum of the LIG, where distinct peaks corresponding at 1337 cm^{-1} (D band) 1569 cm^{-1} (G band) and 2662 cm^{-1} (2D band) are observed. D band is indicative of defect in graphite structure [16] and comes from iTO phonon near K point. The G band arises due to double degenerate zone centre at E_{2g} mode, while the 2D band is due to double resonance process and represents the relation between wave phonon wave vectors and electronic band structure [10]. The I_D/I_G ratio was found to be 0.94 and indicated formation of graphene with high degree of disorder and I_{2D}/I_G was close to 0.4, this indicated the LIG structures to contain more than 4 layers of graphene [18]. The significant splitting of 2D peaks into wider fractions further corroborates the above inference. The average crystallite size of graphene samples was calculated using Tunistra Koenig Relation (Eq. 7) [9] and was obtained as 20.43 nm (Table 2).

3.2 *Morphological Analysis*

The sheet-like appearance in SEM image indicates rapheme sheet-like architecture, while the presence of pores may be attributed to escape of small nitrogen containing molecules owing to photothermal and photochemical effects [3, 7]. The individual sheet-like structures are interconnected 3D porous arrangement and are promising electrochemical applications. This is in corroboration with EDAX spectrum, where the nitrogen content is negligible (Fig. 3).

Table 1 Parameters obtained from XRD spectrum

Parameters extracted from XRD	Value
FWHM	1.79606
2θ	26.0997 (degree)
Crystalline size (D)	0.079246 (nm)
Area under the crystalline peak	3189.3657
Total area under XRD curve	3231.961
Height of the peak	1660.7373 (A.U.)
% crystallinity	98.61%
d spacing	0.3411 (nm)
Dislocation density (δ^2)	159.23 (nm^{-2})
Micro strain (Ɛ)	1.937206

Table 2 Parameters obtained from Raman spectrum

Parameters extracted from Raman	Value
Excitation laser source wavelength	514 nm
I_D/I_G	0.941153
I_{2D}/I_G	0.4263
L_a (nm) (in-plane crystalline dimension)	20.43 nm
Disorder (border 1D defect)	0.04894 nm^{-1}

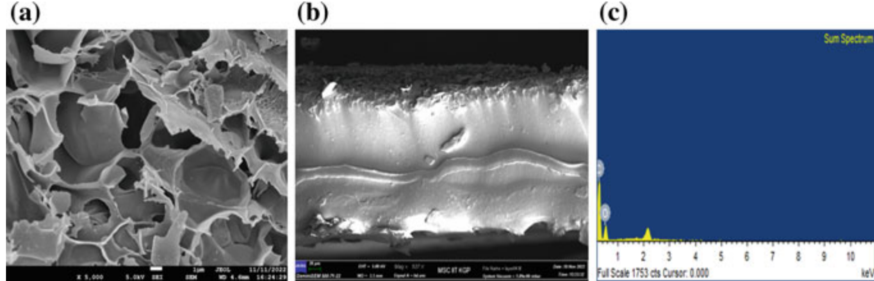

Fig. 3 (**a**) SEM image (**b**) cross-sectional SEM image (**c**) and EDAX spectrum of LIG

3.3 Electrochemical Characterization of Electrodes

The cross-sectional SEM images indicated a thickness of about 60 μm. However, certain LIG works report highly hydrophobic surfaces and hence, it may be assumed that only upper surface of pores has a direct influence on analyte's diffusion characteristics. At lower scan rates, the diffusion layers are sufficiently larger/thicker over the microscopic roughness of the electrodes [1]. Hence, on a physical sense,

major fraction of diffusion occurs over the apparent area concocted by this diffusion layer, and subsequently, the surface becomes smooth/planar and thus, Randle–Sevcik equation is valid in these cases [20]. Electrochemical scan rate studies were performed to harness the electrochemical active surface area. The CV response exhibited a diffusion-controlled mechanism, with peak current being proportional to the square root of scan rate (Fig. 4). From the ΛEp values, it was observed that the electrode surface exhibited irreversible kinetics, and subsequently, the following Randle–Sevcik equation was used to harness the ECSA [11]. Furthermore, the obtained ECSA was used to obtain diffusion lengths in order to affirm the above statement [23].

$$I = +0.496\sqrt{\alpha n'}.nFA_{\mathrm{ECSA}}C\sqrt{\frac{nFD\upsilon}{RT}} \tag{7}$$

where $a = 0.5$ (Assumed), $n' = 1$, $F = 96{,}500\ \mathrm{CMol}^{-1}$, $D = 7.9 \times 10^{-6}\ \mathrm{cm}^2\mathrm{s}^{-1}$, $R = 8.314\ \mathrm{KJKmol}^{-1}$, $T = 298$ K, the Equation Simplifies as

Then,

$$I = 0.003168\sqrt{\vartheta} \tag{8}$$

$$Q = \frac{FA_{\mathrm{ECSA}}\delta C}{2} \tag{9}$$

The ECSA values were obtained as 1.0971 cm^2. Furthermore, in the scan rate regime considered for analysis, I_{pc} versus ν did not exhibit linear characteristics, indicating there was no adsorption on electrode surface and is in contrast to the results reported by Griffiths et al. [13], where I_p of CO_2-based LIG exhibited linear dependence on ν and $\sqrt{\upsilon}$ in the considered (their work) scan rate range. Such phenomenon was attributed to thin-layer diffusion effects, which occurs due to the influx of analyte species into the pores of electrode and contributing to this phenomenon, and is more

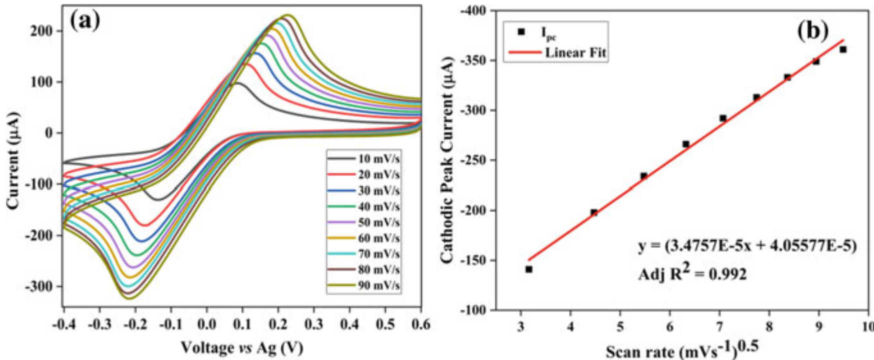

Fig. 4 (**a**) Scan rate optimization of LIG electrodes in 5 mM ferricyanide (in 0.1 M KCl) (**b**) plot of I_{pc} versus $\sqrt{\upsilon}$

Table 3 Parameters extracted from CV spectrum

Scan rate (mV/s)	Diffusion length (μm) (till peak current reached)	I_{pc} (μA)	I_{pa} (μA)	ΛEp (mV)	Charge (C) (till peak current reached)
10	46.34878	– 146	120	210	0.001226
20	41.63919	– 218	190	256	0.001101
30	39.95941	– 231	180	328	0.001057
40	38.74783	– 262	210	354	0.001025
50	35.36806	– 293	240	375	0.000935
60	33.75265	– 314	250	416	0.000893
70	33.29601	– 334	260	436	0.000881
80	30.89628	– 351	270	452	0.000817
90	29.00211	– 361	280	465	0.000767
100	14.04438	– 329	290	460	0.000371

prominent at higher scan rates [5]. The LIGs fabricated in this work did not exhibit such phenomenon, which may be due to pore size, hydrophobicity, or presence of oxygen functionalities that may prevent this adsorption like process [19]. Further works shall be performed in order to assess these aspects. While, XRD indicated formation of graphene oxide and I_D/I_G ratio indicated greater sp^2 content in graphene, and it is expected for the electrodes to exhibit facile electrochemical characteristics. However, the slightly poor electrocatalytic performance is exhibited (Table 3). The decreased ECSA, hence poor electrocatalytic performance, may be attributed to electrode design, where the area of CE is comparable to that of WE [15], furthermore, the greater size of WE may result in increased potential drop due to uncompensated solution resistance [2]. Thus, increasing the area of CE may ameliorate the electrochemical performance. Furthermore, decreasing the length of the conductive track (resistance measured via 2 probe setup 80 Ω) shall decrease the potential drop may also enhance the electrochemical activity [22].

4 Conclusion

In conclusion, this brief work involved fabrication of laser-based electrodes and analysing its structural, morphological characteristics thereby confirming its successful fabrication. XRD data revealed excellent crystallinity characteristics and Raman formation of multi-layer graphene with defect density corresponding to I_D/I_G of 0.9. Albeit, the electrochemical performance was not very appreciable, and this preliminary work affirmed the formation of graphene/reduced-graphene oxide material thus vindicating the fabrication procedures. Furthermore, future works shall involve optimizing electrode design to harness the best electrochemical performance.

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Implementation of Energy Efficient Full Adder for Arithmetic Application

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1 Introduction

Today's portable electronics are all made to be more sophisticated and portable, including laptops, telephones and other gadgets. There are many battery-powered portable applications being developed, which have smaller sizes, and high-throughput and low-power circuits are required. The smaller circuit can reduce expenditures and extra storage space. As a result, while developing microprocessors and other system components, extra attention must be paid to circuits that consume low power.

Different computational operations in a microprocessor depend on addition; the performance of an arithmetic circuit's operation has a significant impact on the overall performance of a digital processor. Therefore, the full adder (FA) is the most crucial component in the microprocessor. Improving the performance of FA enhanced the performance of the processor. In the literature, there are different FA designs already proposed [1–8]. In this work, a novel design of FA is designed, which enhances the performance of the processors.

To increase the performance of the FA circuit, different techniques have been used. However, these FA cells performed the addition with different logic strategies, transistor counts and internal nodes. Because of this, some performance measures are improved by different logic architectures while others are decreased. Some FA

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cell is implemented using a single logic design which is called single logic FA cells. On another side, some FA is implemented using a variety of logic topologies called hybrid logic-based FA designs.

In the recent years, scaling techniques have been used to implement the arithmetic circuit. By scaling the MOSFET at the nanometer scale, leakage current phenomenon is increased. This leads to an increase in the current between the drain and the source region. To overcome the problem of the short channel effect in lower technology, we have to use FinFET technology.

This paper shows a new hybrid FA circuit which is implemented using 16 nm FinFET technology. Section 2 presents a review of the prior design of FA cells. Section 3 presents a proposed full adder. The simulations, findings and analysis are presented in Sect. 4. The paper's final part is Sect. 5.

2 Literature Review of Existing Full Adders Cells

2.1 Single Logic Full Adder

Complimentary pass logic (CPL) used 32 transistors to implement the adder's design. In the CPL logic, NMOS transistors are used to implement the FA design; therefore, voltage drop problem occurs. To overcome the problem, CPL logic requires voltage-restoring buffers when NMOS passes weak logic one. Due to this, the transistors count is increased. Additionally, a large area of silicon is consumable for implementing CPL-based FAs due to the higher transistor count.

The complementary CMOS (CCMOS) logic overcomes the problems of dropping of voltage. This style-based FA is implemented with pMOS and nMOS networks. There are 28 transistors required for CCMOS-based FAs to function at full output swing. The CCMOS FA circuit is capable of good driving capability and full-swing output. The PMOS module, which is lesser mobility than the NMOS module, is the major flaw in static CMOS circuits. In order to get the required performance, the PMOS devices must be scaled up. In static CMOS, every input is connected to the gate of at least an nMOS and a pMOS device. Hence, the input capacitance is crucial [3, 4].

Transmission-function (TF) and transmission-gate (TG) logic used to implement FA have large capacitance, a high transistor counts, all used in the construction of the FA circuit to overcome the threshold. This adder's main problem is that it cannot drive other logic designs, despite the fact that it naturally uses less power. Furthermore, cascading severely affects the performance of TFA or TGA [5].

To improve the performance of FA cells, a dynamic CMOS logic style is used. In this logic style, nMOS transistor is used for implementation, due to which input capacitance is low. However, it has a number of inherent issues, including rapid switching, charge sharing, leakage and reduced noise immunity. In this style, most

of the power consumption is due to clock lines. As a result, throughout this paper's discussions, we do not discuss dynamic logic style.

2.2 Hybrid Logic Full Adders

In the hybrid CMOS logic-based FA, different logic styles are used to realize the different modules. In this FA design, two input signals, A and B, are applied in Module I to realize the XOR and XNOR outputs simultaneously. These intermediary outputs drive the other two modules (Module II and Module III). In hybrid style-based FA, we optimized individual modules to achieve the required results. In this style, the main benefit is fewer internal nodes to implement the circuit, due to which the power consumption of this style is lower than single style-based FA. [6–14]

Another method to implement the FA design is the gate diffusion input (GDI) method, in which the count of the transistor is reduced. However, voltage fluctuation problems in GDI cases have the weak driving capability. Scalability is another significant issue in GDI-based FA design which is presented by Sanapala et al. [16]. GDI-based AND-OR and XOR-XNOR circuits offered by Shoba et al. [17] prevent voltage deterioration and generate the full swing at the outputs. In this work, a new circuit of FA is implemented using the GDI technology.

Present a new, enhanced FA circuit in this study. The new adder is compared to the traditional CPL, static CMOS, TGA, TFA and various hybrid FA circuits and is targeted for low PDP. The offered full adder approach obtained full swing at the internal and external nodes, smaller PDP and good driving abilities without compromising capacity or durability. Additionally, we evaluated how the FA design performed under varying voltage (0.4–1.0 V). When compared to the conventional FA, the novel adder performed better.

3 Proposed Full Adder

Module I (XOR-XNOR) is realized using the TG and PTL logic with 8-transistors. In this circuit, XOR is implemented using two NMOS (n2 and n3) and two PMOS (p2 and p3) transistors, and the XNOR module is implemented using one inverter (p4 and n4) transistors. To recognize the operation of the proposed design of Module I (XOR-XNOR), Table 1 presents the charging and discharging paths. The transistor is participated in obtaining the full swing at the output. It includes all the paths to provide full swing at the output nodes.

According to Fig. 1, Modules II Sum and III Carry out are realized by the TG and PTL logic style. In the proposed design of the XOR-XNOR circuit, there is no feedback signal which causes no glitch in the simultaneous generation of XOR-XNOR (Table 1).

Table 1 Working explanation of Module I (XOR-XNOR)

Input		Path	XOR	XNOR
A	B	Full swing	Logic at the output	Logic at the output
0	0	n2	0	1
0	1	p2	1	0
1	0	p3	1	0
1	1	n3	0	1

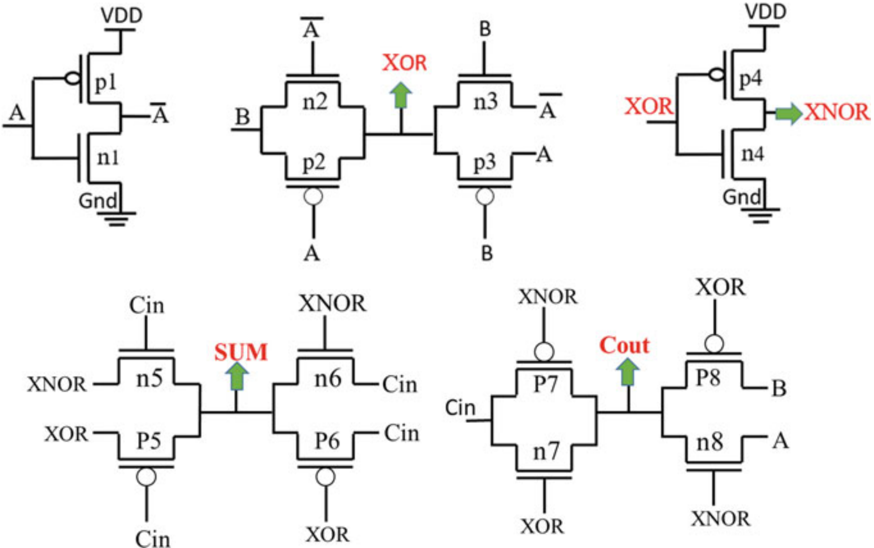

Fig. 1 Proposed hybrid full adder

Table 2 Working explanation of full adder

A	B	Cin	SUM	Cout
0	0	0	0 (n6)	0 (n7)
0	0	1	1 (p5)	0 (n8)
0	1	0	1(p5)	0 (n7)
0	1	1	0(n5)	1 (p7)
1	0	0	1(p5)	0 (n7)
1	0	1	0(n5)	1 (p7)
1	1	0	0(n6)	1 (p8)
1	1	1	1(p6)	1 (p8)

Table 3 Comparison of power, latency and PDP AT 1.0 V power supply voltage

Designs	Power consumption (μw)	Latency (ps)	PDP (aJ)
Mirror FA [2]	4.624	16.69	77.2
CCMOS FA [2]	4.8275	16.52	79.76
TG-based adder [3]	4.3947	11.84	52.07
TG-based adder inverter [3]	4.7806	19.74	94.37
Mehedi [15]	3.2965	13.28	43.77
Shoba design1 [17]	3.8961	13.36	52.05
Mirzaee [18]	4.3486	18.14	78.91
ULPFA [19]	3.2965	13.28	43.77
Ramachandran [20]	4.7229	12.2	57.61
Proposed adder	2.5823	11.81	30.51

4 Simulation Results

To test the circuits, a real simulation setup, as described in [7], is used to establish the real environment. The buffers circuit passes the input signals, and output is measured through the FO4 load.

Latency, power consumption and PDP are evaluated in FA circuits to compare the results. A digital circuit's performance parameters can vary depending on the input configuration. This led to the calculation of AP, taking into account all input combinations. PD has also taken into account crucial path delays (worst case delay). Table 3 gives the simulation results of different adder circuits at a 1.0 V power supply.

Table 3 offers that the proposed design improved the parameters with the prior designs. The proposed design reports lower power consumption and improved PDP.

Using a power supply of 1.0 V and a frequency of 1 GHz, circuits using 16 nm FINFET technology are tested. Further, to examine the reliability of the circuit at the voltage variation effect from 0.4 to 1.0 V, different circuits are re-simulated. Figures 2, 3 and 4 represent the power consumption, latency and PDP of the different FA designs at the different supply voltages. From the analysis, it can be concluded that the novel design offers superior PDP and better energy performance.

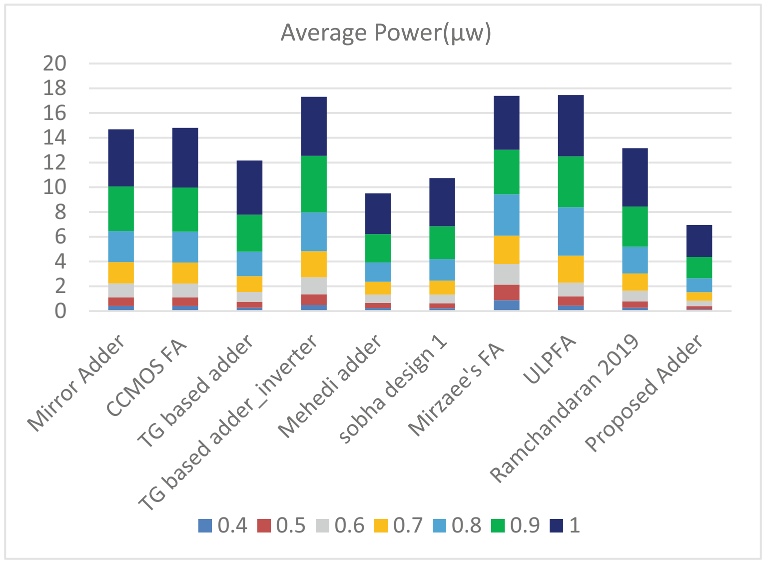

Fig. 2 Energy usage of different FA at voltage variation (0.4–1.0 V)

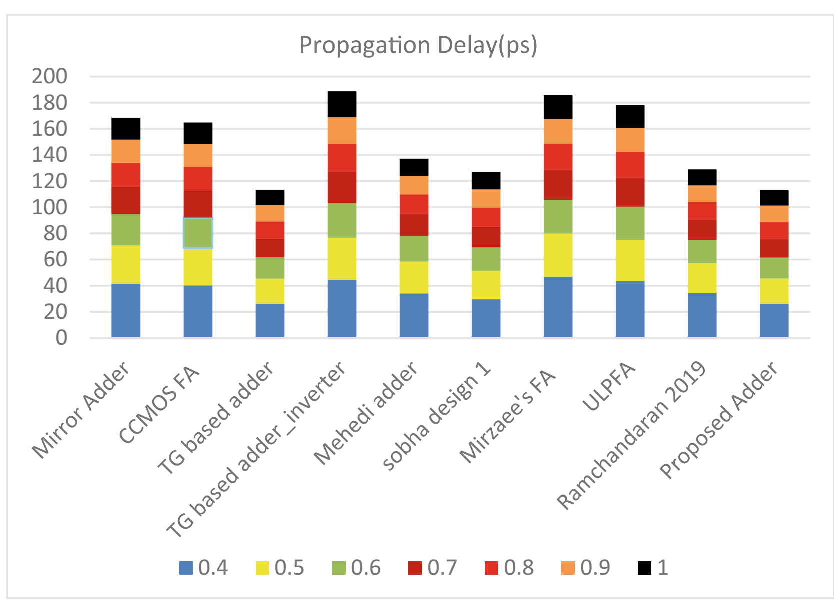

Fig. 3 Latency analysis of different FA with voltage variation (0.4–1.0 V)

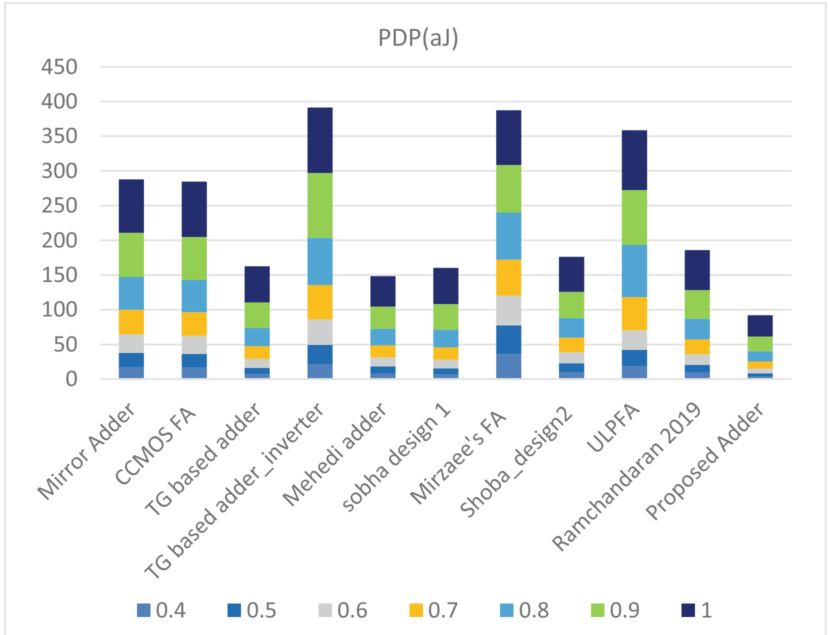

Fig. 4 PDP analysis of FA with voltage variation (0.4–1.0 V)

5 Conclusion

This work presents a hybrid style-based FA circuit which is implemented using the novel design of Module I (XOR-XNOR). Additionally, this work has provided a comparison of existing and offered FA. From the results, it is noted that the proposed FA reports a 29.37% to 71.90% improvement in average power consumption and a 38.96–81.56% improvement in PDP compared to the prior designs. We concluded that the offered complete adder architecture is suitable for low-power VLSI applications. For future work, these full adders can be implemented in other arithmetic blocks, such as multipliers and subtractors, which will be investigated.

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Design and Implementation of Bus Ticketing System Using Verilog HDL

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1 Introduction

India has the second-largest road network in the world, which spans approximately 6.2 million kilometers. Public transportation by bus is one of the most common ways after the railway system. Thousands of people travel by bus to reach their destination daily. The inter-state bus terminal routes allow passengers to travel from one state to another state, whereas buses add up to 90% of public transport in urban India. It shows the vitality of bus transportation in people's daily life. Automated fare collection is a service system for customers to buy tickets, take buses, and exit the station [1]. By introducing the automated fare collection system, it is possible to increase efficiency within the system and improve passenger satisfaction [2, 3]. Indian railway and metro systems of several cities in India introduced automated fare collection systems and got a good response from the passengers.

This paper mainly focuses on the implementation of an automated ticketing system in bus transportation in urban areas, where the passengers are well-versed with technology [4, 5]. The designed system is homogeneous to a vending machine with some added features. We used Verilog HDL to design the module and improve the design efficiency in the design process. The proposed design is implemented in SPARTAN 3-XC3S50 FPGA [6] to simulate the real-time I/O behaviors and estimate the overall performance of the proposed design.

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2 Design Content

This paper mainly designs an automatic ticketing system that can help passengers successfully buy tickets with simple operation [3, 4]. For simplicity, the system can work with Rs 5 and Rs 10 coins. Passengers can choose the bus line, destination, and the number of tickets from the available options on the display. For the simplicity of design, there are two bus line (routes) b1 and b2, where each bus line has three destinations stop_1price, stop_2price, and stop_3price, respectively. A passenger can choose a maximum of two tickets at a time according to the selected path, and the total cost of the tickets will be shown on the display. Students and senior citizens (above age 60) will get a discount on ticket costs. After the cost is displayed, passenger has to insert coins and it will be processed. The ticket will generate and if the passenger inserts more coins than the ticket price, the system will calculate the change and return it to the passenger.

2.1 Ticket Selection

Each passenger can get two tickets at a time, for providing three destinations stop_1price, stop_2price, and stop_3price each cost of Rs 5, Rs 10, and Rs 15, respectively. According to the path selection and the number of tickets, cost of the tickets will be displayed.

2.2 Rebate System

Students, physically challenged, and senior citizens will get a discount on the cost of the ticket, by providing the proper code assigned to them. After they enter the code, the software checks the entered code with our database. If it matches, passenger will get a discount on the cost of the ticket.

2.3 Coin and Change Processing

For simplicity, there are two types of coins accepted, Rs 5 and Rs 10. If the inserted coins are equal to the cost of the ticket, then the ticket will be dispensed, and if the inserted coins are more than the ticket cost, change will be returned (Fig. 1).

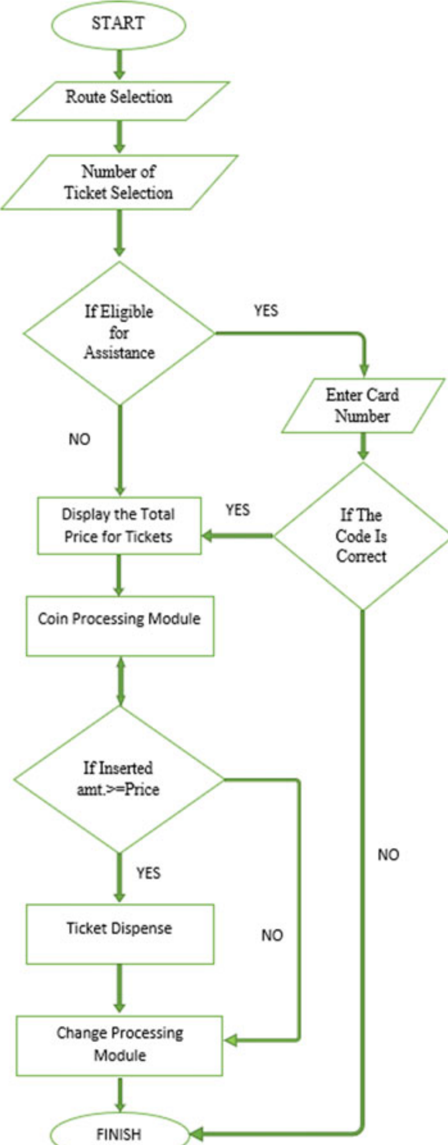

Fig. 1 Flowchart of the entire system

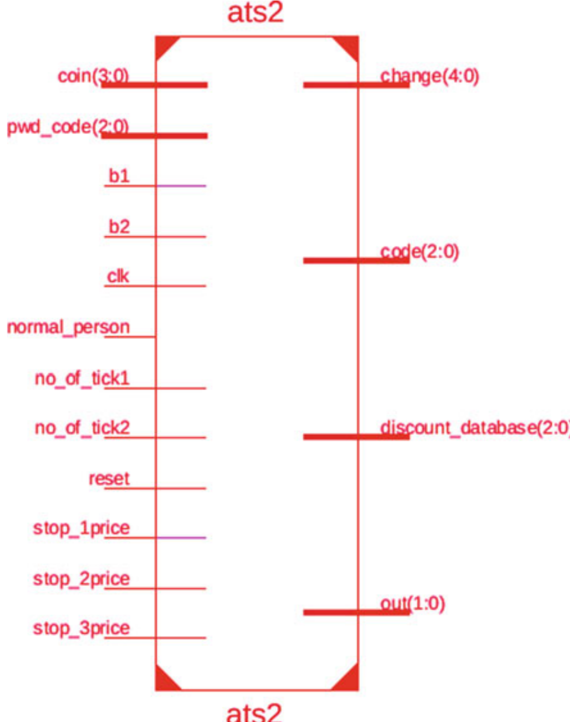

Fig. 2 Pin assignment of the module

3 Design Results

3.1 RTL Schematic

After synthesizing the designed Verilog module in Xilinx Vivado ISE [6], the top-level module has been shown below with the input/output pin assignment. Resister transfer-level schematic is generated (Figs. 2 and 3).

3.2 Simulated Waveform

Simulation for citizens who are eligible to get reimbursement

The simulation results are shown for the selected path is bus line 2, stop_3, and no_tick_2, and the pwd_code entered is 101 which is in the database of automatic ticketing system authority and the system will compare the entered pwd_code and found that it matches, so the passenger will get discount in the cost of the ticket. In this project, we designed that if entered code matches with the database passenger

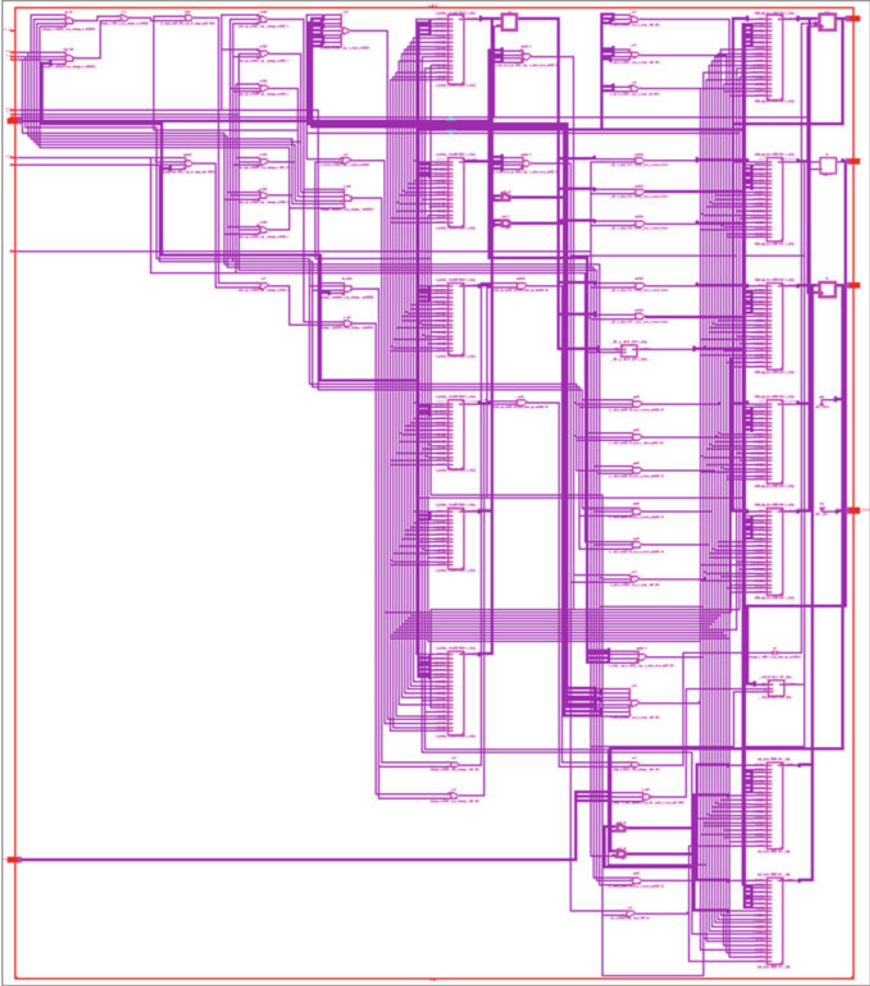

Fig. 3 RTL schematic of the design

will get a ticket for a minimum price (Rs 5). Here coin Rs 10 is entered, and the output is 3 means a ticket is generated for stop_3 and the remaining change is processed to the passenger (Rs 5) (Fig. 4).

Simulation for Normal Citizens

The simulation results are shown for the selected path is bus line 2, stop_3, and no_tick_2, and no pwd_code entered so the passenger won't get a discount on the cost of the ticket. For stop_3, cost of the ticket is Rs 15 and the number of tickets is two so the cost of the ticket is Rs 30. A ticket is generated according to the coins inserted by the passenger and the change processed (Fig. 5).

Fig. 4 I/O waveform simulation with rebate condition

Fig. 5 I/O waveform simulation without rebate condition

3.3 Device Implementation Results

The design has been implemented upon a Spartan 3-XC3S50 device and the results were estimated using Vivado ISE [6].

Device Utilization

See (Table 1).

Timing and Power Analysis Summary

Using the tools such as Timing Analyzer and XPower Analyzer in Vivado ISE, the estimated timing and power reports were generated. It is estimated that the device has a delay of 6.134 ns at a maximum clock frequency of 130 MHz (approx.). Logic delay is 5.535 ns (87.7%) and 0.779 ns (12.3%) delay through route. The designed system has a total power consumption of 27.34 mW.

Table 1 Device utilization summary

Types	Number of device used	Number of device available	Utilization (%)
Slices	96	768	12
Slice flip flops	16	1536	1
4 input LUTs	181	1536	11
Bonded IOBs	29	124	23

4 Conclusion

In this paper, we have successfully designed an automated bus ticketing system with Xilinx Vivado ISE using Verilog HDL and implemented it on FPGA. The simulations meet the expected I/O waveforms. This proposed design falls under smart city projects, which will be able to solve the problems of the existing physical ticketing system and improve efficiency as well as passenger satisfaction. Unlike the existing system, the introduced system will be able to help the bus transportation authority with accurate fare collection.

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Negative Time Interval Measurement Using CMOS Standard Cell-Based Vernier TDC Channel

Pooja Saxena

1 Introduction

Time-to-digital converter (TDC) is used to measure precise time interval between two designated events 'start' and 'stop' in many applications like TOF laser range finding [1], Indian neutrino observatory (INO) HEP experiment [2] and medical imaging [3], etc. Here corresponding to the event, an analog signal is generated using relevant detector. This analog signal is applied to front-end electronics with discriminator which gives logical transition signal working as start or stop input for TDC. In INO experiment and TOF laser range finder, the stop signal defined as 'multi-hit' stop comprises multiple edge transitions. These multiple transitions are corresponding to the received successive eco pulse events from multiple reflections of fired LASER shot (TOF laser ranger finder) and delayed muon interaction events with RPC-based detector (INO experiment).

The measurement of multi-hit stop signal with respect to start is required to find information of delayed and multiple reflection events [4] as well as to implement the time walk error correction method. Moreover, due to the delay in electronic signal processing and criteria of selecting valid events, this multi-hit stop signal may occur before the start signal. The arrival of 'start' after 'multi-hit stop' signal requires TDC having feature of negative time interval measurement with multi-hit capability.

Previously, Vernier ring technique is used in designing various TDCs [5–9] to measure the positive time interval, i.e., when stop occurs after start signal. In [10], the implementation of Vernier technique is extended to incorporate the feature of multi-hit time measurement. Here, when multi-hit stop occurs before start (post-start mode), an external 'event reset' signal is used to measure respective timing of start and multi-hit stop signals individually. The difference in absolute measured timings

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of 'start' and 'multi-hit stop' gives the time interval between them. However, in INO experiment and TOF laser range finder as only 'start' and 'multi-hit stop' signals are available as inputs to TDC, therefore to avoid the dependency on external signal, posed a requirement to analyze the Vernier technique for negative time interval measurement.

In this paper, negative time interval measurement using Vernier technique as its new feature is presented and is explained in Sect. 2. Also, this feature is incorporated in the implementation of Vernier TDC channel with multi-hit capability which makes it suitable for pre-start, post-start, and mixed modes, covered in Sect. 3. Section 4 explains the post layout simulation results and conclusion of this design.

2 Vernier Time Interval Measurement Technique

Vernier technique employs two ring oscillators slow and fast, which are triggered by start and stop signals respectively as shown in Fig. 1a. The time periods of generated slow and fast clocks are 'T_{oscst}' and 'T_{oscsp}', respectively. As 'T_{oscst}' is slightly less than 'T_{oscsp}'; therefore, the rising edge of fast oscillator clock follows the rising edge of slow oscillator clock (Fig. 1b) in each clock cycle with the step size of '$\Delta T_d = T_{oscst} - T_{oscsp}$'. Finally, the rising edges of both clocks either coincide or fast clock leads the slow one which is monitored by a phase detector. The step size 'ΔT_d' defines the LSB of time interval measurement between start and stop signal.

When start signal comes after stop (post-start mode), the measured time interval between them is given with minus sign. Vernier technique can be used for this kind of measurement attributed by definite phase coincidence or leading between slow and fast oscillating clocks. As per Fig. 1c, the fast oscillator starts oscillating before the slow one. In this state, the rising edge of slow clock follows the incoming rising edge of fast clock with step size of ΔT_d. Eventually, the rising edges of both oscillator clocks will either coincide or the rising edge of the fast clock will precede the slow one.

A phase detector is used to detect the phase leading or coincidence [8]. The phase detection is carried out through implementation of sampling and shifting the status of slow clock by fast one. When the previous sample of the slow clock is at logic '1' and the current sample is at logic '0,' the 'eoc' signal is asserted. This happens when rising edge of fast cock leads slow clock, same in both positive and negative time interval measurements. Therefore, the designed phase detector can be used for both positive and negative time interval measurements.

Coarse and fine counters are used to count the elapsed cycles of slow (N_c) and fast (N_f) oscillator clocks, respectively, until phase coincidence is achieved. In positive time interval mode, the coarse counter defines measurement range of $(2^m - 1) \times T_{oscst}$, where m is the width of coarse counter. The fine counter accounts for the cycles of fast clock corresponding to number of steps (ΔT_d) within slow clock time period T_{oscst} till coincidence. Therefore, the width 'k' of fine counter is chosen to handle the total no of steps over T_{oscst}. On the other hand, in negative time interval, the role

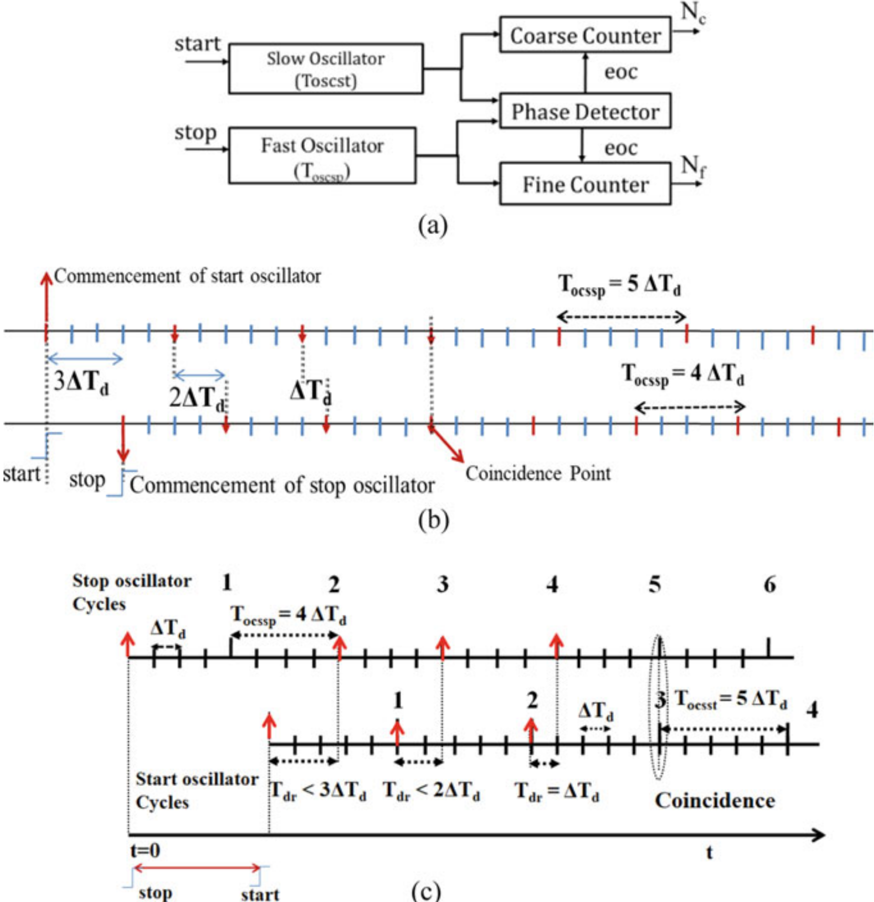

Fig. 1 **a** Block diagram of Vernier time interval measurement technique, **b** edge representation of phase coincidence in positive time interval, **c** in negative time interval

of coarse and fine counter is interchanged. Here, the fine count is greater than coarse count and defines the measurement range. Therefore, in order to achieve the same measurement range both in positive and negative time interval measurements, the width of coarse and fine counters is designed similar.

The time interval being measured is calculated using Eq. (1), where one extra count allowed during phase coincidence is deducted from both the N_c and N_f

$$\mathbf{\Delta T} = (\mathbf{N_C} - 1)\mathbf{T_{oscst}} - (\mathbf{N_f} - 1)\mathbf{T_{oscsp}} \quad (1)$$

The maximum measurable time interval between start and stop signals is-

$$\mathbf{DR} = \left(2^{\mathbf{b}} - 2^{\mathbf{K}} - 1\right) \times \mathbf{T_{oscst}} \quad (2)$$

3 Design of Multi-hit TDC Channel Suitable for Pre-start, Post-start and Mixed Modes

The negative time interval measurement attribute of Vernier technique is applied to the extended Vernier TDC channel architecture [10] with multi-hit capability. This paved the way to utilize the TDC channel for various operating modes like pre-start, post-start, and mixed modes. Pre-start or post-start modes are defined with respect to occurrence time of start before or after the multi-hit signal, respectively. Thus in pre-start mode, the TDC channel works for positive time interval measurement and achieved result is with positive sign. In post-start mode, the measurement is for negative time interval with negative sign in result. If start occurs in between the multiple transitions of multi-hit signal, it works in mixed mode.

As depicted in the block diagram (Fig. 2) of TDC channel, a preprocessor block splits the rising and falling edge transitions comprised in the multi-hit signal into four individual hits. To measure the arrival time of these four hits, the stop channel unit (stop oscillator, phase detector, stop counter, latch) is repeated four times. The start channel block (start oscillator and counter) is shared among four stop channel units. This method is effective for providing double hit resolution of 1 ns and is not dependent on the lengthy conversion time (500 ns [9]) of the Vernier technique.

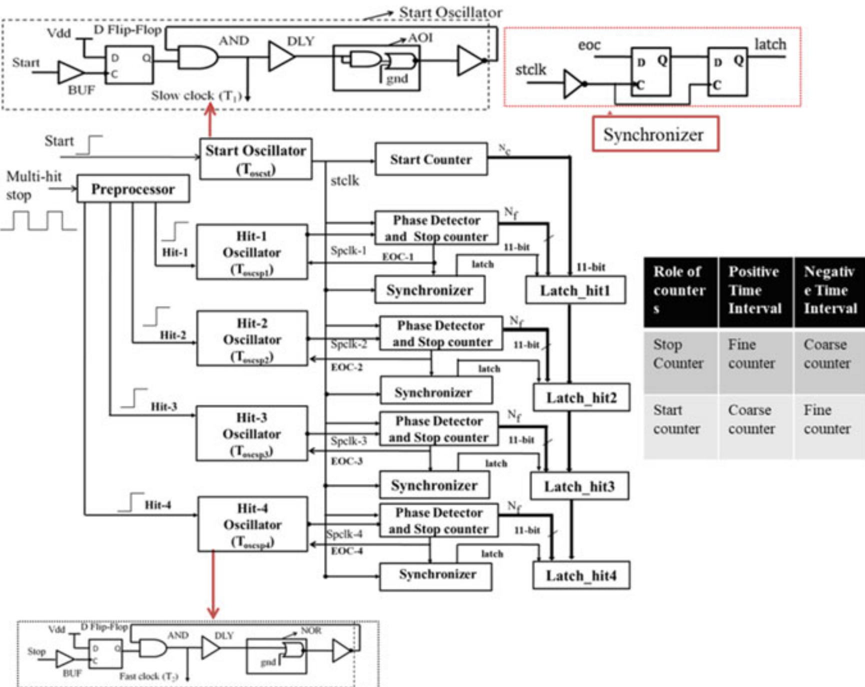

Fig. 2 Block diagram of multi-hit TDC channel using Vernier technique

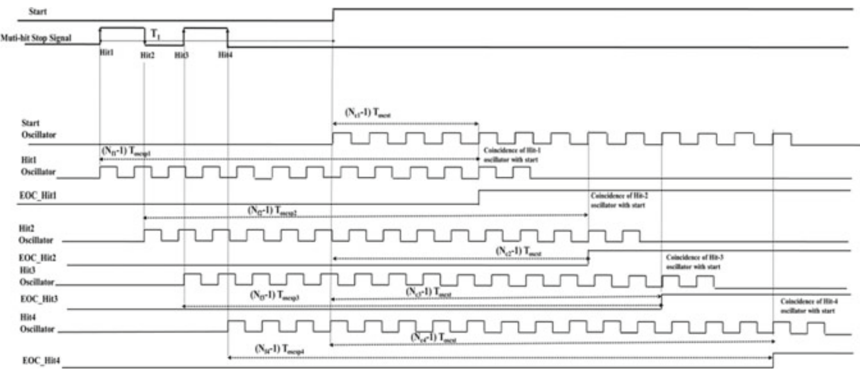

Fig. 3 Time interval measurement using Vernier technique in post-start mode

Figure 3 depicts the timing diagram of TDC channel for post-start mode. Here, the slow ring oscillator is triggered by the ‘start’ signal and oscillates in free running way till the end of dynamic range window. The fast ring oscillator (hit oscillator) in each stop channel block is triggered by ‘hit’ signal, delivered by preprocessor. The phase detector block in each stop channel monitors the chasing of rising edge of start clock with the subsequent rising edge of ‘hit oscillator’ clock. Finally, at the state of phase coincide or phase leading, it asserts an ‘eoc’ signal. The ‘eoc’ signal disables the respective hit counter and oscillator, which benefits in reduction of the power consumption. It is also applied to the synchronizer block, where falling edge of slow oscillator clock samples the logic status of ‘eoc’ signal. This provides a half-clock cycle of time for the ‘eoc’ signal to transition from the logic ‘0’ to ‘1’ state. With this sample, the ‘latch’ signal is obtained with a time margin of 1.5 clock cycles on the subsequent falling edge of the clock. It ensures safely latching the data corresponding to the ‘N_f’ cycles counted by the 11-bit hit counter till phase coincidence of hit oscillator with the start one.

Moreover, the 11-bit start counter data ‘N_c’ corresponding to elapsed cycles of slow oscillator till coincidences is shared among four latches in stop channel unit. This causes a significant wire and fan-out delays associated with the routes of counter data bits. This delay is handled by latching N_c data safely using ‘latch’ signal provided by synchronizer when start counter is in its idle state. However, this way of latching of data takes into account two extra counts in start counter and one extra count in hit counter.

The 24-bit latch data consists of a 2-bit transition ID, an 11-bit start count (Nc), and an 11-bit hit count (N_f). Equation (3) is used to determine the time gap between each ‘hit’ and ‘start’ in all modes. Here, the additional counts taken during the safely latching of start and hit counter data are deducted from N_c and N_f, respectively

$$\Delta \mathbf{T} = (\mathbf{N_C} - 2)\mathbf{T_{oscst}} - (\mathbf{N_f} - 1)\mathbf{T_{oscsp}} \tag{3}$$

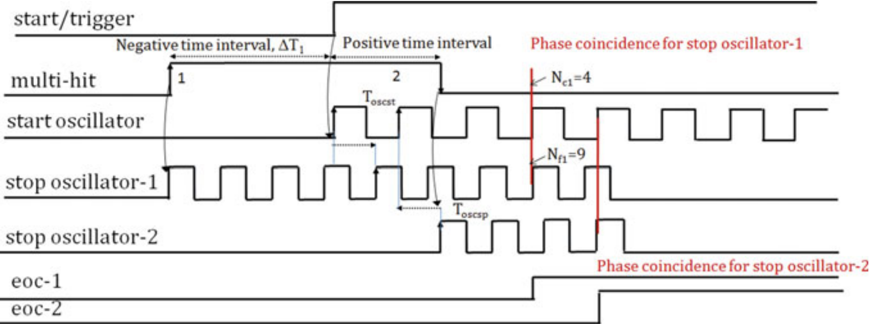

Fig. 4 Time interval measurement using Vernier technique in mixed mode

The pulse width of a multi-hit signal is determined by the time interval between the rising edge and subsequent falling edge transitions. Also, to extract the information for delayed events, the occurrence time of third and fourth transitions is referred.

As shown in Fig. 4 for mixed mode, the start occurs in between the first and second edge transitions in multi-hit stop signal. Therefore, corresponding to first transition, the TDC channel works in post-start mode and gives negative time interval measurement using Eq. (3) as the stop oscillator cycle count N_{f1} is greater than start oscillator cycle clock N_{c1}. Simultaneously, for second transition, it works in pre-start mode and gives positive time interval as here N_{c2} count is greater than N_{f2} count.

4 Simulation Results

The TDC channel is implemented using standard cells of 0.35 μm CMOS technology. Utilizing device models supplied by the foundry, functional, and timing verifications of the extracted netlist of the TDC channel are performed using the SPICE simulator. This method is timing accurate as it takes into account the effect of standard cell routing and MOS devices parasites on TDC performance. On a typical corner, ring oscillator's simulated time periods, T_{oscst} and T_{oscsp}, are 7.402 ns and 7.304 ns, respectively. The difference of $T_{oscst}-T_{oscsp}$ gives resolution of 98 ps. The maximum dynamic range of TDC with 11-bit start counter and 11-bit hit counter is 14 μs as calculated from Eq. (2).

Table 1 displays the simulated values of time periods and resolution for four hit channels across five design process corners. The time periods of four hit (stop) oscillator clocks are similar and there is a maximum 40% variation with respect to typical designed values across process corners. However, the variation in resolution is less than typical designed value of 98 ps. The digital calibration block [9] accounts these variations in time periods and LSB (Table 1), which are used to calculate correct time interval using Eq. (3).

Table 1 Time periods of ring oscillators across process design corners

Corners channels	WP (27°C)	TYP (27°C)	WS (27°C)	WO (27°C)	WZ (27°C)
Stclk: T_{oscst} (ns)	5.422	7.402	9.845	7.501	7.108
$Spclk_1$: T_{oscsp1}(ns)	5.339	7.304	9.66	7.401	6.998
$Spclk_2$: T_{oscsp2} (ns)	5.339	7.302	9.661	7.402	6.999
$Spclk_3$: T_{oscsp3}(ns)	5.339	7.304	9.659	7.401	6.998
$Spclk_4$: T_{oscsp4}(ns)	5.339	7.304	9.659	7.401	6.998
LSB1 (ps)	83	98	185	99	110
LSB2 (ps)	82	100	184	100	109
LSB3 (ps)	83	98	186	100	110
LSB4 (ps)	83	98	186	100	

Figure 5 illustrates the test patterns, used with a Verilog test bench to validate the linearity of the designed TDC channel. Here, in the pre-start mode, the multi-hit signal is linearly time varied with respect to start with a step of 300 ps over a range of 40 ns. Similarly in post-start mode, with respect to the fourth transition in a multi-hit signal, the ‘start’ signal is varied with a step size of 300 ps over 40 ns range. For first transition in post-start mode, the waveform representing the phase coincidence and coarse (N_c) and fine counts (N_f) is shown in Fig. 6. Figure 7 displays the output against input time interval characteristics for the used test patterns (Fig. 5) in both modes. The transition time of four hits is linear with respect to start signal. Further, the absolute time gap between the fourth hit and ‘start’ (a negative time gap) is the same as the time gap between the first transition in a multi-hit and ‘start’ (positive time interval).This shows the efficient working of TDC channel for both positive and negative time interval modes. The linear characteristic (Fig. 7) is used to estimate the DNL and INL errors, which are displayed in Fig. 8.The DNL and INL errors are less than 0.3 LSB and 0.5 LSB, respectively, which are within the acceptable range for the intended TDC channel to operate properly.

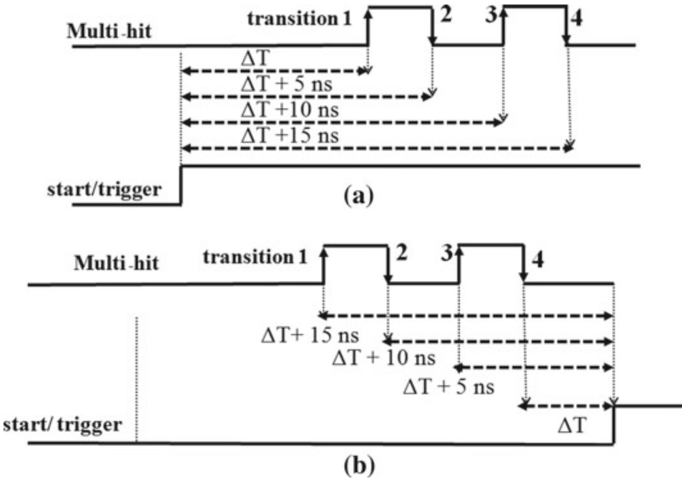

Fig. 5 Time interval **a** pre-start, **b** post-start mode applied test pattern

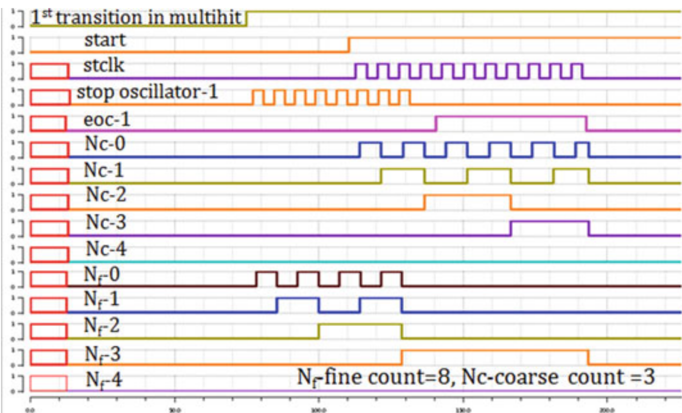

Fig. 6 Post-stop mode: waveform representation of the phase coincidence for transition-1

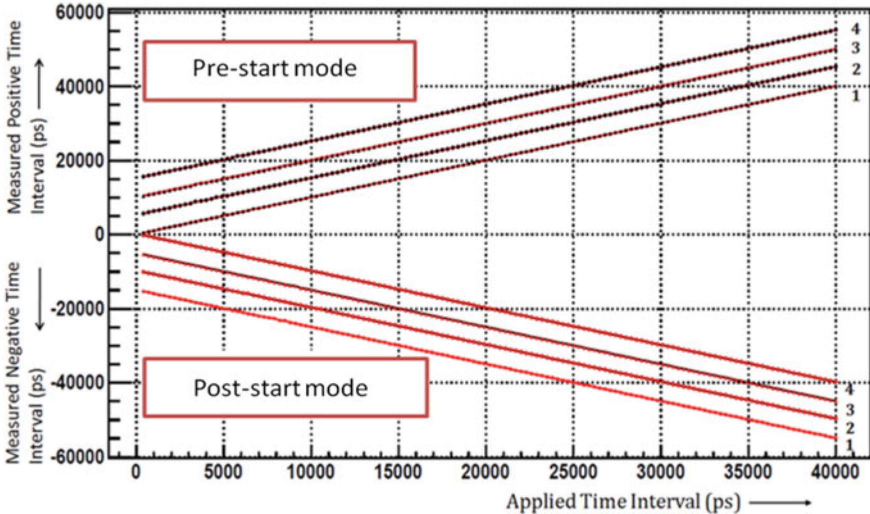

Fig. 7 Output versus input time intervals for applied test patterns in pre-start and post-start modes

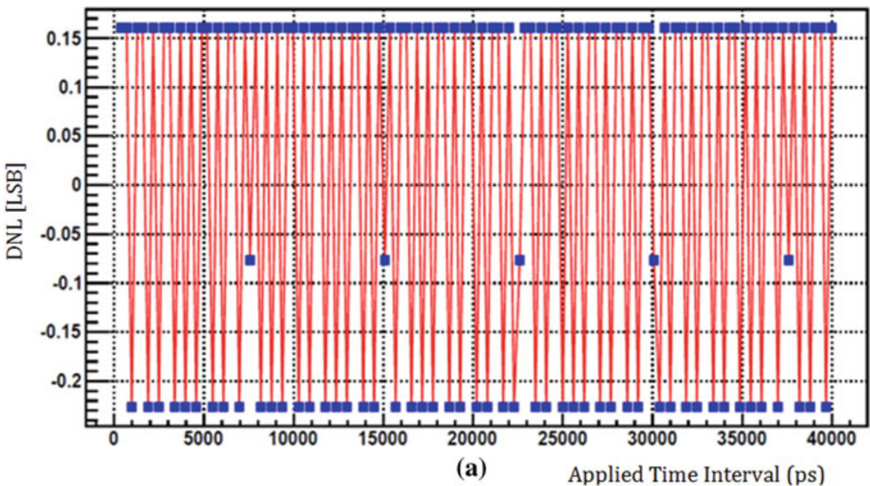

Fig. 8 DNL and INL plots from timing data of first transition in multi-hit signal

5 Conclusion

In this paper, a new feature of Vernier technique as negative time interval measurement between two events is reported. Further, by incorporating this feature, a TDC channel is designed which is suitable for time interval measurement between start and multi-hit stop signals both in pre-start and post-start modes. Using this channel,

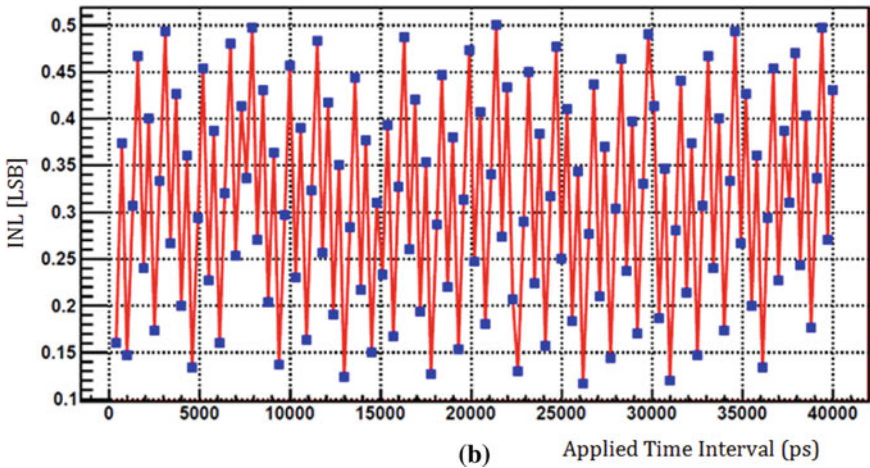

Fig. 8 (continued)

the timing of four hits comprised in multi-hit stop signal is measured with respect to start signal with identical characteristics in both the modes. The TDC channel is implemented using standard cell of 0.35 μm CMOS technology which is advantageous in aspects of less design time, area, and effort. Further, a digital calibrator for time period calibration is included which provides power efficiency in comparison with PLL-based Vernier TDCs. The layout of TDC channel is designed using manual placement and routing approach in order to avoid the mismatch across four hit measurement blocks.

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FPGA-Based Implementation of Convolutional Neural Networks Architecture for Detection of Dysphonia

Jyoti Mishra and R. K. Sharma

1 Introduction

Detection of voice disorders is a challenging task due to the complex nature of speech signals as well as the lack of proper medical technology and equipment. The study of pathological voice diagnosis has caught the interest of the speech processing academic community in the recent decades. As a result, the health of the human voice becomes a key concern. Generally, voice disorders are characterized into two groups, namely organic and functional. Organic voice disorders can be structural or neurogenic [1, 2]. Dysphonia is one of the disorders which can be either organic or functional. Persistence of dysphonia for a long period may lead to larynx cancer. It is one of the severe cases of structural voice disorder. Breathiness, roughness, and hoarseness in voice are the general signs that indicate changes in the larynx. The larynx is a part of the throat that lies between the trachea and tongue [3, 4]. Laryngeal pathology often leads to dysphonia. The pathology results in incomplete closure of glottis, which pairs the subglottic and supraglottic vocal tracts. The coupling leads to change in length of vocal tract and thus formant frequencies get shifted [5]. This study attempts to classify healthy and pathological voice data while concentrating on a single vowel (/a/).

The use of deep learning applications in the healthcare industry can help in the early diagnosis of diseases. Designing of the CNN model along with training and validation on independent datasets has been performed successfully. In automatic detection systems feature extraction of speech, samples are done followed by their processing through various classifiers as it differentiates pathological and

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healthy voice samples [6, 7]. These methods have proven to be quite useful in the prediction of pathological voices in the case of a variety of diseases. Furthermore, several researchers are employing deep learning and machine learning approaches to diagnose and predict symptoms of diseases in the early stages [8–10].

This helps in classification of pathological and healthy speech data. Significant progress has been made by CNN in the area of computer vision and this approach to detect pathological speech have been previously used. Feature extraction from the speech samples followed by processing through classifiers is performed in automatic detection systems. Classifiers differentiate normal voice instances from pathological recordings which have been performed successfully [11, 12]. Voice features may be extracted generally using only two methods either by speech recognition applications which include signal processing tools or by measurement of voice quality from physiological and etiological research [13, 14].

These days, hardware platforms such as FPGAs are emerging as an efficient alternative to software algorithms for image processing and classification. The emergence of programmable devices and system-level hardware programming language has advanced Dual In-line Package (DIP) hardware design. FPGA provides better efficiency, short latency, low energy consumption, high throughput, and accelerated performance of the system [15]. FPGA can change the logic function in just a few hundred milliseconds, has infinitely adaptable logic, and can be used to create accelerators for any algorithm. The accelerators' only trade-off is that they use programmable logic instead of a hardened gate, but this also means that we can use the flexibility of FPGA to further reduce development costs [16]. In both industry and academia, Xilinx FPGAs are widely used as well as they have a high market share as compared to other semiconductor manufacturers.

This work proposes the implementation of CNN architecture using Verilog on the Xilinx Vivado Software tool. In addition to that, the CNN model is trained and validated by a deep network designer of deep learning and machine learning toolbox application in MATLAB. The main aim of this mechanism is to perform a comparative evaluation of CNN's performance on FPGA and MATLAB for the classification of dysphonic and healthy voice samples.

The remaining portion of the paper presents this work as follows: The methodology is described in Sect. 2. Results and discussions are presented in Sect. 3. Section 4 outlines the work's findings and future scope.

2 Methodology

2.1 *The Proposed Architecture for the Detection of Pathological Voice*

This work focuses mainly on the detection of dysphonia with the help of the CNN algorithm. In Fig. 1, the block diagrams of the proposed methodology are briefly presented.

The brief description of block diagrams shown in Fig. 1 is as under:

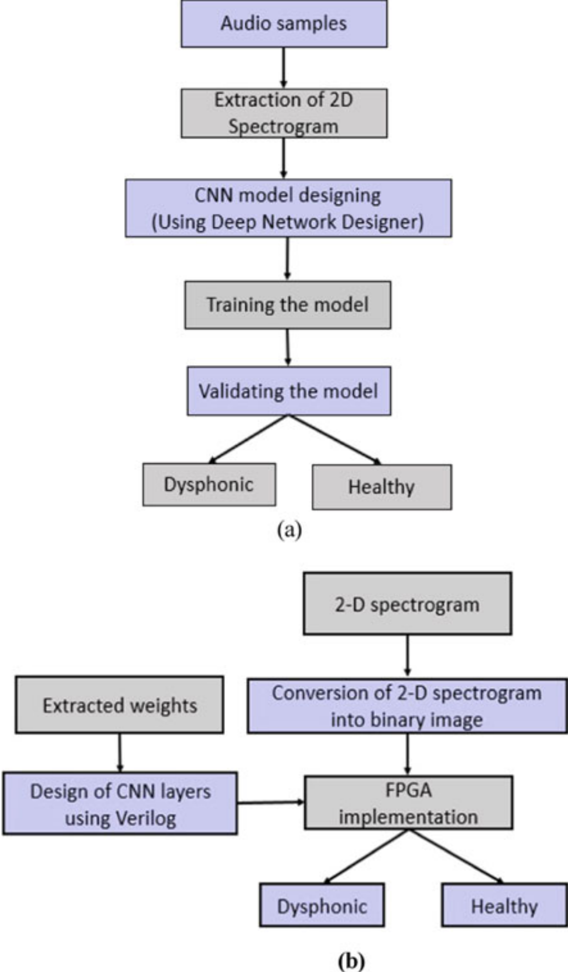

Fig. 1 Block diagrams of proposed methodology **a** MATLAB implementation, **b** FPGA implementation

In order to implement CNN classification network in MATLAB, deep network designer tool has been used. Initially, spectrograms for each audio samples are extracted using MATLAB and given as input to CNN network. Later, this network is trained and validated with available dataset in order to classify dysphonic and healthy audio samples.

In case of FPGA-based implementation of CNN network, spectrogram obtained through MATLAB is converted into binary image and weights are extracted corresponding to each audio sample. Binary image provides matrix corresponding to input spectrogram image. Vivado is used as software development tool to develop the neural network architecture in Verilog. Further, this architecture is implemented on FPGA board in order to classify healthy and dysphonic samples.

2.2 Database

The Saarbruecken voice database collected by the Institute of Phonetics at Saarland University in Germany is utilized in this study. It consists of recordings of 71 different pathologies from over 2000 persons. Each person's recordings contains voices corresponding to sustained vowels /a/, /i/ and /u/ in low, high, low–high-low, and normal pitch. The sustained vowel remains consistent over time and it is easier to spot the changes in it [13]. For our work, we have taken recordings of patients with dysphonia as well as healthy persons. The samples comprise 70 men (30 healthy and 40 dysphonic) aged 16–68 years and 90 women (42 healthy and 48 dysphonic) aged 18–73 years. 80% of data is utilized for training and the remaining 20% for validation.

2.3 Pre-processing of Input Data

CNN has a feature extractor which is generally applied to feature maps. To process the audio recordings through CNN firstly, they need to be converted to two-dimensional Mel-spectrograms from one-dimensional signals. Spectrogram represents the spectrum of recorded audio frequencies over time. Speech signals are initially windowed (window length of 25 ms) after which the frequency components of audio recordings are extracted using the short-time Fourier transform (STFT). Spectrograms have been extracted using Librosa [14]. The obtained image is given as input to the CNN model.

2.4 CNN Architecture

CNN is a multiple-layer deep learning architecture. In each layer, convolution operations are performed for feature extraction. Convolution, activation, pooling, flattening, and fully linked layer are the fundamental layers of CNN model. In convolution, layer filters are applied on input to extract feature maps. After that activation function is applied to convolution layer outputs. This follows a pooling operation such as max-pooling which chooses the highest values from the pixel neighborhood to reduce the network's overall parameters. The output of the pooling layer is sent to flattening layer to obtain a one-dimensional neural architecture which acts as an input for the fully connected layer that classifies the trained neurons in various categories. The CNN model architecture is given in Fig. 2.

The dimensions corresponding to each CNN layer can be given as shown in Eqs. (1)–(5), where rows and columns in the input image are indicated by the symbols x and y, respectively. l and m stand for number of rows and columns in the kernel matrix which corresponds to feature maps in the convolution process.

$$\text{Size of image} = x \times y \tag{1}$$

$$\text{Size of kernel} = l \times m \tag{2}$$

$$\text{Size of Convolutional Layer} = (x - l + 1) \times (y - m + 1) \tag{3}$$

$$\text{Size of Padding Layer} = (x - l + 1 + 2) \times (y - m + 1 + 2) \tag{4}$$

$$\text{Size of Max} - \text{pooling Layer} = \frac{(x - l + 1 + 2)}{2} \times \frac{(y - m + 1 + 2)}{2} \tag{5}$$

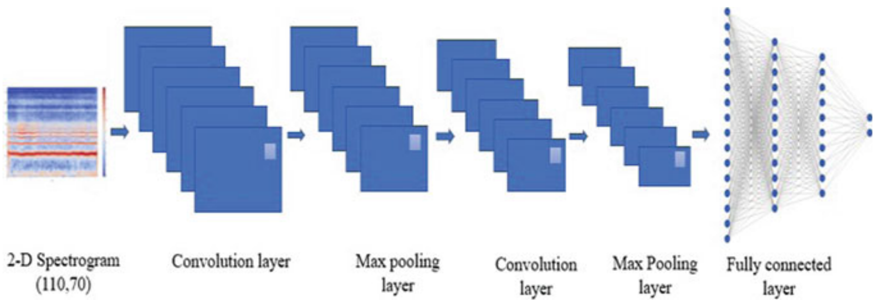

Fig. 2 Detailed architecture of the CNN model. The input for the model is a Mel-spectrogram of size (110, 70) which is obtained from speech recordings

3 Results and Discussion

3.1 MATLAB Implementation

The deep network designer tool is used in MATLAB R2021a to design a CNN classification network. The training and testing phase contains 80% and 20% of data respectively. In this study, the CNN model includes 1 image input layer, and 2 convolution layers with 32 filters each of size 3×3. Each convolution layer follows by a ReLU layer to switch all the negative values to zero and pass on the positive values to the next layer. There are 2 max-pool layers to extract the maximum information from feature maps. Then, we applied one fully connected layer for classification, 1 softmax layer to compute probability distributions of previous layer outputs, and finally a classification layer that estimates cross-entropy loss for classification problems.

For this analysis, MATLAB on Windows PC with Intel Core i7-7500U CPU @2.7 GHz with 8 Gb RAM has been taken. CNN architecture is designed with a validation frequency of 50 iterations, 60 epochs, and a batch size of 60 on a single CPU hardware resource. It resulted in training and validation accuracy of 83.12% and 76.89%, respectively. Further, biases and weights are extracted from this trained model to use on FPGA for hardware design (Fig. 3).

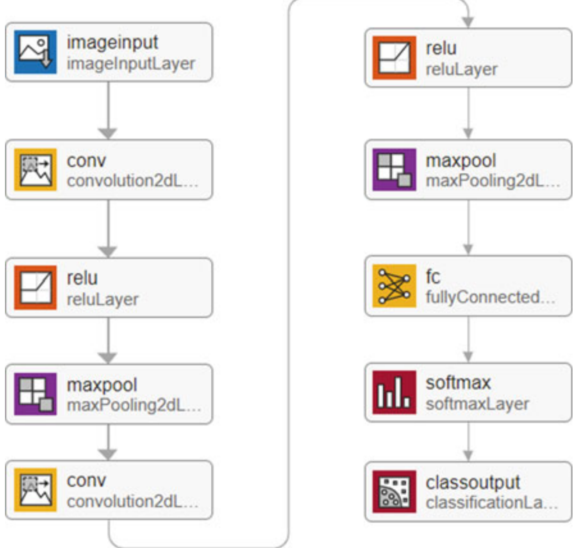

Fig. 3 Proposed CNN architecture in MATLAB

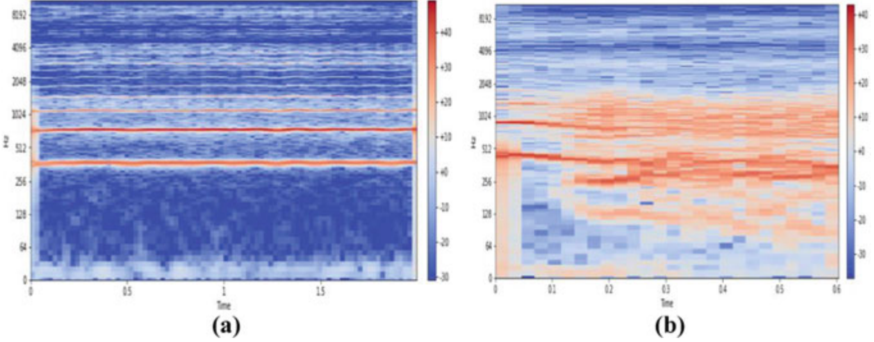

Fig. 4 **a** Example of healthy person's spectrogram, **b** example of dysphonia infected person's spectrogram

3.2 FPGA Simulation and Implementation

Xilinx Vivado tool has been used to implement the proposed CNN architecture on Zynq-7000 FPGA. A total of 88 dysphonic, and 72 healthy images were tested on video simulation. Since for this simulation, the given image is needed to be perceived as matrix, the spectrogram image is initially changed into matrix using a binary image which is extracted from MATLAB code. Later, this matrix is passed to the convolution layer followed by the rest of the CNN layers, i.e., ReLU, max-pooling, flattening, and fully connected layer (Fig. 4).

While testing on FPGA, 134 images out of 160 images have been successfully classified accurately. It was efficient as compared to the accuracy obtained in MATLAB implementation as well as the system performance is accelerated on hardware platform.

4 Conclusion and Future Scope

A technique for recognizing dysphonic voice and distinguishing that from healthy voice has been demonstrated successfully. The difference in hardware and software prototypes has been seen clearly in terms of speed, accuracy, and processing time. The testing accuracy obtained through Xilinx Zynq-7000 FPGA-based model is around 4.86% better than the accuracy obtained in MATLAB. This study finally shows the application of deep learning for detection of dysphonic voice.

For future research work, this system can be extended for a large number of samples as well as for other organic and functional voice disorders. Our purpose is to evolve deep learning methods to acquire better accuracy rates as well as we intend to develop a hybrid system that integrates more datasets and architectures.

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Design and Implementation of an Optimized High-Speed Vedic-Based Squarer Circuit Using Reversible Logic Gates

Saurabh Halder, Mihir Lal Saha, Malvika, Jagritee Talukdar, and Kavicharan Mummaneni

1 Introduction

Vedas are ancient scriptures believed to hold the key to all the knowledge and mysteries known to this world. Vedic mathematics is one such technique derived from the Vedas and presented by Swami B. K Tirtha, who modified the original sixteen sutras in the Vedas on maths in 1965. Vedic mathematics creates a fast and efficient platform to perform mathematical operations, improving computational speed. The handling of auxiliary fractions and recurring decimals by Vedic mathematics has proved to be very fruitful in many engineering applications like FFTs and DFTs. Squarer circuits are the derivative of multiplier circuits. Multiplication operation plays a vital role in many computing devices like microprocessors, microcontrollers, and DSP processors, where performance is measured in the number of multiplications, tasks completed in a given amount of time [1]. Hence, multiplier circuits play a significant role in such circuits. This study mainly emphasis on reversible logic gates. In the case of traditional gates, K × T × ln2 joules of heat is produced for every bit of information loss. Reversible gates lead to reduced power dissipation [2] almost zero information loss, hence reducing heat dissipation, according to a theorem given by Bennett [3]. Along with these advantages, reversible gates can be easily fabricated. Many reversible logic gates exist which are used to increase the quality of the digital circuits in terms of their performance. Nanotechnology, optical computing, quantum dot cellular automata, low power design, and cryptography are

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just a few of the many fields, where reversible logic has many applications. One of the most potential fields for future low-power design proposals is reversible logic. All DSP processors and other portable electronics must minimize power consumption, hence multipliers with fast speeds and low dissipations are essential [4]. The main features of the reversible gate include the count of gates used, the count of the ancilla inputs, and garbage outputs, and most importantly, Total Reversible Logic Implementation Cost (TRLIC), the cost of the quantum circuit for each gate used [5–9]. The proposed design mainly aims to reduce all the parameters mentioned above as compared to the previous works, resulting in the reduction of delay. The paper consists of the following subsections: Sections 1 and 2 comprise the description related to the existing circuit and the proposed design. Section 3 deals with the simulation and the result of the work done throughout this paper. Finally, conclusion follows in Sect. 4.

2 4 × 4 Vedic Squarer Circuit

2.1 Circuit for 2 × 2 Multiplier

The schematic of a 2 × 2 multiplier is illustrated in Fig. 1. The circuit takes two 2-bit binary numbers, i.e., $A = A_1A_0$ and $B = B_1B_0$, as inputs and produces a 4-bit output $Y = Y_3Y_2Y_1Y_0$. It contains two blocks of half adders, where the carry of first half adder block is provided as one of the inputs of second half adder block. The output bit expressions of the 2 × 2 multiplier circuit are given as follows:

Let

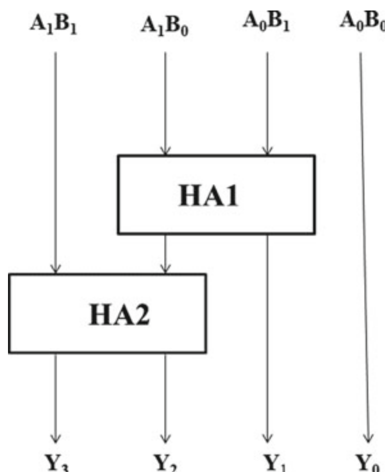


Fig. 1 Schematic of 2 × 2 multiplier circuit

$$C = (A_1.B_0).(A_0.B_1)$$
$$Y_3 = C.(A_1.B_0)$$
$$Y_2 = C \oplus (A_1.B_1)$$
$$Y_1 = (A_1.B_0) \oplus (A_0.B_1)$$
$$Y_0 = (A_0.B_0)$$

2.2 Circuit for 2-Bit Modified Squarer

Figure 2 illustrates the circuit diagram of a two-bit modified squarer. A two-bit modified squarer circuit is derived from a squarer circuit of two bits, which itself is derived from the 2 × 2 multiplier circuit having same two input numbers. The only modification in the 2-bit modified squarer circuit is that the half adder block in the two-bit squarer circuit is replaced by a combination of NOT and AND gates, keeping the output expressions the same.

The modified squarer takes a two-bit binary number $A = A_1A_0$, as input and outputs a four-bit binary number, $Y = Y_3Y_2Y_1Y_0$. The output bits of the circuit have the following relations with the input:

$$Y_3 = (A_1.A_0)$$
$$Y_2 = (A_1.A_0\prime)$$
$$Y_1 = 0$$
$$Y_0 = A_0$$

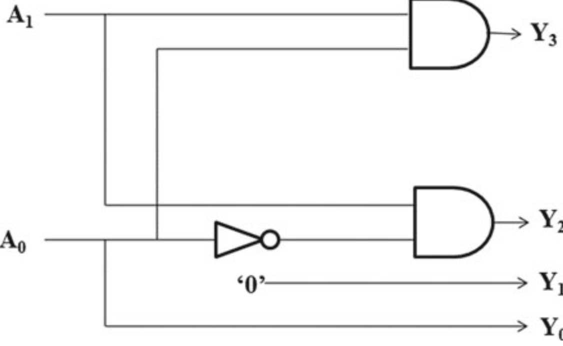


Fig. 2 Circuit diagram of 2-bit modified squarer circuit

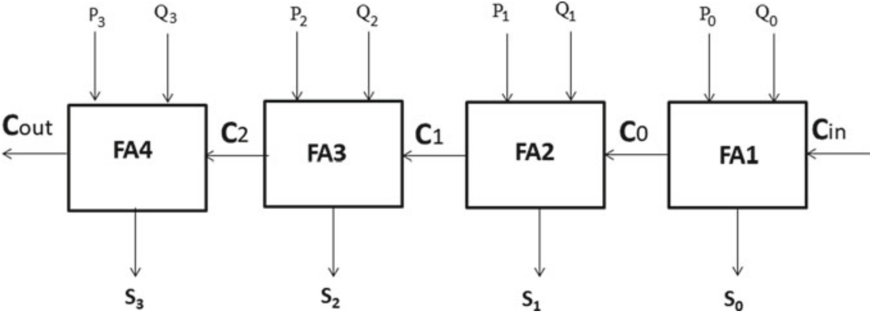


Fig. 3 Schematic of ripple carry adder of four bits

2.3 Circuit for Four-Bit Ripple Carry Adder (RCA)

The block diagram [10] of a four-bit RCA is illustrated in Fig. 3. It consists of four full adders. Two numbers of four bit, $P = P_3P_2P_1P_0$ and $Q = Q_3Q_2Q_1Q_0$ as well as an input carry C_{in}, are taken as the input to the RCA circuit. The output of the circuit is given by $S = S_3S_2S_1S_0$, which gives the sum, along with C_{out}, which gives the output carry. A full adder's output carry is used as the input carry for the next most significant full adder.

The initial input C_{in} is given to the full adder, where the LSBs of the two input numbers are fed. The final output carry C_{out} is taken out from the full adder, where the MSBs of the two input numbers are fed.

2.4 Circuit for 4 × 4 Vedic-Based Squarer

Figure 4 depicts the illustration of a 4 × 4 Vedic-based squarer circuit [11]. The circuit consists of two 2 × 2 modified squarer circuits, one 2 × 2 binary multiplier circuit, one RCA of four bits, one OR gate, and one 2-bit IBO circuit. A four-bit binary number $I = I_3I_2I_1I_0$ is taken as the input twice and an eight-bit output of $Y = Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$ is generated. The following steps are involved in squaring a four-bit number.

The first and the third part (squarer block) of Fig. 4 is computed using the modified circuit discussed in Sect. 2.2. The second part (multiplier block) is computed using the multiplier circuit discussed in Sect. 2.1.

	$I_3I_2I_1I_0$ $\times I_3I_2I_1I_0$	
$(I_3I_2) \times (I_3I_2)$	$(I_3I_2) \times (I_1I_0)$ $(I_3I_2) \times (I_1I_0)$	$(I_1I_0) \times (I_1I_0)$

(continued)

(continued)

Part I	Part II	Part III

The four-bit RCA's C_{out}, and the most significant bit of the two-bit multiplier circuit, W_1 [3] is used as the input of OR gate in Fig. 4. When either C_{out} or W_1 [3] is high, or both are high, the OR gate provides a logic 1 output. The output port of OR gate serves as the enable input En to the 2-bit IBO circuit. The IBO circuit performs its operation only when the En is high; otherwise, it just duplicates the output bits as the input bits.

2.5 *Proposed 4 × 4 Vedic Based Squarer Using Reversible Logic*

For the proposed 4 × 4 Vedic squarer circuit, each block of the existing design has been replaced by an equivalent combination of reversible logic gates. In the upcoming sections, the illustrations of the proposed design are shown, where all the individual blocks are replaced by a combination of reversible gates.

2.5.1 2 × 2 Modified Squarer Circuit Using Reversible Logic

As seen in Fig. 5, a single Fredkin gate is sufficient for the implementation of the modified 2-bit squarer circuit. $P = A_0$, $Q = A_1$ and $R = 0$ are the inputs to the Fredkin gate. $X = M_0$, $Y = M_2$ and $Z = M_3$ are the output port's mappings. The second output bit of the multiplier circuit is always equal to '0'. The total quantum cost of this whole circuit is 5.

2.5.2 2 × 2 Reversible Logic Multiplier Circuit

A combination of two BME gates and two Peres gates is deployed to implement a 2-bit multiplier circuit. The inputs and the outputs of the different gates can be seen in Fig. 6, where Y_3, Y_2, Y_1, and Y_0 are the output bits of the multiplier circuit. This circuit's total quantum cost is 18.

2.5.3 Combined 2-bit IBO and OR Gate Using Reversible Logic

With the help of reversible logic gates, the OR gate and the 2-bit IBO circuit from the previous designs have been integrated to generate the circuit as depicted in Fig. 7, where the individual gate's inputs and outputs may be seen. The combination requires two Fredkin gates and one Peres gate, resulting in an overall quantum cost of 14.

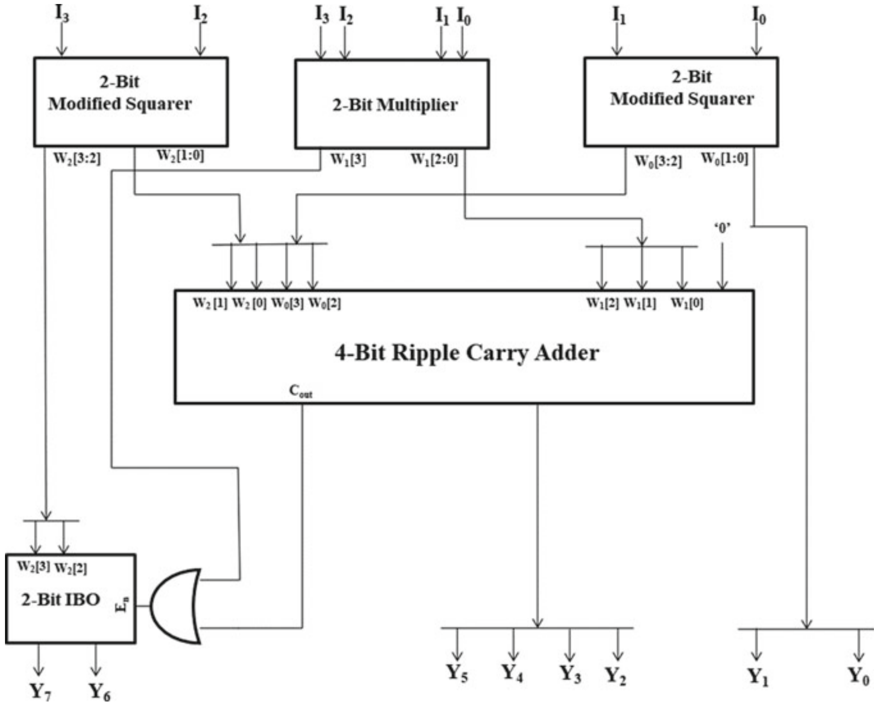


Fig. 4 Schematic of existing 4 × 4 Vedic-based squarer

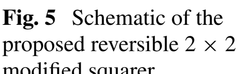
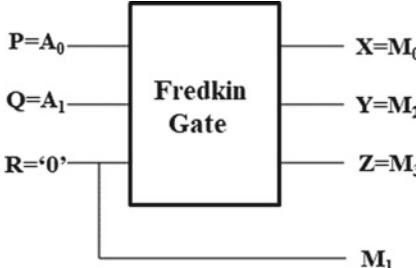


Fig. 5 Schematic of the proposed reversible 2 × 2 modified squarer



2.5.4 Circuit for Four-Bit Ripple Carry Adder (RCA) Using Reversible Logic

A total of four HNG gates are employed to implement the four-bit RCA. A single HNG gate can function as a complete full adder only when the inputs are equal to A, B, C_{in}, and 0, respectively, where A and B are the two numbers to be added. The output obtained is $P = A$, $Q = C_{in}$, $R =$ Sum, and $S = C_{out}$. The respective input and outputs of the ripple carry adder are depicted in Fig. 8. The constructed circuit has a total quantum cost of 24.

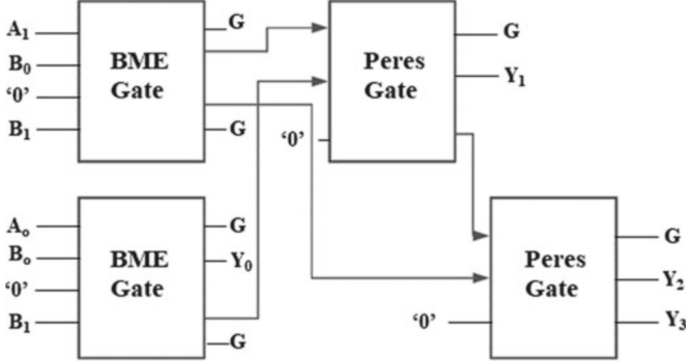


Fig. 6 Schematic of the proposed 2 × 2 reversible multiplier circuit

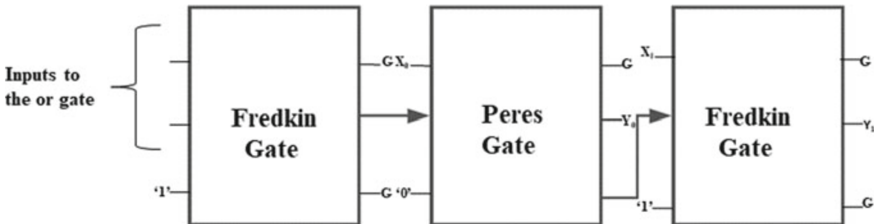


Fig. 7 Block diagram of the proposed OR gate combined with 2-bit IBO circuit using reversible logic gate

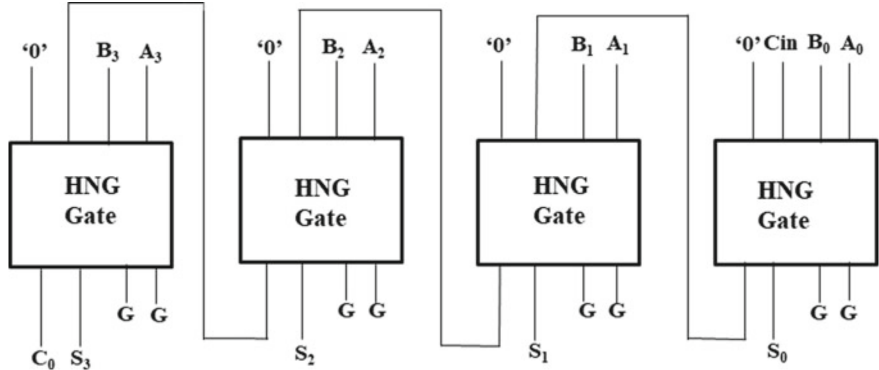


Fig. 8 Schematic of the proposed ripple carry adder of four bits using reversible logic gate

3 Simulation and Results

This section displays the simulated outcomes of the proposed 4 × 4 Vedic squarer circuit using reversible logic gates. The simulations are performed using the iSim simulator in Xilinx ISE. In addition, the implementation and synthesis of the proposed design have been executed on different FPGAs available on Xilinx ISE to analyze the delay. Figures 9 and 10 depict the generated output waveforms of the suggested circuit. The four-bit input is represented by $I = I_3I_2I_1I_0$, and the eight-bit output is represented by $Y = Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$.

$$\text{For I} = 4'\text{b0111},\ \text{output } Y = 8'\text{b00110001}$$
$$\text{For I} = 4'b1111, \text{output} Y = 8'b11100001$$

It is to be noted that, 4-bit multiplier circuits [12–14] are considered for comparison with the proposed design, assuming that both the multiplier circuit's input numbers are kept at the same value, in order to achieve the same function as the squaring circuit.

From Table 1, it can be perceived that, the proposed circuit has been designed by employing only 15 reversible gates which is having 13 ancillary inputs, 19 garbage outputs, and a quantum cost of 66. A maximum of 75.16% improvement and a minimum of 50% improvement is obtained, in relation to the other existing designs, for the proposed work.

Table 2 compares the suggested architecture with the existing designs in terms of the delay (ns) for different FPGAs available on Xilinx ISE. The various FPGAs considered for the comparison are Virtex-4(XC4VSX35), Spartan-3(XC3S50), and Spartan-6(XC6SLX150T). The delay of the proposed work is improved by 2.4, 2.1 and 2.7% for FPGAs Virtex-4(XC4VSX35), Spartan-3(XC3S50), and Spartan-6(XC6SLX150T), respectively, as compared to [11].

In Table 3, the comparison for the amount of utilized FPGA hardware has been shown, keeping number of slices and LUTs used as parameter.

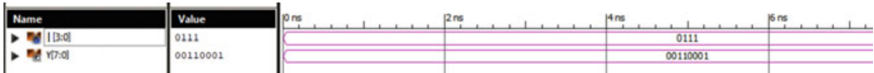


Fig. 9 Simulated output waveform of 4 × 4 Vedic-based squarer using reversible logic gates with binary 0111 as input

Fig. 10 Simulated output waveform of 4 × 4 Vedic-based squarer using reversible logic gates with binary 1111 as input

Table 1 Comparison of different adders on the basis of various parameters

Parameter	Gate count	Ancilla input	Garbage output	Quantum Cost	TRLIC	% Improvement (%)
Proposed work	15	13	19	66	113	–
[12]	31	23	42	130	226	50
[8]	37	29	62	162	290	61
[13]	53	58	58	286	455	75.16
[14]	52	56	56	244	408	72.3
[13]	64	55	56	236	411	72.5

Table 2 Comparison of delays using different FPGAs

FPGA	Proposed work (ns)	[11] (ns)	% Improvement (%)
Virtex-4: XC4VSX35	4.873	4.993	2.4
Spartan-3: XC3S50	7.694	7.862	2.1
Spartan-6: XC6SLX150T	5.389	5.54	2.7

Table 3 Utilized FPGA hardware

Parameter	[12]	[15]	Proposed work
No. of slices used	12	32	10
No. of LUTs used	20	17	17

Table 4 Power comparison for various multipliers

Parameter	[16]	Proposed work
Power (mW)	0.397	0.115

Table 4 compares the amount of power dissipated (in mW), with the analysis done in cadence genus using TSMC 65 nm technology. An improvement of around 71% can be observed between the suggested design and the earlier works.

4 Conclusion

The work presents the implementation of a 4 × 4 Vedic-based squarer circuit using reversible logic gates. When compared to the other existing squarer and multiplier (with both inputs similar) designs, in terms of gate count, ancilla inputs, garbage

outputs, quantum cost, and TRLIC, the suggested design performs better. The performance parameter TRLIC is significantly improved by 75.16%. Moreover, the latency or delay of any quantum circuit is directly influenced by the quantum cost. The proposed architecture significantly lowers the quantum cost and which shows an improvement in the delay of around 2.7% when compared to the counterparts, and hence suitable for high-speed applications. Applications of Vedic multiplier include hardware image processing, digital signal processing, and in FIR architectures [17].

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Low-Power LNA in Analog Front End for Biomedical Applications

Pritty and Mansi Jhamb

1 Introduction

Nowadays, electronics devices are an essential requirement in healthcare systems. Biomedical applications such as a pacemaker, hearing aid, analog cochlear process, neural recording, body area monitoring, and retinal stimulator have adapted [1–3]. The heart component of these devices includes communication subsystems, signal processing, data conversion, sensor, and actuator for interaction with the biomedical environment [4–7]. Also, the battery system has supplied power for the electronics system. Monitoring and diagnosis devices include integrated biomedical sensors [8, 9]. Wireless sensors/IoT transceivers have operated to enhance communication and improve data rates [10]. Figure 1 shows the LNA in different biomedical applications. Low-noise amplifiers (LNAs) have widely used for biomedical applications. Nowadays, tunable feedback capacitors [11], resistor-plus-source-follower [12], triple-coupled techniques [13], gain enhancement techniques [14], active matching components [15, 16], variable gain techniques [17], triple cascode methods [18, 19], bulk CMOS[20], noise canceling/control circuit [21, 22], pseudo-resistor [23], Si-Ge Bi-CMOS[24], tapered distributed [25], and SOI technology [26], K/Ka-Band LNA [27],

Inductor-less LNA [31] and sub-GHz wideband LNA [32–38] have utilized for the schematic of LNA circuits. Analog front end can design with LNA for ECG monitoring and neural recording [39, 28, 40, 41 and 42]. In [15], the operating frequency of LNA has slightly decreased due to parasitic active components. Active

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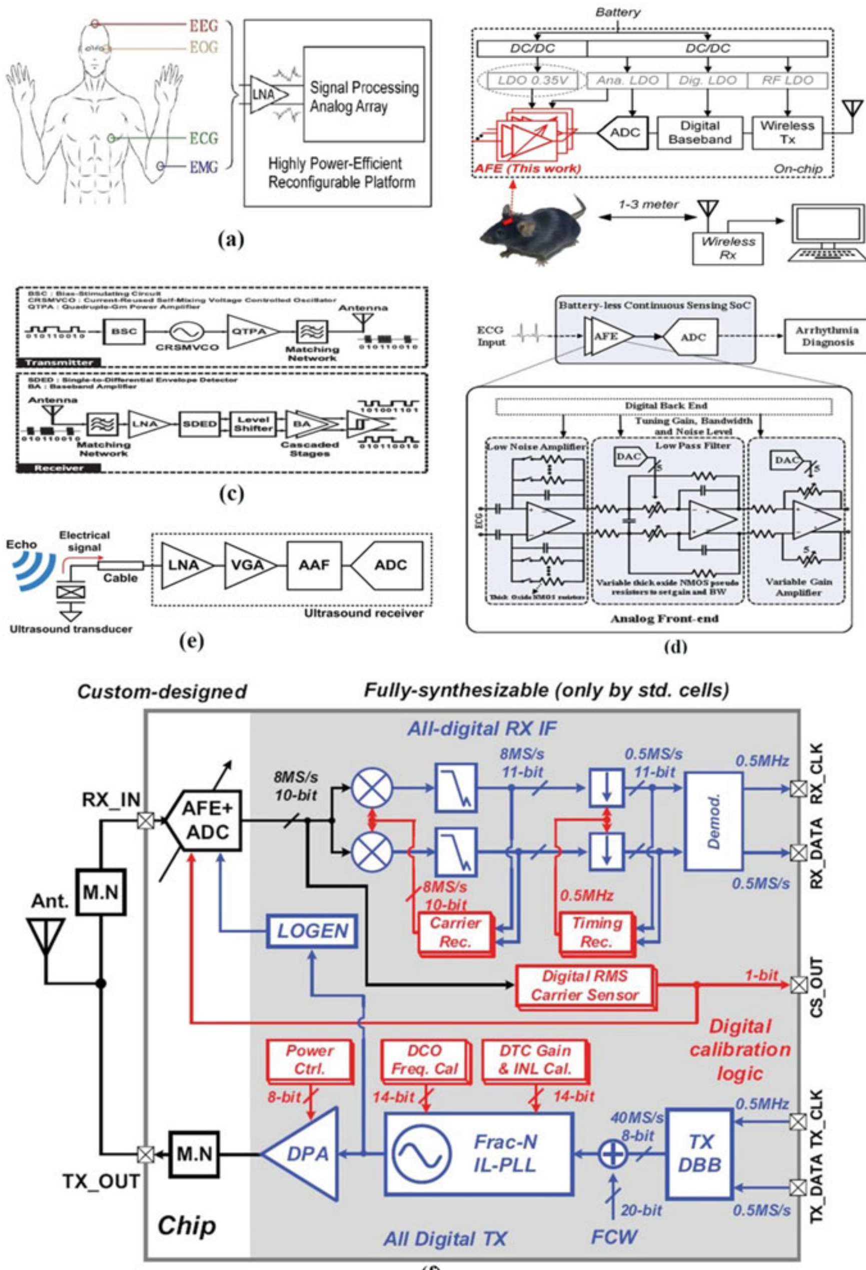


Fig. 1 Different applications of LNA or AFE are **a** bio-potential sensor [8]; **b** wireless neural recording system [28]; **c** biomedical implantable transceiver [29]; **d** ECG monitoring biosensor [3]; **e** ultrasound receiver [21]; **f** IoT transceiver [30]

balun in LNA [17] enhanced the performance compared to the active inductor of LNAs [15, 16]. The figure of merit (FOM) and power has increased due to the triple cascode of LNA [18]. The LNA has out-of-band interference due to a non-specified filter [20]. LNA is a desirable component for ultrasound receivers [21] and IoT transceiver [30] due to its low power and low noise using a noise floor. This manuscript has arranged as follows: an introduction has presented in Sect. 1. Section 2 and Sect. 3 depict the literature on LNA designs and their applications. The result and discussion of this work have shown in Sect. 4 and the conclusion in Sect. 5.

2 Low-Noise Amplifier Topologies

2.1 Variable Gain LNA

In LNA, the input impedance matching network has created capacitors (C_F, C_G), inductors (L_S, L_G), transistors (M_2 and M_1), and (R_G) a resistor. The power dissipation has been minimized with smaller W/L ratios of $M_1 - M_2$ and resulted in a smaller chip area. Gain has improved with the M_3 current reuse technique. The threshold voltage (V_T) across transistors has decreased due to the body biasing in LNA. It provides more flexibility on the circuit.

The drain-source voltage (V_{ds}) of transistors has an induced body effect in Fig. 2a. M_4's gate terminal has managed by V_{B2}; the path of C_B, M_4 forms the negative-feedback variable capacitor. Transistors (M_2, M_1) have introduced multi-gate topology; operate in sub-threshold and saturation regions, respectively. These transistors share (L_S) inductors for a minimal chip area.

2.2 Resistor-Plus-SFF LNA

Voltages V_{bf} and V_{b3} have biased the transistors $M_f - M_{3,}$ and capacitors C_{i2} and C_{i1} have utilized for DC-decoupling. Off-chip bias-T feeds the gate bias (V_{b1}) of M_1 and M_2. V_{DD} to V_{b1} has flow the DC-current of M_f and output matching measured by the common-source output buffer in Fig. 2b. The drain of the buffer transistor is series connected to the inductor $L_{B,}$ and bandwidth has affected due to load capacitance.

2.3 High-Gain LNA with Triple-Coupled Technique

High-gain LNA with triple couple technique has formed using transistors, passive components, and triple-coupled transformers. The cascode configuration has

designed with triple-coupled transformer TF_2. The high-order network between M_4 and M_3 has created using parasitic capacitances, TF_2, and leads to extended operational bandwidth. A large capacitance at the output side has resonated due to inductor L_7 in Fig. 2c. Another resonant network has formed using parasitic capacitors C_{pad} (layout-dependent), C_5, and inductors L_7 and L_8 within the desired frequency range. LNA has increased the bandwidth of output impedance matching.

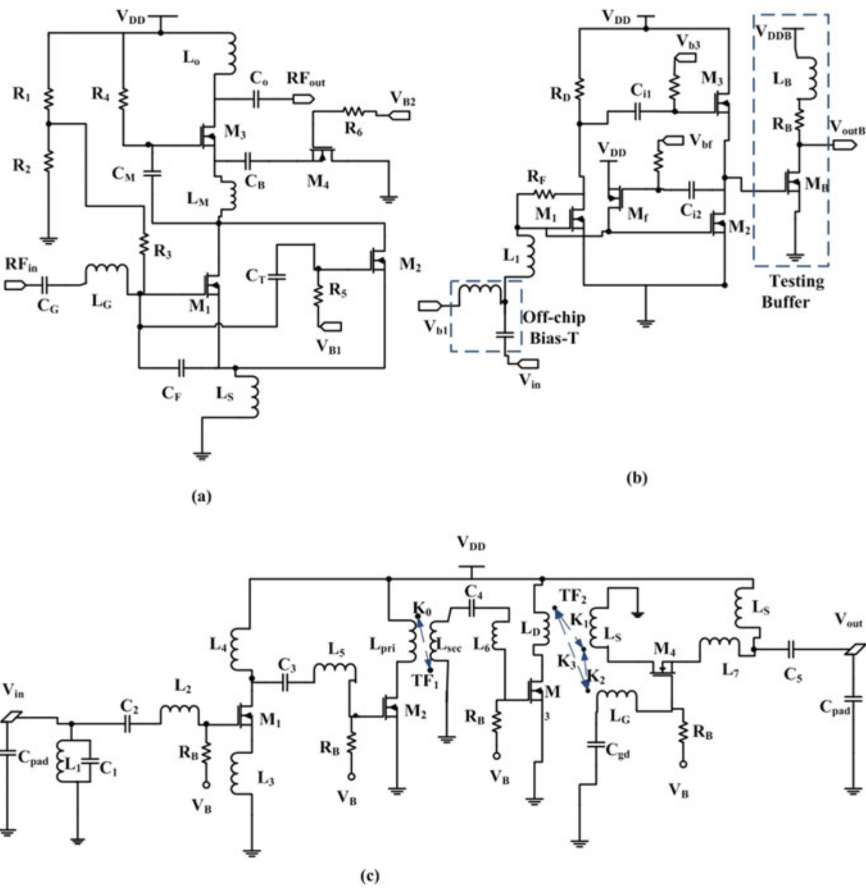


Fig. 2 LNA designs **a** variable gain LNA[11], **b** resistor-plus-SFF LNA [12], **c** high-gain LNA with triple-coupled technique [13], **d** high-gain wideband LNA [14], **e** LNA using active inductor [15], **f** triple LNA with boosted gain [18]

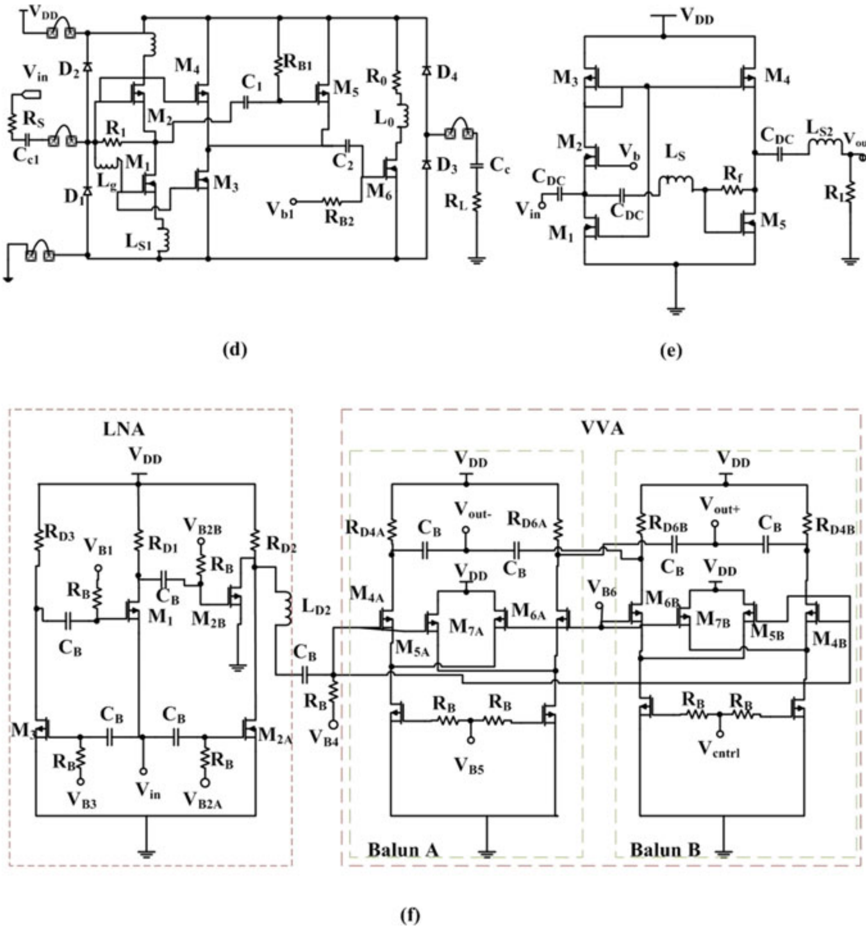


Fig. 2 (continued)

2.4 High-Gain Eideband LNA

Feed-forward noise cancelation method, gate-source inductors (L_{s1}, L_{s2}, L_g), and broad bandwidth matching technique have used for high-gain wideband LNA design in Fig. 2d. The chip area and complexity have reduced in this LNA due to feedback resistor R_f which gives bias voltage to MOSFETs $M_1 - M_4$. A resistor R_{B1} connects the V_{DD} supply voltage to the gate of M_5. The core structure of LNA has integrated with a common-source (CS) shunt inductor buffer and provides gain flatness, high gain, and output matching over a wide range.

2.5 LNA Using Active Inductor

Wideband flat gain LNA has composed of two parts. The input active inductor formed with transistors $M_1 - M_3$, and the noise cancelation part had designed using $M_4 - M_5$ transistors. The current reuse technique has adopted for the reduction of power consumption.

In Fig. 2e, the inductors L_{S1} and L_{S2} have additionally included for extended gain-bandwidth. Load for wideband flat gain LNA is a resistor (50-Ω). LNA using an active inductor (AI) can design using the derivative superposition (DS) method and AI-based bandwidth expansion method, capacitor cross-coupling, and CG stage [16]. Main gain MOSFETs (M_1 and M_2) work in the saturation region. M_3 and M_4 work in sub-threshold mode, and they cancel out the poor linearity of M_1 and M_2. The DS technique has minimum power dissipation. R_B bias resistor has wired to $M_1 - M_4$ gate terminals.

2.6 Triple Cascode LNA with Boosted Gain

Triple cascode LNA with a boosted gain is a combination of inductive triple cascode, common-emitter (CE) stage Q_1, common-base (CB) Q_3, and Q_2 stage in Fig. 2f. Few techniques have used; it improves gain, noise figure (NF), linearity, stability, minimal power, better performance, and functionalities. The low W/L ratio of Q_2 has required a minimum value of L_b. Q_1 drives the collector current of Q_2 and increases the NF of Q_2. L_b has set to 150 pH value, which impacts the noise performance of LNA. An additional method has utilized P1dB enhancement for best operation and power handling capability.

2.7 OTA-Based LNA

Capacitor-coupled closed-loop LNA has designed with the implementation of an operational trans-conductance amplifier (OTA) in Fig. 3a, b. The folded-cascade topology, differential-difference amplifier (DDA), and the current reusing technique have utilized for the OTA. It leads to low-power consumption and noise. This design had two stages, input stages ($M_0 - M_6$) for twice trans-conductance and output stage ($M_8 - M_{13}$) for increasing output resistance. The bias for M_5 has provided by DDA. DDA has designed with common-mode feedback (CMFB). Poor linearity OTA's has appropriate for LNA with low output amplitude. DDA evades the decrease of gain in the OTA circuit. LNA has achieved high PSRR and improved loop stability. Inputs of PMOS and NMOS had connected to feedback networks and DC bias voltages separately. The V_{bp} and V_{bn} voltages have used for biasing positive and negative input voltages of PMOS and NMOS transistors. The diode PMOS pseudo-resistors

have utilized for the LNA design of R_{0p} and R_{0n}. LNA has a 3% increase in power, and it had more efficient in power dissipation than conventional low drop-out regulators (LDO).

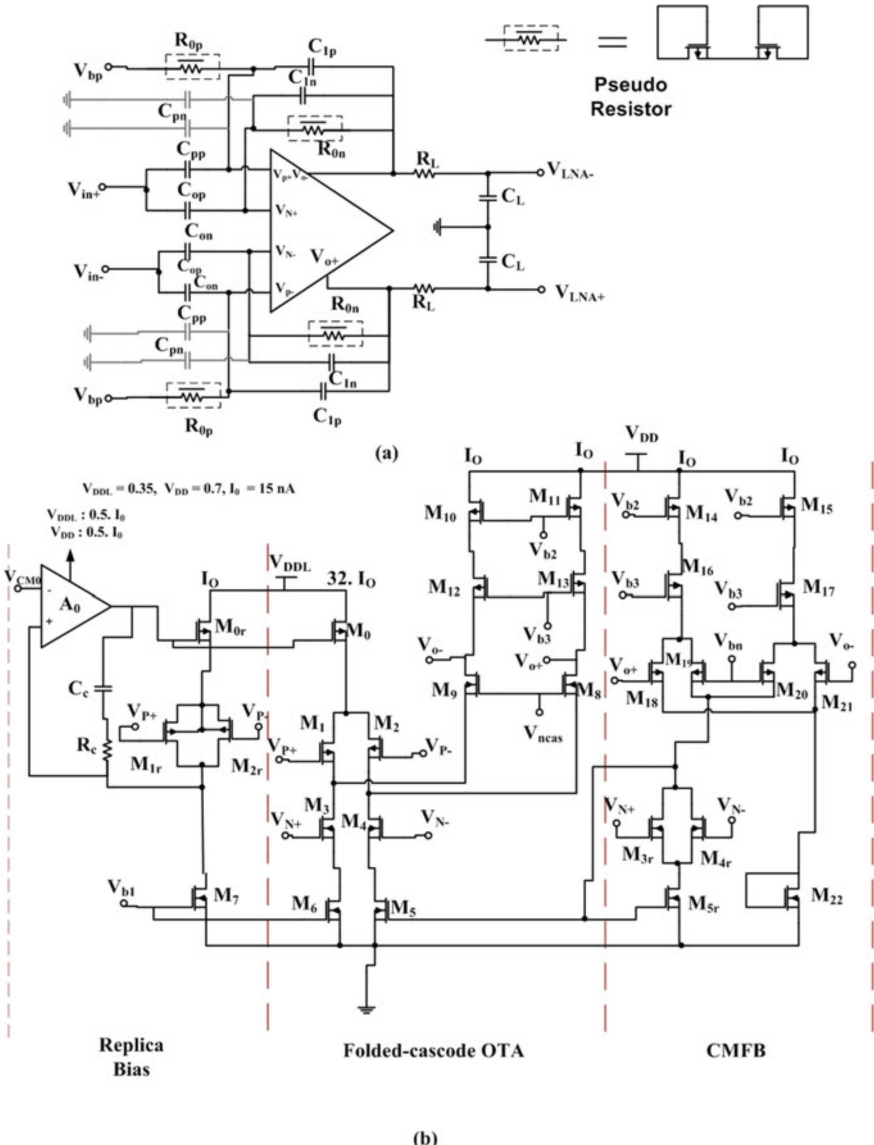


Fig. 3 LNA designs **a** block design and **b** OTA circuit of OTA-based LNA [28]; **c** attenuation-adaptive noise control circuit (AANC) and **d** core amplifier of low-power LNA using AANC [21]; **e** low-power LNA using AANC [21]

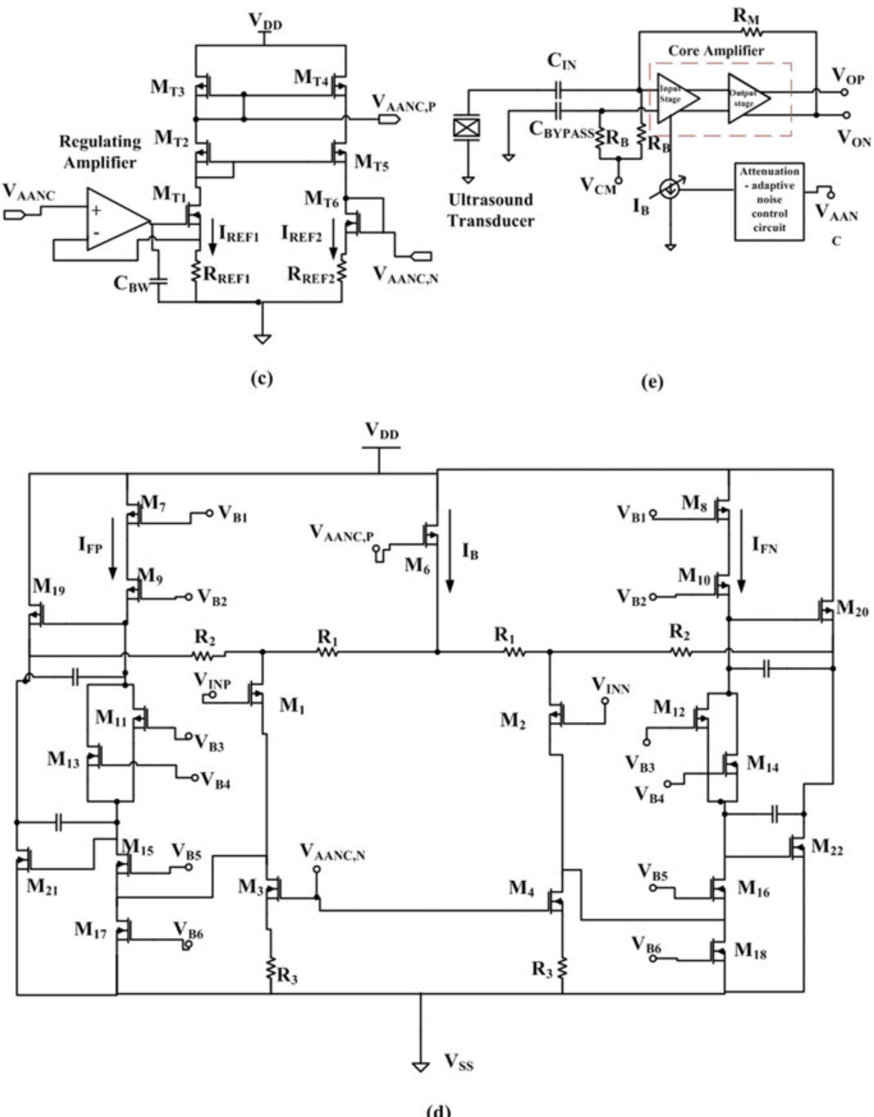


Fig. 3 (continued)

2.8 Low-Power LNA Using AANC

This LNA consists of attenuation-adaptive noise control (AANC) circuit, core amplifier, and passive components in Fig. 3d, e. Current feedback topology has used for a schematic of the core amplifier. Source degeneration ($R_1 - R_3$, $M_1 - M_5$) has helped with the core amplifier's input stage. The output of AANC has maintained

due to I_B current source, R_2, and R_1 finds the gain of LNA. It leads to high linearity, low variation in gain value, and trans-conductance. So, input transistors have formed by PMOS transistors. Current source degeneration resistor R_3 has decreased noise and reduced trans-conductance of M_3 and M_4 (high W/L ratios). Small R_1 and high current values in LNA reduce the noise of M_1 and R_1. IB has controlled due to the AANC circuit. The current ratio (I_{REF2}/I_B) has matched by resistor R_{REF2}. Cross-talk occurs due to mismatches between $R_{3.N}$, $R_{3.P}$, and M_3, M_4. The AANC circuit induced ΔI current and ΔI amplified by the core amplifier. The core amplifier has a high bandwidth value, and the bandwidth in the AANC circuit decreased with the addition of CBW. Regulating amplifiers in the AANC circuit has determined the dominant pole of the AANC design.

2.9 Multi-stage LNA

Multi-stage LNA had usually designed using two stages [1, 4, 22].

In [1], LNA has formed using capacitive feedback, current reuse complementary input (CRCI) technique, pseudo-resistor for the first stage, and capacitive feedback, OTA for the second stage. Figure 4a–d shows the multi-stage LNAs. The first stage of LNA serves as a buffer to drive the load provided by the second stage and inter-stage matching network [4]. The second stage of LNA has formed with source degeneration and parasitic components in [4]. LNA has designed with CG-CS stages and current reuse technique in the sub-threshold region [22].

2.10 Resistive Feedback LNA

Resistive feedback can use for the design of LNA [23, 43, 44]. The trans-conductance boosting, current reuse techniques, and resistive feedback have combined for LNA [43]. High-gain, low-power consumption, low NF, and better performance have provided LNA with a resistive network compared to other LNAs. In [23], LNA has formed with forward body bias and intrinsic self-balanced MOS diode (SMBD) for saving power dissipation and minimal leakage current. Figure 4e, f depicts the resistive feedback LNAs. Modified resistive feedback techniques have also used for LNA [44].

3 Low-Noise Amplifier Application: Analog Front End

Analog baseband is one of the high-power dissipation blocks in transceivers. Analog front end (AFE) and digital baseband are two main parts of the IoT transceiver. The AFE has designed using LNA, mixer, band pass filter (BPF), and variable gain

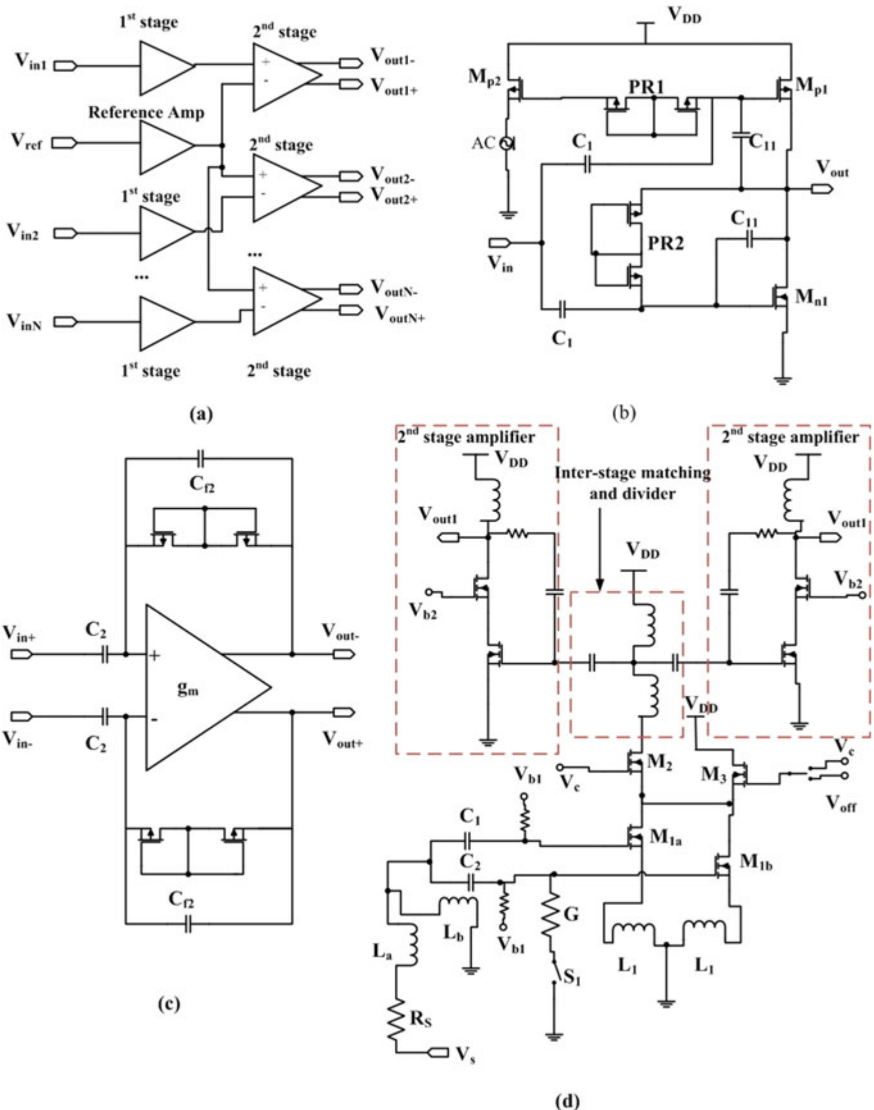


Fig. 4 LNA designs **a** block design, **b** first stage, and **c** second stage of multi-stage LNA [1]; **d** multi-stage LNA using inter-stage matching divider [4]; **e** resistive feedback LNA using double cross-coupling and tank [23]; **f** resistive feedback LNA [43]

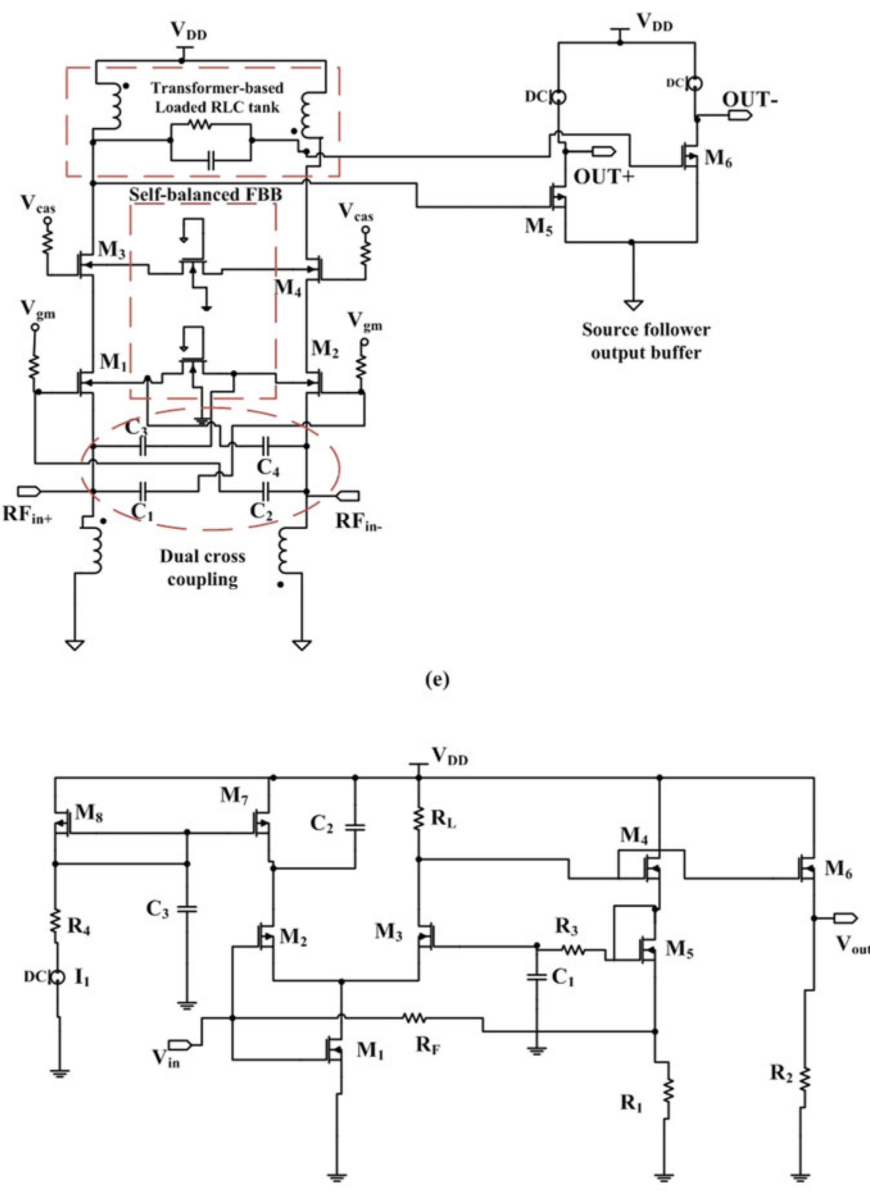


Fig. 4 (continued)

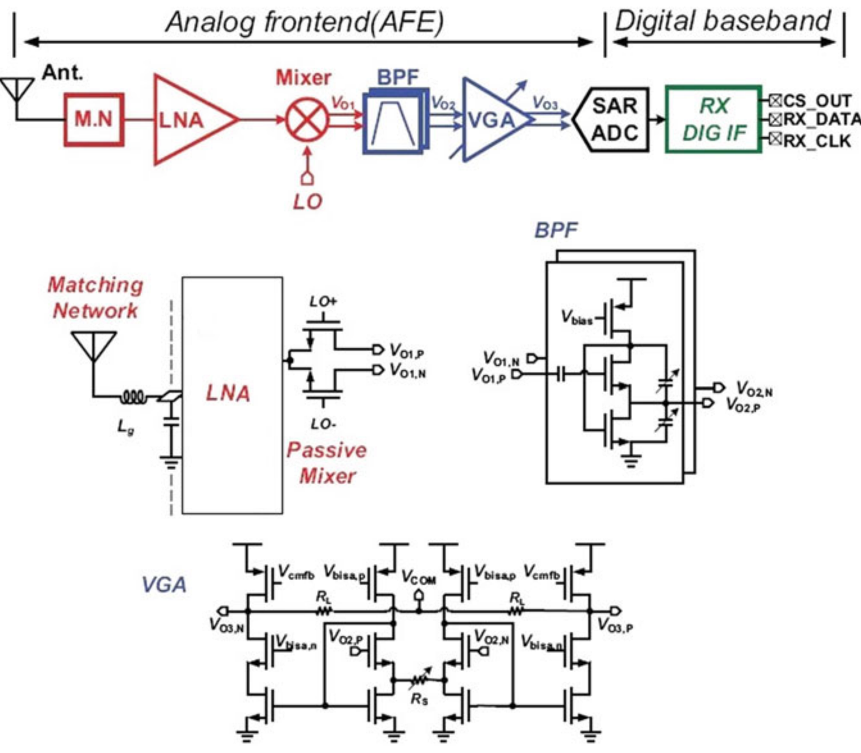


Fig. 5 AFE's block diagram; circuits of mixer, band pass filer (BPF), and variable gain amplifier (VGA)

amplifier (VGA) (Refer Fig. 5). Simulation has performed using different LNA one by one. A low-noise amplifier has amplified the input signal, and the mixer performs the up-to-down conversion.

The mixer output signal has centered at 1 MHz for minimum flicker noise. BPF has filtered the mixer output signal and amplitude controlled using the VGA. Flip-voltage followers (FVFs) have employed by VGA and BPF because of their best linearity and robust PVT variations. In digital baseband, ADC helps convert analog signal to a digital signal for further processing on this signal.

4 Result and Discussion

All LNA and AFE circuits have simulated using a specter simulator of MOS technology (Cadence Virtuoso). Figure 6 shows the power gain, S21, and S11 waveforms of LNAs. Though the cause of comparison and comprehensive comparative results of various LNA topologies have presented in Tables 1, 2 and 3, significant emphasis

is set on the “inductor-less approach” as this approach claims several benefits in IC design. The layout of inductor-less LNA designs has shown in Fig. 7. LNAs have simulated at a voltage range of 0.35–3.3 V and 180 nm, 90, and 65 nm technology with spice software. Tables 1, 2, and 3 have depicted the comparison of different LNAs based on parameters (such as power, gain, and noise figure (NF)) at 180, 90, and 65 nm MOS technology, respectively. The LNA in [14] has consumed 29 mW powers in three modules, 32 mW in [13], and 11.3 mW in [24] from Table 3. When comparing minimum and maximum power dissipation between Tables 1, 2, and 3, then power saving of 10+ times than [39], 90% less power consumption than [44], and 99% less power consumption than [13]. In [28], minimum power has consumed at 65 nm technology compared to [13, 14, 24]. Similarly, LNAs had low-power dissipation of 0.6 mW in [11] at 180 nm and 2.5 mW in [45] at 90 nm compared to other LNAs at respective technologies. Total power consumption has increased with lower nm technology. In [14], the highest gain (20.8 dB) has achieved by module-I mentioned in Table 3. The minimum noise figure values are 2.5 dB in Table 1, 1.5 dB in Table 2 and 2 dB in Table 3 compared to other state-of-art LNA designs. In [14], LNA has obtained NF 2 dB at 2 GHz, 2.5 dB at 3.5 GHz, and 37% minimum compared to other LNAs in Table 3. There are 40% fewer NF as compared to the latest LNA designs. The maximum bandwidth of 20 GHz measured in [13] and minimum bandwidths of 0.49 kHz have obtained in [1]. In Table 2, 97% saving of area has measured in [45] compared to [46]. In Table 3, a 75% lower chip area required [14] than state-of-the-art LNAs [13, 28, 24]. Minimum gain values are 4 dB in Table 1, 10 dB in Table 2, and 16.8 in Table 3. The 16.9 dB, 58.7 dB, and 54 dB maximal gain values had obtained in Tables 1, 2 and 3, respectively. The gain value has increased optimized with lower nm technologies [47, 48].

In [28], minimum power has consumed at 65 nm technology compared to [13, 14, 24]. LNAs had low-power dissipation of 0.6 mW in [11] at 180 nm and 2.5 mW in [45] at 90 nm compared to other LNAs at respective technologies as shown in Fig. 8. Total power consumption has increased with lower nm technology. In [14], the

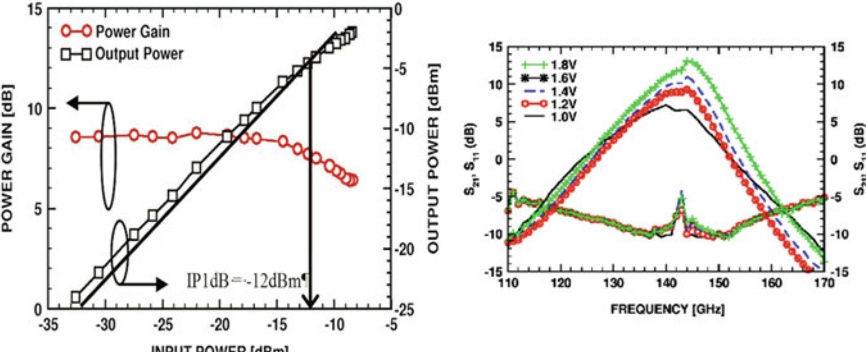


Fig. 6 Power gain and S-parameters of LNAs

Table 1 Comparison table for LNAs at 180 nm

	[4]	[22]	[23]	[16]	[39]	[21]	[11]
Power (mW)	–	1.8	1.68	9.5	10.44		0.6
Frequency (GHz)	10	3	5	0.1–1.45	–	0.033	2.8
Gain (dB)	13.6	13	14.1	16.9	–	19.1	4–10
Supply voltage (V)	3.3	1.8	0.6	1.8	1.8	1.8	0.6
NF (dB)	4.7	6–8	3.65	2.5	4.83	3.69	4
IIP3 (dBm)	9.5	– 9.5	–17.1	5.5	–	–	0
Technique/ components used	Source degeneration and gain switching	CG, CS stages current reused, gain boosting	Pseudo-resistor, forward body biasing	Differential active inductor, CG stage	Capacitive coupled, pseudo-differential	Core amplifier, AANC circuit	Current reuse, forward body biasing, multi-gate topology

Table 2 Comparison table for LNAs at 90 nm

	[45]	[43]	[44]	[46]	[49]	[1]	[50]
Power (mW)	2.5	9.2	25	16	18		1.2
Bandwidth (Hz)	0.01–2.2 G	6 G	0.2–3.2 G	0.1–8 G	0.02–1.1 G	0.49–10.5 k	0.05–0.8
Gain (dB)	10–50	21	15.5	16	15.5	58.7	21.3
Supply voltage (V)	1.2	1.4	1.2	1.4	1.2	1	
|NF| (dB)	17	2	9	9	1.5	1.93	4.5
|IIP3| (dBm)	−3.4	−2.9	1.76–4.5	3.4–5.8	1.43–1.9		7.1
Area (mm^2)	0.01	–	0.134	0.34	0.06	0.137	0.075
Technique/ components used	Multiple stages, phase cancelation		Differential, resistive feedback	Differential, composite transistor pair	Differential	Current reuse, R–C feedback, pseudo-resistor	Current reuse, SFB- CG stage, DTMOS, body-driven

Table 3 Comparison table for LNAs at 65 nm

	[28]	[13]	[24]	Mod-1[14]	Mod-2[14]	Mod-3[14]	[27]	[31]	[32]	[33]
Power (mW)	0.0024	32	11.3	29	29	29	30	5.5	17	28
Bandwidth (Hz)	6.5 k	20 G	6.5 G	40–2900 M	1000–3500 M	400–2200 M	28 G	7 G	26 G	12 G
Gain (dB)	40–54	28.5	16.8	20	20.8	19.8	18.5	17	19.5	19.3
Voltage (V)	0.35/0.7	1	1.2	1.2	1.2	1.2	1	1.2	1	
|NF| (dB)	2.75	2.7–3.2	2.87	2–2.5	2–2.5	2–2.5	2.7–4.8	3.7	2.6–3.5	2.5/2.6
|IIP3|(dBm)			4.5	5	5	5		0.7	3–9.6	5/7
Area (mm^2)	0.04	0.40	0.044	0.16	0.16	0.16	0.28		0.16	0.25
Technique/ components used	OTA, CMFB, DDA, capacitor-coupled	CG stage, triple-coupled cascode	Resistive feedback, SFF	Gate source inductor, current reuse, COB packaged	Gate source inductor, current reuse, COB packaged	Gate source inductor, current reuse, QFN packaged	Inductive degeneration, CS-CG stage	Inductor-less	CS stage, cascode design	CS-CG stages, output matching, differential

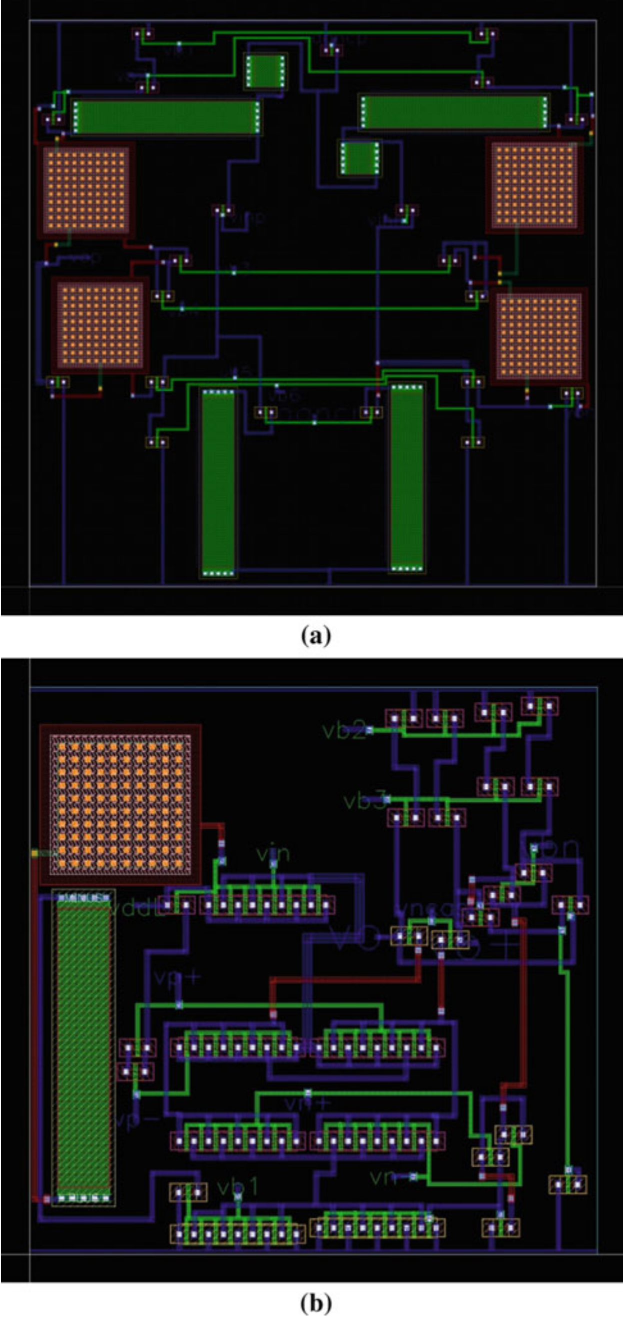
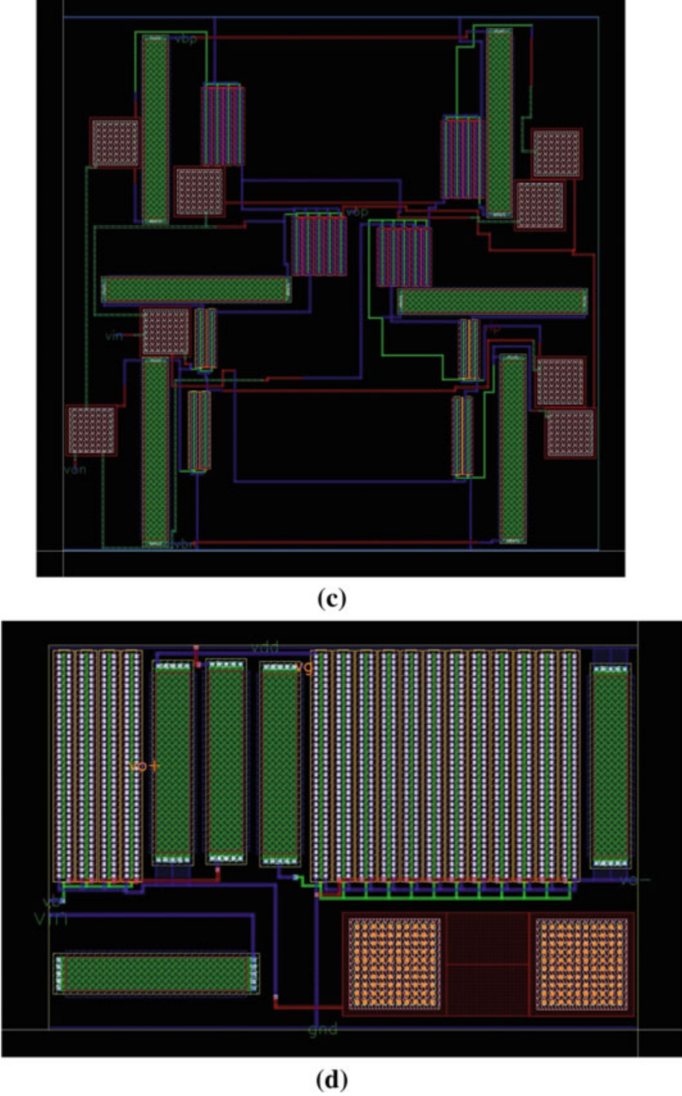


Fig. 7 Layout of different inductor-less LNAs **a** low-power LNA using AANC circuit; **b** OTA-based LNA; **c** inductor-less noise canceling CMOS LNA; **d** sub-GHz wideband LNA



(c)

(d)

Fig. 7 (continued)

highest gain (20.8 dB) has achieved by module-I mentioned in Table 3. The maximum bandwidth of 20 GHz measured in [13], and the minimum bandwidth of 0.49 kHz obtained in [1]. In Table 2, 97% saving of area has measured in [45] compared to [46]. In Table 3, a 75% lower chip area required [14] than state-of-the-art LNAs [13, 28, 24]. Minimum gain values are 4 dB in Table 1, 10 dB in Table 2, and 16.8 in Table 3. The 16.9, 58.7, and 54 dB maximal gain values had obtained in Tables 1, 2 and 3, respectively. The gain value has increased optimized with lower nm technologies.

Different LNAs have utilized for the AFE circuits, and AFE designs show the robust and best performance. The comparison between various AFE designs has represented in Table 4 and Fig. 9. Maximum 1.34 mW power consumed in AFE using LNA[11] and minimum 0.2 mW power dissipated in [4, 32]. It achieved maximal 4.6 GHz bandwidth in AFE using [28] and a minimal 0.93 GHz bandwidth in AFE using [4]. Whereas AFE using [4, 11, 12] obtained a 50 dB low gain, a high 58.7 dB gain, and 14.82% highest than AFE using [28]. The AFE using [50] has minimal 36.06% output-referred noise than that of AFE using [11]. The FoM obtained from AFE with LNA [28] has 93.54% better than AFE with LNA [11] (Fig. 9).

There are different types of limitations for different LNAs. Drawbacks of a few latest LNAs have explained in this paragraph. CS-cascode amplifier stages have formed the LNA circuit and led to an increment in power due to multi-stages and the complexity of LNA design. The third stage has impacted the P1dB and linearity due to low output capabilities [27]. There is an increase in the complexity of inductor-less LNA design [31]. The power and area of LNAs have maximized due to a large number of inductors [32] and passive network addition [35]. In LNA [33], gain imbalances and phase imbalances existed due to matching stages at input and output terminals. LNA has obtained low power and high gain; on the other hand, bandwidth has effected due to body-driven techniques in LNA design [50].

Table 4 Comparison table for LNA application (AFE)

AFE using different LNA circuits	Power P (mW)	Bandwidth Bw (GHz)	Gain A (dB)	Output-referred noise (nV/Hz$^{1/2}$)	Figure of Merit 1 (FoM[a])
AFE with LNA [4]	0.2	0.93	58.7	5.9	1364
AFE with LNA [11]	1.34	0.97	58.7	6.1	212
AFE with LNA [12]	0.52	0.95	58.7	5.7	536
AFE with LNA [14]	1.29	3.9	50.13	4.3	757
AFE with LNA [21]	0.32	1.84	56.26	4.9	1610
AFE with LNA [28]	0.35	4.6	50	5.97	3285
AFE with LNA [31]	0.21	1.7	56.45	4.75	2284
AFE with LNA [32]	0.2	1.99	55.8	4.4	2776
AFE with LNA [50]	0.87	3.98	51.6	3.9	1156

[a]FoM = (A Bw C_L)/P [C_L = 5pF for AFE(LNA application) circuits]

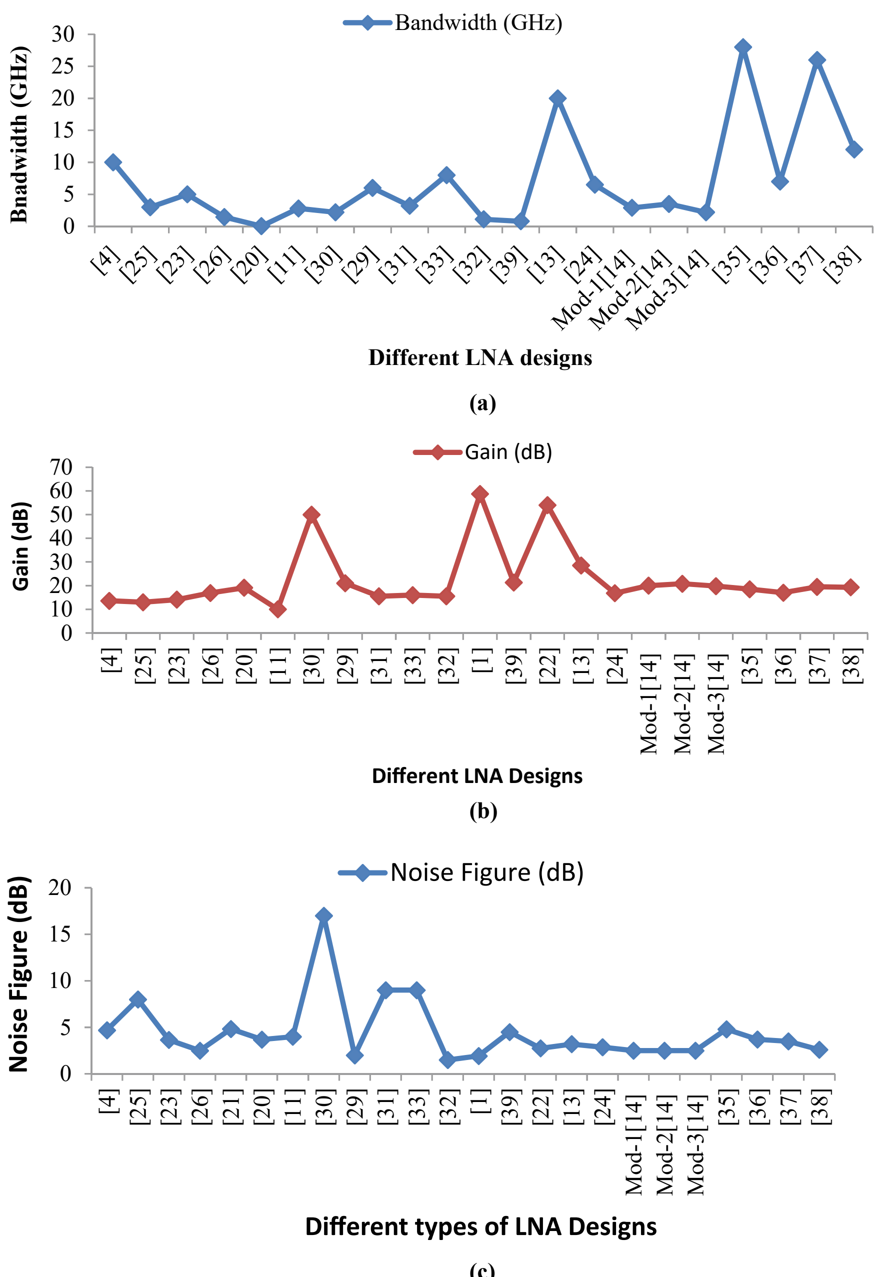


Fig. 8 Graphical comparison of **a** bandwidth, **b** gain, **c** noise figure, **d** power, **e** IIP3, and **f** area for different LNA designs

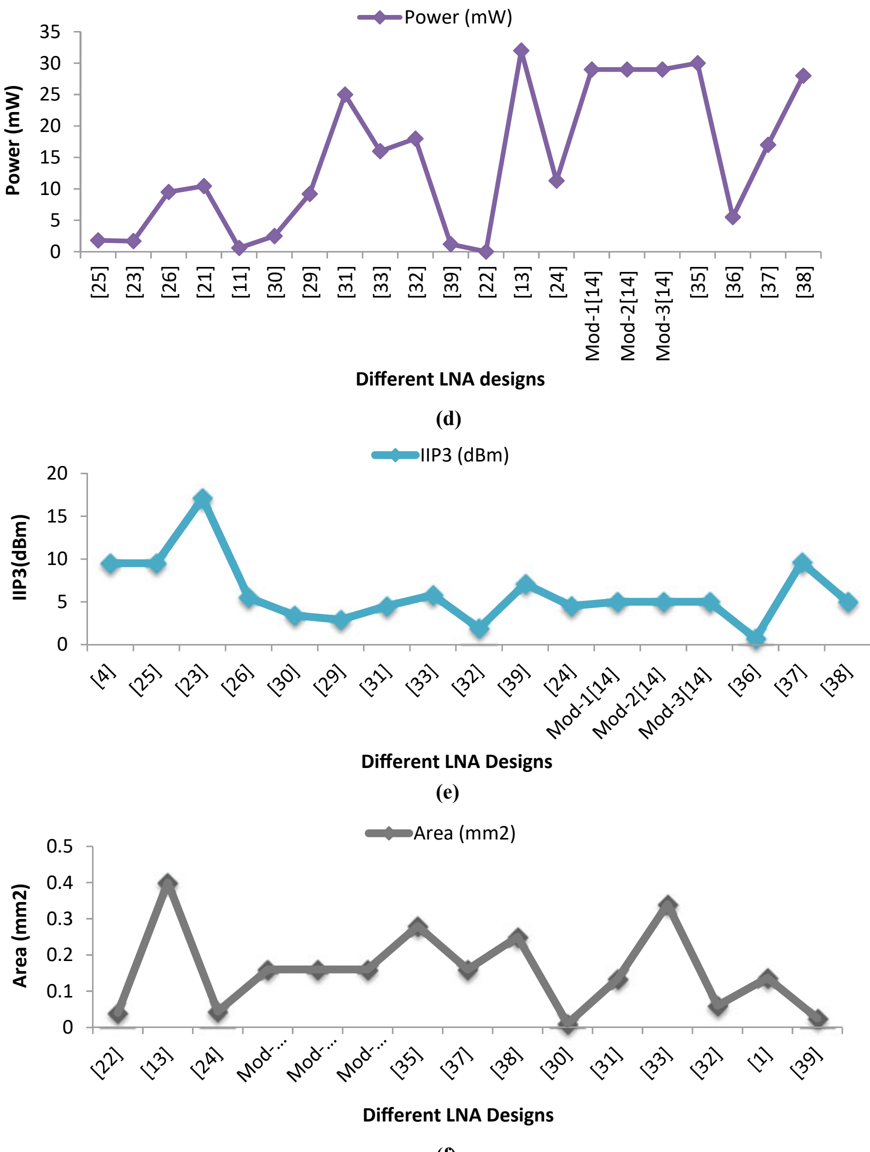


Fig. 8 (continued)

5 Conclusion

The LNAs have simulated at 180, 65, and 90 nm MOS technology of the specter tool of MOS technology. LNAs have compared using different parameters such as technology, gain, power, bandwidth, area, NF, and IIP3. Bandwidth has decreased from GHz to MHz when 65 nm technologies are used instead of 180 nm technology for LNA designs. At different technologies, power and area have reduced from mW to µW and 0.3 mm^2 to 0.01 mm^2 in LNA design. The variable gain LNAs [11, 45] and LNA using OTA [28] have more suitable for low-power applications. High-gain wideband LNA [14], LNA using pseudo-resistor [1], and LNA using active inductor have utilized in minimal noise applications. Based on measured parameters, LNA using OTA [2] and high-gain wideband LNA [14] module-2 have high performance than state-of-the-art LNAs. Both LNAs have designed at 65 nm technologies, which added another advantage in chip area, figure of merit (FoM), and operating frequency. Design AFE has an application of LNA, and simulation results have obtained. AFE shows power savings, higher bandwidth, high gain, low output-referred noise, and high FoM for better operation and work.

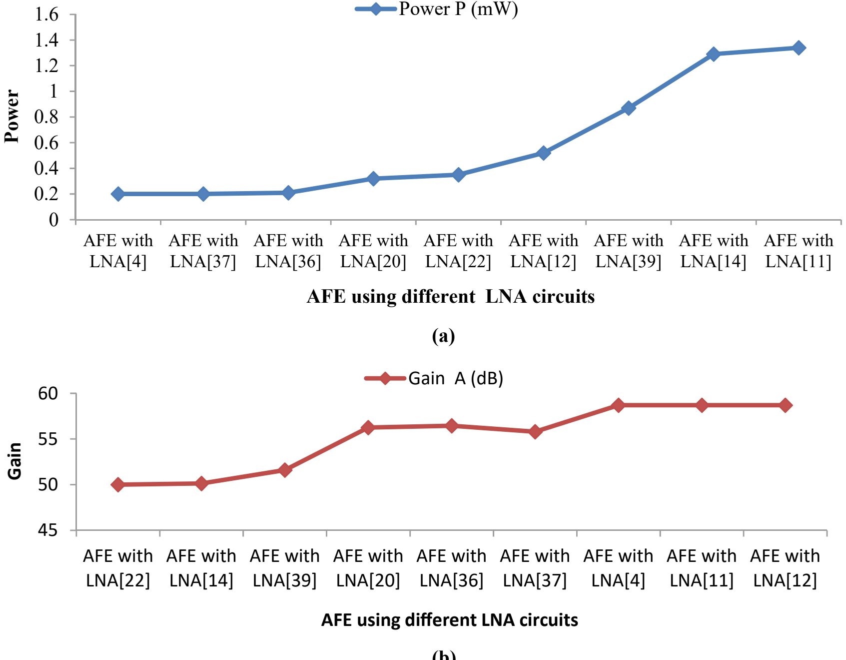
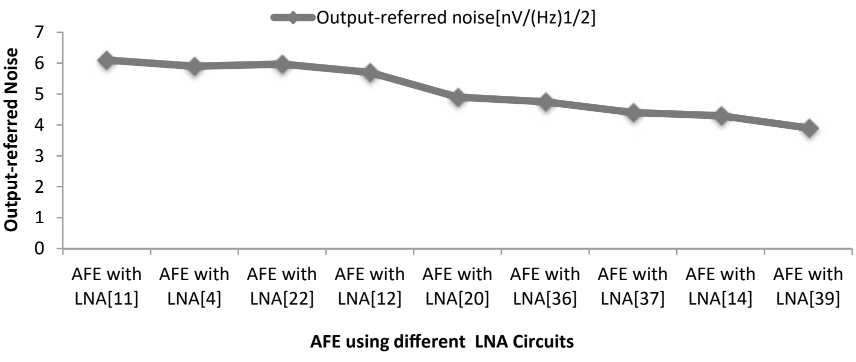
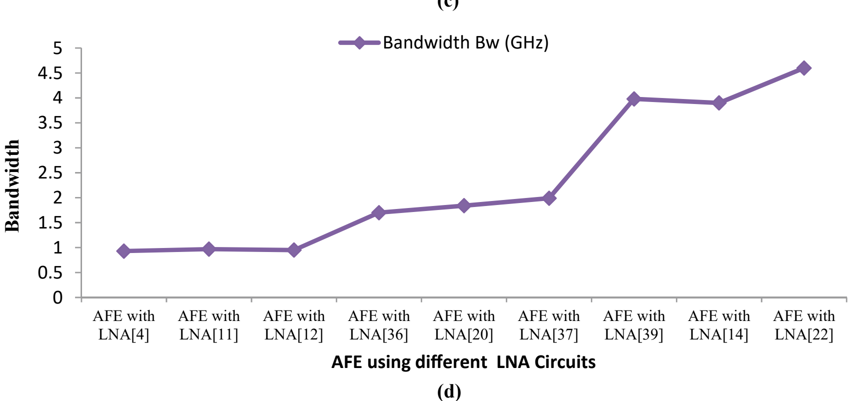


Fig. 9 Graphical comparison of **a** power, **b** gain, **c** output-referred noise, and **d** bandwidth for AFE designs using different LNAs



(c)



(d)

Fig. 9 (continued)

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Design of High-Speed SRAM Cell Using FinFET Technology

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1 Introduction

In the era of high precision and technology, the usage of transistors in the electronic devices has been normal. The transistors are generally the semiconductor devices that are used to amplify the electronic signals [1]. Transistors have been very important because they transform the world of electronics and also have high impact on computer devices. Of all transistors, FinFET is a type of non-planar transistor which has the capability of acting like an amplifier and as a switch. Also it develops numerous advantages when compared to other transistors such as higher speed, low leakage, and low power consumption, and it reduces short channel effects which is a main drawback of MOSFETs [2]. The FinFET transistors are such consistent multilayer devices that are available in single, double, or even trigate structures. Hence, these transistors are placed in an SRAM cell which acts as a computer cache memory to store the data. As we have known, the SRAM cell has been a memory which saves the information in the format of bits until the power is being supplied to it. Unlike the other transistors such as MOSFET, FinFET transistors have been the better option to the upcoming evaluation of electronic circuits [3]. Figure 1 shows the classification of transistors.

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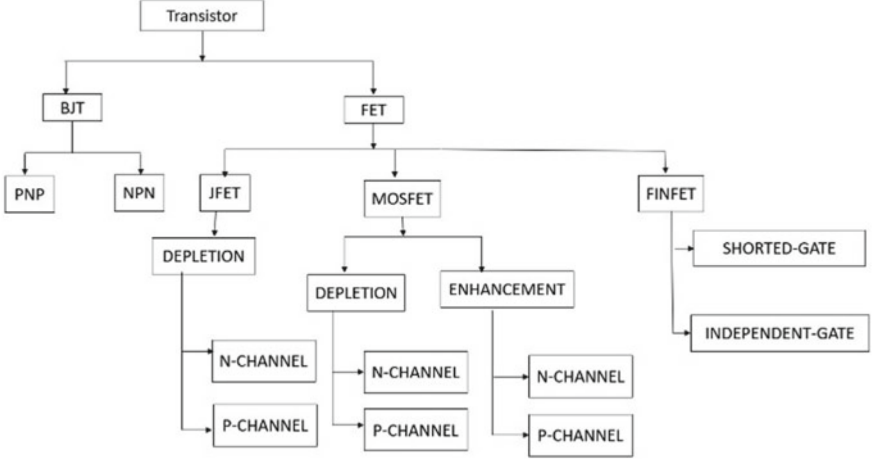

Fig. 1 Classification of transistors

The application of FinFET technology to memories can increase the tolerant capacity of the memory device, saves significant power, and achieves faster operations. SRAM stores data for longer than DRAM, and it allows faster transfer speeds. The basic conventional 6T SRAM cell is shown below. SRAM cell has been mostly used in SOC designs in the process of technology scaling [4].

The further paper will be organized as follows. In Sect. 2, previous research works on FinFET technology and SRAM cell are specified. Section 3 provides the basic design of the FinFET. In Sect. 4, various designing techniques implemented and their simulation results for SRAM cell are mentioned. Sect. 5 conveys the simulation results comparison with respect to various designing techniques.

2 Related Work

"Ground plane fin-shaped field effect transistor (GP-FinFET): A FinFET for low leakage power circuits" In this paper, an investigation is done on fin-shaped field effect transistor (FinFET) structure with the ground plane concept for reducing the DIBL effect. With comparison of device properties of the structure with silicon-on insulator FinFET (SOI-FinFET) and bulk FinFET structures, it shows that the DIBL and leakage current are reduced in the proposed structure [5].

"A current model for FOI FinFETs with back-gate bias modulation" The current model of the fin-on insulator (FOI) FinFET was proposed in this paper. The accuracy of the developed model was validated under both experimental and simulation through TCAD for different back wide valid range for different geometry parameters that include width, height, and bottom parameters of fin. This model will help the device to optimize the parameters of the device [6].

"A single ended 6T SRAM cell design for ultra-low-voltage applications" In this paper, a novel 6T (group of six transistors) simple ended SRAM memory cell is designed for applications operating with ultra-low voltages. By comparing this design with the standard 6T SRAM cell, result shows that the read and write ability is improved and leakage power dissipation is reduced [7].

"A Novel Sleepy Stack 6-T SRAM Cell Design for Reducing Leakage Power in Submicron Technologies" In this paper, there is a detailed explanation is given regarding design of 6T SRAM cell which reduces power leakages at submicron-level technologies. Hence, new technique named "sleep stack" is proposed to reduce problem of leakage in deep submicron technology. The sleepy stack technique yields the best power-saving scheme for the system in standby mode when compared to the sleep transistor technique.

"Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies" In this paper, it is given about the stability analysis of SRAM cell with respect to read and write operations for nanometer technology. As SRAM cell read and write abilities are major concern in nanometer CMOS technology, analysis of read stability in *N* curve metrics is done in comparison with static noise margin. So, the new *N* curve metrics are introduced for write ability of SRAM cell. Since the current information of *N* curve is critical for design of a cell, it allows $0.5V_{dd}$ stability limit. The results show gain in both leakage current and worst case design approach [8].

"Low-Leakage Asymmetric-Cell SRAM" A detailed explanation about the low leakage asymmetric SRAM cell was discussed in this paper. Generally, an SRAM cell reduces the power leakage in the cache, in addition it maintains less latency in access. Hence, there is a proposal where leakage power dissipation gets reduced. It is behind the cache resident memory values. Where the leakage enhanced cell reduces at least 6X about 40X is preferred state [9].

"A Discussion on SRAM Circuit Design Trend in Deeper Nanometer-Scale Technologies" In this paper, the deeper exploration of SRAM circuit design trends in deeper nanometer scale technology. It examines the capabilities of area scaling of several SRAM margin-assist solutions for the VT variability problem based on efforts by not only changing the topology of the cells from 6 to 8T and 10T but also other factors. The discussion is done on the comparing the capabilities of area scaling for various SRAM-based margin-assist solutions for VT variability issues.

3 Design of FinFET

A FinFET is a multi-gate transistor device which is shown in Fig. 2. It is a transistor of non-planar or 3D model having a thin-fin-shaped structure with silicon laid on the substrate wrapped over gate. Source and drain are formed on both sides of the fin, and they are not wrapped under gate. Gate orientation is toward the right angle of vertical fin. Under gate, the channel is formed, i.e., fin.

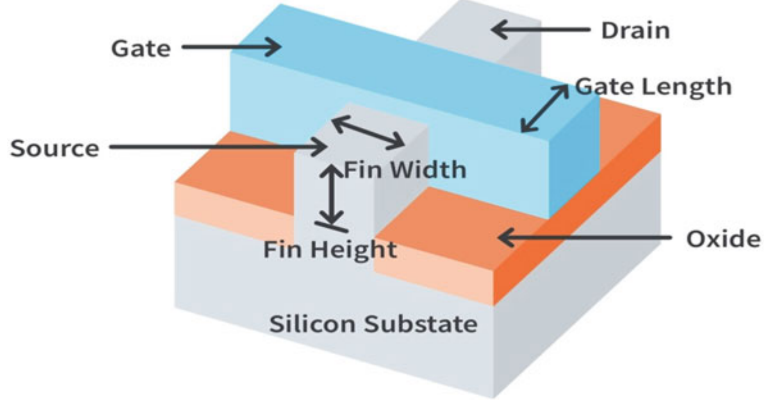

Fig. 2 Structure of FinFET

4 Designing Techniques for SRAM Cell

SRAM cell is designed using MOSFET and FinFET transistors. Under FinFET-based designings, different logic techniques are implemented; those are conventional 6T, sleep transistor, forced stack, dynamic threshold MOS (DTMOS), variable threshold MOS (VTMOS), DTMOS–forced stack, DTMOS–sleep transistor, VTMOS–forced stack, and VTMOS–sleep transistor. These techniques are compared to observe the performance parameters like power consumption and delay of SRAM cell.

4.1 Conventional 6T SRAM Cell Using MOSFET

Conventional 6T SRAM cell is designed using MOSFET at 45 nm technology node as shown in Fig. 3. The simulation is done in Symica DE software to observe the waveforms of control signals and output signals. The power consumption and delay parameters are calculated using Symica DE. The supply voltage is taken as 1 V.

We have given the bit data as input for three control signals as given below, for that data we get the output signal accordingly. The same data is taken for the other designing techniques.

$$\mathrm{wl} = 00110111$$
$$\mathrm{bl} = 0101010101010101$$
$$\mathrm{blb} = 1010101010101010$$

The multiplication of transistor's drain current and the output signal "q" is used to compute power consumption, i.e., $M_{2.\mathrm{d}}$ with the supply voltage V_{dd}.

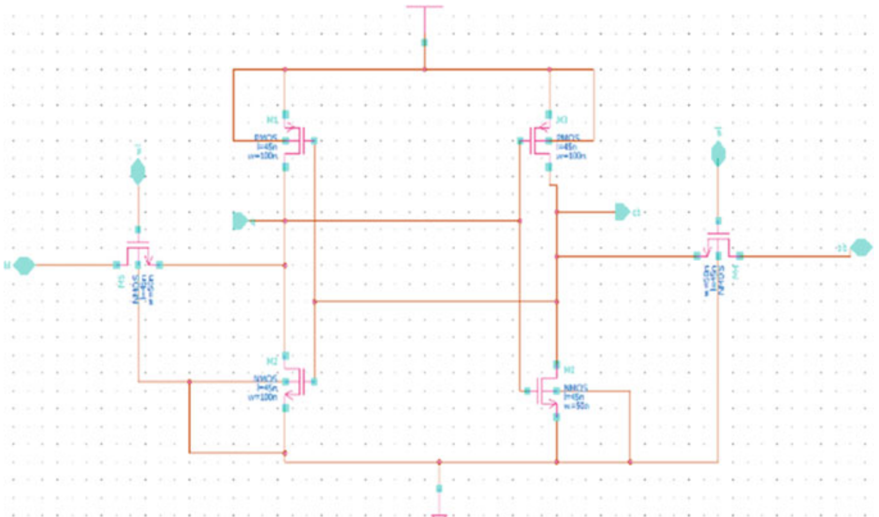

Fig. 3 Conventional 6T SRAM cell using MOSFET

$$\text{Power Consumption} = M_{2\text{d}} \times V_{\text{dd}} \tag{1}$$

After running the above formula on the software, we got the power consumption of 2.07 mw for conventional 6T SRAM cell using MOSFET.

Delay is calculated for the output signal "*q*," and result shows the delay of 5.18 ns for conventional 6T SRAM using MOSFET.

4.2 SRAM Cell Designing Using FinFET

4.2.1 Conventional 6T SRAM Cell

SRAM cell is designed using FinFET transistor at 14 nm technology node which is shown in Fig. 4 and simulated in Symica DE software to observe the waveforms of control signals and output signals. The calculations of power consumption and delay are done in Symica DE. The thickness of the fin is taken as 25 nm for p-type FinFET and 15 nm for n-type FinFET. The supply voltage for the conventional 6T SRAM using FinFET is 1v as shown in Figs. 4 and 5. These are the same specifications used in all design methods. The power rails or ground are cut off by sleepy transistors during the creation of an SRAM cell utilizing the sleep transistor technique.

Calculation of power consumption is done by the multiplication of the drain current (V_{dd}) of the transistor below output signal "*q*," i.e., $I_{2\text{d}}$ with the supply voltage V_{dd}.

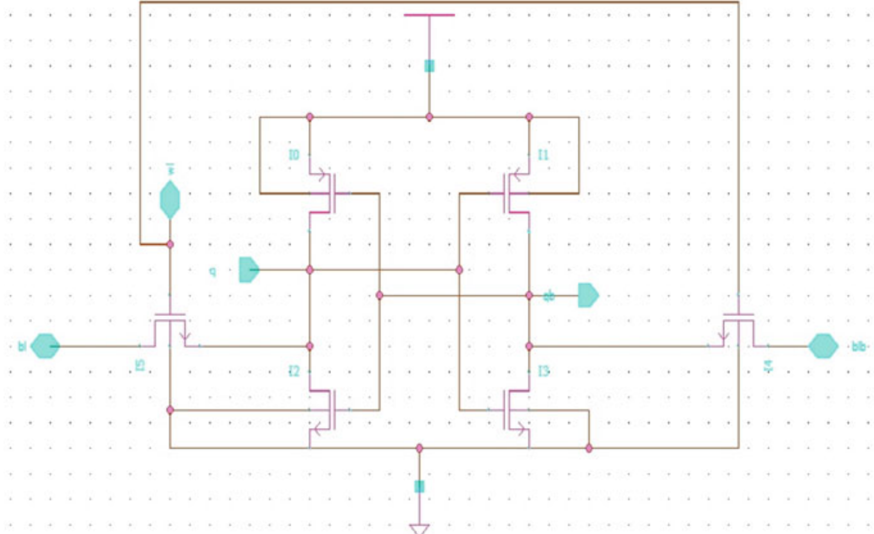

Fig. 4 Conventional SRAM cell using FinFET

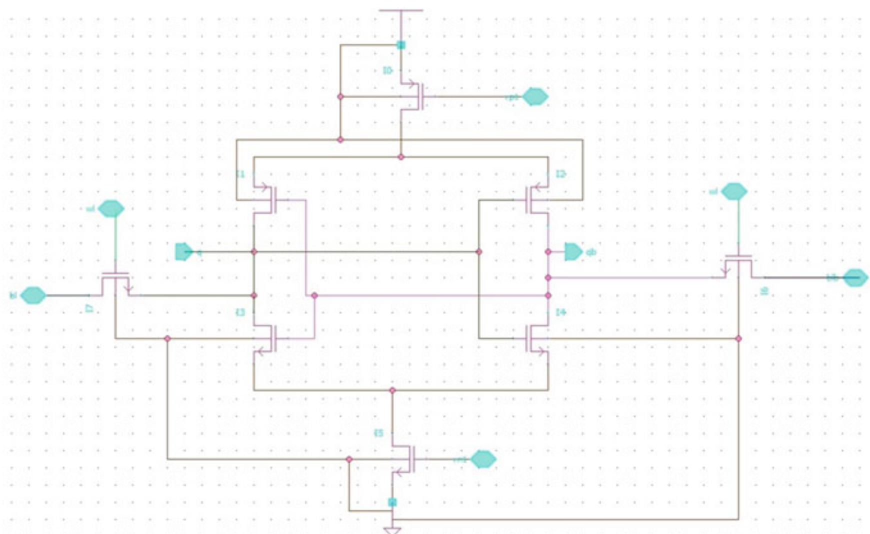

Fig. 5 SRAM using sleep transistor technique

$$\text{Power Consumption} = I_{2d} \times V_{dd} \tag{2}$$

After running the above formula on the software, we got the power consumption of 64.21 μw for conventional 6T SRAM cell using FinFET.

Delay is calculated for the output signal "*q*," and result shows the delay of 1.23 ns for conventional 6T SRAM using FinFET.

4.2.2 SRAM Using Sleep Transistor Technique

The power rails or ground are cut off by sleepy transistors during the creation of an SRAM cell utilizing the sleep transistor technique as shown in Fig. 5.

$$\text{Power Consumption} = I_{2d} \times V_{dd} \tag{3}$$

The simulated result indicates that the power consumption of SRAM cell is 0.55 μw. The simulated result shows the delay of 5.07 ns in sleep transistor technique.

4.2.3 SRAM Using Forced Stack Technique

SRAM cell is designed using the forced stack technique which is shown in Fig. 6. In this method, each transistor in the network is replaced with two transistors in series having half the width of original transistor.

$$\text{Power Consumption} = I_{2d} \times V_{dd} \tag{4}$$

The simulated results provide the power consumption details of SRAM cell as 6.55 μw. The simulated result shows the delay of 3.54 ns for forced stack technique.

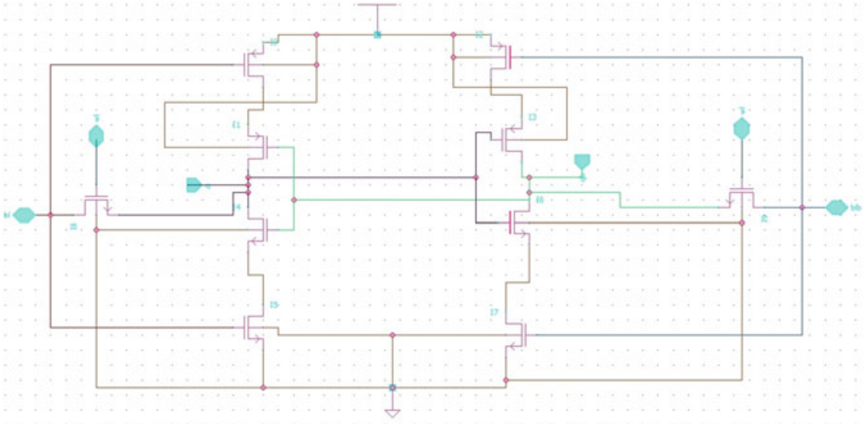

Fig. 6 SRAM using forced stack technique

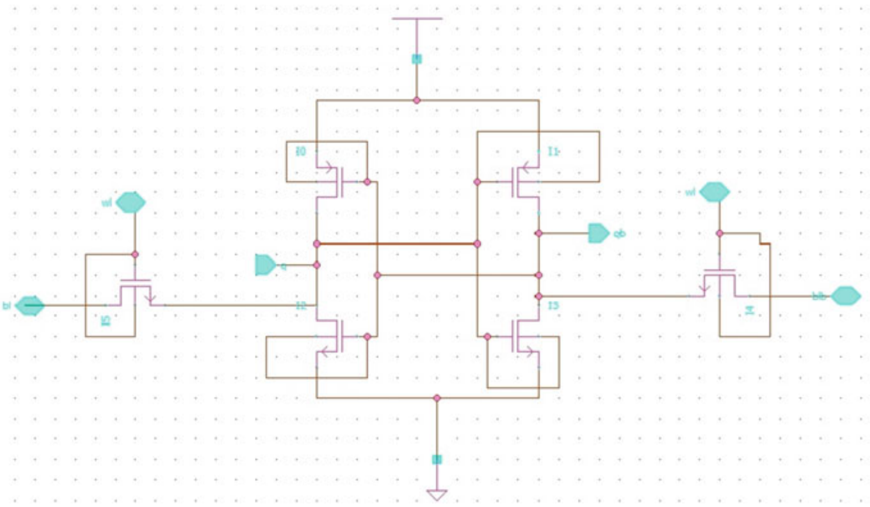

Fig. 7 SRAM using DTMOS technique

4.2.4 SRAM Using DTMOS Technique

SRAM cell is designed using the DTMOS technique as shown in Fig. 7 in which the threshold voltage is altered dynamically to suit the operating state of circuits.

$$\text{Power Consumption} = I_{2d} \times V_{dd} \tag{5}$$

The simulations indicate the power consumption as 64.21 µw for DTMOS technique. We got the delay of 4.38 ns for DTMOS technique.

4.2.5 SRAM Using VTMOS Technique

SRAM cell is designed using the VTMOS technique which is shown in Fig. 8. In VTMOS, the gate is connected to substrate through a biasing voltage. This bias voltage causes large variation of threshold voltage with gate voltage than in DTMOS.

$$\text{Power Consumption} = I_{2d} \times V_{dd} \tag{6}$$

The simulated result shows the 64.44 µw power consumption and the delay of 3.56 ns.

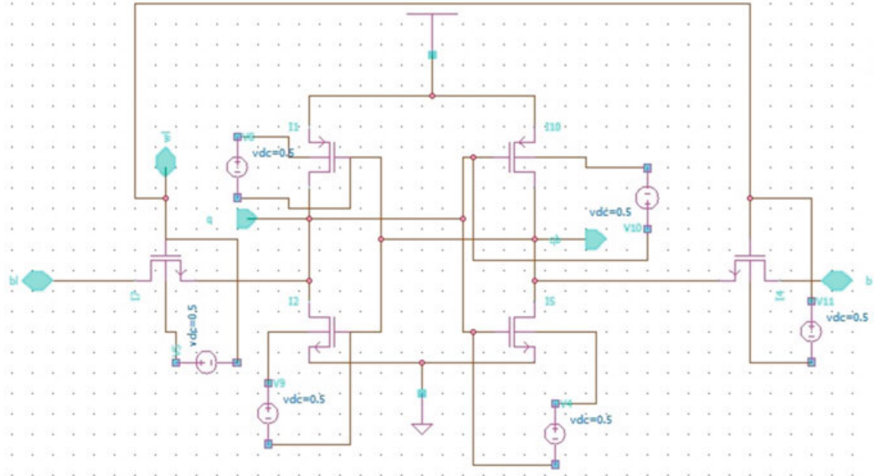

Fig. 8 SRAM using VTMOS technique

4.2.6 SRAM Using DTMOS–Forced Stack Technique

SRAM cell is designed using the DTMOS–forced stack technique which is shown in Fig. 9.

$$\text{Power Consumption} = I_{2d} \times V_{dd} \tag{7}$$

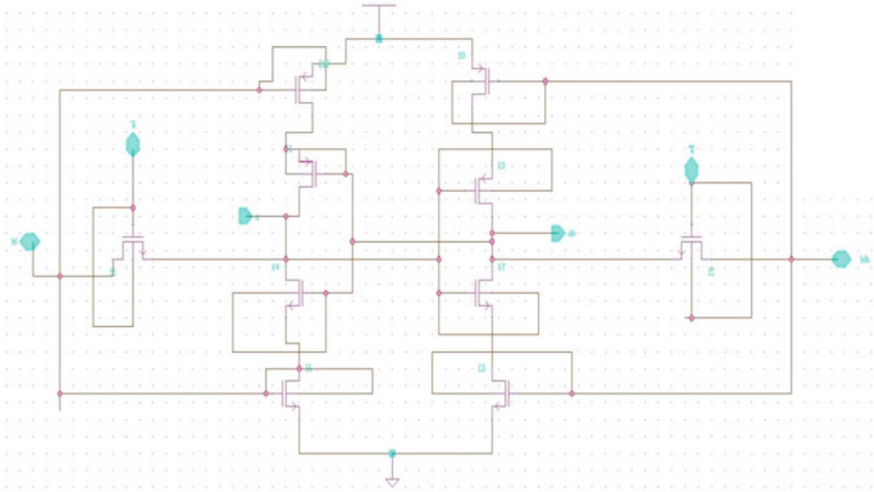

Fig. 9 SRAM using DTMOS–forced stack technique

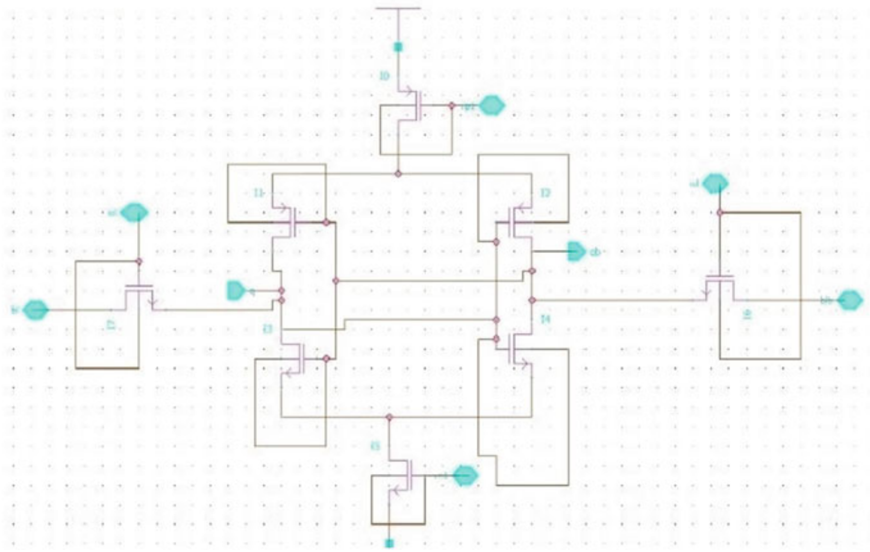

Fig. 10 SRAM using DTMOS–sleep transistor technique

The simulated result shows that the power consumption of 10.24 µw and with 2.94 ns delay.

4.2.7 SRAM Using DTMOS–Sleep Transistor Technique

SRAM cell is designed using the DTMOS–sleep transistor technique which combines both DTMOS and sleep transistor techniques as shown in Fig. 10.

$$\text{Power Consumption} = I_{3d} \times V_{dd} \tag{8}$$

The simulated result shows the power consumption of 22.6 µw and with the delay of 0.91 ns.

4.2.8 SRAM Using VTMOS–Forced Stack Technique

SRAM cell is designed using the VTMOS–forced stack technique as shown in Fig. 11 which is the combination of VTMOS and forced stack technique.

$$\text{Power Consumption} = I_{4d} \times V_{dd} \tag{9}$$

The simulated result shows that the power consumption of 6.50 µw and obtained the delay of 5.07 ns.

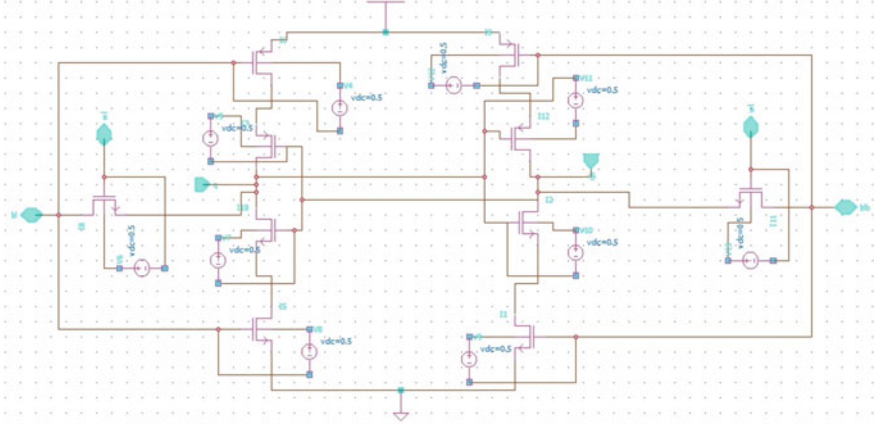

Fig. 11 SRAM using VTMOS–forced stack technique

4.2.9 SRAM Using VTMOS–Sleep Transistor Technique

SRAM cell is designed using the VTMOS–sleep transistor technique which is shown in Fig. 12. This technique is the combination of VTMOS and sleep transistor techniques.

$$\text{Power Consumption} = I_{2\text{d}} \times V_{\text{dd}} \quad (10)$$

The simulated result shows that the power consumption of 0.61 µw and with the delay of 3.96 ns.

5 Results and Discussion

The following results have been obtained for the nine various designs of SRAM cell using FinFET transistor and conventional SRAM cell using MOSFET. The readings are obtained in terms of parameters like power consumption and delay.

From Table 1, we can observe that the consumption of power for a conventional 6T using MOSFET is 2.07 mw and the power consumption of conventional 6T using FinFET is 64.21 µw. So, the FinFET-based SRAM cell is more reliable and consumes less power. In the same way, the conventional 6T using FinFET is faster if we consider the delay of these designs, the delay of conventional 6T using MOSFET is 5.18 ns, and the delay of conventional 6T using FinFET is 5.18 ns. Also, the SRAM cell under different techniques is designed and analyzed using FinFET at 14 nm technology node. Among the designing techniques, SRAM using sleep transistor produces very less power consumption, i.e., 0.55 µw, and SRAM using DTMOS–sleep transistor technique offers less delay, i.e., 0.91 ns, compared to other designing techniques.

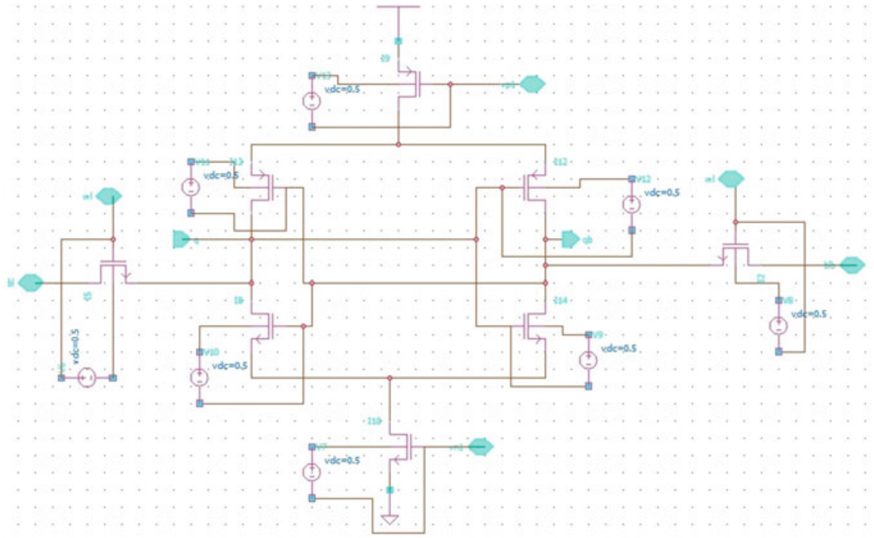

Fig. 12 SRAM using VTMOS–sleep transistor technique

Table 1 Comparison of power consumption and delay along different techniques

Technique	Power consumption (μW)	Delay (ns)
Conventional 6T using MOSFET	2.07	5.18
Conventional 6T using FinFET	64.21	1.23
Sleep transistor technique	0.55	5.07
Forced stack technique	6.55	3.54
DTMOS technique	64.21	4.38
VTMOS technique	64.44	3.56
DTMOS–forced stack technique	10.24	2.94
DTMOS–sleep transistor technique	22.63	0.91
VTMOS–forced stack technique	6.50	5.07
VTMOS–sleep transistor technique	0.61	3.96

6 Conclusion

The 6T SRAM cell based on FinFET of 14 nm technology and other designing techniques for SRAM cell are analyzed here. The conventional 6T SRAM cell using MOSFET at 45 nm and FinFET at 14 nm is designed and analyzed in terms of power consumption and delay. The FinFET-based 6T SRAM cell at 14 nm and MOSFET-based 6T SRAM cell are compared in terms of power consumption and delay. The simulated result shows that FinFET-based SRAM cell performs well with low power consumption and delay. Also the SRAM cell under different techniques is designed

and analyzed using FinFET at 14 nm technology node. Among all the designing techniques, sleep transistor and VTMOS–sleep transistor are the promising solutions for the power consumption issue. As we are considering all the techniques, we found that DTMOS–sleep transistor technique provides less delay when compared to all other techniques.

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Design-Space Exploration of Conventional/Non-conventional Techniques for XOR/XNOR Cell

Uma Sharma and Mansi Jhamb

1 Introduction

Low-power applications have emerged as a top priority for VLSI system designers due to the fast expansion of portable user-friendly electronic gadgets in the electronics industry. More importantly, a significant increase in the use of electrical and electronic devices encourages designers to aim for smaller silicon areas, faster computation, lower power consumption, and improved resilience [1]. The full adder design is fundamental to digital computing, and XOR/XNOR cell is an important key block in the designing of full adder.

Several applications of communication domain, including phase detector in phase-locked loops (PLL), comparator, sequence generator, correlation and sequence pointer, even and odd parity generator, and parity checker make extensive use of XOR/XNOR cells [2]. The performance, i.e., speed, power consumption, energy, and power delay product of XOR/XNOR cell can be improved by proper selection of design style. There are various design styles available in the literature which are used for the implementation of XOR/XNOR cell. Generally, static and dynamic circuit design approaches are the two most well-known design methodologies for the implementation of digital circuits. The dynamic logic style inability to cascade many phases is a drawback. It is possible to cascade many stages using domino logic, a variant of dynamic logic [3]. Due to its higher speed and reduced power consumption, dynamic complementary metal oxide semiconductor (CMOS) logic is chosen over static CMOS logic while implementing high-speed digital circuits [3].

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The supply voltage must be lowered to ensure device reliability as the device channel length is scaled down into the submicron zone and the gate oxide thickness shrinks to nanometer range. The MOS transistor's threshold voltage, which restricts the supply voltage to being equal to or greater than threshold voltage, poses its own constraint on the reduction of supply voltage. As a result, the conventional CMOS technology is no longer effective for the implementation of low-power circuits [4]. FGMOS technology comes up as a solution to cope with these problems of conventional CMOS technology [4]. Also, continuous scaling causes CMOS logic to experience a number of problems. These challenges include short channel effect, limited control over the gate terminal, increased leakage currents, and heavy power usage. Due to these problems, sophisticated technologies such as FinFET, silicon nanowire transistors, single electron transistors (SET), and carbon nanotube field effect transistors (CNTFET) have been explored. Among these technologies, carbon nanotubes field effect transistors (CNFETs) is the most accepted technology for low-power design because it offers additional scalability as compared to MOSFET technology, and this feature drives it acceptable for relacing MOS technology for LVLP VLSI circuit design [5]. In this paper, different conventional and non-conventional design methodologies have been reviewed for the implementation of XOR/XNOR cell. The challenges of these design methodologies have been discussed in this research article. The goal of this research article is to provide a quick overview of some appealing XOR/XNOR cell designs [1–3, 6, 7] for design space exploration of conventional/ non-convention design techniques. Design-space exploration (DSE) is the process of investigating design options before choosing one to use [8]. DSE plays an important role in nanometer regime because finding the appropriate design process for the application is so crucial.

The paper is organized as depicted in the below flowchart:

Section 2 describes the review of conventional and non-conventional design techniques and their challenges. In Sect. 3, literature review of various XOR/XNOR cells have been discussed in detail. In Sect. 4, comparative analysis of XOR/XNOR cells has been given and the significance of each design has been discussed. Section 5 of this review paper provides the conclusion based on the comparative analysis.

2 Review of Conventional and Non-conventional Design Techniques and Their Challenges

Researchers are becoming more interested in low-voltage and low-power circuit design as the need for portable and handheld advanced electronic devices grows [6]. To realize low-voltage low-power circuits, several conventional and non-conventional techniques have been presented in the literature [7–12]. Generally, conventional design techniques use the concept of reducing supply voltage and device dimension for the reduction of power consumption. The techniques for low-voltage and low-power design are then discussed.

2.1 Complementary Metal Oxide Semiconductor (CMOS) Technology

CMOS is one of the extensively used technology in the chip designing industry. In CMOS technology, both NMOS and PMOS transistor are used to design different logic functions. NMOS transistors are used in pull down network, whereas PMOS transistors are used in pull up network. CMOS logic circuit offers low power consumption because static power dissipation is almost zero. The reason behind low static power is that there is no direct path exists between power supply and the ground terminal of the circuit. In contrast to other techniques of logic circuits like TTL or NMOS/PMOS logic, which typically utilize some standing current even when there is no switching, these devices do not produce waste heat. These CMOS properties will enable the high-density integration of logic functions on an IC. Figure 2 shows the basic structure of CMOS logic gate. CMOS offers many advantages such as good noise margin, less power consumption, high speed, high fan-out, and large voltage swing. However, CMOS faces some challenges in nanometer regime. Below 20 nm technology node, many circuit parameters cannot scaled further in consonance with the technology node and that results in increased leakage currents, short channel, and parasitic effects [13].

2.2 Carbon Nanotube Field Effect Transistor (CNFET) Technology

CNFET is one of the promising technologies of nanometer regime. CNTFETs are constructed from hollow carbon cylinders that are formed into single-walled carbon nanotubes, which have semiconducting characteristics [15]. CNFET structure is depicted in Fig. 3.

Graphene sheets are rolled up to form carbon nanotubes. Graphene promises to be the toughest substance so far examined but will require some extra effort to separate from graphite [16]. Between the source and drain, the CNTFET employs CNT as a channel unlike ordinary MOSFETs, which use silicon as their channel. The conductivity of CNT depends upon the atom's angle along the tube, and it is represented by chirality factor. By varying the chirality factor, the threshold voltage of the CNFET can be controlled easily which is very difficult in MOSFET. Also, the temperature variability factor on threshold of CNFET is very less as compared to MOSFET [16]. In short-channel MOSFET devices, the problem of leakage current dominates over other parameters. In case of CNFET device, while decreasing the channel length, the leakage current is also decreased. The detailed study of threshold voltage and leakage current with respect to miniaturization of channel length has been discussed in [16]. However, chirality factor control, fabrication methods, development of CNT, and CNT placement provide huge problems for CNTFETs [17]. Additionally, there is a scarcity of simulation tools for CNTFET devices.

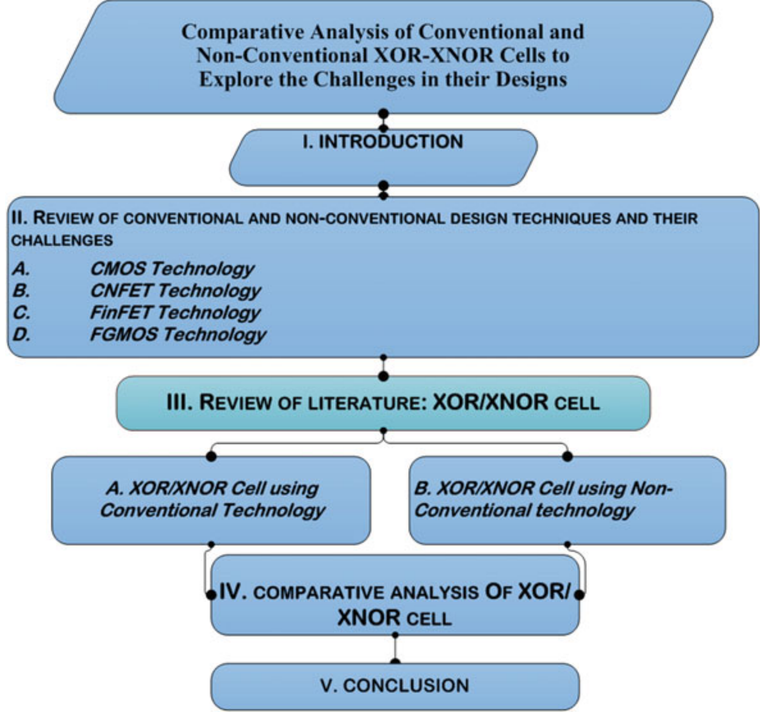

Fig. 1 Flowchart of the paper

2.3 FinFET Technology

For short-channel MOSFET devices, there are some short-channel effects such as drain lowering barrier lowering, punch through, hot carrier effect, and mobility degradation. These effects result in device performance degradation for nanometer regime. FinFET technology is one of the promising solutions to enhance the performance of low-voltage low-power devices in nanometer regime. Figure 4 depicts the structure of a FinFET. FinFETs have three dimensions, both the source and drain areas are higher, in contrary to MOSFETs. The gate is on three sides of the channel region [18]. When compared to other technologies, FinFETs have a number of benefits in terms of power consumption, latency, scalability, output resistance, and current capabilities [19]. Modeling a FinFET device is much more difficult. Extraction of accurate parasites from FinFETs is more difficult. It is considerably more difficult to produce accurate simulation SPICE models than for planar technologies [20]. The FinFET design is much less effective at dissipating heat since heat can readily preserve on the fins [21]. These downsides of FinFET can be solved by using some other material like carbon in place of silicon semiconductor.

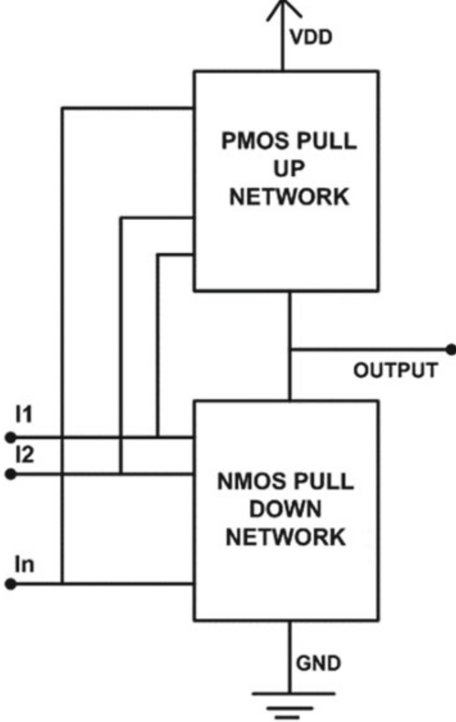

Fig. 2 CMOS logic gate structure [14]

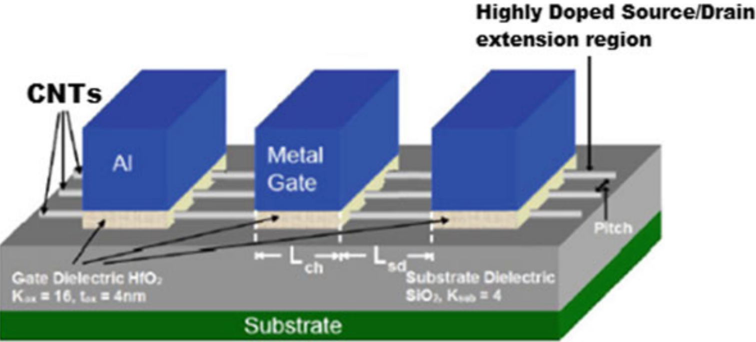

Fig. 3 CNFET structure [15]

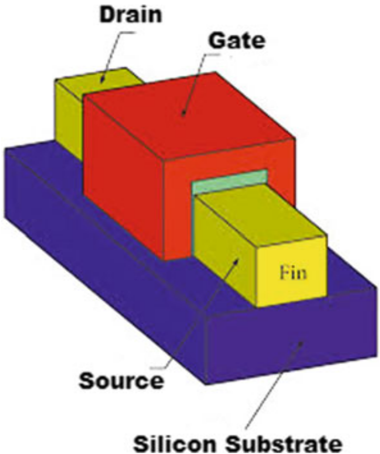

Fig. 4 FinFET structure [19]

2.4 *Floating Gate Metal Oxide Semiconductor (FGMOS) Technology*

FGMOS technology is grown as one of the potential technologies for ultra-low-power VLSI designs. The fabrication process of FGMOS is almost similar to ordinary CMOS technology [22]. FGMOS is a multi-gate structure where threshold voltage is tunable [23]. Figure 5a shows the structural view of FGMOS device. Figure 5a depicts that a number of many secondary gate terminal can be fabricated above the floating gate. Figure 5b represents the equivalent circuit of FGMOS where input is capacitively coupled to the floating gate (FG).

FGMOS technology was used as digital storage element in EPROMs, EEPROMs, and flash memories [4, 24], but nowadays FGMOS technology is used in many analog and digital application such as in logic gates, multiplier, op-amp-based circuits, adders, and many more. There are so many advantages of using FGMOS technology as digital integrated circuit design, viz multiple input terminals, tunability of threshold voltage, and ultra-low power, and voltage applications [10]. Due to

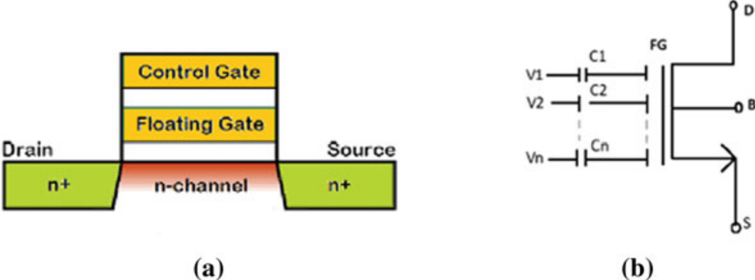

Fig. 5 **a** FGMOS structure, **b** equivalent circuit [22]

different downsides of FGMOS technology, CMOS technology still prevails. The main drawbacks of FGMOS technology are as follows: (1) area requirement is more as compared to ordinary MOSFET because of input capacitances, (2) possibility of accumulation of charge on the FG, (3) reduction in the transconductance and transition frequency, and (4) limited number of simulation models.

3 Review of XOR/XNOR Cell

It has been observed in the recent time that XOR/XNOR cell is the basic building block in the designing of full adders [1–3, 6, 25]. The performance of full adder mainly depends upon the XOR/XNOR cell performance. Therefore, to meet the requirement of nanotechnology, researches are going on to improve the performance of XOR/XNOR cell. To achieve the required performance parameters, different design styles have been used in the literature [1–3, 6, 7, 15, 26–36] to design XOR/XNOR cell.

3.1 XOR/XNOR Cell Using Conventional Technologies

The speed, area, energy consumption, and connection complexity of a circuit are essentially affected by the logic style adopted in logic gates [26]. Radhakrishnan [27] presented a new design of 6-T XOR/XNOR cell (Fig. 6) using pass transistors (PT) and transmission gate (TG). K-map reduction technique along with pass network theorem has been used to design this XOR/XNOR cell. Gate diffusion input logic (GDI) style employed in the XOR/XNOR cell presented in [28]. As compared to ordinary CMOS logic style, GDI logic style requires lesser number of transistors. Also, a feedback transistor is used in this circuit to improve the output voltage swing. A XOR/XNOR cell is proposed in [29] using PT logic which provides bad “0” and bad “1” at the output. Although this design provides a significant improvement in term of power delay product (PDP), but due to non-full voltage swing, an improvement is required in the design.

A full output voltage swing design is proposed using one additional transistor [30] which provides high speed and good current-driving capability. The XOR/XNOR cell presented in [31] is more focused to get full output swing. Here, static inverters are used at the output node. Complementary pass transistor (CPL) logic style is used to implement XOR/XNOR function simultaneous [32]. To maintain the full swing output, a feedback transistor is also used in the design that results in more power consumption and more delay. Kandpal et al. [1] had proposed a CPL-based XOR/XNOR cell (Fig. 7) that uses cross-coupled structure. XOR/XNOR design techniques discussed so far are using static design methodology. The need for chip space is quite high in static CMOS design techniques. Therefore, dynamic logic style evolved as another design alternative to reduce the transistor count, but in dynamic logic style, switching power dissipation is more than static. A key advancement in digital circuit

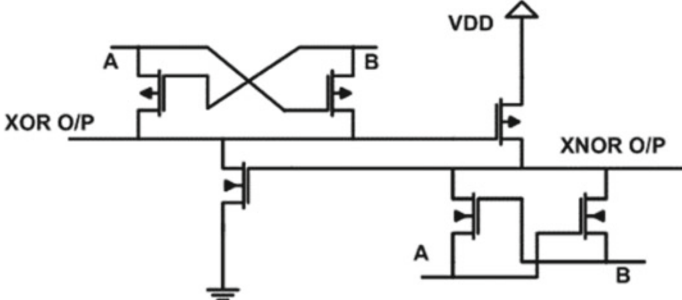

Fig. 6 6-T XOR/XNOR cell [27]

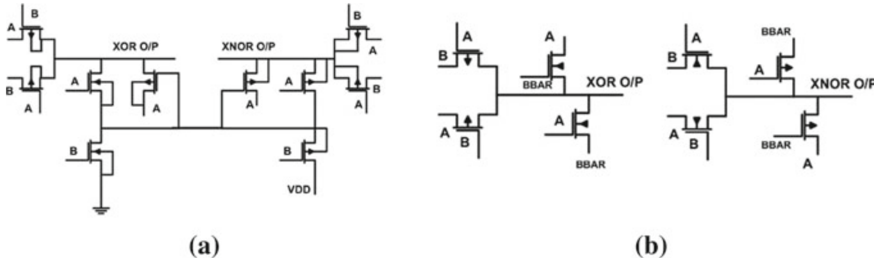

Fig. 7 10-T XOR/XNOR cell **a** [1], **b** [6]

design technology is the domino logic approach, which combines both dynamic and static logic. Compared to conventional single-rail and dual-rail XOR domino gates, the design proposed by Hajiqasemi and Beitollahi [33] depicted in Fig. 8 uses fewer transistors and uses less power without changing the circuit's transmission delay. The complement of the inputs, which is necessary in single/dual rail domino gates, is not required here. A domino logic 9-T XOR/XNOR cell (Fig. 9) is presented by Uma [3] which offers better PDP and EDP since it uses less power than other existing designs.

3.2 XOR/XNOR Cell Using Non-conventional Technologies

The use of non-conventional design techniques and non-conventional devices play a significant role in the digital circuit design at lower technology node. Several XOR/XNOR cell designs are provided in the literature [15, 34–37] which utilized CNFET and FinFET in place of conventional MOSFETs. The author [15] has proposed MCML-based XOR/XNOR cell shown in Fig. 10 and simulated the circuit of XOR/XNOR cell using CMOS and CNFET devices. The author has concluded that the CNFET device emerged as promising technology at 16 nm node as compared to

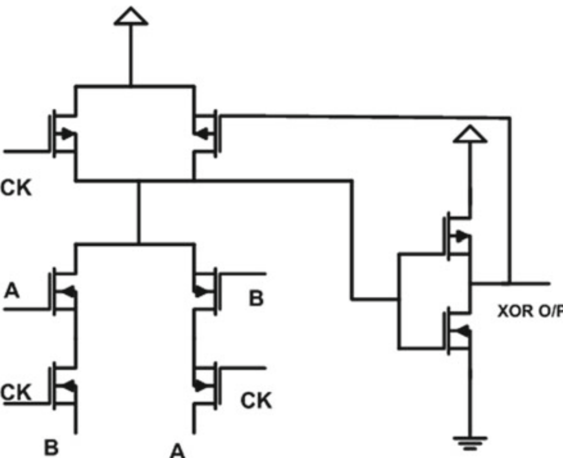

Fig. 8 8-T XOR cell [33]

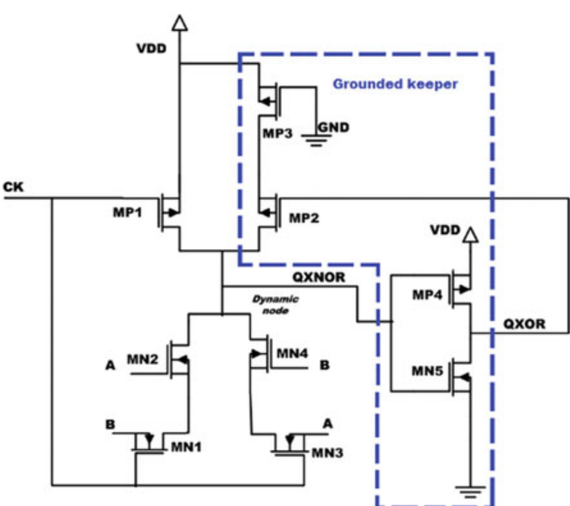

Fig. 9 9-T XOR/XNOR cell [3]

conventional MOSFET. Several XOR/XNOR designs using 3-T, 4-T, 6-T, 7-T, and inverter-based XOR have been discussed in [34].

The author has realized all the design using CMOS and CNFET and found that the CNFET-based results are improved by 68–96%. The author has investigated different XOR/XNOR designs in [35, 36] and found that 8-T XOR/XNOR cell performs better than the other design in term of energy delay product (EDP). The FinFET-based implementation of XNOR/XNOR cell is shown in Fig. 11. EDP variability is also calculated to show the robustness of the design, as EDP considered as an important figure of merit of the circuit [37]. With the use of FinFET, one can reduce the transistor count for multi-input logic circuits. A four-bit XOR/XNOR cell is proposed where pass transistor logic style is used to design the logic circuit [38]. At 20 nm FinFET

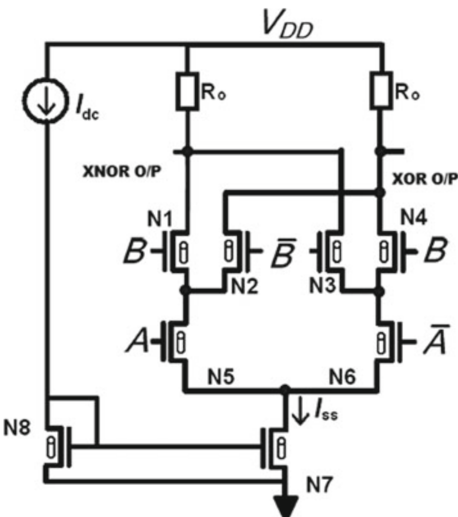

Fig. 10 MCML-CNFET XOR/XNOR cell [15]

technology, the proposed design provides good results in term of transistor count, propagation delay, output swing, and driving capability. Another PTL-based FinFET XOR/XNOR cell design [39] is proposed at 45 nm at 0.7 V supply voltage which offers very less power consumption because of low supply voltage used by the author. FGMOS is one of the non-conventional design techniques used to realize low-power circuit and offers better performance as compared to conventional design techniques. A FGMOS-based XOR cell is proposed with least number of transistors [2] and shown in Fig. 12. As, only three transistors are used in the design, it entails very less power as compared to other designs taken into consideration in this research article. A multi-input FGMOS-based arithmetic logic unit (ALU) is proposed in the literature [40] where XOR/XNOR function have been implemented using FGMOS technology.

4 Comparative Analysis of XOR/XNOR Cell

Table 1 shows the simulation results for various XOR/XNOR cell designs discussed in Sect. 3. The performance of any digital circuit can be determined by calculating four circuit design metrics, power consumption of the circuit, transmission delay, PDP, and EDP of the circuit. Transistor count is also an important design parameter that gives an idea about the area of the circuit.

From the table, it can be shown that CNFET technology provides the fastest speed compared to all other design methodologies. It is also evident that domino logic offers higher speed of operation as compared to static logic style. According to the table, FGMOS technology uses the least amount of power when discussing of the circuit's

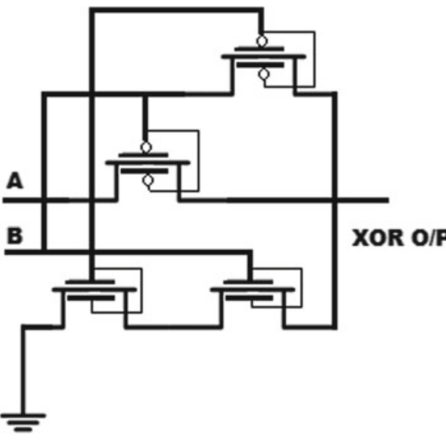

Fig. 11 FinFET-based XOR/XNOR cell [36]

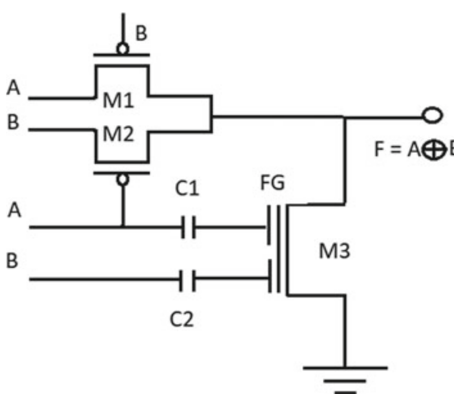

Fig. 12 FGMOS-based 3-T XOR cell [2]

Table 1 Comparative analysis of XOR/XNOR cell

Design parameters	[1]	[6]	[27]	[33]	[3]	[7]	[2]	[15]	[36]
Technology used	CMOS static			CMOS domino			FGMOS	CNFET	FinFET
Logic style	Hybrid		PTL	Hybrid		FDSTDL	PTL	MCML	PTL
Delay (ps)	14.86	14.42	32.64	15.94	5.341	50.11	27.9	2.27	–
PWR (μW)	2.169	2.105	2.65	7.23	0.314	0.477	5.39×10^{-6}	44.2	–
PDP (aJ)	32.23	31.291	86.5	115.2	1.675	23.9	0.00015	100.5	0.0254
EDP (aJ ps)	478.95	451.44	2823.2	1837	8.946	1197.75	0.0042	228.6	–
Transistor count	10	10	6	8	9	15	3	10	4
Technology node (nm)	22	22	22	22	22	22	22	16	16

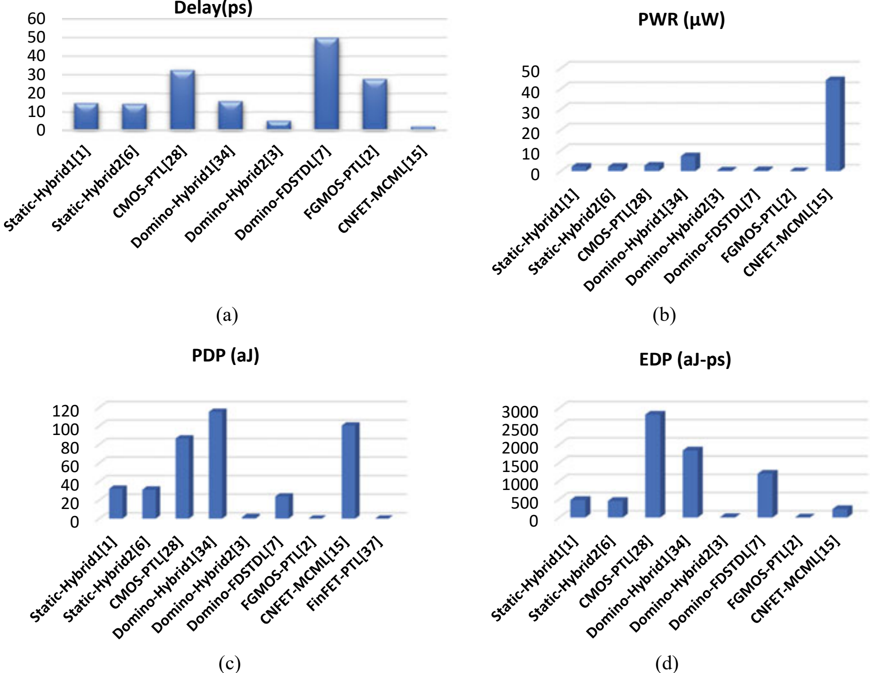

Fig. 13 Comparative analysis of **a** delay, **b** power consumption, **c** power delay product **d** energy delay product

power consumption. It is evident from the table that for lower technology node, non-conventional design techniques (e.g., FGMOS) or non-conventional devices (e.g., CNFET, FinFET) provide better results in term of all the design metrics. For the better understanding on the simulation results for various XOR/XNOR cell designs, clustered bar charts have been shown in Fig. 13.

These non-conventional design techniques have the magical feature to reduce the number of transistor and hence produce the better results. It has been discussed in the previous section that at lower technology node conventional design techniques may suffer from different short channel effects. Therefore, it is better to use conventional design methodologies for higher technology node.

5 Conclusion

In this paper, a detailed study of different conventional and non-conventional design methodologies has been performed. The reader will gain a comprehensive knowledge of the significance of each technology from this research article. It can be concluded that due to the ballistic transport of carriers in CNTFET technology, it is suitable

for high-speed applications while due to the threshold tunability and multiple input facility, FGMOS technology is much suitable for low-voltage low-power applications. The comparison investigation also demonstrated that the domino logic method is faster than static since it uses less transistors. However, a charge-sharing issue between the nodes affects domino logic performance. Finding the appropriate design process for the application is so crucial. Therefore, it is advised that non-conventional design methods emerge as a benefit below the 20 nm technological node, whereas at higher technology node conventional CMOS technology performs well.

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A Review on Neural Amplifier Design for Brain–Machine Interface

Sourav Nath, Koushik Guha, and Krishna Lal Baishnab

1 Introduction

Neural recording interfaces are now more widely used to monitor brain activity and for other neural disorder early detection and treatment. Precise and high-quality neural signal acquisition is quite challenging for the neuroresearcher. Important neural recording includes electrocorticograms (ECoG), [1–5] electroneurograms [6], and electroencephalogram (EEG). The system as a whole is closed loop. In order to treat the patient, neural signals are first recorded and processed, then analyzed, and finally a neurostimulator is turned on based on the analysis' findings [1, 7–10]. The essential requirements for the aforesaid applications are high-quality signal acquisition with low-noise amplifiers followed by signal conditioning circuits [11, 12].

Commercially available amplifier devices can be used to record neural activity. [13–16]. However, customizing neural amplifiers results in superior noise performance and reduced power consumption, as well as the advantages of lightweight and tiny form factor. These features of custom neural amplifier design allow device portability and implantable neurodevices. Dorman et al. [17] reported the first neural IC design. The noise-versus-power trade-off in neural amplifiers has seen consistent and significant improvements as a result of ongoing advances in IC fabrication technology and novel circuit design approaches. According to Moore's law, [18] which has so far correctly predicted the ongoing progress in dropping transistor sizes with concurrent advancements in IC performance, such IC chips' area density has likewise increased. Despite advances in IC-based brain amplifiers, creating such amplifiers remains a difficult task that necessitates knowledge in circuit design as well as a thorough understanding of the biological elements of neural recording.

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2 Neural Signal

Different techniques can be used to extract the neural signal, including intracranial electroencephalography (iEEG), electrocorticography (ECoG), electroencephalography (EEG), and intracranial electrocorticography, which extracts the extracellular activity of the neurons [19]. The extracted neurons signals are very low in amplitude ranges from 10 μV to 10 mV and frequency in the range of few 1 MHz to 10 kHz [19]. The EEG recording can be done by noninvasive method, i.e., from the electrode or sensors that are placed in the scalp and signals are recorded. The second method is the invasive method, the electrode is placed in the surface of the brain in the cerebral cortex, and the signals are captured. The brain signal captured from this method has higher SNR compared to the EEG method. High spatial and temporal resolution is seen in this type of signal [19]. The most efficient way to directly control an artificial prosthetic device is to record this signal using a microelectrode placed inside the scalp.

To capture the action potential signal produced by the interaction of sodium and potassium ions in the neuron cell membrane between the axon and dendrite, the third method involves inserting a biocompatible microelectrode probe into the brain [19]. This technique allows for the intercellular or extracellular recording of neuronal activity from a single neuron in the brain [20]. Extracellular action potentials (APs), which are produced when the membrane of a neuron depolarizes, have a millisecond time scale and a frequency range from of 100 Hz to 10 kHz. The APs occurs somewhere between 10 and 120 times every second. The extracellular APs' amplitude, which ranges from 50 to 500 μVpp, is influenced by how close the activated neuron is to the recording electrode [21]. The steps for extracting the local field potential (LFP) and APs (spikes) are described below. The mean field potential created by the neurons next to the electrode is known as the LFP. After sensing, the neural activity is first amplified, then high-pass filters (HPF) and low-pass filters (LPF) are used to obtain the LFP and identify the activity of individual neurons, respectively, utilizing algorithms for spike detection and sorting [22]. Lower-frequency brain waveforms with amplitudes ranging from 500 μVpp to 5 mVpp are included in the LFP. These potentials hold additional vital information and are used for brain–computer interface (BCI) applications [23, 24]. Extraction of neural spikes from the incoming signal is accomplished by high-pass filter. Amplitude threshold methods are used to detect these spikes. The features of the spikes are extracted and sorted next. It should be highlighted that neurons situated 50–100 μm from the electrode have an SNR, i.e., sufficient to distinguish between the activity of each individual unit [25, 26]. Despite the noise, it is still possible to identify spikes from neurons that are between 100 and 150 μm away from the electrode. These are clustered together to form a unit. However, neuron beyond the 150 μm distant from the electrode cannot be detected, and these signals act as background noise.

A pointed glass micropipette is inserted into a neuron of a slice of brain in the case of the extracellular and intracellular methods of recording described in the study [27]. After a few hours of recording, the neurons in the brain slice die. An amplifier

Table 1 Parameters of neural signal [19]

Signal type	Amplitude	Bandwidth
Extracellular action potential	50–500 μVpp	100 Hz–10 kHz
Intracellular action potential	10–70 mVpp	100 Hz–10 kHz
Local field potentials	0.5–5 mVpp	1 MHz–200 Hz
Electroencephalogram	10–400 μVpp	1 MHz–200 Hz
Electrocorticography	10–100 μVpp	1 MHz–200 Hz

is attached with the contact of electrolyte along with metal electrode positioned inside the micropipette. The range of intracellular AP amplitudes is 10 m to 70 mVpp. Table 1 summarizes the brain signal characteristics of various recording methods [19].

3 Neural Recording Architectures

Generally, there are three main neural recording architecture in the literature are shown in Fig. 1 [19]. The most popular architecture is the multichannel neural recording system shown in Fig. 1a, which uses an analog multiplexer to share an analog-to-digital converter (ADC) with all of the channels. This reduces the use of separate ADC for each channel which in turn reduces the overall circuit complexity of BMI. However, performance of analog multiplexer decreases when the number of channel increases drastically. The number of channels increased to improve the spatial resolution of the brain signals; as a result, the sampling frequency of the ADC and analog multiplexer had to be raised, which increased power consumption [19]. This limitation is fixed by using separate ADC for each channel which is shown in Fig. 1b.

Here, instead of using analog multiplexer, the architecture uses separate ADC for each channel followed by digital multiplexer. The primary benefit of utilizing a digital multiplexer is the elimination of power-hungry buffers and ADC drivers, as well as inter-channel cross-talk noise. This is because digital signals are more stable and have higher noise margins than analog signals do, making them more resistant to cross talk and other noise. However, the higher silicon area and power consumption in this architecture are due to the use of large number of ADCs. Therefore, approaches for reducing area and power should be used during the design phase. This architecture is reported in [28].

In the third architecture shown in Fig. 1c which uses one ADC for each n number of column with *m* number of rows, for all rows in a column, there is an analog multiplexer whose output is fed to the column ADC. All column output is fed to the digital multiplexer followed by wireless transmitter. For large number of channels, this architecture provides best solution. The analog multiplexers used in this design are small and less power hungry, as a result overall power consumption can be reduced along with cross talk. A further advantage of this architecture is that, since

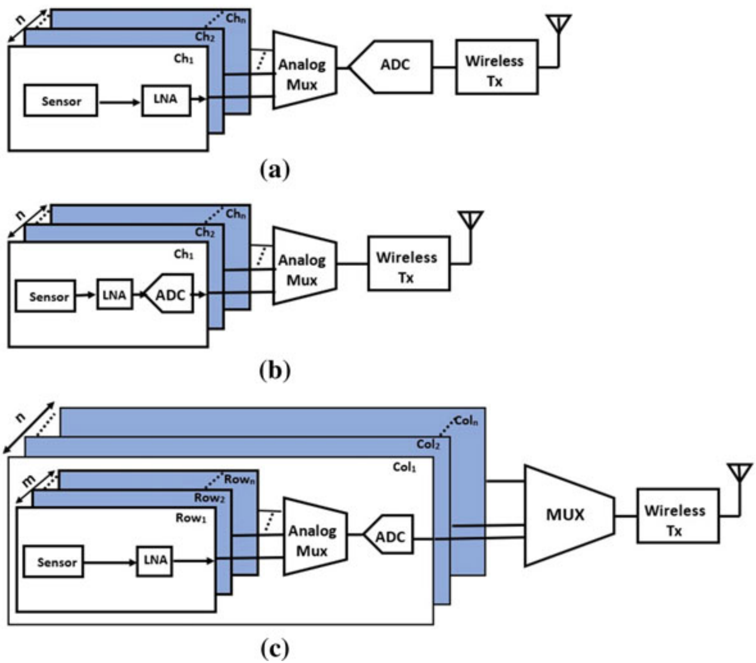

Fig. 1 Multichannel neural recording architectures [19]

the number of columns (n) defines how many ADCs will be present, choosing an acceptable value for n results in the lowest value for both power consumption and area, particularly when the total number of channels is fairly high. This architecture is discussed in [29].

Apart from these mainly used architecture, there are some non-popular architectures reported in the literature [30] where no ADC block is involved. Instead of ADC, the pulse-width modulation (PWM) technology is used to transform the analog signals to temporal duration before they are delivered to the outside of the body. Although it is desirable to increase the number of channels in order to improve the spatial resolution, doing so increases the output data rate and power consumption, particularly in the transmitter. Researchers have suggested many ways to compress the data in order to reduce the data rate. The time domain analysis is one of the primary ways to compress the data used in neural extracellular activity. Only the APs are identified and sent outside the body using this technique. The data can only be compressed by a maximum factor of 50 as the duty cycle of this approach is between 2 and 20%. Both in digital and analog domains this technique can be used.

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4 Neural Amplifiers

4.1 Design Requirements and Challenges

Modern neural recording systems are implanted in the brain and are powered by batteries. These systems ought to be compact, so that the brain only needs to be controlled in the smallest possible area to prevent harm to the neural cells. The lifespan of the systems is a further key need, and as a result, low power in the region of nW or lower μW is required. In order to prevent significant heat dissipation and consequent damage to the brain tissues, modest area (about 500 μm^2) and low-power dissipation are essential prerequisites in addition to a suitably high gain of at least 40 dB in the neural amplifier design. Recording high-quality brain potentials despite the presence of inherent electronic noise, noise caused by recording microelectrodes, and noise caused by external electrical interference is another difficult task in the amplification of neural signals [31].

By keeping a low input referred noise of roughly 5 μV, the noise that is inherent to electronics and recording electrodes can be reduced. This is characterized by another figure of merit called noise efficiency figure as defined in Eq. (1). It primarily serves to compare the effectiveness of neural amplifiers. However, there is a trade-off between noise and power consumption [32].

$$\mathrm{NEF} = V_{\mathrm{rms,in}}\sqrt{\frac{2I_{\mathrm{total}}}{\pi 4\mathrm{KTU_T BW}}} \tag{1}$$

where $V_{\mathrm{rms,in}}$ = Input referred noise, ITOT = Total amplifier bias current, thermal voltage, UT = 26 mV, Boltzmann's constant, $K = 1.38* 10–23\ \mathrm{J\ K^{-1}}$, T = Absolute temperature, and BW = Effective noise bandwidth of amplifier.

In order to reduce noise from outside interference, neural signals are recorded using the differential recording configuration that was previously stated in Sect. 3. In such a configuration, the interfering noise source would produce a signal that appeared as a common-mode signal at the differential input of the neural amplifier. This common-mode signal can be suppressed in an ideal circumstance by having a common mode rejection ratio (CMRR) of infinite. In the case of practical neural amplifiers, however, the CMRR varies from 60 to 120 dB, which is adequate for suppressing common mode interference in bio-potential recordings [31]. Furthermore, as the first major component of the neural recording system, the neural recording amplifier is directly interfaced with the microelectrodes and thus must meet the requirement of a high input impedance (in the MΩ range) that models the characteristics of the tissue–microelectrodes interface [32]. Input noise from the electrode can be suppressed using a variety of methods, the most popular and widespread of which is the use of an input dc blocking capacitor [33].

4.2 Neural Amplifier Topologies

There are several topologies suggested in the literature. Some of the most commonly used topologies are capacitive feedback topology, open-loop topology, Miller integrator feedback network (MIFN) topology, capacitive amplifier feedback network (CAFN) topology, and Miller compensated capacitive feedback network (MCCFN) topology [19]. The most widely used topology is the capacitive feedback topology as it has the feature of offset cancellation and provide low input referred noise. All these topologies are not discussed here, but all the topologies use the same most important block called operational transconductance amplifier (OTA) as low-noise amplifier (LNA). This paper mainly focusses on various OTA design techniques used in present and past state-of-the-art neural amplifier design.

4.3 Operational Transconductance Amplifier (OTA) Design Strategies

The design of brain–machine interfaces and recording devices has received a lot of interest in recent years. Several works have been published on the design of high-performance neural recording systems and amplifiers aimed at different design parameters, as well as the trade-offs between them. The capacity to record from more brain locations while retaining power dissipation and size, two key determining criteria, has been made possible by technological advancements in portable recording devices with numerous recording channels [31]. The design of neural amplifiers, the first significant building element in neural recording systems, is extremely important in determining the performance of the overall systems and has thus attracted a lot of attention over time. In Harrison and Charles [34], neural recording amplifier provides an appropriately high mid-band gain of roughly 40 dB with an input referred noise of 2.2 μV using a typical folded cascode OTA and MOS pseudo-resistors for rejecting offset at the tissue–electrode interface. However, the power dissipation of the designed amplifier was 80 μW, which is a major restriction for it to be used in a neural recording system. Similar works were performed by Mohseni and Najafi [35] who proposed an open-loop neural front-end amplifier design achieving a mid-band gain of around 35 dB but with a high input referred noise of approximately 10 μV, which is very high. A major breakthrough in the design of neural amplifier was proposed by Wattanapanitch et al. [33] in which the design of a capacitive feedback neural front-end amplifier was proposed as shown in Fig. 2a. The design was highly efficient in terms of a sufficiently high gain of around 40 dB with a very low input referred noise of 3.1 μV for recording action potentials which is achieved by employing a current scaling polysilicon-based resistors in the conventional folded cascode OTA as shown in Fig. 2b. The design included an amplifier as well as a tunable band-pass filter, as shown in Fig. 2a.

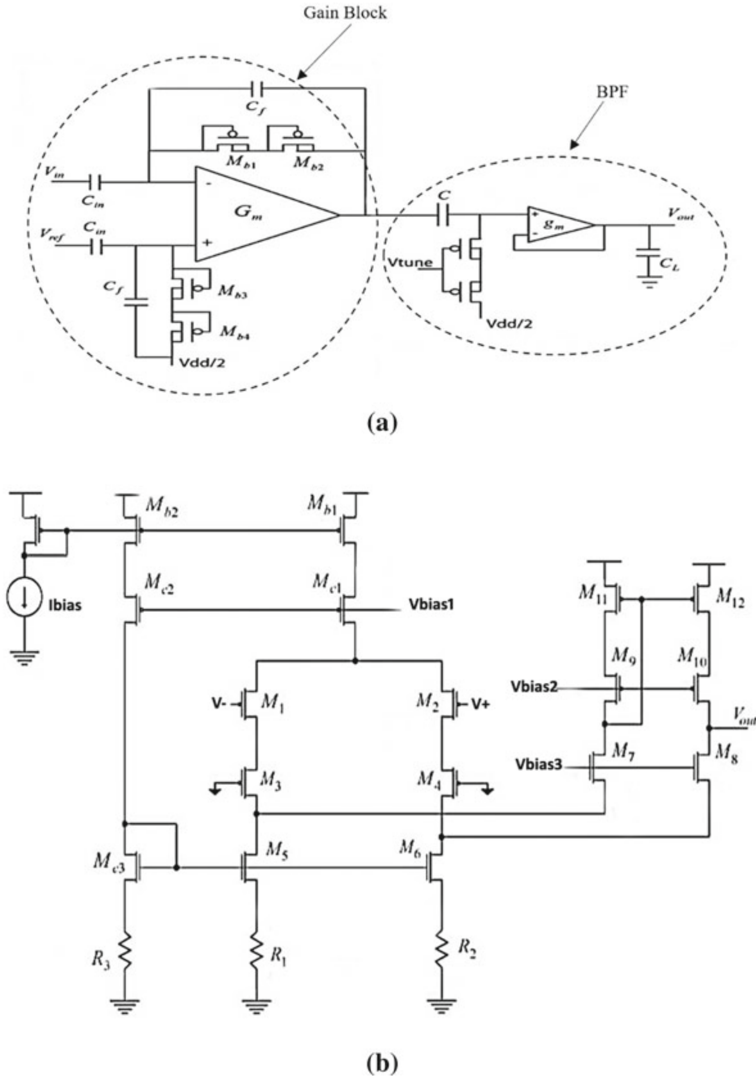

Fig. 2 **a** Block schematic of the neural front-end amplifier proposed in [4], **b** circuit schematic of the OTA used in [4]

By adjusting the filter's tunable bandwidth, the amplifier could be used to record both action potentials and local field potentials [33]. The design's high current consumption of 2.8 μA, which results in a higher power consumption compared to the state of the art, was a significant drawback. Additionally, the output swing of the amplifier designed is further constrained by using a standard folded cascode OTA. However, the current scaling method that they have proposed is a significant advancement in the design of low noise amplifiers, and it serves as the foundation

for many of the neural amplifiers created before it. A 100-channel neural recording system with a very high power dissipation of 13.5 mW/channel and input referred noise of 5.1 μV was proposed by Harrison et al.

A neural recording front-end amplifier with a high mid-band gain of 49.5 dB and a sufficient CMRR as well as a power supply rejection ratio (PSRR) of each 50 dB and an input referred noise of 5 μV was proposed by Gosselin [36] for a neural recording system chip for recording action potentials. However, it was discovered that the amplifier used 8 μW of power, which is a little too much when compared to more recent amplifier designs. Chaturvedi et al. [37] presented the design of a low power open-loop neural recording front-end amplifier as shown in Fig. 3a. As open-loop amplifier has more input referred noise than their capacitive feedback counterpart [38], the design utilized an OTA as shown in Fig. 3b employing a current stealing circuitry so as to minimize input referred noise contributed by the transistors M3 and M4 by lowering their transconductance. The design reported a very low power dissipation of 1.5 μW with an input referred noise of 5.5 μV. However, the mid-band gain was marginally acceptable having a value of 37 dB, which is a major limitation in their work. Majidzadeh et al. [39] proposed a neural recording front-end amplifier with improved noise efficiency figure. The mid-band gain achieved by the design was 49.5 dB with a low input referred noise of 3.5 μW. However, the power consumption was high with a value of 8.4 μW. Zhang et al. [40] proposed the design of a capacitive feedback amplifier for acquisition of neural signals. The design consisted of a fully differential telescopic cascode topology operating from 1 V supply. One more capacitive feedback complementary amplifier was fabricated on the same die, and a complementary open-loop amplifier chip was also designed. The main capacitive feedback amplifier reported a marginal mid-band gain of 40 dB, a high current consumption of 12 μA leading to a higher power dissipation and an input referred noise of 3.3 μV. Muller et al. [41] proposed an IC for acquiring neural signals, and the amplifier designed reported an input referred noise of approximately 5 μV, but with a high-power dissipation of 5 μW.

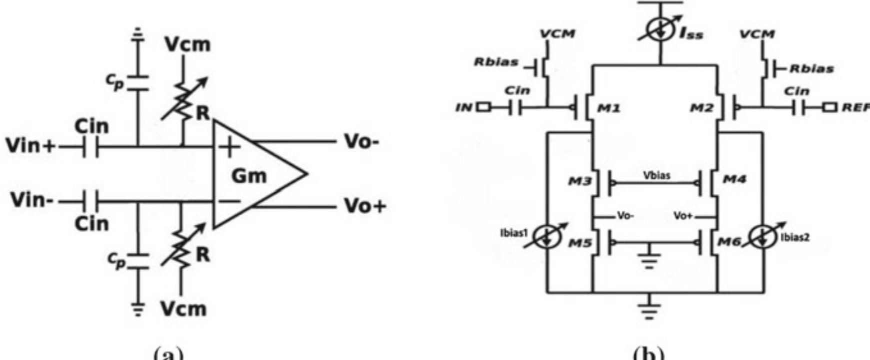

Fig. 3 **a** Block schematic of the neural front-end amplifier proposed in [37] based on open-loop topology, **b** circuit schematic of the OTA used in [37]

Bharucha et al. [42] presented an extensive literature survey of various neural front-end amplifiers proposed till 2014. A comparative analysis of different neural amplifier topologies was performed, and finally, it was concluded that capacitive feedback topologies performed efficiently in terms of better input referred noise with mid-band gain controlled by an impedance element which varies proportionally with bandwidth. On the other hand, open-loop topologies performed better in terms of lower power dissipation and area with the mid-band gain controlled by the transconductance amplifier itself. Lopez et al. [43] proposed capacitive feedback neural front-end amplifier operating from a 1.8 V supply which reported a low mid-band gain of 29.5 dB having bandwidth 6.1 kHz. The design reported an overall power dissipation of 7 μW/channel which is considerably high with an input noise of 3.8 μV. Amaya et al. [38] reported a neural amplifier design for recording action potentials. A study of various LNA topologies was also presented along with a new amplifier topology named as 'feed-forward compensated capacitive feedback' as shown in Fig. 4. The design was similar to the conventional MCCFN topology employing two OTA's, OTA1 realized by current reuse topology as in [40] and OTA2 realized using differential architecture; however, the compensation technique was modified to create double in the lower cut-off rather than a pole-splitting approach in MCCFN. An optimal-sizing procedure for MOS transistors based on design specifications as constraints was presented which was reported for the first time in their work. The design demonstrated an improved mid-band gain of 46 dB as compared to most of the previously reported works, with a low power dissipation of 1.92 μW and bandwidth of 7.4 kHz, which, however, was achieved at the cost of increased input referred noise and a marginal increase in area as compared to open loop and capacitive feedback topologies.

Dwivedi and Gogoi [44] presented a neural front-end amplifier targeting low power as its main criteria. This was achieved by voltage scaling; however, it resulted in a low mid-band gain of 34 dB and very high input noise of 24 μV as compared to other previously reported amplifier designs. Feng et al. [45] proposed a neural IC design

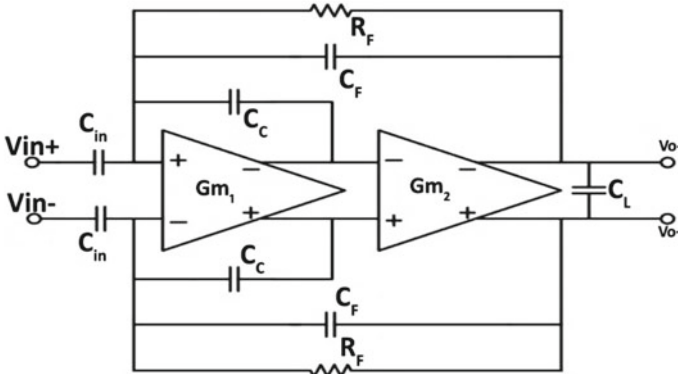

Fig. 4 Block schematic of the neural front-end amplifier proposed in [38]

and also tested it in in-vitro environment. The amplifier reported an appreciable improvement in mid-band gain with a value of 58.4 dB and a CMRR of around 90 dB, but a large trade-off in input referred noise having a value of 21 μV and a front-end power consumption of 742.5 μW/channel resulted in an overall poor performance. Ng et al. [46] presented a review of many neural recording systems and amplifier reported from the period 2007 to 2014. The works mostly reported an input referred noise ranging from 3.3 μV to 5.5 μV and a power dissipation in the range of 0.5 mW to 13.5 mW. It was concluded that none of the designs could achieve low power and low input noise at the same time and thus have an inherent trade-off among themselves. Ng et al. [47] proposed the design of a capacitive feedback neural amplifier. A single-ended inverter-based OTA was used to realize the first stage as shown in Fig. 5. The design reported a high mid-band gain of 52 dB with a power dissipation of 2.8 μW and input referred noise of 4.2 μV. As inverter-based OTA design resulted in a poor CMRR of around 50 dB, an additional common mode feedback network (CMFB) was designed for improving the CMRR. However, this was at the expense of greater area. Deepika and Rao [48] suggested a 180 nm low-noise neural front-end amplifier. The design drew inspiration from the works reported in [33], having the same topology and OTA architecture. However, the resistors were realized using MOS-based active resistors rather than polysilicon-based resistors as in [33]. The design reported a mid-band gain of 53 dB, however, with a very low bandwidth of 1.1 kHz which does not cover the entire action potential range. The current consumption was found to be 3.2 μA leading to a higher power dissipation. Kim et al. [49] reported a 32-channel neural recording system for deep brain stimulation which can be mainly used in treatment of Parkinson's disease. The amplifier reported in the design was realized using a capacitive feedback topology having two-stage OTA architecture as shown in Fig. 6 and achieved a mid-band gain of 55 dB with a bandwidth of 5.8 kHz, high input referred noise of 10.2 μV, and an overall front-end power dissipation/channel of 62.5 μW. A second-stage programmable gain amplifier (PGA) was designed in which the gain can be tuned by varying the input capacitances controlled by switches. Bhamra et al. [50] proposed a front-end architecture for biomedical applications. The architecture was designed with an objective of noise-power-area optimization considering their trade-off. The amplifier design consisted of a low noise front-end amplifier along with a second-stage PGA. Both the amplifiers were realized using fully differential folded cascode OTA architecture using the current scaling technique as in [33] for reducing power dissipation. However, the first-stage LNA had more restriction on the input referred noise as compared to the PGA. To decrease systematic offset, MIM capacitors were employed to implement the input and feedback capacitors, and a shared centroid layout method was used. The amplifier reported an overall gain adjustable in the range of 38–72 dB from a 1.4 V supply, with a bandwidth of around 10 kHz, which is low considering the use of two stage amplifiers. The reported CMRR was 72 dB with an input referred noise of 2.6 μV and a power dissipation of 5.8 μW, which is also quite high considering the trade- off with gain achieved.

Most recently, Park et al. [51] proposed a neural amplifier design which reported an input noise of 3.4 μV with 60 dB CMRR and a high front-end current consumption/

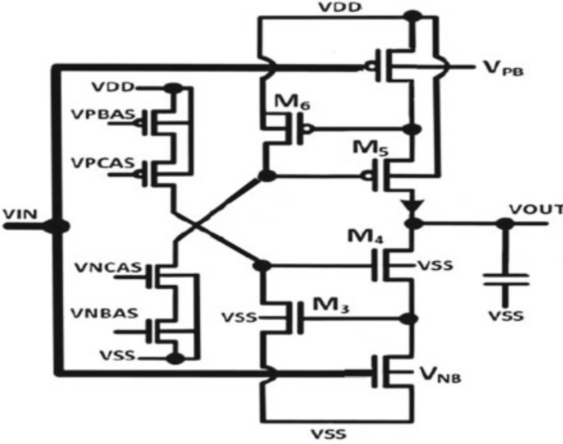

Fig. 5 Inverter-based OTA as proposed in [47]

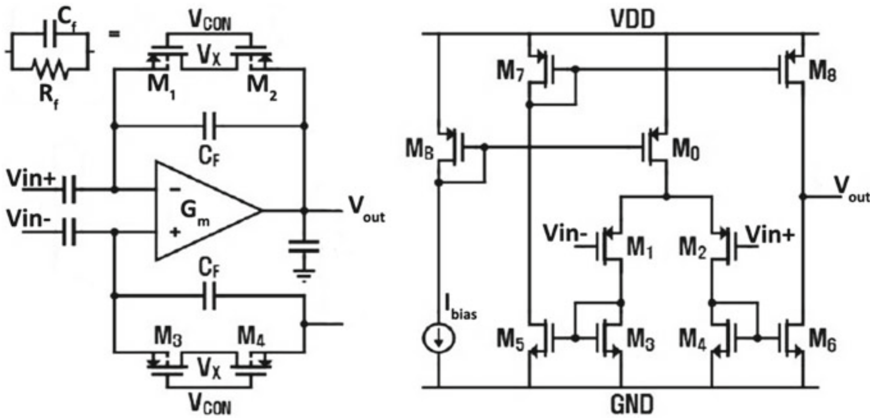

Fig. 6 Neural recoding amplifier with OTA topology as proposed in [49]

channel of 18 μA. Chandrakumar and Markovic [52] reported a capacitive feedback-based neural recording amplifier designed for recording both AP's and LFP's using a band-pass filter. Two amplifier stages were designed using a simple differential amplifier for both the stages. The amplifier reported a low mid-band gain of around 26 dB with a bandwidth of around 5 kHz for recording AP's. The power dissipation/channel was reported to be 2 μW with an input referred noise of 7 μV, which is also high considering all the trade-offs. Luo et al. [53] reported a neural amplifier having capacitive feedback topology using two-stage OTA architecture having miller compensation. The design reported a low mid-band gain of 26 dB with an input referred noise of 4.7 μV with a bandwidth of 13 kHz. The sizing of the MOS transistors was mainly aimed at achieving a high CMRR of 103 dB which is better

than most of the reported designs. Shen et al. [54] reported a neural recording amplifier with a split capacitor feedback. This means that the basic input and feedback capacitors were distributed/split into four capacitors each, which behaved in the same way as normal capacitive feedback. The main advantage of such an approach was an improved systematic offset voltage. The OTA was realized using an inverter stacking topology as shown in Fig. 7, which allows for a reduced power dissipation of 250 nW from a 1 V supply. However, the major limitation of such an approach is a reduction in the output swing due to vertical stacking of transistors. The mid-band gain reported is also very low and is equal to 25 dB with a 10 kHz bandwidth and a high input referred noise of 7 μV which are also the limitations of their proposed approach. Kim and Cha [55] proposed a capacitive feedback neural amplifier using a two-stage OTA. A telescopic cascode first stage was designed for low power dissipation, whereas a common source second stage was used with current buffer compensation. The use of such a compensation technique allowed an improvement in gain bandwidth product (GBW). For lower flicker noise, large sized input differential pair was designed. The design reported a sufficient mid-band gain of 39 dB with a CMRR of 78 dB and bandwidth of 10 kHz. However, the reported input referred noise was 5.8 μV with a current consumption of 2 μA from a 1.2 V supply voltage, which is again high considering the trade-off with the gain. Kim and Cha [56] proposed an ultra-low noise neural amplifier design using capacitive feedback topology. The design uses a telescopic OTA architecture with a CMFB circuitry for improving the CMRR. In order to improve the noise performance, the current reuse concept is used which boosts the input transconductance. Further, a two-stage OTA-based PGA is used for enhancing the gain and controlling the bandwidth. A capacitor bank of 4 input capacitors is used controlled by digitally programmable switches which tunes the gain from 43 to 61 dB and the bandwidth from 6.3 to 7.7 kHz. The power is reported to be 2.28 μW with a high input referred noise of 4.7 μV.

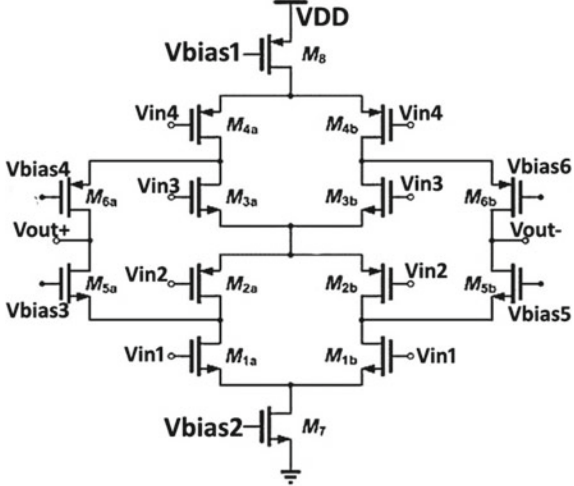

Fig. 7 Inverter stacking amplifier topology as proposed in [54]

In addition to these, many other researchers have also proposed the design of high performance PGA. Some of the benchmark works includes that by Perlin et al. [57], Ashmouny et al. [58], Dehsork et al. [59], among others. Perlin et al. [57] reported a capacitive feedback programmable neural amplifier architecture with gain programmed using tunable input capacitances as shown in Fig. 8. The capacitor selection was performed from a bank of capacitance in the range of 5pF to 55pF using digitally controlled switches and the OTA was realized using two-stage architecture. The gain was tuned in the range of 30–65 dB with a maximum bandwidth of 9 kHz, however, consuming a power of 50 μW. Ashmouny et al. [58] modified the design proposed in [57] by making the compensation capacitor in the two-stage OTA tunable along with the input capacitance, thus achieving an improvement in the bandwidth and phase margin along with varying gain while operating from 1 V supply consuming 9 μW of power. The mid-band gain varied in the range of 6–28 dB using digitally controlled switches as previously. Dehsork et al. [59] reported tunable neural recording capacitive feedback amplifier. The tuning was achieved using tunable pseudo-resistors rather than capacitors in the previous works as variation in capacitors leads to larger area requirement. However, this resulted in a very low tuning range of 52–57 dB in the mid-band gain with a bandwidth of 4–10 kHz. The input referred noise was reported to be approximately 3 μV with a higher power dissipation of 20 μW. Aliabad et al. [60] proposed a PGA with tunable gain and bandwidth by varying the pseudo resistors along with the capacitances. The gain varied in the range of 40–60 dB with a low bandwidth of 50–300 Hz suitable for local field potentials only. The design reported an ultra-low power of 160 nW with a high input referred noise of 4 μV.

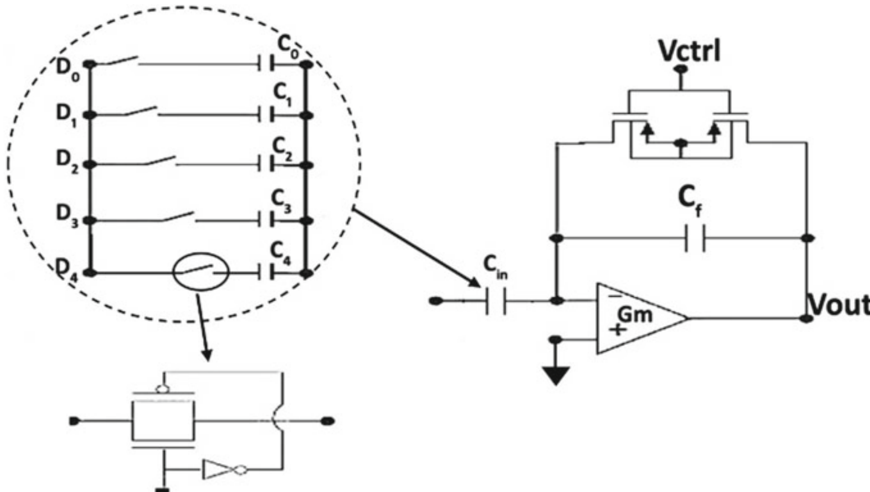

Fig. 8 Programmable gain amplifier (PGA) as proposed in [55]

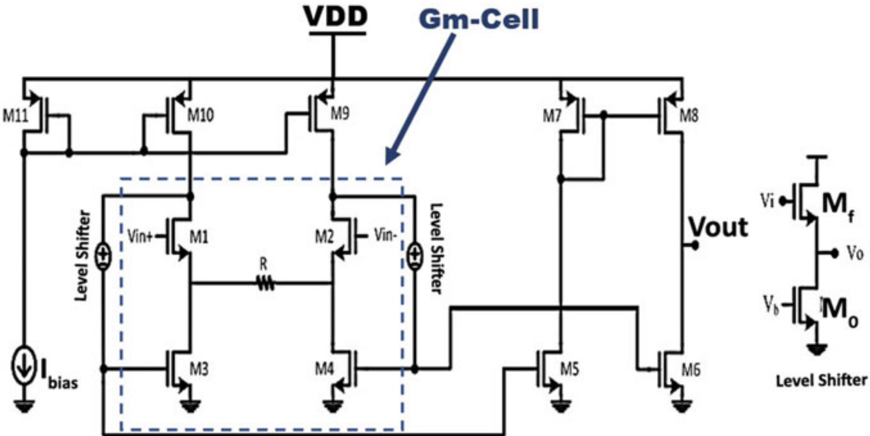

Fig. 9 OTA design [61]

Farouk et al. [61] in his work reported a transconductance cell (Gm-Cell) which used two flipped voltage follower (FVF) circuit and a resistor in between as shown in Fig. 9, and OTA using this cell is shown in Fig. 9. Upon using this technique, they got a most valuable feature of bias current independency on transconductance (Gm), thus making it more reliable to use it for low-power circuit design. They proposed this technique for designing the OTA, and further by using the same OTA, they showed two neural amplifier design, one is capacitive feedback, and other is integrator feedback neural amplifier, but from first one they got low mid-band gain around 38 dB, and from later one, they got high mid-band gain of around 58 dB. These two amplifiers show huge trade-off in noise and power along with chip area utilization.

Another most recent work reported by Sharma et al. [62] proposed some techniques to improve the circuit parameters. In this work, tunable pseudo-resistor structure, composite transistor structure, and gate-controlled bulk driven (GCBD) input stage structure is being proposed. The capacitive quasi-floating gate (CQFG) technique is used to make the tunable resistor, and GCBD technique is used to get some extra amount of gain from bulk and thus can suppress the input referred noise. Composite cascode technique is used to increase the effective length of transistor without decreasing the transit frequency (ft) of the transistor and also to get some extra channel impedance. Using all these techniques, the circuit parameter mainly noise has been improved significantly at the cost huge power consumption as well as silicon area. The circuit component along with OTA is shown in Fig. 10 for better understanding.

From the above discussion, it can be inferred that the major drawback in most of the reported works is that they cannot meet the demand of an ultra-low power in nW or lower μW range as well as ultra-low noise in nV or lower μV range design, at the same time while meeting the criteria of high gain of around 60 dB and bandwidth in the range of 10 kHz. Furthermore, it is evident that in most of the reported works capacitive feedback topology is employed rather than an open

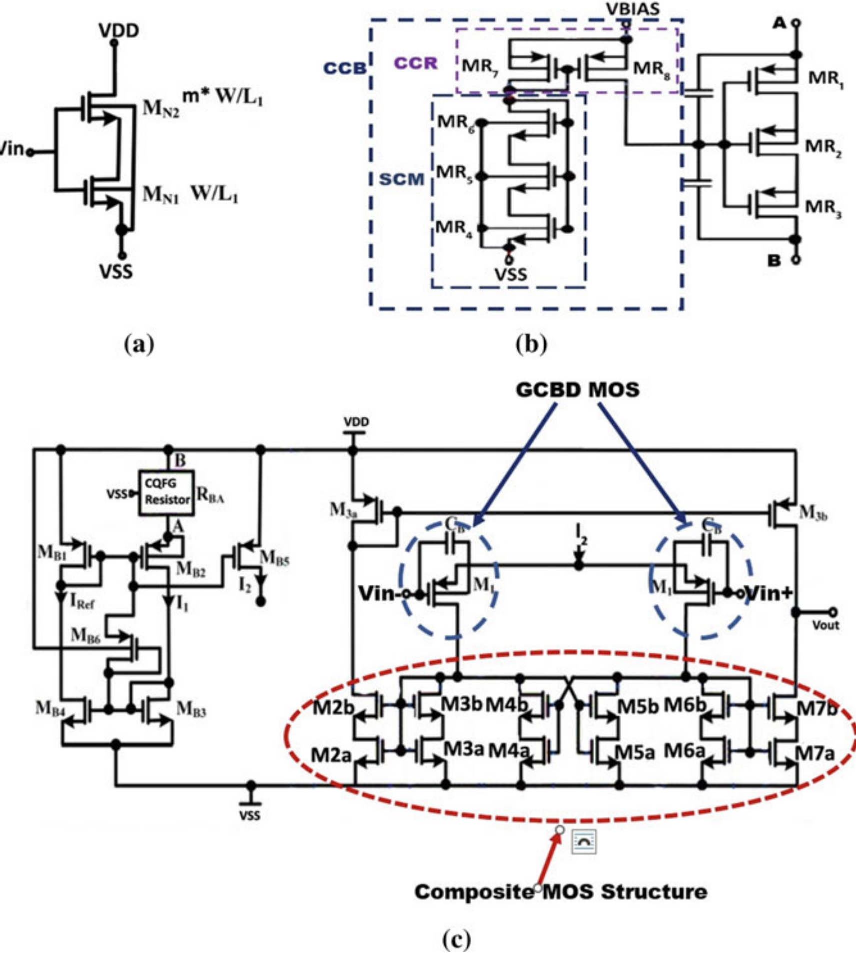

Fig. 10 **a** Composite MOS structure, **b** CQFN-based pseudo-resistor, **c** OTA design using this structure [62]

loop one, even though open-loop topology results in low area as well low power. The main reason behind this is that open-loop topology gives a comparatively higher input referred noise, which is another major design criteria for neural amplifiers [42]. Additionally, open-loop neural amplifiers have lesser ability to be reproduced without requiring large tuning in parameters [40]. Capacitive feedback, on the other hand, makes use of an impedance element to control the gain with corresponding trade-off with bandwidth [42] and can be easily reproduced for low noise or low power with suitable design techniques such as current scaling or current stealing. Thus, to design a high-performance neural amplifier, the following specifications as in Table 2 has to be met. The detail comparison of most prominent works is shown in Table 3.

Table 2 Specifications for neural amplifier/OTA design

Design criteria	Specifications
Slew rate, (SR) (V/μs)	≥10
Av (dB) (gain)	>40
f − 3dB (KHz) (cut-off Frequency)	≤15
$ICMR_{min}$, VCM (min) (V)	≥−1.6
$ICMR_{max}$, VCM (max) (V)	≤1.6
CMRR (dB)	>60
PSRR (dB)	> 50
Power, P (μW)	≤ 7
Output voltage (min), V_{out} (min) (V)	≥ −1.8
Output voltage (max), V_{out} (max) (V)	≤ 1.8
$Sn(f)$ (V/$\sqrt{}$Hz) (input referred noise)	≤500 n

Table 3 Detail comparison of neural amplifier/OTA design

Work	BW (Hz)	Gain (dB)	NEF	Vin rms (V)	Supply (V)	Power (μW)	Technology (μ)	Area (mm^2)
Wattana et al. [33]	0.025–7.2 k	39.5	2.7	3.1	2.8	7.56	0.5	0.16
Gosselin et al. [63]	105–9.2 k	52	4.9	5.6	1.8	8.6	0.18	0.05
Lee and Song [64]	0.5–500 k	47.6	2.91	2.24	1.8	0.855	0.18	0.065
Luo et al. [65]	0.3–200 k	NR	2.37	0.65	1.8	NR*	0.18	0.2
Zhang et al. [40]	0.5–10.5 k	40	2.9	2.2	1	NR*	0.13	0.072
Laskar et al. [66]	13.4 k	61.5	2.64	3.3	1.8	3.34	0.18	NR*
Farouk et al. [61]	110–9.7 k	52	4.27	4.7	1	5.2	0.13	0.047
Sharma et. al. [62]	5.3–8.6 k	49.9	2.27	2.6	0.9	11.5	0.18	0.192
Bagheri et al. [29]	400–6.5 k	52	7	5	1.2	9.5	0.13	0.018

5 Conclusion

From the literature survey carried out, it has been observed that there is sufficient gap in the research work in the current area of neural amplifier design and optimization. In the design of neural amplifier, there is a stringent requirement of achieving high gain

with acceptable bandwidth while maintaining a low noise and low power. But noise and power have an inherent trade-off among themselves. However, it has been seen that very few works have been reported in the design of neural amplifier considering this important aspect of high gain with ultra-low noise and ultra-low power trade-off. In this paper, the survey covered up to the literature published till the year 2022. Some prominent work has been compared finally to show the performance parameter comparison of the OTA for the use of neural amplifier design. Main focus of this review is to know the available state-of-the-art design of OTA for neural amplifier and also to find their limitations, so that improvement can be done and the research on neural amplifier may continue.

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Investigation on Performance for Silicon and GaAs Channel of Double-Gate MOSFETs

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1 Introduction

The performance properties of MOSFET are directly based on the dimensions of the device. Switching is a prime factor of field-effect transistors (FETs) due to its improvement in switching speed over bipolar transistors, and this technology has ruled over the semiconductor industry in past years as at present different low-power applications are related to it [1]. Currently, the dimensions of the transistors are reducing to 10 nm, and a lot of research work is performed in the nanometer region. However, in the modern electronic age of MOSFET, scaling is going to an end as the technology shifts from the microscale to the nanoscale with enhanced performance. Therefore, the research is going for a novel device that extends low-power circuit applications further on [2–4]. The roadmap of improving transistor density through miniaturization initiates different demerits in conventional MOSFETs size results in short-channel effects (SCEs) that become significant in terms of important phenomena those are drain-induced barrier lowering, hot carrier effects, channel length modulation, etc. [5, 6] Multiple-gate MOSFET structure like double-gate (DG) MOSFETs, SOI MOSFET, double FinFET (DFF) MOSFETs, tri-gate, gate all around MOSFETs and nanowire FETs, cylindrical surrounding gate MOSFETs, and FinFETs are devices that offer better control over conventional bulk MOSFET structures in terms of superior immunity to SCEs as natural length is an important constant in reducing SCEs, and also it predicts the variation in the value of threshold voltage of MOSFET devices [7] and higher current drive [8] which are considered as the suitable alternative for continuing the downscaling of CMOS technology down below 22 nm hereby sustaining Moore's law as well as the ITRS roadmap [9]. The

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main cause for reducing the dimension of the device is for increasing the number of transistors (CMOS structures) in an integrated circuit (IC) are low operating power, functionality, and speed as it moves from one technological node to another [6]. The downscaling in MOSFET device dimensions is the driving force for the current growth in the semiconductor industry showing a remarkable enhancement in power dissipation, cost, packaging density, and speed [10]. As MOSFET channel potential is controlled through every terminal, there occurs an increase in drain controllability and a decrease in gate controllability. With the scaling down of channel length (L), short-channel effects get enhanced and lead to greater Off current,punch through, and drain-induced barrier lowering effects; such unwanted effects weaken the control of the gate, and to overcome these effects, there is a need for stronger gate control. Such drawback helps in preventing the conventional MOSFET as a superior candidate for applications in the next-generation nanoscale devices. A lot of efforts are made to recover from such undesirable effects that have resulted in the growth of DG-MOSFET technology from many other technologies which show a unique variation of the multiple-gate transistors over conventional MOSFET architecture [8–11]. Sekigawa has invented the novel design of the DG-MOSFET in 1984 which holds greater promise for nanoscale transistors in highly dense IC design which has been adopted in the previous years as the mainstream device of logic structures for replacing it with the conventional planar MOSFETs for achieving enhanced suppression over short-channel effects. The basic technique of the DG-MOSFET utilizes placing both gate terminals at the top and bottom of the channel in an ultra-thin body, thereby allowing effective gate control over the channel from both gates. The enhanced gate control improves the "ON" state drain to source current, and the "OFF" state would reduce leakage current to flow between the drain and source terminals. The DG-MOSFET is electrostatically superior in comparison with single-gate MOSFET (SG-MOSFET) as here both gates are applied for controlling the channel from both sides. The two gates together control roughly twice as much current as a single gate, resulting in stronger switching signals. Each gate can control one half of the device, and its operation is completely independent of the other [12, 13]. With the recent advancements in small-scale device technology, silicon material is becoming a lesser choice of interest in ultra-scale in minimizing. Therefore, wide bandgap (WBG) semiconductors act as a replacement over silicon material in terms of lower on-resistance, quicker switching speed, high voltage, and temperature operation [14–20].

2 Device Architecture

Figure 1 represents the 2D cross-sectional schematic view of DG-MOSFET. The simulations are being carried out by using the Silvaco Atlas 2D device. The models used are Auger, conmob, fldmob, and SRH, respectively, which were incorporated. The Auger mobility model is applied for ionized impurity scattering as well as temperature dependence, Shockley–Read–Hall (SRH) recombination is applied for active carrier lifetime and density, and conmob and fldmob mobility model is applied

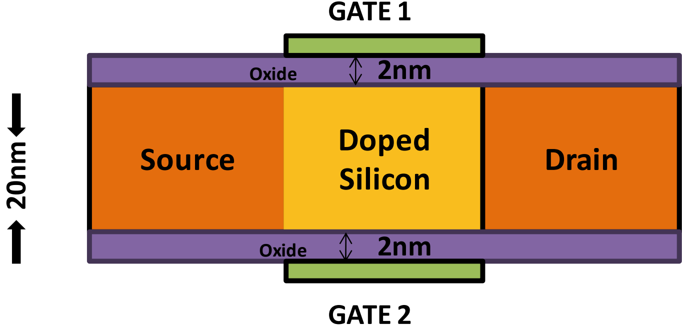

Fig. 1 2D Schematic view of DG-MOSFET

Table 1 Simulation parameters of DG-MOSFET

Parameters	Proposed DG-MOSFET
Gate length (nm)	50
Oxide thickness (nm)	2
Gate height (nm)	10
Source/drain region length (nm)	20
Doping concentration of source/drain (cm^{-3})	1×10^{20}
Dielectric constant of oxide (SiO_2)	3.9

for capturing the concentration and field-dependent mobilities. The parameters used in the simulation study are listed below in Table 1.

This manuscript is organized in the following order: Sect. 2 introduces the device architecture, Sect. 3 deals with comparative results and discussion, and Sect. 4 finally deals with the conclusion of the work.

3 Result and Discussion

Figure 2a, b depicts the input characteristics for silicon as well as GaAs channel double-gate MOSFET. With the GaAs channel device, it has obtained a greater On current value which results in a greater shift in threshold voltage variation and greater transconductance value.

Figure 3 depicts the output characteristic of DG-MOSFET. Here, it is noticed that the GaAs device has offered a greater drain current value than the silicon device, and the drain current value is nearly two times higher value as the electron concentration is more in GaAs case than the silicon device.

Figure 4 plot depicts that the threshold voltage is considered a useful parameter for the device. It is noticed from the plot that there is a positive shift in the threshold

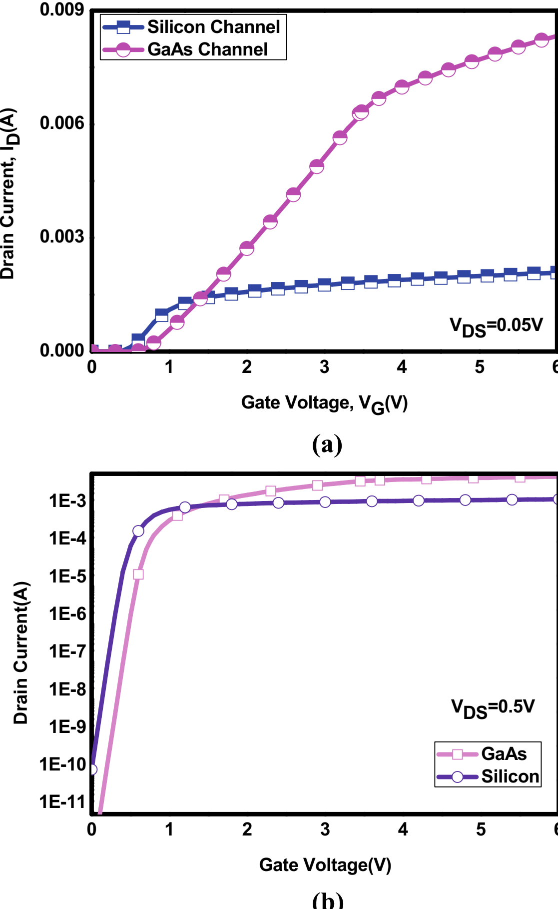

Fig. 2 **a** Input drain current characteristic (linear scale) for silicon and GaAs channel DG-MOSFET. **b** Input drain current characteristic (log scale) for silicon and GaAs channel DG-MOSFET

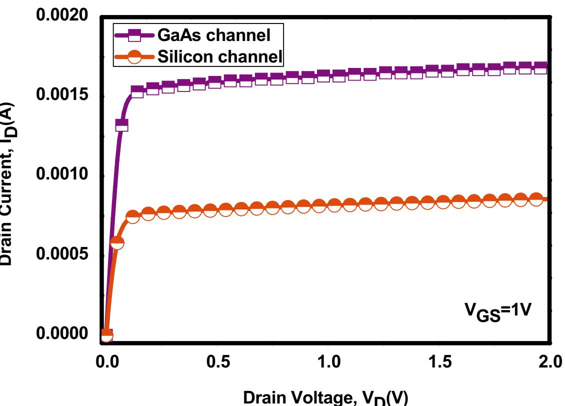

Fig. 3 Output drain current characteristic for silicon and GaAs channel DG-MOSFET

voltage value for the GaAs DG-MOSFET device which reflects a good indication for the device. Figure 5 plot represents the change in threshold voltage the two factors which are considered for the variation ΔV_t are both the charge effect and dielectric constant.

$$\Delta V_{\text{th}} = V_{\text{th2}} - V_{\text{th1}} \tag{1}$$

Figure 6 plot represents the variation in $I_{\text{ON}}/I_{\text{OFF}}$ variation. From this plot, it is noticed that the On current value is rising significantly with the GaAs channel from Fig. 2 and the Off state current value remains as it is, so the change ratio is maximum for the case of the GaAs channel.

Figure 7 plot depicts the variation in subthreshold slope. From this plot, is noticed that the SS value is higher for the case of the silicon channel, whereas it gets slightly reduced for the case of the GaAs channel.

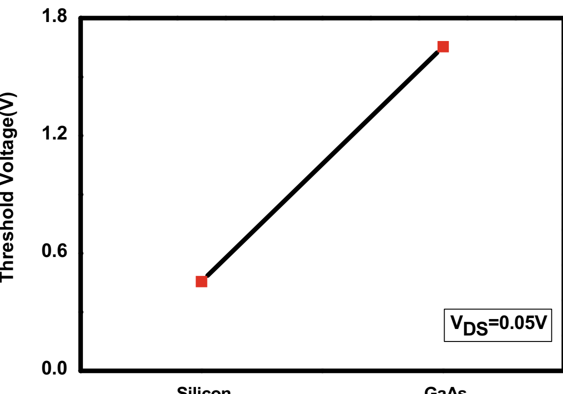

Fig. 4 Threshold voltage variation for silicon and GaAs channel DG-MOSFET

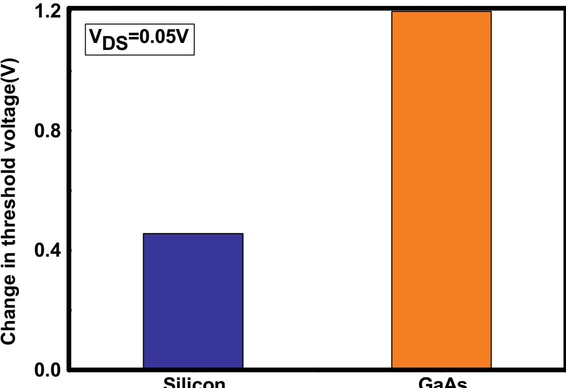

Fig. 5 Change in threshold voltage for silicon and GaAs channel DG-MOSFET

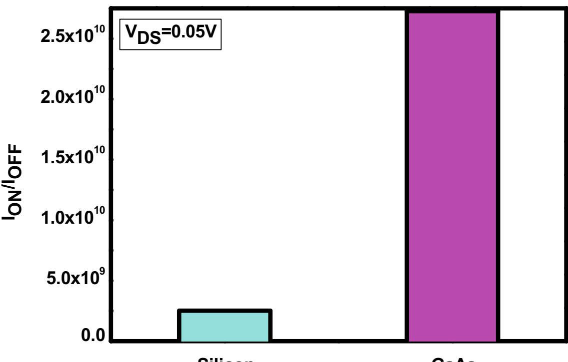

Fig. 6 I_{ON}/I_{OFF} ratio variation for silicon and GaAs channel DG-MOSFET

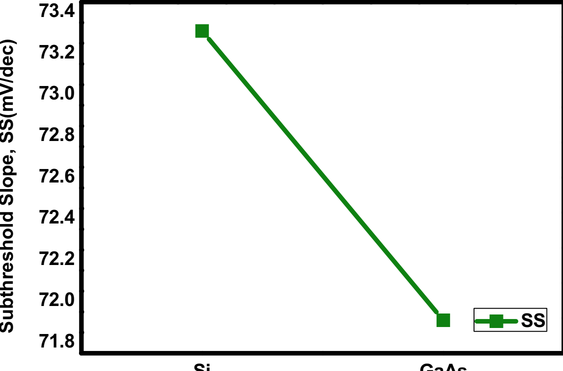

Fig. 7 Subthreshold slope variation for silicon and GaAs channel DG-MOSFET

$$S = \ln(10)\frac{dV_G}{d(\ln I_D)} \tag{2}$$

Figure 8 represents that with the increase in temperature value, Off current increases. In the strong inversion region with the increase in temperature crystal lattice vibration becomes more as a result mobility degradation takes place due to surface phonon scattering, whereas in the subthreshold region, the current value increases with an increase in temperature as it strongly depends on temperature and with the increase in value of temperature.

In Table 2, the DIBL and SS results for GaAs channel obtained are comparatively lesser as compare to silicon-channel-based DG-MOSFET device including other figure of merits.

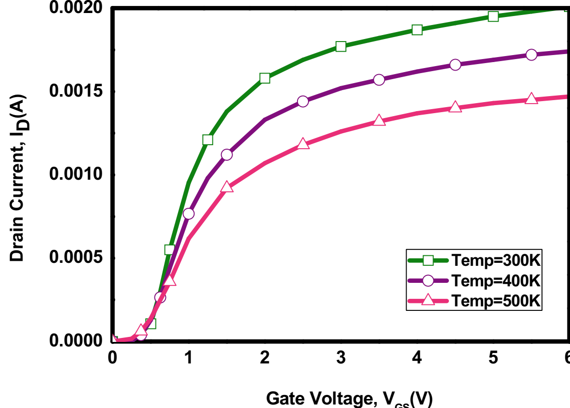

Fig. 8 Temperature variation effect for DG-MOSFET

Table 2 Comparison of figure of merits for both GaAS and silicon channel of DG-MOSFET

Parameters	Silicon channel	GaAs channel
Threshold voltage (V)	0.5	1.7
Change in threshold voltage (V)	0.45	1.2
SS (mV/dec)	73.4	71.6
DIBL (mV/V)	80	14
I_{ON}/I_{OFF}	2.0×10^9	2.5×10^{10}

4 Conclusion

DG-MOSFET has proved to be the pioneer of the next-generation transistors, and its emergence has sparked innumerable research venues for exploring. The prime motivation of our research work as we move forward from device design to its applications in the real world. Therefore it would be a development for the device design of DG-MOSFET which is more effective and also offers better gate voltage control. Double-gate (DG) MOSFETs offer superior electrical properties like higher drain current, higher effective mobility, and an improved subthreshold slope because of charge coupling. Wide bandgap devices facilitate power density, higher efficiency, and better reliability, which promises to revolutionize the future generations. To eradicate the issues of SCEs, the device can be investigated by enhancing the thickness of gate oxide between the gate terminal and channel material and also by changing the conventional SiO_2 layer with different high-k dielectric materials. Such type of unique design offers better results in both the On state and Off state current.

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Micro/Nanoelectronics Systems

Design of a Sensitivity-Improved On-Chip Temperature Sensor Based on Inverse-Widlar Architecture

Abhishek Kumar, Abhishek Sahu, Anurag Dwivedi, and Shree Prakash Tiwari

1 Introduction

With progressive reduction of device geometry to accommodate more transistors on a chip, the design processes have become more complex. The tolerances of some vital transistor characteristics like temperature, power consumption, etc., have become dire to control and manage. With increasing transistor density, various dynamic parameters such as localized hotspots, reduced logic reliability, reduced chip life, and power supply variations have starting to pose major design challenge [1–4]. Furthermore, increasing the operating frequency and number of cores in a processor, the dynamic thermal monitoring system has never been more crucial. When such processors are used at high utilization, more power is consumed and heat is generated [5]. To overcome this, task scheduling methods are used which focuses mostly on processor's under-utilization and neglect above-mentioned pernicious thermal effects. Hence, a thermal-aware task-scheduling method must be adopted for dynamic thermal management. One such method is load bouncing across the cores inside the processor chip away from overworked chip [4, 6, 7]. To locate overheating sites, which are also called hotspots, small on-chip temperature sensors are required which can fit adjacent to such cores [8–12].

Various temperature sensors have been proposed over the years which include resistance based, BJT based, diode based, thermal diffusion based, MOSFET based, etc. [13–17]. However, small area, less power consumption, high accuracy, and linearity make threshold-voltage-based temperature sensors a more suitable choice [18]. Single transistor and inverse-Widlar architectures are being widely used, but there is still a scope for further increasing the sensitivity. Even if the area of sensor

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element increases a little, the smaller ADC area in the sensor interface can compensate the increase.

In this work, an improved design of on-chip threshold-voltage-based temperature sensor is demonstrated with high sensitivity and high linearity, which utilizes self-stabilized inverse-Widlar architecture. The circuit was implemented using SCL 180 nm CMOS technology, and the simulation results were analyzed to extract the sensitivity and INL. The proposed temperature sensor exhibited enhanced performance parameters with sensitivity values reaching up to 1.81 mV/°C, and INL of ± 1 °C in the temperature range of − 20 to 100 °C, with small area requirement (438 μm^2). These results indicate that improved inverse-Widlar architecture is suitable for applications in efficient thermal guardbanding in high performance processors. Moreover, Monte Carlo simulations confirmed the reliability of the circuits.

2 Proposed Circuit

This section covers the thermal guardbanding and dependence of threshold voltage over temperature and nonlinearity incurred. Starting with the conventional designs of single MOS-based temperature sensors and inverse-Widlar, the proposed circuit improved inverse-Widlar architecture which is thoroughly discussed analytically.

2.1 Thermal Guardbanding and Need for Sensor Accuracy

In Fig. 1a, a block diagram of a typical multicore processor is shown [5, 19]. Multiple cores are clustered together repetitively inside a processor, making it convenient to place thermal monitors along the clusters with inside cores. With clever floor planning, these monitors can be placed close to highest density of cores [20]. These hotspots can vary significantly up to 20 °C from rest of the chip. Instantaneous change in power consumption will not result in instantaneous temperature changes due to thermal capacitances. These delays provide a small time window to regulate temperature by shifting the load to other cores. Maintaining these hotspots under a certain thermal threshold is of grave importance. Various processors available by different manufacturers claim this threshold to be in the range of 80–100 °C [1, 5]. When designing these chips, thermal managers have to make an informed decision about the safe operating zone of a processor with trade-off between performance and chip temperature.

In Fig. 1b, a typical operating temperature range of a processor is shown along with processor core status. Consider a typical processor chip with threshold temperature of 100 °C beyond which irreversible damage to chip may occur. When using a thermal management system with tolerance of 5 °C, due to false reading, damage may occur even when thermal monitor shows 95 °C. This will result in delayed action to control the temperature. To overcome this, shutdown process for cores will start earlier and

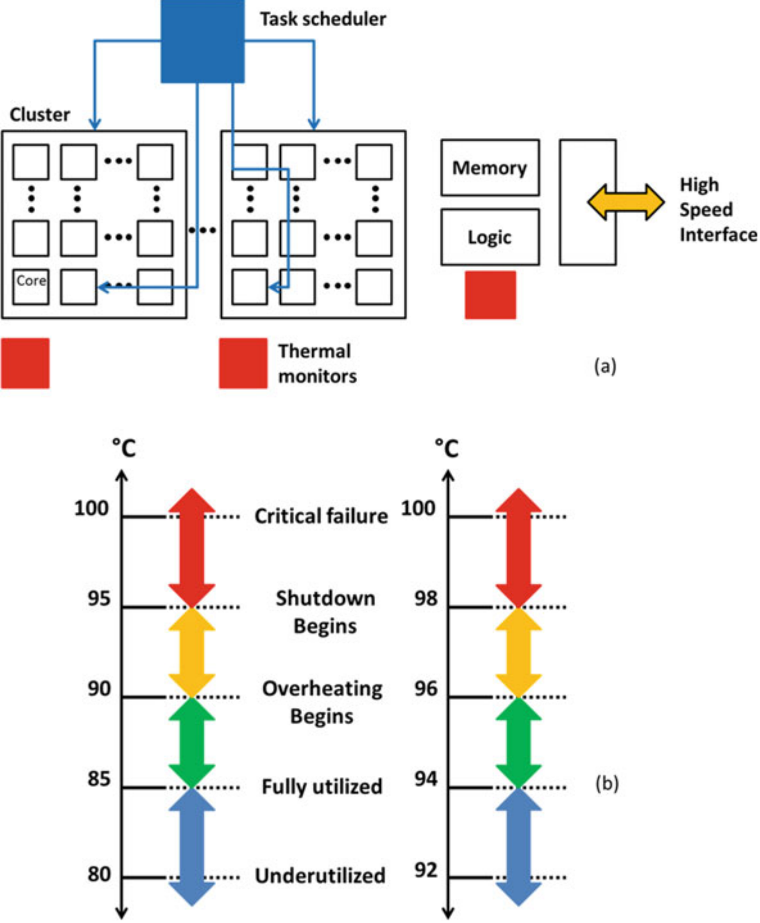

Fig. 1 **a** Typical high core processor with thermal sensors, and **b** an example of thermal guardbanding with comparison between sensors of 5 °C and 2 °C tolerance

hence result into underutilized processor. A thermal management system of lower tolerance, i.e., 2 °C, will help in effective processor utilization. From this example, it is quite evident that a low tolerance thermal management system is needed. For such cases, temperature sensor with high sensitivity and accuracy is of dire necessity. Consecutively to allocate these sensors inside of clusters with multiple cores, smaller size will be preferred.

Temperature sensors consisting of self-biased, supply voltage insensitive bias generator circuits will be focused in this work. These circuits provide the output which is directly dependent on threshold voltage V_{th} of a MOS transistor and the change in output can be indicated in terms of change in temperature. These circuits have very small area and consume very low power. The most basic threshold-voltage-based

temperature sensor can be a NMOS with resistive load. But, recently self-stabilized inverse-Widlar based temperature sensor circuit has also been proposed. Our work proposes improvements over this circuit by adding resistive loads to achieve higher sensitivity while keeping high linearity and small size.

2.2 *Effect of Temperature on Threshold Voltage*

The threshold voltage equation in a MOSFET is given as following [11, 18].

$$V_{\text{th}} = V_{t0} + \left(\gamma\sqrt{|2\phi_{\text{f}} - v_{\text{sb}}|} - \sqrt{|2\phi_{\text{f}}|}\right) \tag{1}$$

where V_{to} is threshold voltage when no biasing is applied and γ is body effect parameter, which is independent of change in temperature. The term ϕ_{f}, Fermi potential, varies with temperature, T as below.

$$\phi_{\text{f}} = \frac{\text{KT}}{q}\ln\frac{N_{\text{a}}}{N_{\text{i}}} \tag{2}$$

The term N_{i} varies logarithmically with temperature, and it will pose very small deviation to V_{th} in the small temperature zone of − 20 to 100 °C [21, 22]. We can call this deviation as nonlinearity in this range.

2.3 *Conventional Temperature Sensor Circuits*

MOSFET-based temperature sensors which are widely popular are given below.

(a) Basic single MOS-based sensor: A basic single MOS-based sensor circuit (ckt(1)) is given in Fig. 2a, which also functions as resistive load inverter. The NMOS M acts as the enhancement-type driver transistor and R_{L} acts as linear resistive load. The current through load R_{L} is also equal to the drain current of NMOS as I. At saturation, the current through NMOS M is given as following [11].

$$I = \frac{1}{2}\mu_n C_{\text{ox}}\frac{W}{L}(V_{\text{b}} - V_{\text{th}})^2 \tag{3}$$

V_{th} is threshold voltage for M. This same current I through load R_{L} can also be simply written using Ohm's law.

$$I = \frac{V_{\text{dd}} - V_{\text{out}}}{R_{\text{L}}} \tag{4}$$

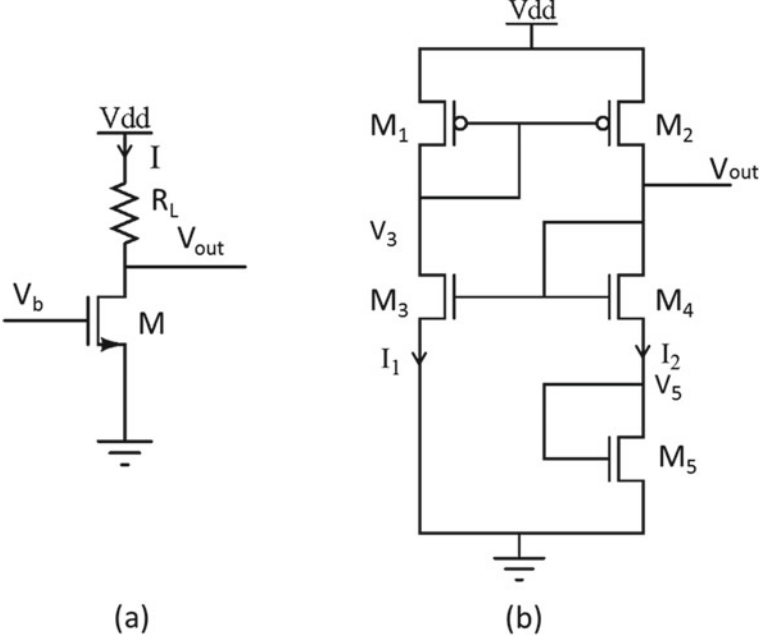

Fig. 2 Conventional temperature sensor circuit diagrams. **a** NMOS with resistive load (ckt(1)), and **b** inverse-Widlar architecture (ckt(2))

To keep *M* in *ON* state, the bias voltage V_b can be kept equal to V_{dd} (1.8 V). Upon solving, following expression for V_{out} is achieved.

$$V_{out} = V_{dd} - \frac{R_L}{2}\mu_n C_{ox}\frac{W}{L}(V_{dd} - V_{th})^2 \quad (5)$$

Here, it is evident that the V_{out} is dependent on supply voltage and threshold voltage to second degree. Hence, this circuit is not suitable for supply independent temperature sensor. Also, the previously discussed nonlinearity in V_{th} will be prominent here.

(b) Self-stabilized inverse-Widlar architecture based sensor: This circuit (ckt(2)) in Fig. 2b can be seen as two cross-coupled inverters forming a self-stabilized feedback loop. First inverter consists of transistors *M1* and *M3*, where *M1* acts as diode connected load. Similarly, second inverter consists of *M2*, *M4*, and *M5* where *M4* and *M5* are two series diode-connected loads. Hence, the loop has two inputs at the gates of *M1* and *M2* in feedback to each other. As the DC input impedance of both *M2* and *M3* are theoretically infinite, there will not be any DC loading at output of each inverter. Consider the output at terminal V_{out} for the given sensor architecture. Here, the dimensions of transistors *M1* and *M2* will drive the ratio between I_1 and I_2. Using the square law model for saturation current in MOS device, the ratio of current passing through *M3* and *M4* can be given by following equation.

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{out} - V_{t3})^2 = G_1 \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_4 (V_{out} - V_5 - V_{t4})^2 \tag{6}$$

where G_1 is the current mirror gain. Considering $\left(\frac{W}{L}\right)_3$ as K_3, $\left(\frac{W}{L}\right)_4$ as K_4, and $\tau_{34} = \sqrt{\frac{K_3}{G_1 K_4}}$, V_5 can be obtained.

$$V_5 = V_{out}(1 - \tau_{34}) + V_{T3}\tau_{34} - V_{t4} \tag{7}$$

Again considering the current passing through M_3 and M_5, following is obtained.

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{out} - V_{t3})^2 = G_1 \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_5 (V_5 - V_{t5})^2 \tag{8}$$

Similarly, for $\left(\frac{W}{L}\right)_5$ as K_5 and $\tau_{35} = \sqrt{\frac{K_3}{G_1 K_5}}$ following solution for V_5 is obtained.

$$V_5 = (V_{out} - V_{T3})\tau_{35} - V_{t5} \tag{9}$$

Using Eqs. (7) and (9), we get the following solution for V_{out}.

$$V_{out} = \frac{V_{t3}(\tau_{34} - \tau_{35}) - (V_{t5} + V_{t4})}{\tau_{35} + \tau_{34} - 1} \tag{10}$$

From Eq. (10), it can be inferred that during operation in active region, output voltage V_{out} is independent of supply voltage for unity current gain and only depends on threshold voltages and device dimensions. The current mirror gain G_1 can also be given as following.

$$G_1 = \frac{R_2}{R_1} \tag{11}$$

R_1 and R_2 are both resistances seen at output of both inverters, i.e., at V_3 and V_{out}, respectively. Using small signal analysis, where g_m is the transconductance and r is internal resistance for the transistor, G_1 can be calculated as the following equation.

$$G_1 \simeq \frac{r_2 \left\| \frac{1}{g_{m4}} + \frac{2}{g_{m5}} \right.}{r_3 \left\| \frac{1}{g_{m1}} \right.} \tag{12}$$

2.4 Proposed Temperature Sensor

Comparing the circuit (ckt(3)) in Fig. 3 with Fig. 2b, the arrangements of transistors *M3*, *M4*, and *M5* seem similar. Using the currents ratio of I_1 and I_2, the equation for V_{out} would turn out to be the same as in Eq. 10. This shows that the V_{out} is independent of V_{dd} as shown in Fig. 4 with negligible nonlinearity. So, to increase the gain G_2 for this circuit, R_2 needs to be increased. From Eq. (11), value of G_2 for this circuit can be increased by adding a resistor R_{L2} in series with M2. Also, to compensate for higher order nonlinearities, a resistor R_{L1} in series with M1 is also added. The current gain thus can be given as the following equation.

$$G_2 \simeq \frac{(R_{L2} + r_2)\left\|\left(\frac{1}{g_{m4}} + \frac{2}{g_{m5}}\right)\right.}{r_3\left\|\left(\frac{1}{g_{m1}} + R_{L2}\right)\right.} \tag{13}$$

With intuitive calculation using the typical values and $R_{L2} \gg R_{L1}$, it can be observed that the current gain $G_2 > G_1$, which is further proven using simulation.

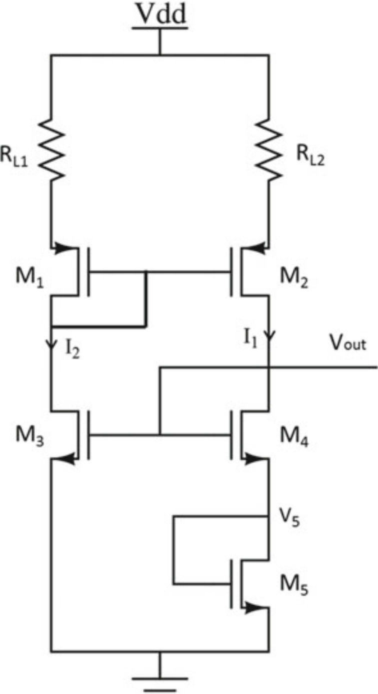

Fig. 3 Proposed self-stabilized inverse-Widlar architecture based sensor

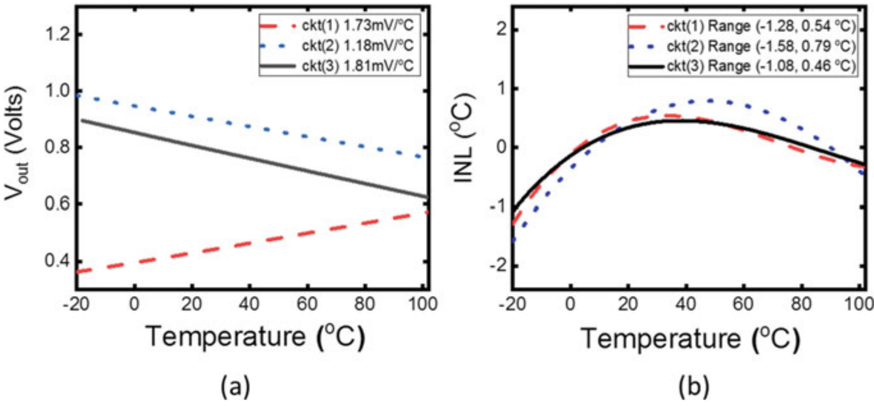

Fig. 4 **a** Output voltage of circuits, and **b** integral non-linearity of circuits versus temperature

3 Results and Discussions

All the circuits were simulated using cadence in SCL 180 nm technology. While designing the layout, area was kept minimal. The simulation was performed in the temperature range over − 20 to 100 °C for typical process corner (TT) as shown in Fig. 4. In Fig. 4a, the V_{out} for all the circuits are plotted with varying temperature and their integral non-linearity (INL) in terms of temperature variation in Fig. 4b. The ckt(1) is simulated with R_L of 1 KΩ and shows good sensitivity of 1.73 mV/°C but maximum INL of − 2.22 mV or − 1.28 °C. As our objective is to achieve supply independence and high linearity too, this will not be suitable for given application. Ckt(2) is supply independent but has very low sensitivity of 1.18 mV/°C and high maximum INL of − 1.86 mV which translates to 1.58 °C error. The proposed circuit in ckt(3) shows lowest maximum INL of 1.23 mV (0.68 °C) among all three and high sensitivity of 1.81 mV/°C. Hence, ckt(3) achieves less than 1 °C INL target in TT process corner.

The proposed circuit's performance for other process corners, fast–fast (FF), and slow-slow (SS), were also explored. For ckt(3), it can be observed here that output voltage, V_{out} for TT ranges from 0.98 to 0.77 V making the sensitivity of 1.81 mV/°C as shown in Fig. 5a. Also, the SS and FF process corners ranges are around 1.15–0.94 V and 0.77–0.54. respectively, maintaining the similar high sensitivity of 1.76 and 1.9 mV/°C. Since there is some non-uniformity in sensitivities for different process corners, error control circuitry post the sensor signal conditioning will become more vital. On the other hand. it is evident from the plot that due to process variations, there is a uniform voltage level variation of 0.39 V, which can be easily corrected with a single point calibration. It was also observed that for the FF process corner, above 105 °C, there is a sudden increase in integral nonlinearity (INL) which limits the operational range for such case. These sudden changes are not observed for TT and SS process corners earlier than 120 °C. Figure 5b shows the

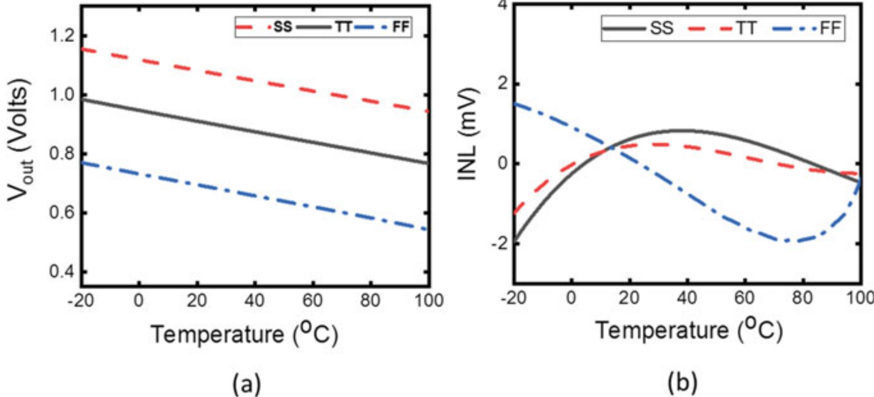

Fig. 5 **a** Output voltage variation, and **b** INL with change in temperature for different process corners for reduced-load self-stabiliszed inverse-Widlar architecture based sensor

deviation of V_{out} from mean output (most fitting line in TT with lowest peak error) in terms of INL. For ckt(3) the slow and typical (SS and TT) processes are more linear with minimal deviation from the mean than fast (FF) corner. The maximum nonlinearity is determined by the extremes of all process corners as in the range of − 1.95 and 1.5 mV which are both at − 20 °C.

The result in Fig. 5a has shown one point simulation for a various processes, the real-world results may vary based on process technologies. The 1000 points simulation for V_{out} and power consumption variation using Monte Carlo simulation technique were performed for TT process corner, and the results are shown in Fig. 6 for the proposed circuit ckt(3). Figure 6a shows all the process variation simulations and their mean average V_{out}. Here, the V_{out} ranges from 1.01 to 0.96 V with an average of 0.985 V at − 20 °C. The standard deviation is lowest near lower temperature (11 mV) but becomes high near higher temperature, reaching 12 mV at 100 °C. Power consumption varies in a very narrow range of 23–24 μW and average 23.2 μW with very small standard deviation of less than 0.2 μW as shown in Fig. 6b.

As modern processors may operate at lower supply voltage region for better power efficiency, sensor should also be evaluated for different supply voltages. In Fig. 7, the supply Vdd for ckt(3) is varied from 1.8 to 1.0 V, and the results show it to operate with same linearity till 1.1 V and starts deteriorating from 1.0 V making it more suitable for low voltage operation up to 1.1 V. Table 1 shows the comparative study with the previously results for similar application sensors. The proposed sensor shows highest sensitivity among all and is scalable for wide range of supply voltage. The error, however, increases w.r.t. [11] and [18] but is lesser than [12]. Comparing with [12] and [18], it consumes more power but equals [11].

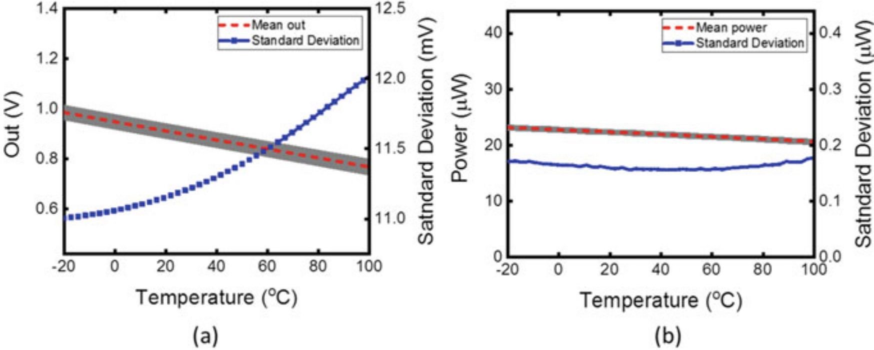

Fig. 6 1000 points Monte Carlo simulation of proposed sensor for **a** output voltage V_{out} and **b** power consumption, with mean and standard deviation

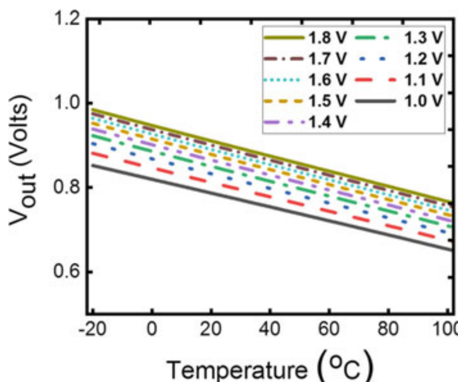

Fig. 7 Output voltage variation for different supply voltages V_{dd}

Table 1 Comparison of results with similar reports

SRAM	[11]	[12]	[18]	This work
Technology (nm)	65	180	180	180
Sensitivity (mV/°C)	1.27	0.95	1.12	**1.81**
Supply voltage (V)	[0.4, 1]	1.2	1.8	[1.1, 1.8]
Error (°C)	[− 0.4, 0.6]	[− 1.45, 1.5]	0.21	[− 1.06, 0.83]
Power consumption (μW)	25	0.071	1	23.2
Area (μm^2)	30.1	90,000	328.6	438

4 Conclusion

In this work, a linear and highly sensitive on-chip threshold-voltage-based temperature sensors for high workload demanding processors is demonstrated. Increasing current gain by controlling current passing through both the branches in supply independent self-stabilized inverse-Widlar temperature sensor architecture by adding resistors has increased both sensitivity and linearity. These modifications make it more suitable as on-chip temperature sensors for low tolerance applications. Small area requirements for the proposed designs make this circuit suitable alternative for dynamic thermal monitoring in high performance processors.

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A Modular and Compact RF-MEMS Step Attenuator for Beamforming Applications in the Evolving 5G/6G Scenario

Girolamo Tagliapietra and Jacopo Iannacci

1 Introduction

The comprehensive framework of 5G established itself as an historical field of convergence between several kinds of devices and communication paradigms. Beside the most "obvious" mobile telephony, the 5G network is expected to support a wide variety of communications in multiple contexts.

Beside the extensive use of artificial intelligence (AI) [1] and machine learning (ML) [2] to fully exploit the potentialities of the overall network, the expansion of the available spectrum and the adoption of mMIMO systems for the fixed wireless access (FWA) represent one of revolutionary aspects of 5G, as compared to the previous communication standards [3]. According to the last available released standard [4], the FWA is guaranteed by different kinds of cells, depending on the number of expected users (e.g., from the metro cells playing the role of the more classic base stations, up to the femtocells for interior deployment), operating over extended intervals of frequencies, namely frequency range 1 (FR1, from 410 to 7125 MHz) and frequency range 2 (FR2, from 24.25 to 71.0 GHz). The outstanding data rates conceived in 5G standard (20 Gb/s peak download, 10 Gb/s peak upload) rely on the exploitation of the high-frequency bands of FR2, and especially on the use of mMIMO systems, housing tens or hundreds of radiating elements and permitting an effective use of beamforming (BF) techniques to maximize the achievable throughput.

BF basically consists in varying the shape and/or the orientation of the radiation pattern of the overall antenna array in order to maximize the power emitted toward a

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specific direction and to suppress interfering signals by setting the nulls of the radiated pattern in correspondence of their directions of arrival [5]. At physical level, this is performed by varying the phase and the amplitude of the signal provided to each radiating element. Among the advantages of BF, it is possible to cite an increased physical system security, energy efficiency and in particular, an improved spectral efficiency [6]. In fact, by maximizing the power radiated toward the intended user equipment, the highest signal-to-noise ratio (and in turn, the throughput) will be achieved. From the point of view of the hardware architecture, the best arrangement is the so-called “hybrid architecture”, combining the advantages and overcoming the limitations of the fully analogic and of the fully digital architectures [6]. In hybrid architectures, the assignment of the phase and amplitude variation (called coding) is done partially in the digital domain, and partially in the analogic domain, by an analogic BF network connected to the radiating elements. Such network is composed by several transmit-receive-modules (TRM), controlling multiple or single radiating elements, and housing both passive electronics like a phase shifter and an attenuator and active electronics like amplifiers [7].

Some features of the 5G ecosystem, such as the tremendous amount of exchanged data by means of low-latency and reliable wireless links, determined the current trends in the research regarding the hardware components involved in mMIMO systems. In particular, while the use of high-frequency bands implies a reduced footprint of the radiating elements, and in turn, an increased attention toward the miniaturization, the operability over large fractions of the spectrum imposes a broadband and highly linear behavior for the employed components [8]. From a circuit point of view, while the juxtaposition of many signal routes and components on the same mMIMO platform requires a strict control over crosstalk interference (< -50 dB) [9], the required low-latency imposes a fast commutation time (< 1 ms) [10]. From the point of view of the electrical performances, the employed components should exhibit minimal losses (< -1 dB) and high isolation (< -30 dB) over the widest achievable range. Such challenges related to the current 5G paradigm and to the future 6G scenario could be effectively addressed by radio frequency micro-electromechanical-systems (RF-MEMS) technology, which has been developed since the early 90s to realize switches, switching matrixes, phase shifters, attenuators, filters, and the rest of passive components for RF front ends [11]. Regardless the operational principles of such microsystems based on the movement of metallic movable membranes (electrothermal, electromagnetic, piezoelectric, or electrostatic actuation), the constant attention of the research community toward such technology is due to the electrically remarkable, wideband, and linear behavior of its devices [12]. For this reason, MEMS-based components like switches, phase shifters, and attenuators represent suitable building blocks for realistic mMIMO systems in the current scenario [13].

Within the framework of the research on RF-MEMS components, the field of attenuators is generally less investigated as compared to switches or phase shifters. Although some analogic implementations have been proposed recently [14, 15], the vast majority of the available research items is focused on devices of digital nature (featuring a discrete number of attenuation states). Among the desirable features of

RF-MEMS attenuators, there are a broadband linear behavior and an extended reconfigurability, determining devices showing multiple and flat attenuation curves, along the widest possible frequency interval [16]. In fact, over the past years, researchers focused on extending the maximum attenuation level, the number of states, and the operational bandwidth of the devices. As an example, the 6-bit attenuator reported in [17] guarantees 64 attenuation levels, with a maximum attenuation of − 19.7 dB, along the 0–13 GHz frequency interval. In [18], the 7-bit attenuator encompassed in coplanar waveguide (CPW) configuration provides a greater number of states (128) and maximum attenuation (− 38.5 dB) over an increased interval (0–40 GHz). The device reported in [19] features a remarkable maximum attenuation of − 70 dB, achievable by 10 dB steps, and a reduced discrepancy between the measured and simulated attenuation levels (< 3%) along the 0–20 GHz range. As compared to the previous device, the attenuator considered in [20] is characterized by finer steps (5 dB) and by a comparable error (< 5%), although the maximum achievable attenuation is − 35 dB along the same frequency interval. The previous example has been developed as general-purpose attenuators, so that the attention has been paid to the constant improvement of the maximum achievable attenuation level and/or operational states and frequencies. This was reached at the expenses of the physical footprint of the final devices, which, in some cases, would make problematic the adoption of such devices in TRMs of realistic mMIMO systems. In fact, while the 3.2 mm^2 area reported in [20] is not alarming, the 8.77 mm^2 or the 2.45 × 4.34 mm^2 footprint of the devices reported in [17] and [19] are not suitable for mMIMO use cases.

In this work, a compact and modular arrangement of RF-MEMS step attenuator for beamforming applications in the current 5G framework is proposed. Starting from a reference 1-bit attenuation module comprising a movable membrane controlling two shunt resistors, versions offering different attenuation levels (− 1, − 2, − 3, and − 4 dB) are developed and arranged in a single compound. Such step attenuator is conceived for mMIMO antenna systems embedded in femtocells for interior deployment, whose reduced number of users does not require extensive BF capabilities (and thus, extremely high-performance attenuators and phase shifters with a high number of operational states). The specific frequency range of interest corresponds to the band of the 5G FR2 to be employed in European countries, ranging from 24.25 to 27.5 GHz.

The paper is organized as follows: after the summary regarding the 8-masks fabrication technology onto which the overall device relies, reported in the following Sect. 2, a validation of the simulation phase will be performed in Sect. 3. While in Sect. 4, the basic 1-bit attenuation module and the different versions will be described, in Sect. 5, the simulation results of the complete compound will be presented and discussed. Eventually, Sect. 6 will draw some considerations regarding the achieved results and the possible future improvements.

2 Fabrication Technology at Fondazione Bruno Kessler (FBK)

The layout of the proposed device relies on the 8-mask fabrication process employed at FBK facilities and detailed in the previous works [21–23].

The process is developed on a quartz or silicon wafer, with a diameter of 6 inches and a thickness of 525 μm, onto which a layer of silicon oxide is deposited. As shown in Fig. 1c, the first mask consists of a polycrystalline silicon (poly-silicon) layer, whose solids play the role of buried electrodes or resistors. The resistance of the bodies can be controlled by the doping of the material, thus obtaining the desired sheet resistance. The second mask is represented by the etching operated after the deposition of a silicon oxide layer, which is meant to isolate the stacked layers, and etched where an electrical connection between them must be established. With the same thickness as the ones of the first mask (630 nm), the solids of the third mask are made by a multi-metal compound based on aluminum, usually deposited where a buried section of the RF signal line must be traced. The subsequent fourth mask consists in the openings in the oxide that will be filled with the same material adopted for the fifth mask; the openings will electrically connect the multi-metal to the solids of the fifth mask: a layer of evaporated gold with a thickness of 150 nm (Fig. 1h). Such gold layer composes the contact surfaces onto which the movable membrane is expected to collapse during actuation, and it is also present where an electrical connection must be established with the subsequent layers. The sixth mask corresponds to a solid of photoresist sacrificial layer, onto which the movable membrane will be laid. Like the ground and signal sections of the CPW framework encompassing the device, the movable membrane consists of two layers of electroplated gold. Characterized by a thickness of nearly 2 μm, the first layer (seventh mask, Fig. 1k) will constitute the actual structure of the movable membrane, while the second and thicker (nearly 3 μm) layer of gold is electroplated on the surfaces of the membrane that are meant to be stiffer. The last step of the fabrication process is represented by the removal of sacrificial layer by oxygen plasma etching, thus releasing the movable structure.

3 Validation of the Simulation Phase

In the present section, simulation results and actual measurements concerning a 1-bit attenuation module will be compared in order to assess the accuracy of the simulation approach onto which the following results are drawn. The validation is based on a series 1-bit module which is dual as compared to the shunt design to be discussed in the following section. In fact, as visible in the layout displayed in Fig. 2, on one hand, the module is encompassed in CPW framework, and it features the same clamped–clamped and electrostatically driven membrane as the one reported in Fig. 5, but on the other, it is characterized by a series resistor inserted along the buried section

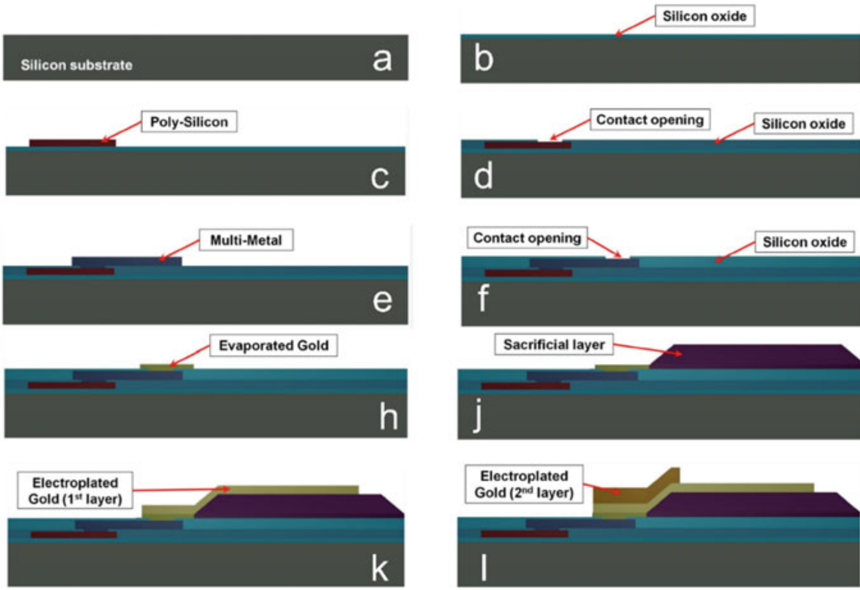

Fig. 1 Layering of the 8-masks fabrication process adopted at FBK facilities

of the RF signal line. From a functional point of view, when the membrane is in rest position (OFF state) the RF signal is attenuated by the series resistor, whereas the actuation of the membrane (ON state) will short-circuit the resistor. Additional considerations regarding the fabricated samples of this basic module can be found in [24].

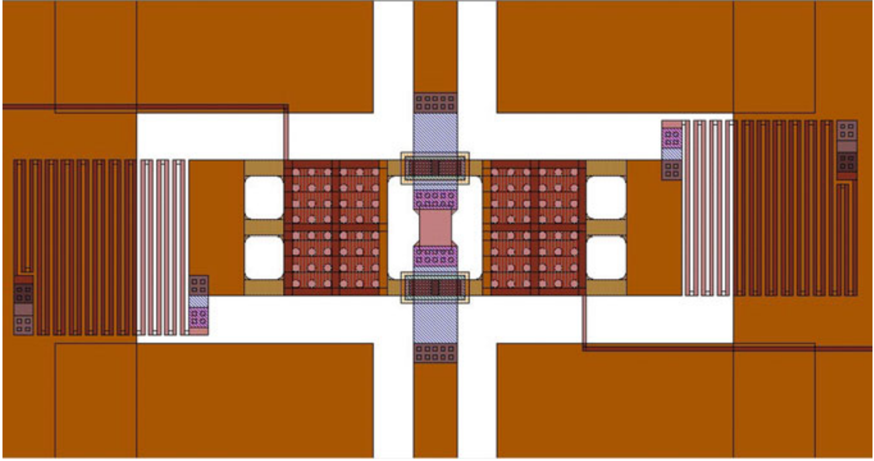

Fig. 2. 2D layout of the series 1-bit attenuator module employed for validation purpose

While the following simulation results have been computed in Ansys high-frequency structure simulator (HFSS) environment, based on the finite element method (FEM), the reported measurements on actual fabricated samples have been obtained by a programmable network analyzer (PNA) connected to ground-signal-ground (GSG) probes. As compared to the wide frequency interval considered in [24], the following comparisons are based on a narrower frequency range (30 GHz) for sake of a better visual comparison along the frequency range of interest. In Fig. 3, the comparison between simulated and measured return loss (S11) is reported, considering both the ON and OFF states. It is possible to notice that at the center frequency (25.87 GHz) of the 24.25–27.5 GHz interval of interest, the curves concerning the ON state show an 8 dB discrepancy. Despite the entity of such discrepancy, the facts that, except for the low frequencies (0–1 GHz), both the curves show a similar monotonic behavior, and the measurement curve does not exceed the − 10 dB threshold, make the discrepancy not particularly dramatic. In contrast to the previous case, the curves concerning the OFF state show an excellent agreement. In particular, the difference does not exceed the 0.6 dB along the entire 30 GHz interval, indicating a value of nearly 0.4 dB at the center frequency.

In Fig. 4, the comparison between simulated and measured S21 curves is reported, considering both the ON and OFF states. In the ON state, the attenuation caused to the RF signal is due to the losses introduced by the device itself, so that the curves represent the insertion loss of the device. In this case, the difference does not exceed the 0.3 dB along the entire 30 GHz interval, showing a value of nearly 0.1 dB at the center frequency. In the OFF state, the attenuation is caused by the resistor inserted along the signal line. So that the comparison is between two attenuation curves. As visible in the following plot, the curves concerning the OFF state show a good agreement, with a maximum difference of 0.8 dB at low frequencies, and a difference of nearly 0.3 dB at the center frequency.

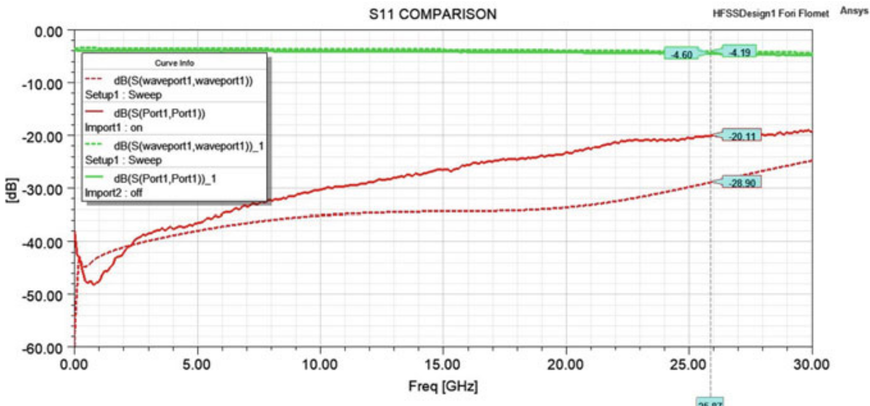

Fig. 3 Comparison between the simulated (dashed) and the measured (solid) curves reporting the return loss of the series attenuation module, in both the ON (red) and OFF (green) states

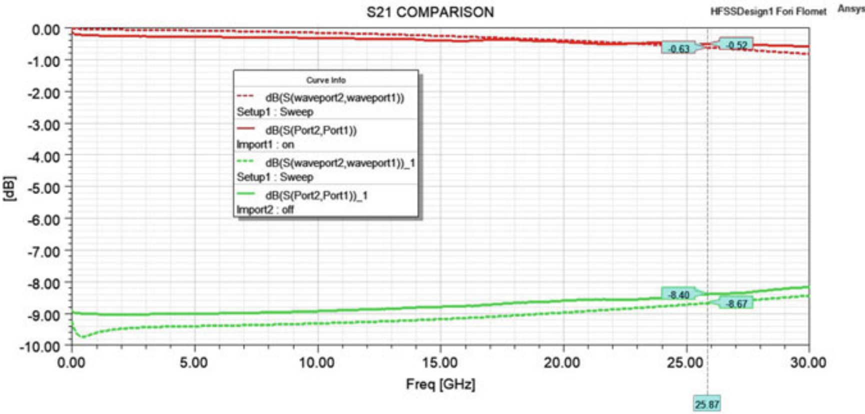

Fig. 4 Comparison between the simulated (dashed) and the measured (solid) curves reporting the insertion loss and attenuation curves of the series module, in both the ON (red) and OFF (green) states

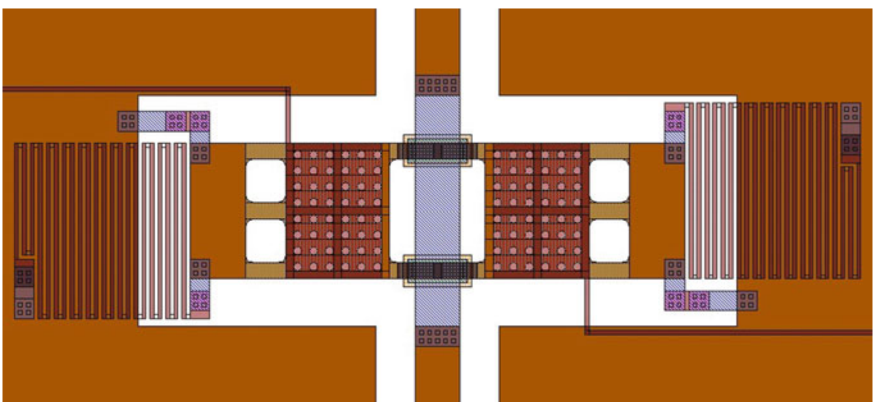

Fig. 5. 2D layout of the basic 1-bit shunt attenuator module

From a general point of view, the reported curves demonstrate a good agreement: while on the qualitative side the simulated and measured curves display a quite similar monotonic behavior, on the quantitative side, most of the reported curves exhibit minimal discrepancies, quantifiable in fractions of a decibel. Such considerations about the correctness of the simulation procedure lay the foundations for the simulation results reported in the following section.

4 Design Principles of the Basic Modules

The basic attenuator module is a 2-states (ON/OFF) device, encompassed in CPW transmission line framework and driven by electrostatic actuation. As visible in Fig. 5, the two central poly-silicon electrodes (in red) are buried under the membrane, and they will cause the actuation by electrostatic attraction, once bias voltage is provided by the routes. The movable membrane is kept at null voltage by the serpentine-shaped decoupling resistors connecting the ground planes to the anchor points of the structure. Their huge resistance value (nearly 300 kΩ) avoids any possible flow of the RF signal toward the ground planes, which may take place just by means of the other two smaller shunt resistors. Their dimensions (together with the sheet resistance of the poly-silicon) determine their resistance, and thus, the attenuation caused to the RF signal traveling along those route. The electrical connection between the different conductive layers is represented by the small quadrangular openings.

In the OFF state, the central membrane is elevated (in its rest position), and the RF signal travels along the central line, composed by the two uppermost electroplated gold layers and by the evaporated gold transitions to the central and buried multi-metal section (in light blue). In the ON state, the membrane is in touch with the underlying contact pads of electroplated gold. Because of the electrical connection between the contact pads and the buried multi-metal signal line, part of the RF signal power will be dissipated along the conductive paths that link the movable structure and the ground planes. Starting from the anchor points of the membrane, these paths develop through the transitions of electroplated gold and multi-metal leading to the shunt resistors and vice versa up to the ground planes.

From a mechanical point of view, the central MEMS structure reported in Fig. 5 covers an area of $620 \times 170\ \mu m^2$, including a $70 \times 170\ \mu m^2$ anchor, three $50 \times 20\ \mu m^2$ straight supports, and a $130 \times 170\ \mu m^2$ drilled area facing the buried electrode, on both sides of the RF signal line. The default thickness of the movable membrane corresponds to the one of the first layer of electroplated gold (nearly 2 μm), and it reaches a total 5 μm thickness in the points where the second gold layer is electroplated for an enhanced stiffness, such as on the borders of the drilled areas and on the anchoring points. The drills and the central opening in the movable structure have a twofold purpose: to ease the removal of the photoresist sacrificial layer during the last fabrication step and to decrease the viscose friction of the air during the actuation of the membrane. In the ideal condition, the actuation of such membrane would take place when a 35 V bias is provided, however, as reported in [24], fabricated samples demonstrated to operate in the range 48–50 V. The reason behind such discrepancy relies on the presence of residual stress within the gold layers of the membrane, because of the thermic treatments involved in the fabrication.

The actuation voltage (also known as “pull-in voltage”) in the ideal case and the vertical deformation of the membrane at pull-in have been retrieved by simulations performed in Ansys Workbench environment. As visible in Fig. 6, with a bias of 35 V, the maximum vertical displacement covers the entire air gap between the membrane in rest position and the underlying surfaces (nearly 3 μm). The contact is established

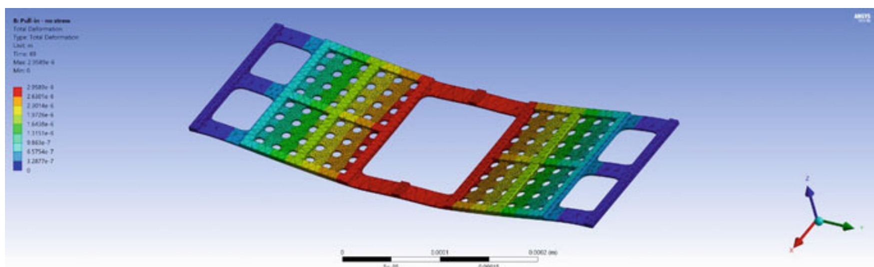

Fig. 6 Vertical displacement of the considered membrane at the ideal actuation voltage in Ansys Workbench

in the central part, while the lateral drilled parts of the membrane are sloped but quite planar, because of the enhanced stiffness offered by the second layer of electroplated gold.

From the point of view of the electromagnetic behavior, such kind of attenuation module based on a shunt arrangement demonstrated promising results in terms of broadband flatness of the attenuation curve. In fact, measured samples featuring poly-silicon resistors with a sheet resistance of 140 Ω/sq demonstrated an attenuation in the range between − 3.5 dB and − 5.2 dB up to 50 GHz (S21 in ON state) and an insertion loss better than − 2.6 dB along the same frequency interval (S21 in OFF state). Additional considerations regarding the previously fabricated samples can be found in [24].

Because of the favorable premises of such arrangement, a complete 3D model has been developed, parametrized, analyzed, and optimized in Ansys HFSS in order to obtain four versions of the present design, targeting − 1 dB, − 2 dB, − 3 dB, and − 4 dB attenuation levels along the desired 24.25–27.5 GHz frequency interval. As shown in Fig. 7, the parametrization of the module affected the dimensional features of the shunt resistors. The third parametrized feature is the sheet resistance of the poly-silicon, initially set to a reference value of 100 Ω/sq. On the basis of the resistor's width and length, the adjacent bodies have been parametrized, such as the length of the multi-metal transition toward the anchors, as well as the width and the positions of the other transitions toward the ground planes.

The simulated results obtained after the optimization phase are quite satisfying, since all the modules show a return loss (S11) smaller than − 10 dB along the entire 0–30 GHz considered interval, as visible in Figs. 8, 9, 10, and 11. In particular, the − 1 dB version reported in Fig. 11 exhibits the smaller return loss within the 24.25–27.5 GHz interval of interest, ranging from − 22.26 dB to − 24.49 dB, with a value of − 23.35 dB at the center frequency (25.87 GHz). The results regarding the − 1 dB version have been achieved by a 190 Ω/sq sheet resistance. In terms of attenuation, all the four modules display a quite precise value in the vicinity of the center frequency; in fact, the greatest discrepancy between the expected and the achieved attenuation value can be traced in the case of the − 3 dB module in Fig. 9. The attenuation value is rather flat along the frequency range of interest for all the

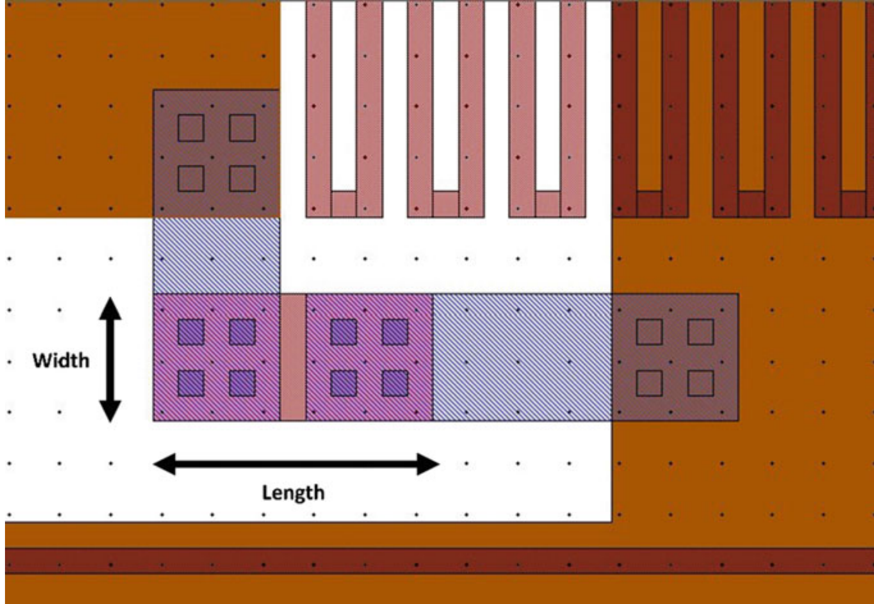

Fig. 7 Detail of the shunt poly-silicon shunt resistor, linked to the gold layers by quadrangular transitions and buried multi-metal sections, and dimensional parameters considered during the optimization phase

four modules, since as compared to the target value achieved at the center frequency, the value achieved at the edges shows a minimum variation of ± 0.09 dB (Fig. 10) and a maximum variation of ± 0.12 dB (Fig. 8).

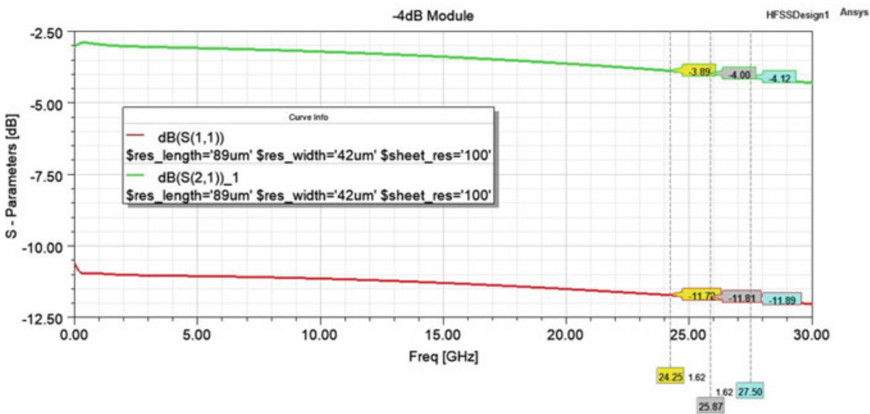

Fig. 8 Simulated S parameters of the − 4 dB version of the attenuation module in ON state

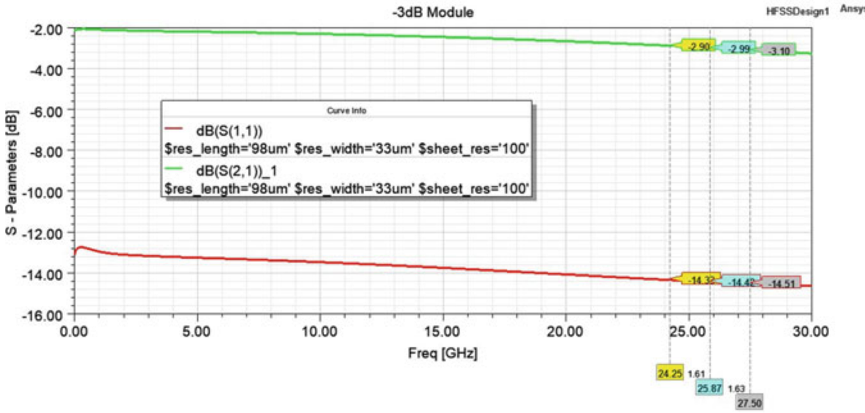

Fig. 9 Simulated S parameters of the − 3 dB version of the attenuation module in ON state

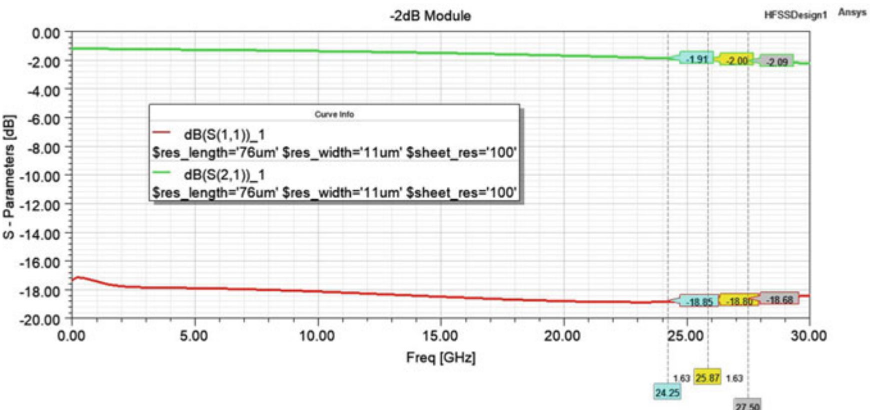

Fig. 10 Simulated S parameters of the − 2 dB version of the attenuation module in ON state

5 Complete Compound

In this section, the performance of the compound will be critically evaluated, on the basis of the simulation results obtained in Ansys HFSS environment. In the complete layout, the single modules discussed in the previous section have been combined by sequentially collocating them, in order of attenuation, and by maintaining a spacing of 100 μm between the outer border of the contact pads underneath each movable membrane. In terms of dimensions, the overall layout is quite compact, with a total footprint of 1.56×1.35 mm^2. As visible in Fig. 12, the first − 4 dB module features the widest resistors (42×89 μm^2), while the subsequent − 3 dB module is characterized by 33×98 μm^2 resistors. The remaining − 2 dB and − 1 dB modules comprise 76×11 μm^2 and 151×10 μm^2 resistors, respectively. For sake of conciseness, out

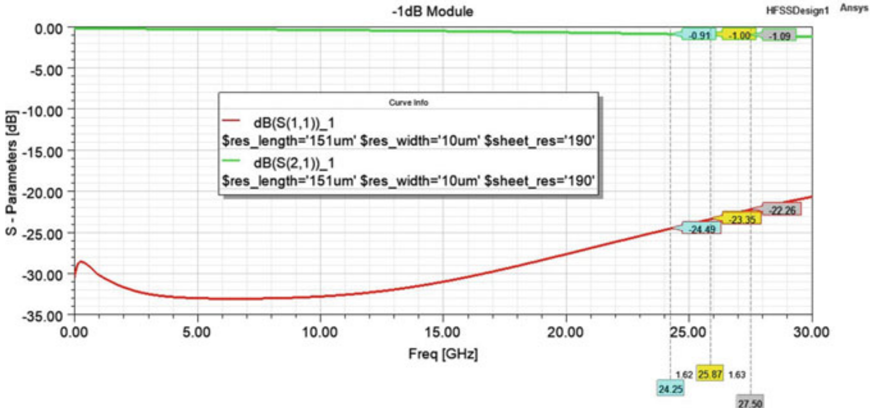

Fig. 11 Simulated S parameters of the − 1 dB version of the attenuation module in ON state

of the 16 possible states of such device, just the most representative results will be reported and discussed in this section.

From a general viewpoint, as compared to the single modules, the increased complexity of the overall device alters the performances in terms of reflected power and losses along the considered frequency range. In addition, the resulting topology is the one of a non-symmetric arrangement, which implies a different behavior in terms of S parameters, depending on the considered input port. More specifically, according to the following simulation results, while no difference can be observed between attenuation or insertion loss curves (S21 and S12), a non-negligible gap can be noticed between return loss curves (S11 and S22) in some cases, as visible in Fig. 13. Another common feature among the different results is an increased amount of attenuation, as compared to the desired one. As an example, in Fig. 13,

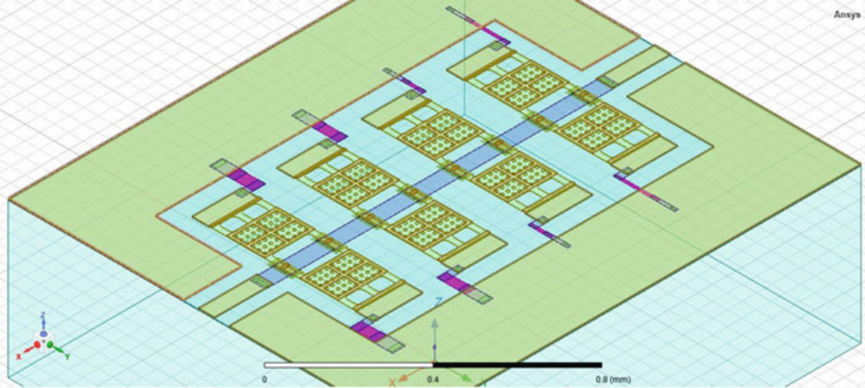

Fig. 12 Detail of the four couples of shunt resistors comprised in the 3D model simulated in Ansys HFSS environment

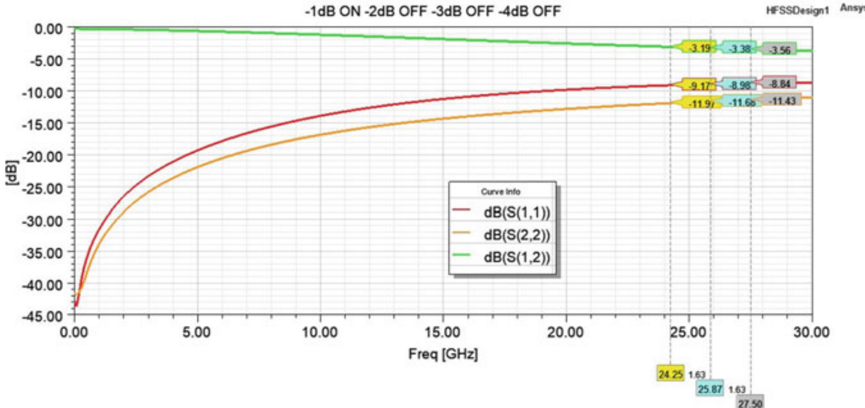

Fig. 13 S parameters results of the reported compound in the − 1 dB attenuation state

attenuation is produced just by − 1 dB module, and the value of the S12 curve at the center frequency is − 3.38 dB. Although the S22 curve remains below the − 10 dB threshold along the frequency interval of interest, such values are substantially different from the values of insertion loss of the single module reported in Fig. 11 (ranging from − 22.26 dB to − 24.49 dB).

The reason behind the observable increased return loss and attenuation level is the impedance mismatch caused by the whole network to the incoming signal, produced by the juxtaposition of multiple modules characterized by different resistive loads. Such effects could be mitigated by varying the spacing between the modules and/or by inserting additional sections for matching purposes, such as tapered matching sections. The need of such impedance matching becomes clearer by looking at Fig. 14, in which a − 2.81 dB attenuation is applied to the RF signal, while all the membranes are in rest position, and no shunt restive load is active. In this case, both return loss curves are below − 10 dB along the frequency range of interest and along vast majority of the 0–30 GHz interval.

Other representative results are displayed in Figs. 15 and 16, with the former reporting the state of maximum attenuation that can be achieved by the proposed compound. Thus, the proposed compound features 16 states, whose attenuation levels at the center frequency range between − 2.81 and − 8.46 dB.

In Fig. 15, it is possible to notice the increasing discrepancy between the return loss curves along the span of the considered frequencies, which becomes quite substantial in Fig. 16. Given the values assumed by the return loss curves in the 16 different states of the device, the values of the S22 curves are generally smaller than the ones of the S11 curves; as a consequence, since the power reflected at port 2 (left side in Fig. 12) is generally smaller than the one reflected at port 1 (right side), it would be preferable to use the port 2 as input port of such non-symmetric compound device.

One of the configurations which nearly fits the desired attenuation level is reported in Fig. 16. In this configuration, the attenuation presents a nearly ± 0.2 dB variability

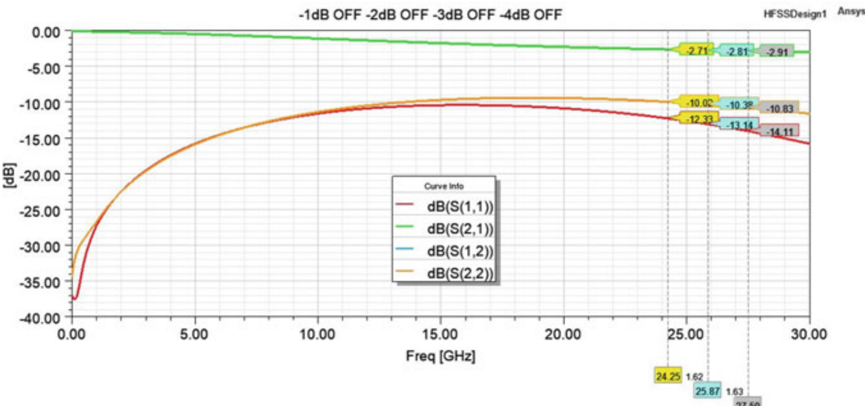

Fig. 14 S parameters results of the reported compound in the 0 dB attenuation state

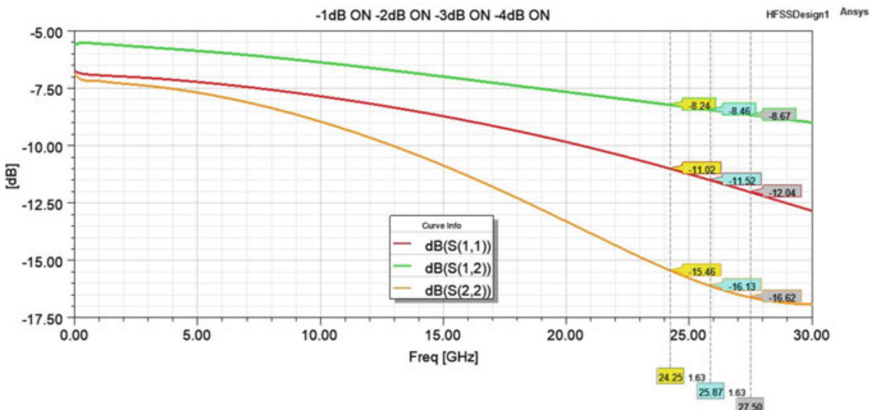

Fig. 15 S parameters results of the reported compound in the − 10 dB attenuation state

around the − 6.1 dB, reached at the center frequency, while the S22 remains between − 19.9 dB and − 21.6 dB along the frequency interval of interest.

The reported simulation results show some room for improvement to be investigated. The modifications to be brought to the present design will have an enhanced impedance matching as primary target, which will result in fairer levels of reflected power and attenuation. Such modifications would probably lead to a slight increase in the overall area of the device. However, given the basic compactness of the proposed topology, the resulting footprint would not be reasonably affected.

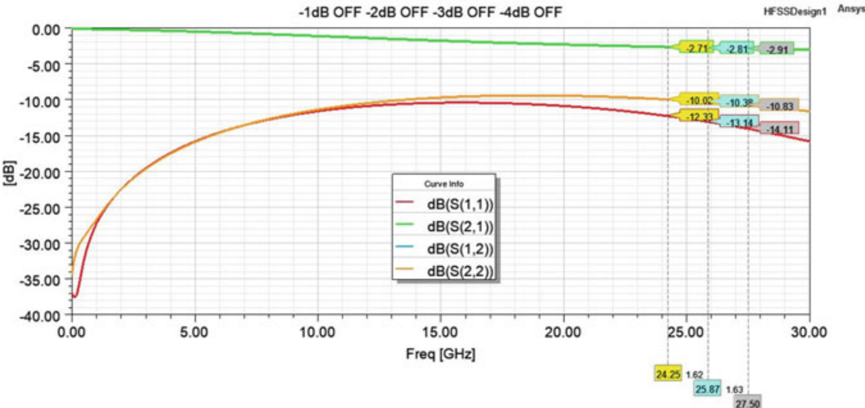

Fig. 16 S parameters results of the reported compound in the − 6 dB attenuation state

6 Conclusion

In this work, a 4-bit RF-MEMS step attenuator for beamforming applications in the evolving 5G/6G scenario is proposed. Targeting small cells for interior deployment operating in the 24.25–27.5 GHz frequency interval, a compact and modular compound is developed on the basis of four 1-bit attenuation cells featuring shunt resistors. After an optimization phase, the cells characterized by − 1 dB, − 2 dB, − 3 dB, and − 4 dB attenuation levels have been combined in a single arrangement, aiming at a device with − 10 dB as maximum attenuation, achievable by 1 dB steps. Among the different resulting simulation outcomes, the most representative cases are displayed and critically evaluated. Beside the cases in which the achieved attenuation level nearly coincides with the desired one, a generally increased amount of reflected power, and an underlying discrepancy in the obtained attenuation levels can be traced in the reported results. The reason behind such non-idealities relies on the impedance mismatch caused by the whole topology, the solution of which will require some design modifications, ranging from the variation of the modules' spacing to the insertion of impedance matching sections. Although the future modifications could slightly increase the overall dimensions of the device, the minimal footprint of the proposed arrangement would not be dramatically affected.

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A Study on Electricity Generation Using Hybrid Vegetative and Fruits Extract for Practical Utilizations

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1 Introduction

Due to Russia and Ukraine war, the use of the traditional energy sources is very difficult [1–5]. The effect of this war falls in to around the world [6–9]. The load shading is now happening in our country now and then. As a result, the economy is facing a critical situation [10–15]. At this moment, renewable energy is needed for electricity generation purposes [16, 17]. The solar photovoltaic systems are proving electricity around the world. In our country, solar home system (SHS) is proving electricity at the off grid region [18–22]. It is popular at the off grid region. Although it has some problems till today [23–26]. The floating solar PV is also becoming popular day by day. The grid connected solar photovoltaic system and the building integrated system are using more or less in our country [27–29]. To keep it in mind, we have performed this research work. It has several advantages. This electricity can be used in the rainy season, in the night and day time similar way [30]. The main

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advantages to use the vegetative and fruits extracts are available in the market [31]. It is environment friendly end low cost. It is available, and any one can cultivate these vegetative and fruits.

2 Methodology

2.1 Electrolytes

Ginger, pumpkin, balsam, potato, jute leaves, and onion extracts. The quantity of each electrolyte is 250 mL. The age of the each extract is 6 months.

2.2 Electrodes

Zinc and Copper. Each compartment has two plates. One is zinc plate, and other is copper plate. The distance between two plates is 5 cm.

2.3 Battery Box

A battery box is made by plastic which has six compartments. Each compartments are connected by a connecting wire. The Zn and Cu plates are fixed by plastic clips in the battery box (Fig. 1).

It is shown from Fig. 1 that the ginger, pumpkin, balsam, potato, jute leaves, and onion extracts have been put in the each box separately as an electrolyte. Zinc and copper plates have been immersed in to the box as an electrodes.

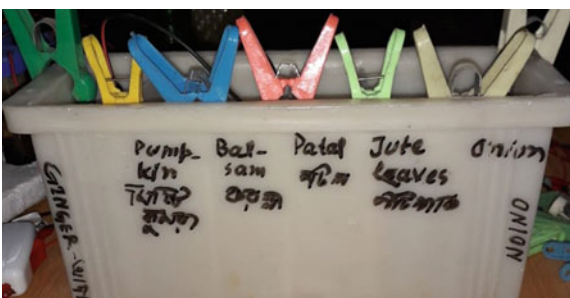

Fig. 1 Experimental setup of the hybrid electrochemical cell

2.4 LED Light

The LED light is made by semiconductor diode which is collected from the local market. It needs 3 V to operate for lighting which has been provided by the bio-voltaic battery. The ginger, pumpkin, balsam, potato, jute leaves, and onion extracts are put into the 6 compartments as an electrolytes (Fig. 2).

It shows (Fig. 2) the procedure to fill the electrolytes into the compartment of the battery box. The onion extract is used as an electrolyte. The copper and zinc electrodes are immersed in to the onion extract.

In Fig. 3, it is shown a LED lamp using hybrid vegetative and fruits extract for practical utilizations. There is a switch with LED lamp. A calibrated multimeter has been used to take the readings like open circuit voltage (V_{oc}) and short circuit current (I_{sc}).

Fig. 2 Ginger, pumpkin, balsam, potato, jute leaves, and onion extracts are put into the 6 compartments as an electrolytes

Fig. 3 Experimental setup of a hybrid vegetative and fruits extract for practical utilizations

3 Results and Discussion

All results have been discussed by the tabulated data (In Table 1) and represented graphically.

It is shown from Fig. 4 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for ginger extract electrochemical cell with the change of TD (hrs). It shows that the V_{oc} is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases slowly for 80 h. The maximum power decreases slowly for 80 h. The internal resistance is almost constant for 80 h (Table 2).

It is shows from Fig. 5 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for pumpkin extract electrochemical cell with the change of TD (hrs). It is shows that the V_{oc} is almost constant of pumpkin extract electrochemical cell for 80 h. The short

Table 1 Data collection for ginger extract

Time duration (h)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc} (mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	1.01	8.84	8.93	0.11
10	0.98	8.07	7.91	0.12
20	0.98	8.00	7.84	0.12
30	0.97	7.98	7.74	0.12
40	0.96	7.93	7.61	0.12
50	0.95	7.81	7.42	0.12
60	0.94	7.75	7.29	0.12
70	0.93	7.70	7.16	0.12
80	0.92	7.60	6.99	0.12

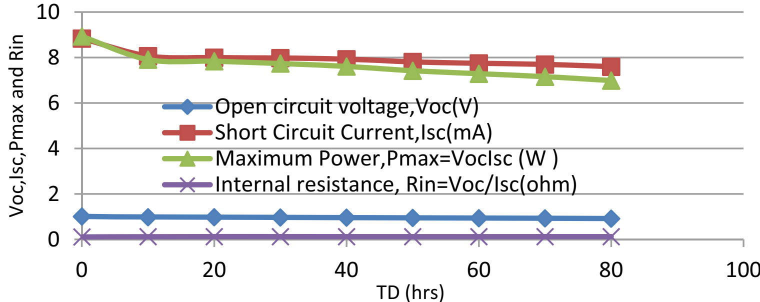

Fig. 4 Change of V_{oc}, I_{sc}, P_{max}, and internal resistance (R_{in}) for ginger extract electrochemical cell with the change of TD (hrs)

Table 2 Data collection for pumpkin extract

Time duration (h)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc} (mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	1.01	5.96	6.02	0.17
10	0.97	5.90	5.72	0.16
20	0.94	5.85	5.10	0.16
30	0.92	5.80	5.32	0.16
40	0.91	5.76	5.24	0.16
50	0.90	5.64	5.08	0.16
60	0.89	5.50	4.89	0.16
70	0.86	5.45	4.69	0.16
80	0.85	5.40	4.59	0.16

circuit current decreases slowly for 80 h. The maximum power decreases slowly for 80 h. The internal resistance is almost constant for 80 h (Table 3).

It is shown from Fig. 6 that the variation of open circuit voltage (V_{oc}), short circuit current (I_{sc}), maximum power (P_{max}), and internal resistance (R_{in}) for balsam extract electrochemical cell with the variation of TD (hrs). It is shown that the open circuit voltage is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases slowly for 80 h. The maximum power decreases slowly for 80 h. The internal resistance is almost constant for 80 h (Table 4).

It shows from Fig. 7 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for potato extract electrochemical cell with the change of TD (hrs). It is shown that the open circuit voltage is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases rapidly for 80 h. The maximum power also decreases rapidly for 80 h. The internal resistance is almost constant for 80 h (Fig. 8; Table 5).

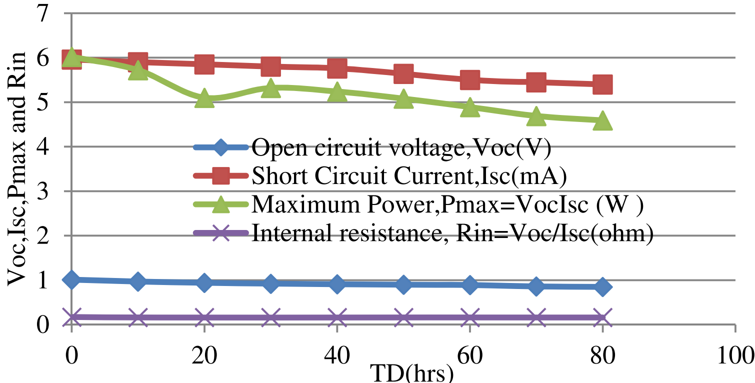

Fig. 5 Change of V_{oc}, I_{sc}, P_{max}, and internal resistance (R_{in}) for pumpkin extract electrochemical cell with the change of TD (hrs)

Table 3 Data collection for balsam extract

Time duration (hrs)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc} (mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	0.97	18.80	18.24	0.05
10	0.96	18.70	17.95	0.05
20	0.95	18.50	17.56	0.05
30	0.93	18.45	17.16	0.05
40	0.92	18.40	16.93	0.05
50	0.90	18.32	16.49	0.05
60	0.89	18.20	16.20	0.05
70	0.88	18.00	15.84	0.05
80	0.88	17.90	15.75	0.05

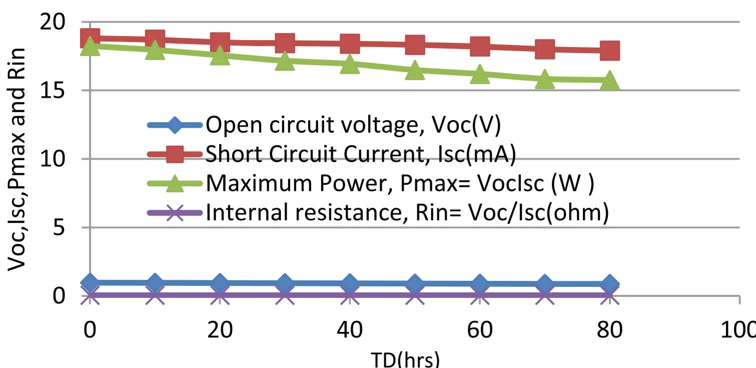

Fig. 6 Change of V_{oc}, I_{sc}, P_{max}, and internal resistance (R_{in}) for balsam extract electrochemical cell with the change of TD (hrs)

Table 4 Data collection for potato extract

Time duration (hrs)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc} (mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	0.99	35.29	34.94	0.03
10	0.98	33.27	32.60	0.03
20	0.98	30.00	29.40	0.03
30	0.97	27.05	26.24	0.04
40	0.96	26.01	24.97	0.04
50	0.95	25.02	23.77	0.04
60	0.94	23.09	21.70	0.04
70	0.92	22.00	20.24	0.04
80	0.90	21.00	18.90	0.04

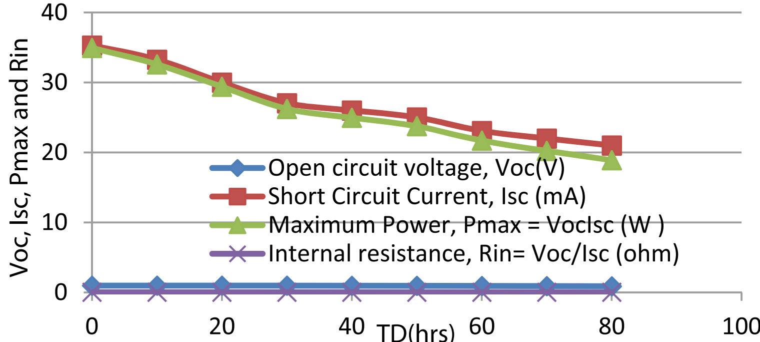

Fig. 7 Change of V_{oc}, I_{sc}, P_{max}, and internal resistance (R_{in}) for potato extract electrochemical cell with the change of TD (hrs)

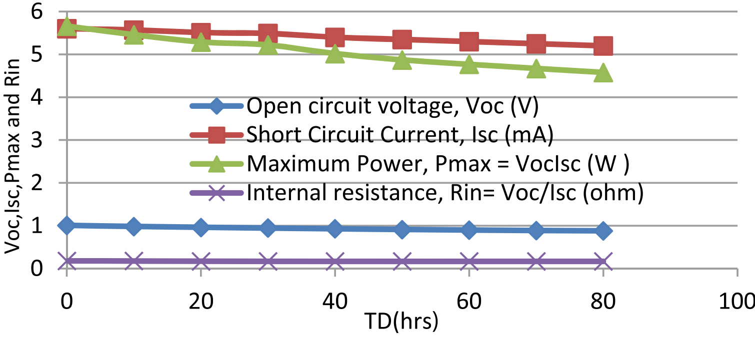

Fig. 8 Change of V_{oc}, I_{sc}, P_{max}, and internal resistance (R_{in}) for jute leaves extract electrochemical cell with the change of TD (hrs)

Table 5 Data collection for jute leaves extract

Time duration (hrs)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc} (mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	1.01	5.60	5.66	0.18
10	0.98	5.57	5.46	0.18
20	0.96	5.51	5.29	0.17
30	0.95	5.49	5.22	0.17
40	0.93	5.40	5.02	0.17
50	0.91	5.35	4.87	0.17
60	0.90	5.30	4.77	0.17
70	0.89	5.25	4.67	0.17
80	0.88	5.20	4.58	0.17

It shows from Fig. 7 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for jute leaves extract electrochemical cell with the change of TD (hrs). It is shown that the open circuit voltage is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases slowly for 80 h. The maximum power decreases slowly for 80 h. The internal resistance is almost constant for 80 h (Table 6).

It is shows from Fig. 9 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for onion extract electrochemical cell with the variation of TD (hrs). It is shown that the open circuit voltage is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases rapidly for 80 h. The maximum power decreases rapidly for 80 h. The internal resistance is almost constant for 80 h (Table 7).

Table 6 Data collection for onion extract electrochemical cell

Time duration (hrs)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc}(mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	1.01	39.28	39.67	0.03
10	1.01	36.01	36.37	0.03
20	1.00	33.09	33.09	0.03
30	1.00	30.05	30.05	0.03
40	0.99	28.05	27.77	0.04
50	0.98	26.04	25.52	0.04
60	0.97	24.09	23.37	0.04
70	0.96	23.00	22.08	0.04
80	0.95	22.01	20.91	0.04

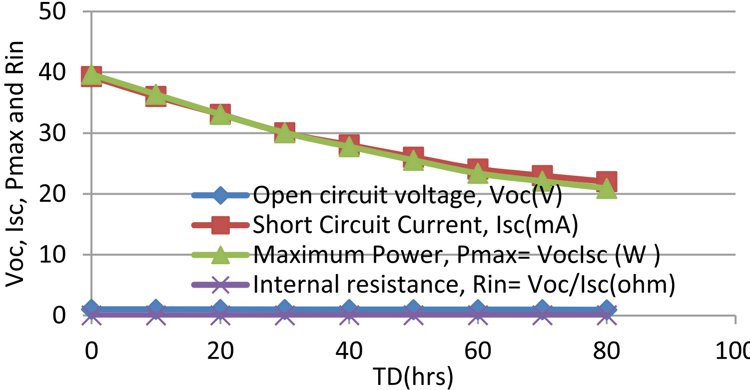

Fig. 9 It shows from Fig. 7 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for onion extract electrochemical cell with the variation of TD (hrs)

Table 7 Data collection for hybrid ginger, pumpkin, balsam, potato, jute leaves, and onion extract electrochemical cell

Time duration (hrs)	Open circuit voltage, V_{oc} (V)	Short circuit current, I_{sc} (mA)	Maximum power, $P_{max} = V_{oc}I_{sc}$ (W)	Internal resistance, $R_{in} = V_{oc}/I_{sc}$ (ohm)
00	5.98	11.65	69.67	0.51
10	5.85	11.00	64.35	0.53
20	5.75	10.60	60.95	0.54
30	5.70	10.40	59.28	0.55
40	5.43	10.20	55.39	0.53
50	5.40	10.17	54.92	0.53
60	5.37	10.15	54.51	0.53
70	5.30	10.12	53.64	0.52
80	5.25	10.10	53.03	0.52

It is shows from Fig. 10 that the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for ginger, pumpkin, balsam, potato, jute leaves, and onion extract electrochemical cell with the change of TD (hrs). It is shows that the open circuit V_{oc} is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases slowly for 80 h. The maximum power decreases linearly for 80 h. The internal resistance is almost constant for 80 h.

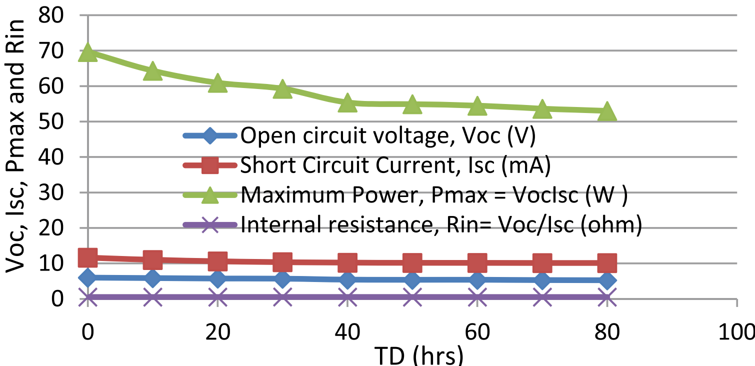

Fig. 10 Change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for hybrid ginger, pumpkin, balsam, potato, jute leaves, and onion extract electrochemical cell with the variation of TD (hrs)

4 Conclusions

It is shown the change of V_{oc}, I_{sc}, $P_{max,}$ and internal resistance (R_{in}) for hybrid ginger, pumpkin, balsam, potato, jute leaves, and onion extract electrochemical cell with the variation of TD (hrs) together and separately. It is found that the result for together is good than the separated conditions. It is shown that the open circuit voltage is almost constant of ginger extract electrochemical cell for 80 h. The short circuit current decreases slowly for 80 h. The maximum power decreases linearly for 80 h. The internal resistance is almost constant for 80 h.

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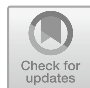
A Comparative Study of Diverse RF-MEMS Switch Design Concepts Experimentally Verified up to 110 GHz for Beyond-5G, 6G and Future Networks Applications



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1 Introduction

Current research in pivotal areas like electronics and telecommunications is recently dominated by wide-perspective application scenarios and paradigms, among which the Internet of things (IoT) and 5G are certainly the most well-known. Besides, relevant research efforts are aimed already today at what next telecommunication protocols, standards and generations will be. To this end, the uptake of buzzwords like beyond-5G (B5G), 6G, super-IoT and tactile Internet (TI) is relentlessly spreading out.

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Fig. 1 Four main paradigm shifts (PSs) of 6G discussed in [3]

Trying to explain in simple terms, the plethora of key enabling technologies (KETs) and key performance indicators (KPIs) expected for the mentioned paradigms is not a trivial task. Some simplification is needed, and to this end decomposition in terms of paradigm shifts (PSs), as proposed in [1, 2] and rearranged in [3], looks practical and effective. In brief, the disruption that 6G will bring is broken down according to four macro-areas (i.e., PSs), visually reported in Fig. 1 and termed as follows: (1) scattered intelligence (SI); (2) seamless coverage (SC); (3) spectrum diversity (SD); (4) enhanced security (ES).

In simple terms, the PS of SI has to do with the capillary and massive exploitation of artificial intelligence (AI), targeting seamless evolution of services as well as, more notably, to self-adaption and evolution of network operation [4]. SC addresses ubiquity of services, aiming at maintenance of the same KPIs, regardless of the specific point of access to the network takes place in a metropolitan, rural or remote area. Scoring such a challenge is possible by means of a highly-diversified space-air-ground-sea physical infrastructure [5], schematically shown in Fig. 1. Moreover, SD indicates the exploitation of frequencies for communications ranging from sub-GHz, to millimeter-waves (mm-Waves), again to sub-THz (100–300 GHz), THz and signals in the optical domain [6]. Finally, ES will be necessary to address important aspects related to data security, privacy and trust, which the scattering of intelligence to the edge typical of 6G will unavoidably trigger [7].

In order to add more qualitative considerations on the discussed scenario, Table 1 summarizes some reference KPIs expected for 6G, as reported in [8].

Given the broad frame of reference discussed above, this work focuses on the telecommunication segment of 6G and on the PS of SD. Within this context, moving the focus at low-complexity hardware (HW) components, a key-component to enable the KPIs in Table 1 is the switch, necessary to realize a variety of functions, like commuting RF signals from one channel to another, reconfiguring antennas and massive-multiple-input-multiple-output (MIMOs) [9], as well as driving multi-state networks, as tunable filters, delay lines and so on.

Table 1 Summary of the most relevant expected 6G KPIs as reported in [8]

	5G	Beyond-5G (B5G)	6G
Data rate (average per user)	1 Gbps	100 Gbps	1 Tbps
End-to-end (E2E) delay	5 ms	1 ms	Below 1 ms
Radio delay	100 ns	100 ns	10 ns
Processing delay	100 ns	50 ns	10 ns
E2E reliability	99.999%	99.9999%	99.99999%

The actual technology here at stake for the realization of switches is known in the scientific community with the name of RF-MEMS and is concerned to the exploitation of microelectromechanical-systems (MEMS), i.e., microsystems, for the realization of radio frequency (RF) miniaturized passives.

Around mid-1990s, micro-fabrication steps typical of MEMS technology started to be exploited to manufacture highly-miniaturized and low-loss waveguides, like coplanar waveguides (CPWs) and microstrip lines [10], as well as reactive elements (capacitors and inductors), stubs and other microwave fixed passive components. Shortly after, complete MEMS devices started to be exploited for the realization of RF passives, yielding components capable of reconfiguring their state. To this end, the first reconfigurable RF-MEMS appearing in literature was ohmic and capacitive micro-switches [11]. Then, elementary RF-MEMS reconfigurable elements, in essence switches, commenced to be combined together, to implement multi-state miniaturized complex passive networks, like phase shifters [12].

Starting from the early works just cited above, the research community was very active in subsequent years around the development of innovative RF-MEMS-based devices and design concepts, along with significant efforts in filling gaps at technology level, e.g., with regard to reliability, yield, packaging and integration. For the purpose of completeness, a few relevant works are now going to be listed, offering a brief yet comprehensive overview of the main research achievements linked to RF-MEMS technology.

With reference to the basic element of micro-relays of various types realized in RF-MEMS technology, a few significant design and experimental results achieved by the research community are available in [13–16]. Focusing the attention of RF-MEMS micro-switches with improved reliability, essential for the employment of such a technology within practical and commercial applications, relevant findings are discussed in [17–21]. Starting from the mentioned basic components, complex and multi-state passive networks in RF-MEMS technology were demonstrated and reported in literature. In this respect, reference examples are higher-order switching matrices [22–25], reconfigurable phase shifters and delay lines [26–30], RF power step attenuators [31–34] and tunable filters [35–38].

In light of the above discussion, the work is structured as reported below. Following the introductive section, Sect. 2 will add more details around the proposed RF-MEMS switches design concepts and the employed micro-fabrication technology. Section 3 reports on the validation of 3D simulated models, by comparing the expected RF performance (scattering parameters—S-parameters) against experimental datasets. Thereafter, Sect. 4 develops a comparative discussion around the tested characteristics of the proposed RF-MEMS switches design variations, while Sect. 5 collects some conclusive considerations.

2 RF-MEMS Technology and Micro-switches Design Concepts

The electrostatically controlled micro-switches that are going to be discussed are manufactured in a 6 in. surface micromachining RF-MEMS technology, which has been already reported and discussed in literature [39] and is available at Fondazione Bruno Kessler (FBK), in Italy. The technology, capitalizing on electrodeposition of gold thin suspended movable membranes, was demonstrated for manufacturing a variety of RF-MEMS passives, exhibiting good RF characteristics up to 40–50 GHz [40]. A cross section highlighting the stacking of layers is shown in Fig. 2. The three layers of oxide visible in the schematic refer to the same material, which is silicon oxide, despite they are deposited at different times during the processing.

Bearing in mind the KPIs listed in Table 1, the main challenge ahead is boosting the RF characteristics of RF-MEMS passives for frequencies much higher than 50 GHz. In this sense, some work was already performed around the experimental characterization of RF-MEMS reconfigurable step power attenuators [41], despite further efforts are necessary.

Pursuing an approach oriented to problem simplification, regardless of the level of complexity of the RF-MEMS passive at stake, the most critical element exerting significant influence on the whole device RF characteristics is the micro-switch, necessary to enable reconfigurability and tunability. Having said that, new design concepts of RF-MEMS micro-switches were developed, specifically conceiving them

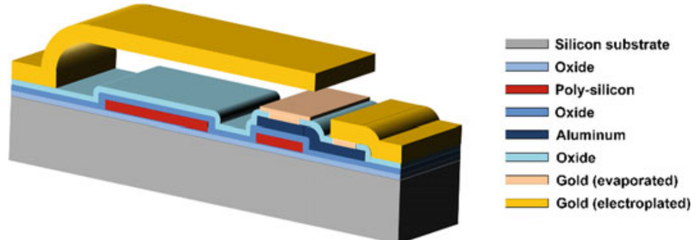

Fig. 2 Cross section of the FBK RF-MEMS technology

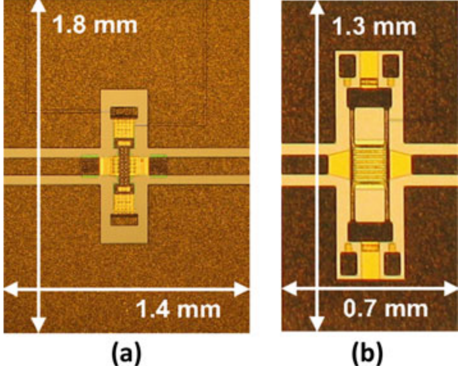

Fig. 3 Photograph of a traditional RF-MEMS micro-relay design, named Device A, reported in figure (**a**), and of an innovative design concept, named Device B, reported in figure (**b**)

to reduce the losses at high frequencies. The microphotographs in Fig. 3 report a couple of RF-MEMS series ohmic micro-switches design concepts.

The device in Fig. 3a, named Device A, is a traditional realization of an RF-MEMS micro-switch. The area of the entire devices, as visible in figure, is $1.4 \times 1.8\ \text{mm}^2$. Differently, the micro-relay in Fig. 3b, named Device B, is a novel design concept for high frequency operation. Its area, as visible in figure, is $0.7 \times 1.3\ \text{mm}^2$. Both devices reported in Fig. 3 are characterized against their electromechanical properties, exhibiting activation (pull-in) voltages in the range of 20–40 V. More details around the RF characteristics of the discussed design variations are going to be covered in the following sections.

3 Validation of Simulated Results Against Experiments

The RF-MEMS micro-switches geometries in Fig. 3 are experimentally measured in the RF domain, performing on-wafer measurements on a probe station, featuring a vector network analyzer (VNA) connected to the devices under test (DUTs) with micro-probes (GSG—ground-signal-ground). In particular, the scattering parameters (S-parameters) are observed from 100 MHz up to 110 GHz, both in the switches isolating OPEN state (MEMS transducer OFF, in the rest position) and conducting CLOSE state (MEMS transducer ON, in the pulled-in position). For the scope of the present section, some of the mentioned experimental datasets are going to be exploited for validation of the 3D finite element method (FEM) models. Diversely, in the following Sect. 4, such RF data will be discussed, to build a comparative assessment of the different characteristics related to the reported RF-MEMS switches geometries and concepts.

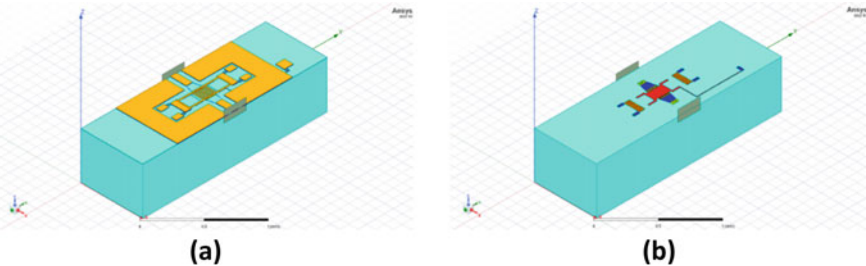

Fig. 4 **a** Full 3D Ansys HFF model of the RF-MEMS switch named as Device B in Fig. 3b. **b** View with the gold layers of the MEMS and CPW made invisible, to highlight the distribution scheme of the underlaying biasing and under-passing layers

Full 3D models of the switches are built from the 2D layout within the Ansys HFSS simulation environment (https://www.ansys.com/products/electronics/ansys-hfss), then exploited for running S-parameters simulations. Despite both geometry variations in Fig. 3 are simulated, for the sake of brevity, just one 3D model is reported below. To this end, the following Fig. 4 shows the HFSS model of the RF-MEMS switch named as Device B (in Fig. 3b). Into more details, Fig. 4b highlights the 3D model of Device B, after hiding the gold layers that constitute the actual MEMS and surrounding coplanar waveguide (CPW) structures, thus offering a view of the underlying biasing and under-passing layers.

The comparison of the simulated vs measured S-parameters characteristics, from 100 MHz up to 110 GHz, is reported in Figs. 5 and 6, for what concerns Device A (see Fig. 3a) and Device B (see Fig. 3b), respectively. In particular, the plots are arranged according to the following rationale. The measured and simulated reflection parameter (S11) of the RF-MEMS series ohmic switches in OPEN state, i.e., when the micro-membrane is in its rest position (OFF), is reported for Device A and Device B in Figs. 5a and 6a, respectively. The isolation (S21) of the switches in OPEN state is reported for Device A and Device B in Figs. 5b and 6b, respectively. Moreover, the measured and simulated return loss (S11) of the RF-MEMS series ohmic switches in CLOSE state, i.e., when the MEMS membrane is pulled-in (ON), is reported for Device A and Device B in Figs. 5c and 6c, respectively. Finally, the insertion isolation (S21) of the switches in CLOSE state is reported for Device A and Device B in Figs. 5d and 6d, respectively.

As visible, the simulated traces are able to reproduce the experimental characteristics with a rather good accuracy. In some cases, the quantitative disagreement is quite marked. However, it must be stressed that the qualitative behavior is always captured in a satisfactory fashion by the 3D FEM models, and that the observed frequency range is very wide, which is a challenging condition, purposedly chosen by the author to explore the capacities of the simulation tool. Also relevantly, the analyzed designs, i.e., those reported in Fig. 3, are significantly different, while the accuracy of simulations remains the same, proving that the chosen methodology is rather robust.

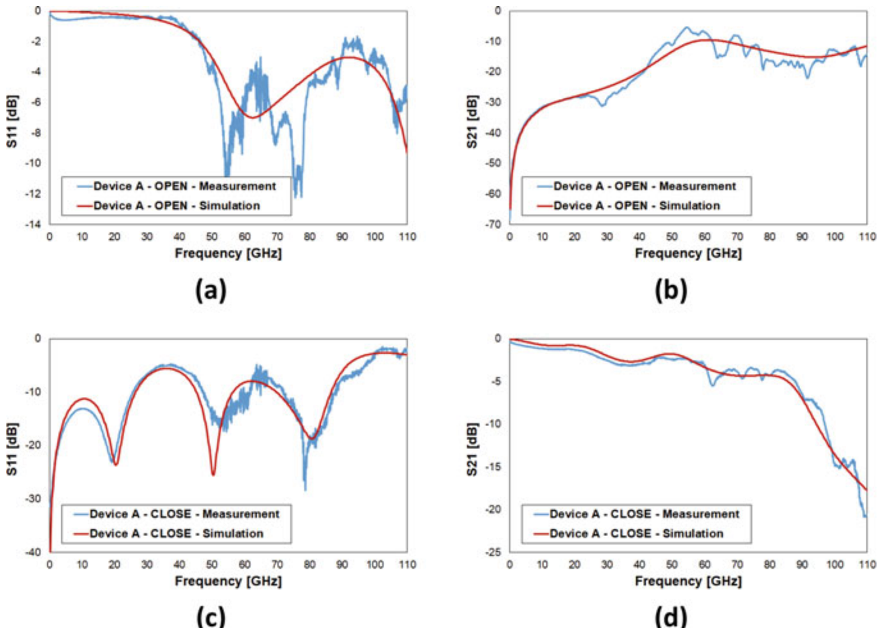

Fig. 5 Measured versus simulated S-parameters of the RF-MEMS series ohmic switch named Device A in Fig. 3a, with reference to **a** the reflection parameter (S11) and **b** isolation (S21) in the OPEN state (MEMS switch OFF), as well as to, **c** the return loss (S11) and **d** the insertion loss (S21) in the CLOSE state (MEMS switch ON)

4 Comparative Discussion of RF-MEMS Micro-switches RF Performances

The experimental results related to Device A (Fig. 3a) and Device B (Fig. 3b) are summarized in the plots shown in Fig. 7. The graphs are arranged according to the same fashion previously exploited in Fig. 6. Therefore, reflection (S11) and isolation (S21) when the switches are OPEN (OFF state) are reported in Fig. 7a, b, respectively, while the return loss (S11) and insertion loss (S21) of the micro-relays in CLOSE configuration (ON state) are reported in Fig. 7c, d, respectively.

Since the observed frequency range is significantly wide, the 110 GHz span is split in two sub-ranges. To this end, the plots in Figs. 8 and 9 cover the range from 100 MHz up to 50 GHz and from 50 GHz up to 110 GHz, respectively. The plots arrangement, in terms of S11 and S21 in the OPEN and CLOSE configurations, is the same as exploited before.

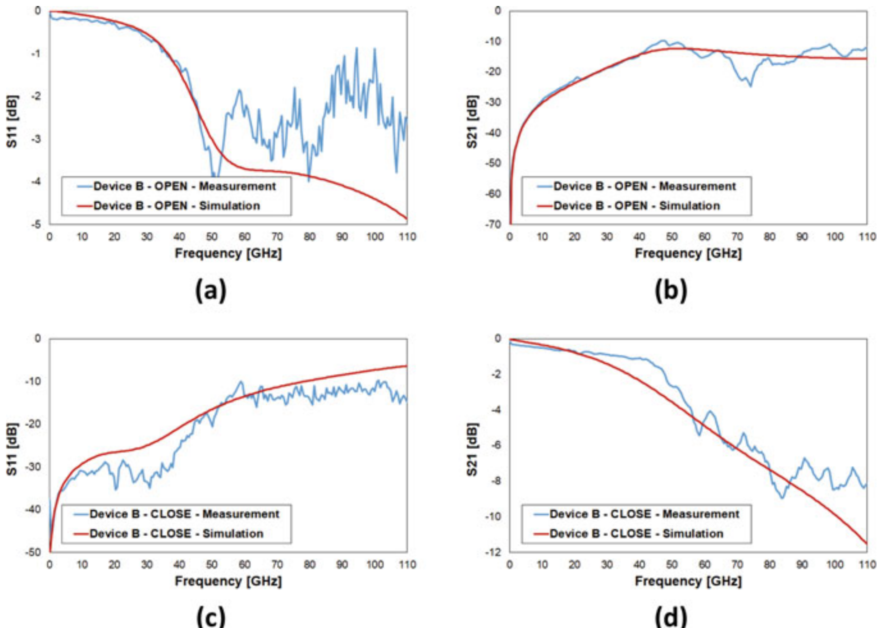

Fig. 6 Measured versus simulated S-parameters of the RF-MEMS series ohmic switch named Device B in Fig. 3b, with reference to **a** the reflection parameter (S11) and **b** isolation (S21) in the OPEN state (MEMS switch OFF), as well as to **c** the return loss (S11) and **d** the insertion loss (S21) in the CLOSE state (MEMS switch ON)

With reference to the OPEN state, the isolation (S21) is the parameter deserving more attention and providing valuable insight. Therefore, while reflection (S11) is reported for completeness in Fig. 7a, the main discussion has to be developed around the plot in Fig. 7b. In the lower range, visible in Fig. 8b, Device A (Fig. 3a) marks the most valuable characteristic up to 45 GHz. It is better than − 30 dB up 30 GHz, and better than − 12 dB up to 45 GHz. Diversely, Device B (Fig. 3b) is characterized by a fair performance, showing a markedly linear S21 trace, from − 28 dB at 10 GHz to − 10 dB at 50 GHz. Above 50 GHz (see Fig. 9b), Device B exhibits an S21 parameter better than − 10 dB up to 110 GHz, while for Device A poor isolation is visible.

Moving the attention on the RF behavior in the CLOSE state (pulled-in MEMS), reflection (S11) in Fig. 7c returns valuable insight around the matching of impedance with respect to frequency, while the insertion loss (S21) in Fig. 7d is undoubtedly crucial to analyze. Device A, regardless of its traditional design, marks a behavior deserving attention. Entering into more details, the S21 parameter gest worse to − 3 dB losses at 38 GHz (Fig. 8d). However, above that threshold frequency, the insertion loss of Device A gest better. In fact, it is better than − 3 dB up to 60 GHz (Fig. 9d). Subsequently, it remains fairly constant around − 5 dB up to around 88 GHz. In the remaining observed range it becomes worse, down to − 20 dB at 110 GHz. Focusing on the new micro-switch design concept, Device B hits the non-negligible target

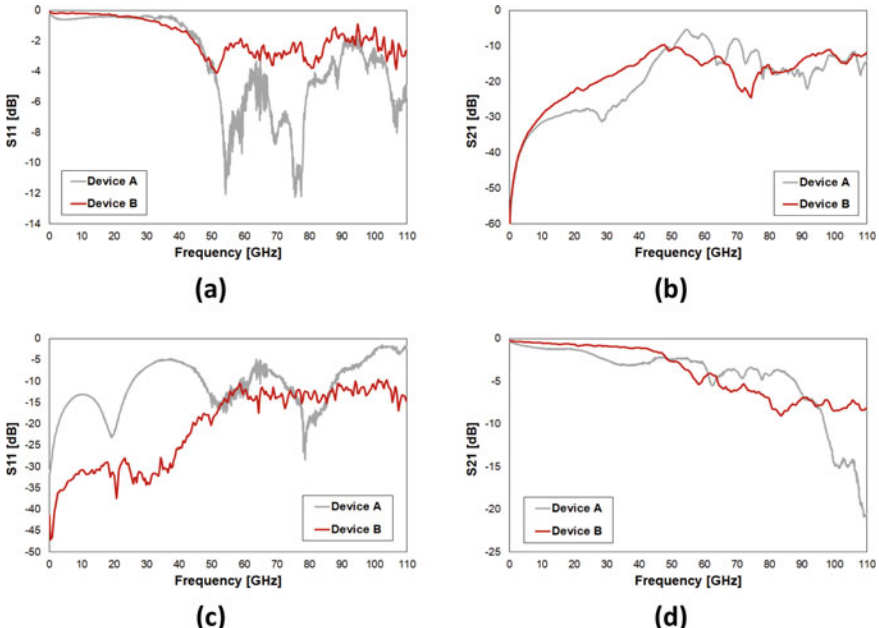

Fig. 7 Comparison of the S-parameters behavior, experimentally characterized from 100 MHz up to 110 GHz, of the RF-MEMS switches in Fig. 3 for what concerns reflection (S11) in the OPEN state (**a**), isolation (S21) in the OPEN state (**b**), reflection (S11) in the CLOSE state (**c**) and insertion loss (S21) in the CLOSE state (**d**)

of exhibiting losses (S21) within − 1 dB up to 40 GHz (Fig. 8d). Stepping up in frequency, the return loss is better than − 3 dB up to 50 GHz. Subsequently, it worsen according to a rather linear trend, down to − 10 dB at 85 GHz (Fig. 9d). Above, the S21 sets around − 8 dB up to 110 GHz, marking in any case a more encouraging characteristic if confronted to Device A.

Eventually, the performance in terms of insertion loss (S21) in the CLOSE state configuration can be significantly improved by reducing the size of the RF-MEMS intrinsic micro-relay, along with that of the coplanar waveguide (CPW) framed around it. In this sense, a loss better than 1 dB up to 40 GHz can be regarded as a good performance. In any case, additional efforts are needed to yield smaller switching devices, along with avoiding to place them in a crossing (i.e., transversal) fashion across the RF conducting line, diversely from all the RF-MEMS designs reported in this work. The just mentioned solution would help reduce even more the parasitic effects arising from the MEMS suspended membrane, especially in the higher portion of the frequency range, along with losses. In particular, with reference to the latter performance indicator, it would be desirable maintaining it below − 1/ − 2 dB up to 110 GHz and above.

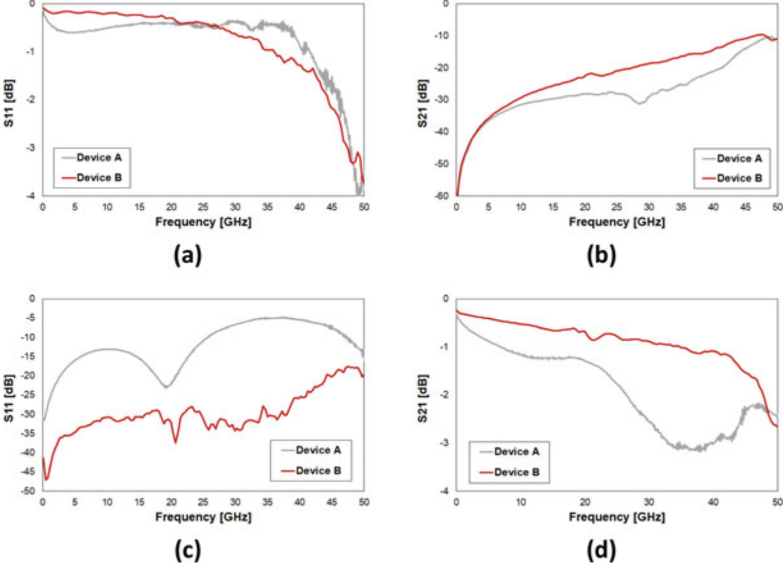

Fig. 8 Close-up comparison of the S-parameters, from 100 MHz up to 50 GHz, of the RF-MEMS switches in Fig. 3 for what concerns reflection (S11) in the OPEN state (**a**), isolation (S21) in the OPEN state (**b**), reflection (S11) in the CLOSE state (**c**) and insertion loss (S21) in the CLOSE state (**d**)

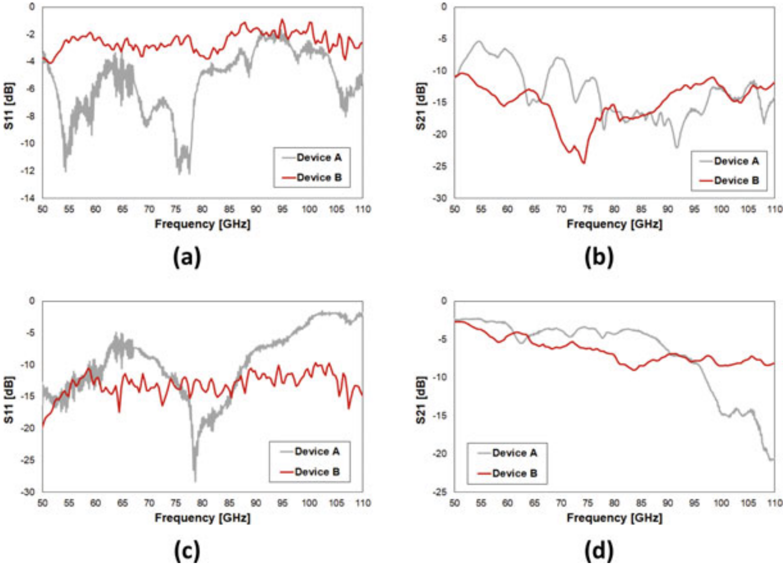

Fig. 9 Close-up comparison of the S-parameters, from 50 GHz up to 110 GHz, of the RF-MEMS switches in Fig. 3 for what concerns reflection (S11) in the OPEN state (**a**), isolation (S21) in the OPEN state (**b**), reflection (S11) in the CLOSE state (**c**) and insertion loss (S21) in the CLOSE state (**d**)

5 Conclusion

Future emerging applications, like beyond-5G (B5G), 6G and super-Internet of things (IoT), are expected to drive unprecedented disruption at various levels of research, starting from applications and services, to the physical infrastructure, as well as for what concerns hardware (HW) systems, sub-systems and low-complexity components, like sensors, actuators and transducers.

In this work, the focus was concentrated around the radio frequency (RF) portion of the infrastructure, and in particular on micro-relays for channel commuting and reconfiguration of passive elements. We reported high-performance and highly-miniaturized micro-switches based on microelectromechanical-systems (MEMS) technology, known as RF-MEMS. A couple of diverse design concepts of RF-MEMS-based series ohmic switches were discussed in details, including technical characteristics of the manufacturing process, 3D simulations and experimental datasets concerned to their RF behavior (S-parameters), observed up to 110 GHz.

The reported result will be the basis for further considerations around the design and development of advanced RF-MEMS device concepts for B5G and 6G applications. On one side, the discussed validation of 3D models' finite element method (FEM) simulations will be essential for the behavioral prediction of the upcoming designs. On the other hand, the comparison of experimental data related to the two different switches reported above already provides important indications around how new devices should be conceived.

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The mentioned project, despite technically focused on Energy Harvesting, provides proper institutional coverage for pursuing joined activities between NIT Silchar and FBK, as the one discussed in this contribution.

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Proposal, Design, and Performance Investigation of ZnO-Based ISFET pH Sensor

Ankita Porwal, Chitrakant Sahu, and Nawaz Shafi

1 Introduction

In both chemical and biological processes, the measurement of pH is crucial [1, 2]. Although a glass electrode can measure the pH, it has some drawbacks, such as the fragility of glass and less flexibility, so it cannot be employed in the food industry. To measure pH, different types of field effect transistors are modified, such as ion sensitive field effect transistor (ISFET) and extended gate field effect transistor (EGFET), which is reported in the literature [3].

High sensitivity, selectivity, reliability, and affordability are the performance criteria for evaluating pH sensors. Recently, ZnO-based detectors have caught much attention because of the nontoxicity, thermal stability, electrochemical signaling, fast electron transfer, and biocompatibility nature of ZnO [4]. ZnO is a wide-band gap semiconductor and has a high ionic bonding. Zinc oxide as a sensing material is analyzed in many fields, such as chemical sensors, solar cells, electrochemical cells, biosensors, and light-emitting diodes [5, 6]. Apart from sensing hydrogen ion (H^{+}), recently, ZnO-based nanorod FET has been fabricated for the detection of phosphate (PO_4^{-3}), nitrate (NO_3^{-}), and potassium ions (K^{+}) by K. S. Bhat et al. with high sensitivity and selectivity and low detection limits [7]. ZnO as a sensing layer is integrated with EGFET, and this device shows high voltage & current sensitivity (53.21 mV/pH and − 10.43 $\mu A^{1/2}$), respectively [8]. To examine in a noninvasive manner, ZnO-based EGFET was fabricated by sol-gel process, and the device shows a voltage sensitivity of 63.15 mV/pH and linearity of 0.99 [9].

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The fabrication of the semiconductor-based sensor is the succession of well-established Si Technology [10]. The silicon-based sensor is favorable because of its low cost, reproducibility, and controllable electronic response. However, this sensor cannot work at critical points such as high temperature and pressure. Wide-bandgap semiconductors such as ZnO can replace mature silicon technology because of their attractive properties (biocompatibility, piezoelectric, non- toxicity, stability, and label-free sensing) [11]. ZnO can absorb the protein or enzymes with a low isoelectric point (IEP) of 4.5 because of its high isoelectric point (9.5) [12].

To measure the pH among a variety of biosensors, ISFET is mainly used, which has multiple advantages such as rapid response, small size, low output impedance, highly reliable, and on-chip integration of biosensor arrays [13]. ISFET is employed to detect the enzyme, immune, DNA, and cell-based material used in the healthcare industry, environment monitoring, DNA detection, food industry, and biomedicine that can be easily integrated with microfluidic for sensing applications. In 1970, Bergveld first fabricated the ISFET; since then, continuous modifications have been going on to improve the performance and figure of merits (sensitivity & signal-to-noise ratio) [14].

To overcome the short channel effects, achieve high sensitivity, and attain high switching capability, a conventional sensing layer of ISFET is replaced by a new material ZnO. This structure is a field effect transistor compatible with the CMOS fabrication process. Portability, compactness, simplicity, cheap cost, and ease of manipulating the sensor based on FET enable in situ monitoring [7]. A FET can work as a biosensor by replacing a metal gate electrode with a sensitive layer, which reacts with the solution to be measured. The gate and reference voltage are supplied to provide biasing in the circuit.

In literature, ISFET is characterized through simulation, modeling, and fabrication [15, 16]. ISFET is an electrochemical sensor with chemical input in the form of ion concentration. In an ISFET at interfaces (electrolyte and electrolyte-oxide), an electrochemical reaction happens that helps detect ions. Gouy-Chapman explained this electrochemical reaction in terms of Stern double-layer capacitance [17].

In this paper, in conventional ISFET, gate oxide material SiO_2 is accompanied by ZnO as a sensing layer in addition to junctionless geometry in the structure, significantly improving sensitivity. The design of ISFET is almost similar to MOSFET, where a reference gate replaces the top gate in the electrolyte solution with a sensing membrane. A stern layer surrounds the top gate layer with a capacitance of 20 $\mu F/cm^{-2}$ and a thin membrane layer.

2 Model Simulation

The projected device's schematic construction is depicted in Fig. 1, and the measurement of various layers in device design is represented in Table 1. The electrolyte solution is considered an intrinsic semiconductor because of similar properties of cations and anions with electrons and holes in the semiconductor. The electrolyte solution

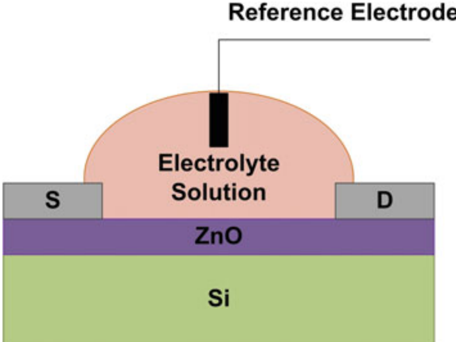


Fig. 1 Schematic structure of proposed ZnO ISFET

Table 1 Measurement of various layers of ZnO ISFET

Parameter name	Symbol	Value
Electrolyte thickness	T_{el}	10 nm
Length of channel	L_{ch}	100 nm
Thickness of oxide	T_{ox}	2 nm
Thickness of silicon	T_{si}	8 nm
Doping in the channel	N_{ch}	1.2×10^{24} m^{-3}
Doping in the source and drain	N_{ch}	1.2×10^{24} m^{-3}
Stern layer thickness	T_{st}	1 nm

is simulated considering the dielectric constant of water ($k = 78$), electron & hole mobility of ZnO, and properties of the ZnO semiconductor (affinity, permittivity, energy bandgap, and density of states) [18]. The intrinsic semiconductor material consists of thermal-generated mobile carriers. The ion molar concentration of the electrolyte solution is defined by the density of states in the conduction and valence bands [19]. The electrolyte solution interacts with the oxide (sensing membrane) and generates surface charges.

The structure consists of a ZnO semiconductor material as a sensing layer, enhancing the figure of merits. The simulation parameters and framework of the proposed device have been maintained coherently with our previous works [20]. A thin membrane layer is also considered between the electrolyte solution and the stern layer. The membrane layer is simulated as silicon with a high dielectric constant ($k = 77.8$), and the density of states in the conduction and valence band is ($N_c = 4.16199 \times 10^{25}$ and $N_v = 3.74 \times 10^{23}$), respectively. The stern layer is considered an oxide of thickness 1 nm and $k = 21$. Various models such as concentration-dependent mobility (conmob), field-dependent mobility (fldmob), Fermi-Dirac model (fermidirac), Shockley-Read-Hall recombination model (srh), and basic model are applied during the simulation of the proposed ISFET. The charge concentration is considered at the interfaces (electrode and electrode/oxide interface) to model the device accurately.

In an ISFET, the concentration of ions can be measured by electrical potential when the sensing layer interacts with an electrolyte solution. The sensitivity parameters can be derived from the site binding model [21]. In the proposed device, ZnO is the insulating layer; when this layer interacts with the pH solution following reaction occurs at the interface:

$$\mathrm{ZnOH} \leftrightarrow \mathrm{ZnO}^{-} + \mathrm{H}^{+} \tag{1}$$

The membrane layer incorporates the charged ions, which are situated between the electrolyte solution and the stern layer. The membrane layer assists in the alignment of the biomolecules to be detected in the sensing layer. Water in an ionized form is represented as

$$\mathrm{H_2O} \leftrightarrow \mathrm{H}^{+} + \ \mathrm{OH}^{-} \tag{2}$$

The concentration of carrier is described as per Boltzmann Statistics considering holes equal to H ions and electrons equal to hydroxyl ion ($p = [\mathrm{H}^+]$, $n = [\mathrm{OH}^-]$, and $E_c - E_f = E_g/2$). The density of states in the conduction and valence band (N_c and N_v) is defined as

$$N_c = \mathrm{ne}^{\frac{Eg}{2kT}} \tag{3}$$

$$N_v = \mathrm{pe}^{\frac{Eg}{2kT}} \tag{4}$$

The link between density of states in the conduction and valence band and the pH change in the electrolyte solution is established by above equations.

3 Simulation Results and Discussion

The device is characterized at $V_{GS} = 0$–2 V, $V_{DS} = 0.1$ V, and the electrolyte solution contains pH = 3–11. Figure 2 shows the contour plot of potential along the device at all voltages equal to zero ($V_{GS} = V_{DS} = 0$ V). A horizontally cut line is drawn at the surface of ZnO to extract the potential.

The potential fluctuation in the channel region is illustrated in Fig. 3. The sensing performance of the ISFET depends upon the sensing membrane's potential variation. The potential changes with pH according to the site binding model. The variation in potential further leads to variations in the drain-to-source current of ISFET. Site binding theory states that variations in the surface potential voltage at the interface of the aqueous electrolyte solution-sensing layer can result from the concentration of active binding sites on the oxide layer. The surface potential of the sensing layer and pH of the electrolyte solution are related through site binding model, and mathematically, it is represented as [22]:

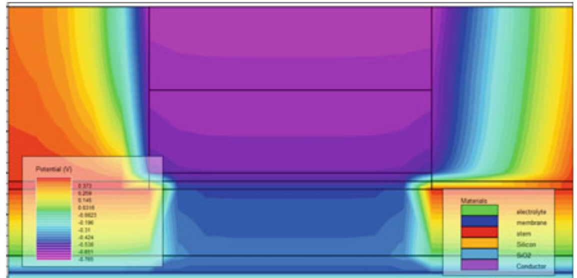


Fig. 2 Contour plot of the variation of potential along the device

$$2.303\left(\mathrm{pH}_{\mathrm{pzc}} - \mathrm{pH}\right) = \frac{q\varphi_o}{kT} + \sin h^{-}\frac{q\varphi_o}{kT} * \frac{1}{\beta} \tag{5}$$

where pH_{PZC} is the pH value at the point of zero charge on the sensing layer, q is for the charge of a single electron, k stands for Boltzmann's constant, T defines the temperature, and β is the sensitivity parameter that indicates the sensitivity of the oxide layer.

The variation of energy in the conduction band and valence band at different pH values ranging from 3 to 11 is shown in Fig. 4. An Ag/AgCl reference electrode is considered, which has stability against variations in the electrolyte solution. The reference electrode is dipped in the pH solution to measure the current at different pH values. The reference electrode supplied a bias to the sensing layer, and the drain current was measured. The drain-to-source voltage value is kept at a low value (0.1 V) to minimize the leakage current. At zero gate voltage, leakage current is almost negligible (10^{-13} A/μm), and at high gate voltage $V_{GS} = 2$ V, the current is in the range of (10^{-5} A/μm). The con- centration of ions varies with pH, so the current is because ions are exchanged between an aqueous electrolyte solution and the sensing surface layer. The device also exhibited a high I_{ON}/I_{OFF} current ratio,

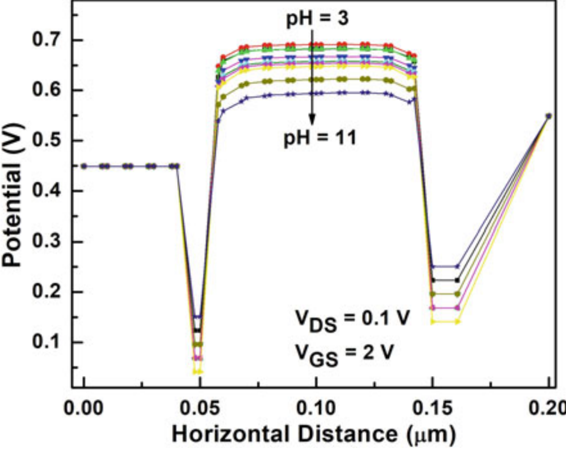


Fig. 3 Variation of potential along with pH solution

i.e., 10^{-8}, as shown in Fig. 5. By dividing the highest on-state current by the most negligible off-state current, the I_{ON}/I_{OFF} ratio is calculated.

At low pH values, the concentration of hydrogen H^{+} ions is higher in the solution, accumulating in the oxide interface. More positive voltage is provided to the gate electrode when more positive hydrogen ions are present, boosting the drain current.

The transconductance curve of a ZnO ISFET is shown in Fig. 6 at gate voltage $V_{GS} = 0$–2 V in 0.01 steps, with the variation in pH values ranging from 3 to 11. The transconductance (g_m) is calculated by differentiating Fig. 5 at the constant drain-to-source voltage $V_{DS} = 0.1$ V. g_m values increase at a particular gate voltage, and then, it starts decreasing. The transconductance is highest (0.342 mS/μm) at $V_{GS} = 1.9\ V$ and pH = 11. A high value of g_m denotes the greater drain current change for a given surface charge change.

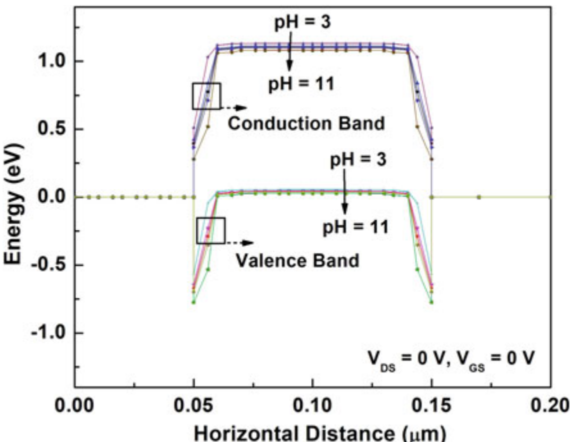


Fig. 4 Energy band diagram of the proposed device in the conduction and valence band

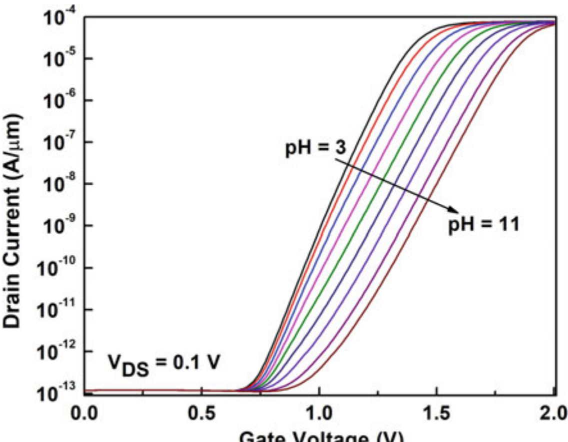


Fig. 5 Transfer characteristics of a ZnO-based ISFET

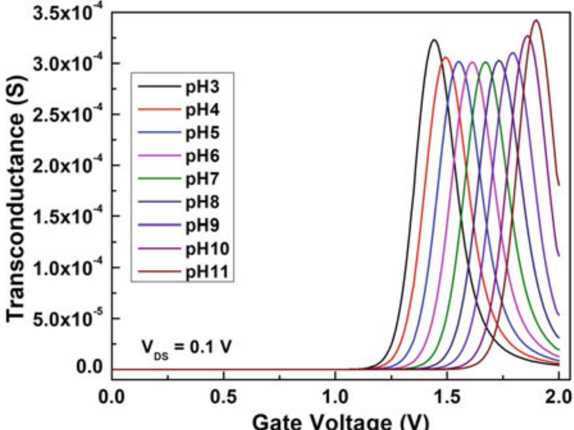


Fig. 6 Transconductance characteristics along with the variation in pH values

4 The Figure of Merits (FOMs)

The proposed device is characterized by various figure of merits (sensitivity, signal-to-noise ratio, and transconductance-to-current ratio).

4.1 Sensitivity

The Nernst equation defines the sensitivity of an ideal biosensor, i.e., 59 mv/pH at room temperature. The Nernst equation is an equation, as shown below, that describes the link between electric potential of the cell membrane and the ionic concentrations that occurred during the electrochemical reaction.

$$E = E_O + 2.303\frac{RT}{nF}\,\text{pH} \tag{6}$$

where E and E_o are the measured and standard potential, respectively, R defines the universal gas constant, T denotes the absolute temperature, n stands for the number of moles of electrons transferred in the electrochemical reaction, and F is the Faraday constant.

The sensitivity of an ideal biosensor is calculated through the Nernst equation which is given as [23]:

$$S_{\text{Ideal}} = 2.303\frac{kT}{q} \approx 59\text{mv/pH} \tag{7}$$

where kT/q defines by the thermal voltage.

In FETs, sensitivity is calculated from FET's characteristics, such as transconductance and the on-off ratio of drain current. The average sensitivity is estimated by the change in threshold voltage and drain current with respect to pH. Threshold voltage varies with pH solutions, as does the concentration of carriers in the solution, which further influences the change in drain current. The threshold voltage sensitivity is defined as

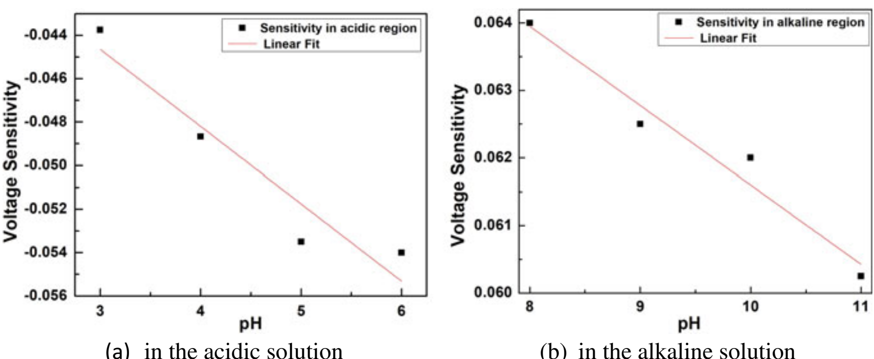
$$SV_{\text{th}} = \frac{V_{\text{th}}(\text{pH2}) - V_{\text{th}}(\text{pH1})}{\text{pH2} - \text{pH1}} = \frac{\Delta V_{\text{th}}}{\Delta \text{pH}} \quad (8)$$

The device's sensitivity is tested with the ZnO layer at various pH solutions (pH = 3–11). The gate voltage ranges from 0 V to 2 V, while the drain voltage is maintained at 0.1 V during the simulation. The electrolyte and oxide interface's properties affect a sensor's sensing ability.

For the calculation of the threshold voltage, a constant current method (10^{-7} * W/L) is used at $V_{DS} = 0.1$ V. Figure 7 represents the voltage sensitivity in the acid medium (pH = 3, 4, 5, and 6) and alkaline medium (pH = 8, 9, 10, and 11). From the voltage sensitivity graph, it can be understood that the device shows 60 mV/pH threshold voltage sensitivity, near the Nernst limit (59 mV/pH).

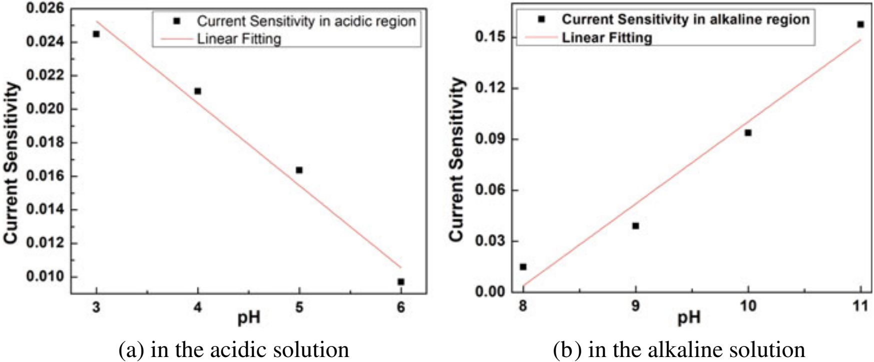
$$\text{Current Sensitivity } (\Delta I_{\text{DS}}) = \frac{I_{\text{var}} - I_{\text{cons}}(\text{pH} = 7)}{I_{\text{cons}}(\text{pH} = 7)} = \frac{\Delta I_D}{I_D} \quad (9)$$

The current sensitivity of the device in mathematical form is represented in above equation and plotted in acid and alkaline mediums shown in Fig. 8.



(a) in the acidic solution (b) in the alkaline solution

Fig. 7 Threshold voltage sensitivity



(a) in the acidic solution

(b) in the alkaline solution

Fig. 8 Current sensitivity

4.2 Signal-to-Noise Ratio (SNR)

SNR measures the detection ability of a device, and it is defined as the ratio of usable signal to noisy signal. SNR can also be represented by power spectral density (PSD), and in mathematical form, it is described as [24]:

$$\text{SNR} = \frac{\delta I_{\text{us}}}{\delta I_{\text{ns}}} = \frac{\delta I_{\text{us}}}{\sqrt{\int S_I dF}} \tag{10}$$

$$S_{I(f)} = \frac{S^2\alpha}{fN} \tag{11}$$

where S_I is the power spectral density of the drain current, f is the frequency, N is the carrier concentration, and α is the Hooge constant.

Figure 9 represents the SNR curve of the proposed device at $V_{\text{DS}} = 0.1$ V and $V_{\text{GS}} = 2$ V, and it shows a sharp peak at $V_{\text{GS}} = 1.25$ V. SNR follows the transconductance, and higher SNR shows a lower detection limit of the sensor [25].

4.3 Transconductance-To-Current Ratio (g_m/I_{DS})

g_m/I_{DS} is also applied as a sensing parameter for FET devices to observe the change in ion concentration [26]. g_m/I_{DS} is an analog performance indicator. The transconductance-to-current ratio characteristics of the ZnO ISFET obtained by sweeping gate voltage is shown in Fig. 10. These characteristics follow the pattern of transconductance. It means g_m increases at a fixed voltage, attains a peak value, and then starts decreasing with the increasing gate voltage.

The proposed device is demonstrated through simulation with excellency for pH application and, in future, can be fabricated through a simpler fabrication process. The

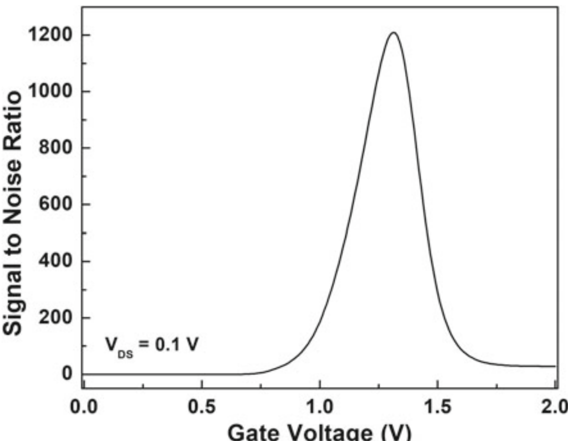


Fig. 9 Signal-to-noise ratio of ZnO-based ISFET

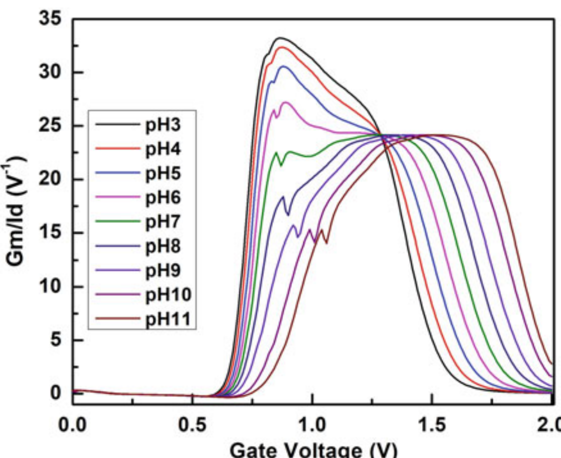


Fig. 10 Transconductance-to-current ratio curve at various pH values

ZnO-based ISFET can be employed in various fields, including life science, point-of-care testing (POCT) devices, medicine, and product safety. The ever-growing application of ZnO-based devices leads to the accumulation of zinc oxide (ZnO) nanomaterials that cause severe consequences to environment and human health. High-care of insulation and disposal must be taken care of while incorporating such devices in health care and environmental monitoring applications.

5 Conclusion

In this paper, the impact of ZnO as a sensing layer of a junctionless ISFET is studied over the various parameters (potential, drain current characteristics, transconductance, and sensitivity), and the results proved that ZnO is an effective sensitive material for detecting H^+ ions in an ISFET. The drain current characteristics show the pH-dependent behavior of a ZnO-based ISFET and confirm that this device can be used as a pH sensor. Polycrystalline ZnO-based TFT pH sensors show Nernst limit sensitivity besides the advantages of ease of fabrication and CMOS process compatibility. The simulated device shows excellent potential as a pH sensor.

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A Wearable Modulated Scattering Technique (MST) Sensor for Early Detection of Skin Tumours

Massimo Donelli, Mohammedhusen Manekiya, Jacopo Iannacci, and Koushik Guha

1 Introduction

One of the most dangerous and mortal skin tumours is the malignant melanoma. When MM symptoms appear, it is too late for saving the life of patient because it easily metastasizes and the vital organs are already invaded. In the past, different research groups tried to develop diagnostic based on microwave probe able to early detect skin tumours [1–5]. Despite their effectiveness, these probes are too much invasive or expensive. In such scenario, MST systems can lead to enormous benefits as demonstrated in the following applications aimed at detect tumours [6, 7] and also in other interesting practical engineering applications [8–12]. MST probes work thanks to the scattering properties of small passive antennas; this characteristic permits to strongly miniaturize the probe and make them particularly suitable for

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wearable biomedical diagnostic apparatus. MST probes present small dimensions, they are cheap and customizable, and they can operate at microwave frequency bands. Moreover, with a proper hardware configuration, they can detect the electric characteristics of materials which surround the antennas probe [11]; this characteristic is of particular interest especially in for the detection of malignant tissues (such as tumours) that presents anomalous dielectric characteristics with respect to healthy tissue. The simplest MST sensor schema consists of an antenna closed on different resistive loads by means of a switch. Usually, the MST probes are powerless because they require very small power that can be extracted directly from the impinging electromagnetic wave by means of a rectenna unit as in [8, 11]. The main limitation of these probes is the switch [9], aimed at changing the different antenna-resistive loads. Micro-electromechanical system (MEMS) switches can help to overcome this strong limitation, as it has been demonstrated in [14, 15]. This work proposes a wearable diagnostic device consisting of a MST sensor and a MEMS switch, aimed at changing the antenna loads. The proposed device can easily estimate the skin electric properties . The goal is to identify skin anomalies that can be related to the appearance of malignant skin cancer. The system is described and designed, and a preliminary experimental measurement campaign has been done in order to assess the prototype in realistic conditions. The results of preliminary measurement campaign are very promising.

2 Mathematical Formulation

The schematics reported in Fig. 1 describe a typical monostatic MST system composed by a reader and a tag. As it can be noticed, MST probes are inexpensive, with compactness and costs comparable to commercial RFID tags [16]. The probes act providing an amplitude modulation switching the antenna tag on different resistive loads by using electronic switches. The changes of impedance at the antenna tag produce variations on the backscattered waves that can be detected by the reader [17, 18]. MST tags can be powerless, and they must be provided with microcontroller, a set of resistive loads, and an electronic switches. In this application, the wearable probe must be powerless since they must be applied to the patient skin. In particular, the backscattered signal that reaches the reader carries information concerning the surrounding media, in this application the dielectric characteristics of the human skin. The power detected at the reader output is reported in the following:

$$P_{\text{reader}} = P_{\text{imp}} S_{11} + S_{env} + P_{\text{inc}} Z_{\text{transf}} \frac{1}{Z_{\text{tag}} + Z_L} + P_{\text{noise}} \tag{1}$$

where P_{imp} is the power of interrogating electromagnetic wave at the reader and S_{11} is the return loss of the antenna reader, and it takes into account reflection due to impedance mismatches. S_{env} is the contribution that takes into account the non-free space condition of the scenario under measurement (since we assume to be in not free

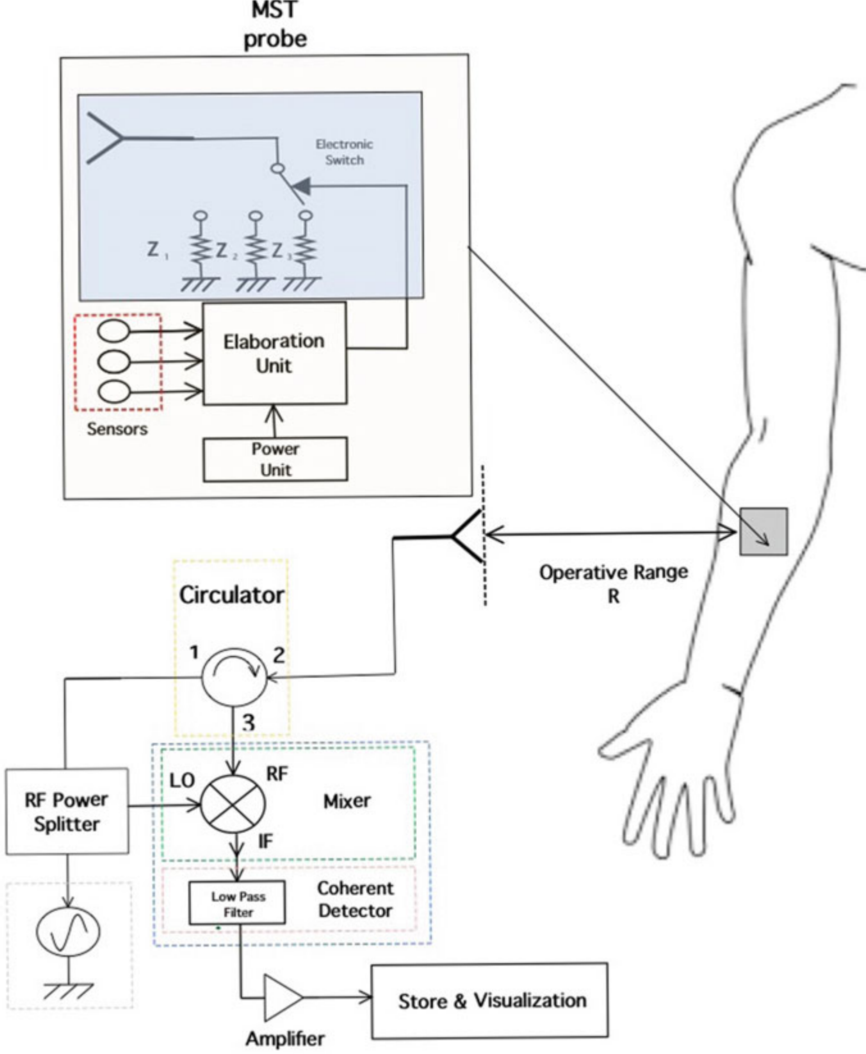


Fig. 1 Schema of the proposed wearable sensor based on a monostatic MST system

space environment), P_{noise} is background noise. The term $P_{\text{inc}} Z_T \frac{1}{Z_{\text{transf}}+Z_L}$ is the only useful contribution that carries the information provided by the tag, where Z_{transf} is the transfer impedance. The transfer impedances take into account the coupling between reader and tag antenna [19], and it is provided by $Z_{\text{transf}} = \frac{(V^{\text{oc}})^2}{2P_{\text{inc}}}$ where V^{oc} and Z_{tag} are the open circuit voltages measured at the MST tag antenna and the tag antenna impedance, respectively. Z_L is the MST resistive load impedance. A suitable amplitude modulation is introduced in the backscattered wave by modifying the Z_L

values and indicated in [9]). Thanks to the modulation, useful information can be isolated from the other unmodulated terms. MST tags are able to detect the changes on electric characteristics of the media surrounding antenna tag, as detailed in [17], by solving the following system of equations:

$$\begin{bmatrix} 1 & Z_{L1} & -\Gamma_{\text{tag}}^{(1)} \\ 1 & Z_{L2} & -\Gamma_{\text{tag}}^{(2)} \\ 1 & Z_{L3} & -\Gamma_{\text{tag}}^{(3)} \end{bmatrix} \begin{bmatrix} \eta_{\text{back}} + \Gamma_{\text{tag}} Z_{\text{tag}} \\ \Gamma_{\text{und}} \\ Z_{\text{tag}} \end{bmatrix} = \begin{bmatrix} \Gamma_{\text{tag}}^{(1)} Z_{L1} \\ \Gamma_{\text{tag}}^{(2)} Z_{L2} \\ \Gamma_{\text{tag}}^{(3)} Z_{L3} \end{bmatrix} \tag{2}$$

where $\Gamma_{\text{und}} = S_{11} + \frac{S_{\text{env}}}{P_{\text{imp}}}$, $\Delta Z_{Li,j} = (Z_{Li} - Z_L j)\, j, i = 1, 2, 3$, $\Gamma_{\text{tag}}^{i}, i = 1, 2, 3$ can be measured at the reader output; the three resistive loads $Z_{Li}, i = 1, 2, 3$; are known and fixed quantities. $Z_{Li}, i = 1, 2, 3$; must be properly chosen. If the antenna tag is embedded in a homogeneous media with a dielectric constant $\varepsilon_r^{(0)}$ and with an impedance η_{back}, the Z_{tag} is modified according to the following relation [17]:

$$Z_{\text{tag}}\left(f, \varepsilon_r^{(0)}\right) = \sqrt{\frac{\varepsilon_r^{(0)}}{\varepsilon_r^{(S)}}} Z_{\text{tag}}\left(f, \varepsilon_s^{(0)}\right) \left(f \cdot \sqrt{\frac{\varepsilon_r^{(0)}}{\varepsilon_r^{(S)}}}, \varepsilon_s^{(0)} \right) \tag{3}$$

where $\varepsilon_r^{(0)}$ and $\varepsilon_r^{(S)}$ are the reference and relative dielectric constant of the medium which surround the antenna tag, respectively, and f is the working frequency.

2.1 System Description

The schema of the proposed skin cancer diagnostic tool is detailed in Fig. 1. It consists of two main sections, an interrogating section and a wearable tag probe.

Reader description Let us start to describe the interrogating section called reader. The reader schema is reported in Fig. 1 which works like a standard monostatic radar (with only one TX/RX antenna); the signal is generated with a programmable direct digital synthesis (DDS) generator able to work from 10 MHz up to 12.5 GHz. The system works at a working frequency of $f_w = 10$ GHz. The antenna reader, aimed to send the electromagnetic wave towards the probe and to retrieve the scattering signal reflected by the MST probe, is a pyramidal horn antenna characterized by a $G_{\text{tx}} = 17$ dBi gain. The signal generator power is $P_{\text{tx}} = 50$ mW. The low power of generated electromagnetic wave does not create health or electromagnetic compatibility problems. The receiver is a combination of an unequal splitter, a microwave mixer, model AKD12000, and a seventh-order Chebichev equal ripple 0.5 dB low-pass filter, at the mixer output. The backscattered signal by the MST probe, placed on the patient skin, is extracted by the coherent detector that converts the microwave signal into a low-frequency signal, called baseband signal. The received signal is amplified thanks to two low noise monolithic microwave integrated circuits amplifiers. In this configu-

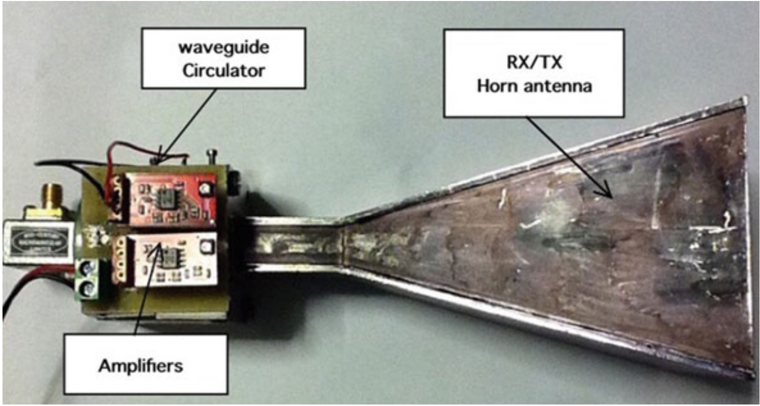


Fig. 2 MST monostatic reader photography

ration, the receiver shows a detectable power of about $P_{rx} = -120$ dBm. A photo of the reader prototype with a detail of circular patch antenna is shown in Fig. 3

MST tag description The wearable MST-RF-MEMS probe is equipped with a Rx circular patch antenna, a power splitter, a rectifying circuit, three different resistive loads Z_1, Z_2, and Z_3, and an 1P3T electronic switch based on RF-MEMS. A detailed tag schema is shown in Fig. 2. For this application, the tag antenna itself is capable to retrieve the skin electric characteristics. The probe works as follows: The incoming EM reaches the tag antenna, and part of the impinging power is used as supply to activate the electronic MEMS switch and the square wave generator. The switch is aimed at changing the antenna tag impedance, modulates the backscattered wave retrieved at the reader output, and provides the information concerning dielectric properties of the media (in this application the skin) that surround the antenna probe as reported in [11] (Figs. 3 and 4).

2.2 Experimental Assessment

In this section, the experimental assessment of the proposed MST system is carried on. In particular, different experiments are carried out to estimate the efficiency of wearable MST tag to detect variations of the skin permittivity and consequently to monitoring the presence of anomalous tissues. A scenario in a controlled environment (a RF laboratory) has been used to create real operative conditions and to characterize the skin with different hydration and the presence of anomalous tissues. In this preliminary assessment only, the dielectric constant has been considered, and the variations of skin conductivity can be neglected because it provides too much

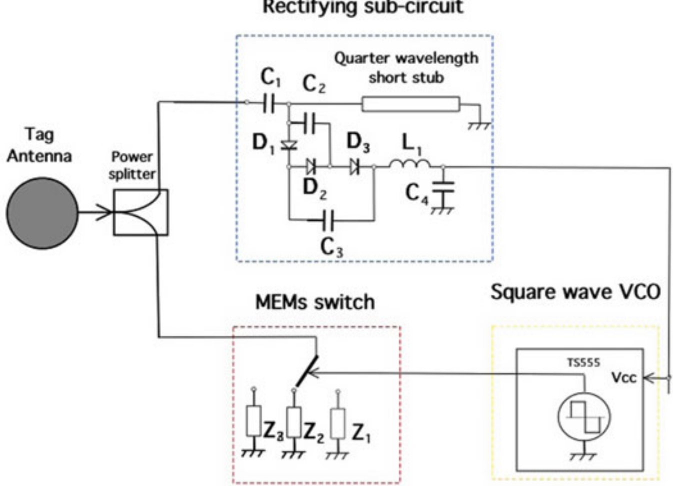


Fig. 3 Schema of the wearable MST tag

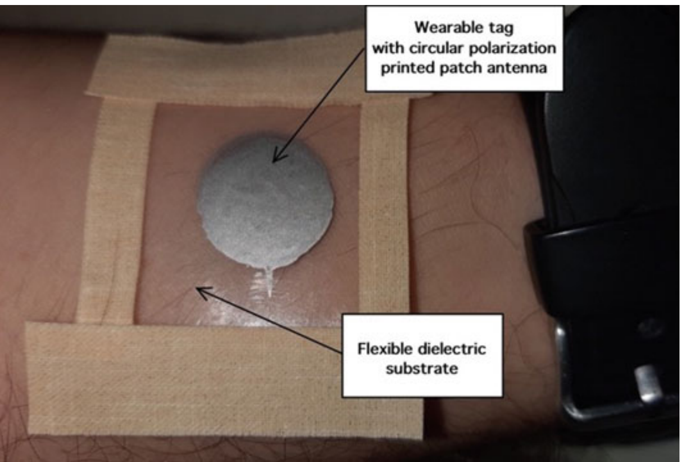
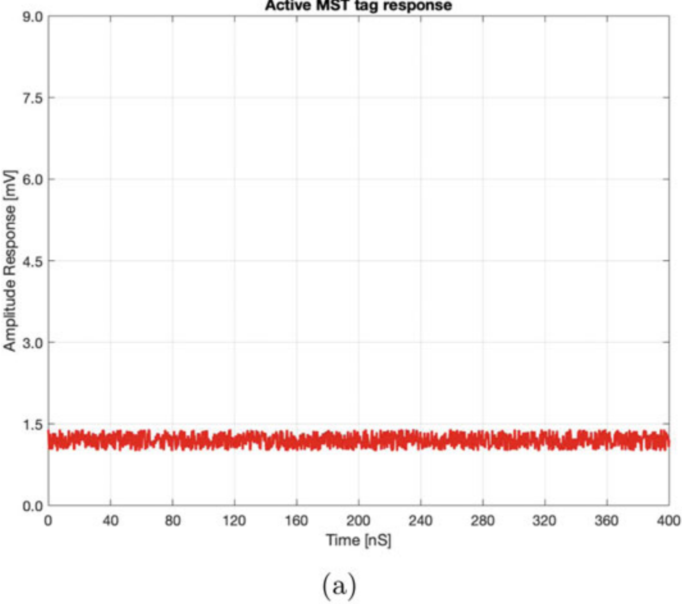
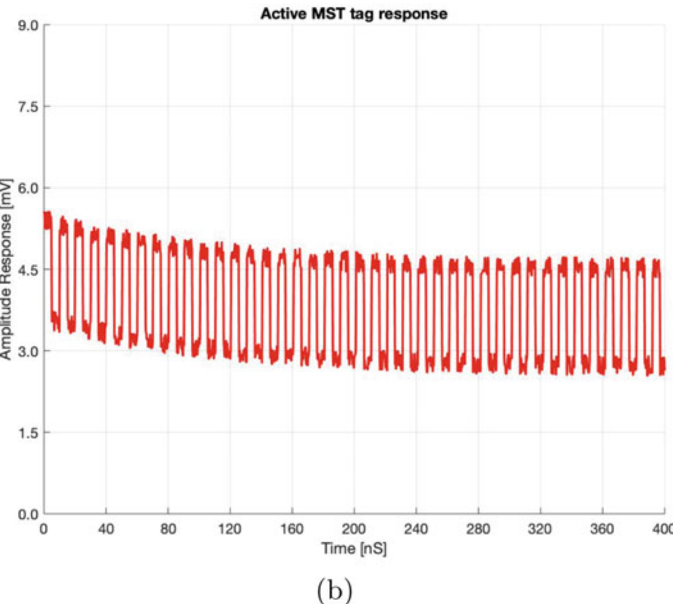


Fig. 4 Photo of the MST tag placed on a subject forearm. Particular of the circular patch antenna printed with a silver ink

variations due to different external factors such as temperature or air humidity. In the first experiment, the distance between MST tag and reader is $r = 2m$. The reflected signal at the system output is measured by means of a digital storage oscilloscope (DSO) and shown in Figs. 5. In particular, Fig. 5a reports the output reader with a deactivated tag, while Fig. 5b shows the low-frequency modulation (at 100KHz) of an active MST tag. In the next experiment, the tag collects the electric characteristic of the skin. The probe is activated, and the MEMS electronic switch has been



(a)



(b)

Fig. 5 Signal measured at the output reader with **a** an inactive MST tag, **b** and a responding MST tag

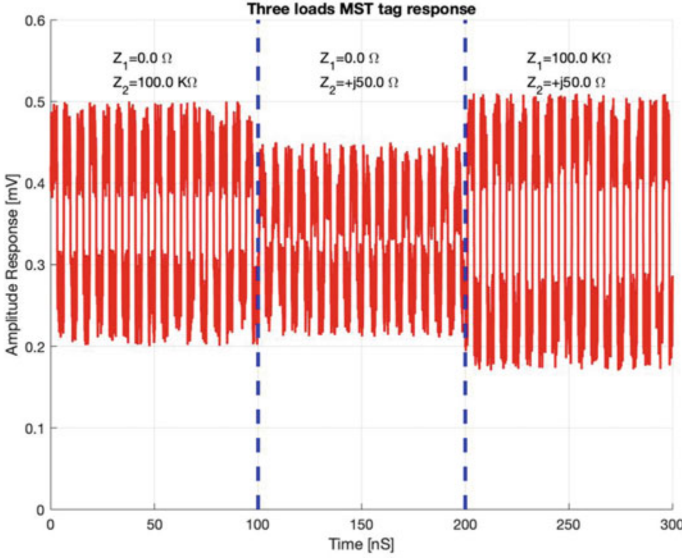


Fig. 6 Effects of the antenna tag impedance changes measured at the reader output

set to alternatively change the antenna impedance with three different impedances. The effects of impedance changes introduce the information useful to retrieve the value of the dielectric permittivity in the backscattered wave by solving the system of Eq. 2. The signal detected at the reader output, for this scenario, is reported in Fig. 6. The data reported in Fig. 6 clearly demonstrated the effects of three loads measured at the output of interrogating section. Skin dielectric permittivity of the subject under test is retrieved by measuring the required parameters at the reader output and then uses them to solve the system 2. The obtained $\varepsilon_r = 31.12$ is compatible with the value of an healthy skin tissue as indicated in [21] which indicates the normal dielectric permittivity of interior forearm at 10 GHz belonging to a range equal to $\varepsilon_r = 26.27 \pm 4.46$.

3 Conclusion

In this work, a skin tumours diagnostic system has been designed and experimentally tested. The tool consists of a wearable probes, and a reading section aimed at providing an impinging interrogating electromagnetic wave and to receive signals reflected back by the wearable probe. In particular, the backscattered signal carries on information related to the electric characteristics of the media which surround the antenna tag. In particular, anomalies and skin deterioration can be remotely detected

with a noninvasive analysis. The preliminary experiments showed the capabilities of this diagnostic tool for the early detection of skin tumours.

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Aspect Ratio Approximation for Simultaneous Minimization of Cross Axis Sensitivity Along Off-Axes for High-Performance Non-invasive Inertial MEMS

Sonali Biswas, Anup Gogoi, and Moushumi Biswas

1 Introduction

Cross axis sensitivity occurs due to the 3D effect of the sensor geometry. An inertial MEMS which measures acceleration must sense the signal in its prime axis and should measure almost zero in the off-axes. But very often, the structure is such that there a slight rotation and tilt in the device. This may be responsible for some cross axis sensitivity in the other two off-axes, which needs to be minimized for high-performance applications [1]. Misalignment and orthogonality are the special parameters in inertial sensors which need immediate attention [2]. Miniaturization of sensors has brought a revolution in every part of the society and application in medical diagnosis is no exception [3]. Human body is the most sophisticated machine and signal pick up from the human body parts requires higher precision and sensitivity in addition to its miniaturization and bio-compatibility.

An inertial sensor when employed for high-performance applications in medical diagnosis demands different design requirements. Inertial MEMS accelerometer which are designed for capturing tremor signals to diagnose nerve disorders usually sense and measure acceleration in one particular axis [4].

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In addition to this, the design requirement for such sensor is that the microsensor should pick up the minimum signal from the off-axis. It is important that for high-performance applications sensor measures almost zero acceleration in the off-axes. Sensor geometry when designed sometimes fails to achieve this and gives rise to cross axis sensitivity which is a critical parameter and therefore should be of prime concern. In order to improve the performance of such sensors in terms of precision and sensitivity, we need to reduce the cross axis sensitivity. The cross axis sensitivity poses a challenge and demands necessary design changes in geometry.

In this work, an attempt is made to improve the performance of the inertial MEMS accelerometer by optimization of aspect ratio in order to reduce the off-axis sensitivity. The objective is to approximate the aspect ratio in such a way that cross axis sensitivity value obtained for both the X and Y axis is reduced and almost equal for both axes. There are several methods with regard to geometry by which one can try to minimize the cross axis sensitivity which include different material considerations, sensor geometry, increase the stiffness by various material considerations. Also, proper arrangement of the piezoresistive elements in the form of Wheatstone bridge can cancel the compressive and tensile strains occurring in the lateral axes [1]. Thus, null voltage appears in the undesired axes.

As reported in many literature, out of all the methods available for minimizing the cross axis sensitivity, novel design geometry configuration can prove to be the most efficient technique. Different geometric configurations for high performance having both merits and demerits have been proposed in literature by Bao and particularly, piezoresistive accelerometers were given by many researchers [4, 5]. Different types of simply supported structures with quad beam and cross beams which gives reduced cross axis sensitivity have been proposed by Kampen [5]. Most of the researchers worked on a central proof mass with support beams having piezoresistors on top of the beams at various junctions to sense tensile and compressive strain. The method where thickness of the proof mass was reduced followed by electroplating with active metal like gold also reduces the off-axis sensitivity to certain extent as reported [6]. In order to enhance the prime axis sensitivity, cross axis sensitivity reduction is a must which can be done by increasing the number of support beams. But this method had fabrication difficulties.

In the present work, the quad structure having primary sensing axis as Z axis is chosen. The aspect ratio which is defined as the ratio of the width of the proof mass to its length is the parameter of optimization. It is very important that the aspect ratio change should not make a considerable weight change of the proof mass. This caution is important to maintain the prime axis sensitivity. The objective of the present work is to propose the approximated aspect ratio for the proof mass which gives the same low value of cross axis sensitivity in both the X and Y axis. Further elimination of the cross axis may be done with the help of Wheatstone bridge circuit. Thus, the novel design proposed has high prime axis sensitivity in out of plane and low cross axis sensitivity of same value in both X and Y direction.

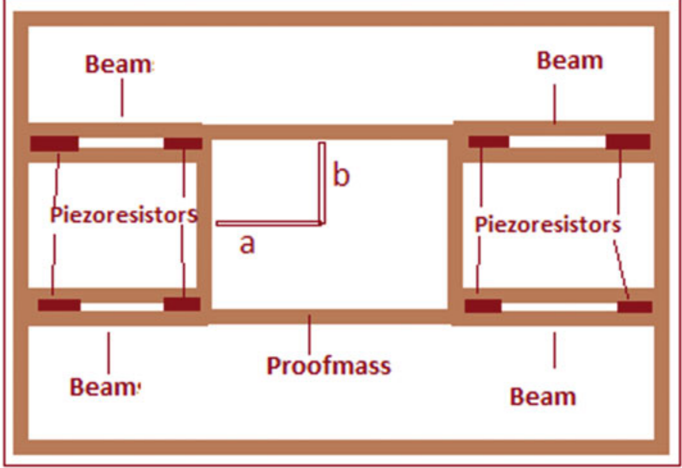

Fig. 1 Quad structure of inertial MEMS

2 Approach for Obtaining Minimized Cross Axis Sensitivity

The quad structure of the inertial MEMS is chosen and the distance from the centre to the proof mass edge in either direction is taken to be *a* and *b* as shown in Fig. 1. The basic approach adopted is based on Kampen Theory [5]. The stiffness of the beam has to be increased so that the sensor does not sense acceleration in the off-axes. This means the stiffness of the beam in *X* direction normalized w.r.t prime axis stiffness is given by ($k_{\theta x}/k_z = b^2$) must have a higher value. Similarly, stiffness in Y direction normalized w.r.t prime axis stiffness is given by $\{k_{\theta y}/k_z = (l^2 + 3al + 3a^2)/2\}$ where l is the length. This can be obtained by maximizing the distance from the centre to the edges in both the direction.

3 Investigations Based on Aspect Ratio Optimization

The aspect ratio plays the key role in deciding the cross axis sensitivity. There are different structures for vibration sensing which are reported in literature. The most popular structure is the quad beam. At first, we consider the aspect ratio that is the width to height ratio of the proof mass which is 1:1 and the cross axis obtained is 4.49 μm^2/rad and 2.5 μm^2/rad along *X* direction and *Y* direction, respectively. This shows that for the initial design, the sensitivity obtained is different for both axes. As the performance of the sensor is dependent upon the cross axis sensitivity, so an attempt is made to approximate the aspect ratio which influences it. Therefore, the

cross axis sensitivity is observed for various values of aspect ratio keeping the mass constant.

3.1 Increase of Length in Horizontal Direction and Decrease of Height in Y Direction

In order to minimize the undesirable off-axis sensitivity along *X* axis, the proof mass length is increased along the horizontal direction and its height is reduced in the *Y* direction, without disturbing the overall mass. It is observed that with increase in aspect ratio, there is a reduction of cross axis sensitivity in *X* direction, whereas cross axis sensitivity increases along *Y* direction. But as the beam length reduces subsequently, mechanical sensitivity increases.

Thus, it is observed that with the increase in aspect ratio, mass remaining the same, mechanical sensitivity increases and the cross axis in *X* direction is minimized. But the limitation is the cross axis sensitivity in *Y* direction is slightly increased.

3.2 Width is Decreased and Subsequently, the Height is Increased

In order to decrease the cross axis sensitivity in *Y* axis, the width is decreased, and subsequently, the height is increased along *Y* axis of the proof mass. With decrease in aspect ratio, the cross axis sensitivity is decreased along the *Y* direction, but along *X* direction, it is slightly increased. As the beam length keeps increasing, the stiffness or mechanical sensitivity goes on decreasing in this manner. It is observed that with the decrease in aspect ratio keeping mass constant, there is a minimization of undesired sensitivity in *Y* direction.

Therefore, the off-axis sensitivity obtained from lateral axes is evaluated in order to observe their dependency on aspect ratio.

With this, it converges our attention to reduce the undesired cross axis sensitivity in both the off-axes simultaneously.

3.3 Simultaneous Minimization of Cross Axis Sensitivity on Both Off-Axes

The cross axes sensitivity is different in both *X* and *Y* direction when the aspect ratio chosen is 1:1. The aspect ratio approximation should be such that the value obtained for the off-axis sensitivity for both the lateral axis is equal. The investigations are made keeping beam length and mass constant so that prime axis sensitivity is

Table 1 Aspect ratio approximation for minimizing cross-axis sensitivity

Aspect ratio	Cross-axis sensitivity	Value (μm^2/rad)
1:1	For X axis	4.49
	For Y axis	2.5
1.4:1	For X axis	3.5
	For Y axis	3.5

maintained. The proposed design has a newer dimension of the proof mass with a aspect ratio of 1.4:1. This is the proposed aspect ratio approximation which gives equal and reduced cross axis sensitivity on both off-axes. The normalized stiffness is around 3.5 μm^2/rad on both the off-axes. The results are shown in Table1.

4 Reduction of Cross Axis Sensitivity by Wheatstone Bridge Method

The perpendicular acceleration coupled gives the cross axis sensitivity. This value can be minimum if the beams are edge aligned with the proof mass and appropriate choice of material which gives higher stiffness. The temperature effect can be nullified by arranging the piezoresistor sensing elements as shown in Fig. 2a, b. The piezoresistors on the arms of the Wheatstone bridge undergo tension (T) and compression (C) as shown in Fig. 2. It has been observed that when we apply acceleration in lateral axis, though ideally under balanced condition the output should be zero, but practically as the stress will not be equal in magnitude, a small value of output voltage exist. This automatically cancels the off-axis perturbations and the temperature variation and at the same time enhances the desired axis signal. This method is popularly used for such applications, and the results are as shown in Table 2.

5 Results and Discussion

In this paper, an investigation is done on a quad micro-inertial sensor for enhancing its performance in terms of low cross axis sensitivity and high prime axis sensitivity. At first, we consider that the aspect ratio of the proof mass chosen was is 1:1, and the cross axis obtained is 4.49 μm^2/rad and 2.5 μm^2/rad along X direction and Y direction, respectively. It has been observed that cross axis sensitivity depends upon the design geometry, so an attempt is made to approximate the aspect ratio. It is observed that with increase in aspect ratio, there is a reduction of cross axis sensitivity in X direction, whereas cross axis sensitivity increases along Y direction. With decrease in aspect ratio, the cross axis sensitivity is decreased along the Y direction but along X direction, it is slightly increased. Therefore in order to obtain

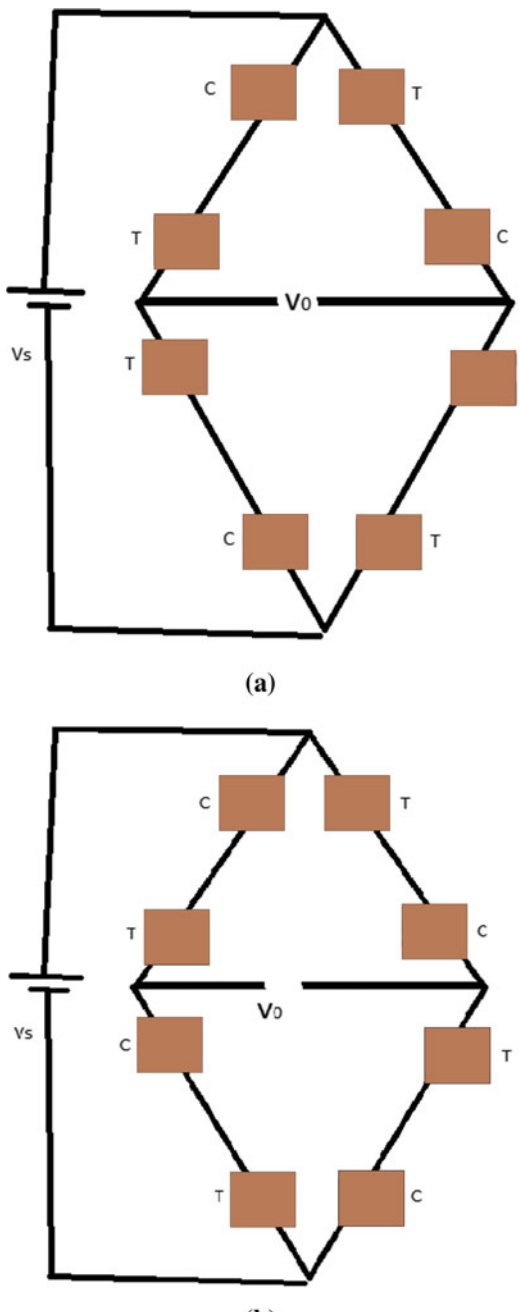

Fig. 2 **a** Bridge circuit with acceleration on *Y*-axis, **b** bridge circuit with acceleration on *X*-axis

Table 2 Obtained off-axis sensitivity on *X* and *Y* axis

Cross axis sensitivity	Value of voltage (mV/V/g)
X axis	0.0004
Y axis	0.0016

reduced and equal cross axis sensitivity in both the axes, an approximated aspect ratio is proposed for the sensor geometry. The proposed design has a newer dimension of the proof mass with a aspect ratio of 1.4:1. This is the proposed aspect ratio approximation which gives equal and reduced cross axis sensitivity on both off-axes. The normalized stiffness is around 3.5 μm^2/rad on both the off-axes. In this regard, an attempt is made to keep the mass constant at the same time in order to have high mechanical sensitivity on prime axis. It can be concluded that cross axis sensitivity which is a critical parameter can be controlled by the approximation of the aspect ratio of the proof mass. Further, the temperature effects are taken care of by bridge circuit which can enhance the sensor performance. The cross axis sensitivity is further reduced to 0.0004 mV/V/g and 0.0016 mV/V/g on both the *X* and *Y* axis, respectively.

Thus, this study brings out the exact dependence of cross-axis sensitivity on aspect ratio. Thus, the cross axis sensitivity obtained is further reduced using the hybrid scheme. Hence, it can be concluded that the approach is novel hybrid scheme involving both aspect ratio approximation and Wheatstone bridge scheme to minimize the cross axis sensitivity.

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A Study on Structural and Magnetic Properties of Magnesium Cobalt Zinc $Mg_{0.6-x}Co_xZn_{0.4}$ $(Fe_{1.5}Cr_{0.5})O_4$ (x = 0.0, 0.2, 0.4, 0.6) Ferrite Nanoparticles

K. A. Khan, Ariful Islam, Bithi Paul, N. I. Khan, Md. Ohiduzzaman, Sazzad Hossain, S. R. Rasel, Rehana Akter Ruma, and Md Shahidul Islam

1 Introduction

Ferrite nanoparticles are a group of metal oxide magnetic nanoparticles with spinel structure of metallic cations at tetrahedral and octahedral crystallographic sites [5, 8, 9]. The ferrite magnetic nanoparticles have shown the excellent magnetic properties and have avowed a great attention for their potential application in numerous field like high-density data storage system, storage the information, magnetic bulk cores, magnetic fluids, microwave absorbers, rechargeable lithium batteries, photocatalysts, biosensor, drug deliveries, therapeutics, etc. [2, 5, 16, 23]. The low electrical loses,

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high saturation magnetization, high chemical stability, and electrical DC resistivity have made the ferrite magnetic nanoparticles as dynamic candidate for the advancement of nanotechnology [8, 21]. Moreover, in the structure of ferrite nanoparticles, the magnetic domains are existed which make ferrite nanoparticles a potential candidate for being used as magneto-optical sensors, catalyst, water treatment, and data storage devices [24–26]. There are many conventional synthesis methods of magnetic ferrite nanoparticles such as sol–gel, Co precipitation, hydrothermal, solid-state reaction, thermal decomposition, solvothermal, microwave-assisted, etc. Among all of these methods, sol–gel synthesis process is considered very eminent because this method offers a low-cost route of synthesis without any special instrumentations, and the polymerization reactions to the formation of gel are happened at low temperature in this synthesis process [9, 22]. After forming the gel of magnetic ferrite nanoparticles, heat treatment is required to remove the residuals volatile elements from the final crystalline structure [9]. Moreover, sol–gel method is very preferable to synthesis the ferrite nanoparticles by adjusting the parameters like sol concentration, stirring rate, and annealing temperature to control the size and shape of NPs [1]. Different types of nanocomposites such as $CoFe_2O_4$ [1, 17], $MnFe_2O_4$ [3], $NiFe_2O_4$ [6, 10, 11], Pr-substituted Mg–Zn ferrites [6], $CuFe_2O_4$ [10], and $ZnFe_2O_4$ [7, 12] were synthesized by using same method. In this study, four kinds of magnesium-cobalt-zinc Mg0.6-xCoxZn0.4 (Fe1.5Cr0.5)O_4 NPs were synthesized by varying the cobalt contents (0.0, 0.2, 0.4, and 0.6) through sol–gel process. Ferrite NPs were probed by vibrating sample magnetometer (VSM), X-ray diffraction (XRD), and high-precision impedance analyzer (Wayne Kerr-6500B). The metal–oxygen bond stretching vibrations of Ferrite NPs were probed by the FT-IR spectroscopy.

2 Methodology

2.1 Chemicals and Reagents

The selection of reactant chemicals is very important to synthesis the desired magnetic ferrite nanoparticles. Highly pure chemical reagents were used to synthesis the ferrite NPs. Commercially available chemicals like $Co(NO_3)_2.6H_2O$ (Merck, Germany), $Zn(NO_3)_2.6H_2O$ (Merck, Germany), $Mg(NO_3)_2.6H_2O$ (Merck, Germany), $Fe(NO_3)_3.9H_2O$ (Merck, Germany), $Cr(NO_3)_3.9H_2O$ (Merck, Germany), ammonia solution (NH_3), acetone (CH_3COCH_3) (Merck, India), ethanol (CH_3OH) (Merck, India), and DI water were purchased for this research work.

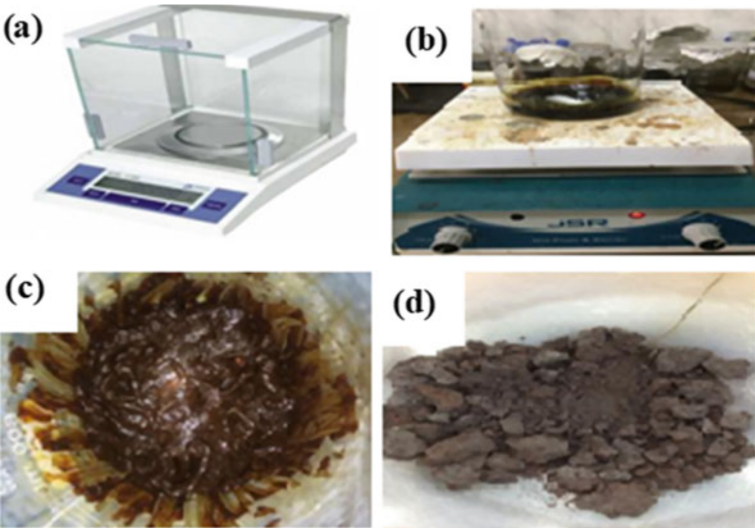

Fig. 1 Synthesis arrangement of ferrite nanoparticles **a** weight machine, **b** mixture solution, **c** gel formation, and **d** dry ferrite powder

2.2 Weighing and Mixing

The raw materials were weighted in their calculated quantity. Then all of the materials were taken in a glass beaker, and small amount of ethanol was added to dissolve the materials. Then it was placed on the magnetic stirrer and stirred until all of the materials were dissolved completely. It took different time depending on the materials. After adding certain amount of ammonia, a "gel" is formed where pH of the solution was controlled strictly at 7. It was then placed on hot plate at 80 °C for 5 h. The gel was dried, and ash is formed. Finally, the ash was hand-milled by ceramic mortar to make it powder form. Figure 1 represents the synthesis arrangement of ferrite nanoparticles.

3 Results and Discussion

3.1 XRD Analysis

Figure 2 showed XRD pattern of $Mg_{0.6\text{-}x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ ferrites nanoparticles with different cobalt contents. The cubic structure was confirmed by the XRD data. Due to the higher substitution of Cr^{+3}, few weak signals were found for Cr_2O_3 phase.

Good crystallization of all ferrite NPs was observed in XRD pattern. The peaks are assigned due to the corresponding planes of (220), (311), (400), (511), (440),

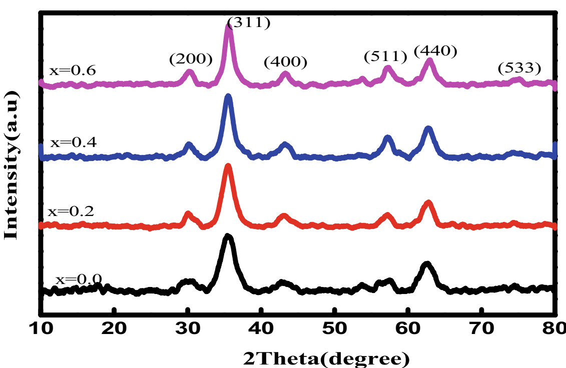

Fig. 2 XRD pattern of $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ ferrites

Table 1 Variation of the value of 2θ with different concentrations of Co contents

Co content (*x*)	Value of 2θ for (220) (deg)	Value of 2θ for (311) (deg)	Value of 2θ for (400) (deg)	Value of 2θ for (511) (deg)	Value of 2θ for (440) (deg)	Value of 2θ for (533) (deg)
0.0	30.01	35.33	43.11	56.99	62.48	74.54
0.2	30.26	35.51	43.36	57.18	62.74	74.45
0.4	30.19	35.52	43.16	57.03	62.61	74.71
0.6	30.21	35.52	43.14	57.02	62.62	74.61

and (533), respectively [4, 8, 9, 18]. Similar peaks are observed for standard Mg-Co-Zn ferrite NPs, and no other phase is present in these nanoparticles. The sharp peaks also indicated the well-crystalline ferrite NPs. It is observed that the highest intensity (311) is found at 35.33, 35.51, 35.53 and 35.66° for $x = 0.0$, 0.2, 0.4, and 0.6, respectively. It is observed that the highest intensity peak shifted to higher angle for $x = 0.0$, 0.2, 0.4, and 0.6, respectively. The peaks of [311] plane were shifted to the higher angle, and lattice constant was decreased for higher cobalt-concentrated ferrites. The cell volume whereas increases of lattice constant which are responsible for peak shifting to lower angle [8]. Table 1 represents the variation of 2θ value with different concentration of Co content.

3.2 *Lattice Constant*

The lattice constant is plotted against Co content in Fig. 3. In Fig. 3, the lattice constant increased with the increase of Co content in $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ nanoferrites. The highest lattice constant was found for 0.2 cobalt content. The lattice constants for $x = 0.0$, 0.2, 0.4, and 0.6 are found 8.38, 8.41, 8.33, and 8.35 Å, respectively.

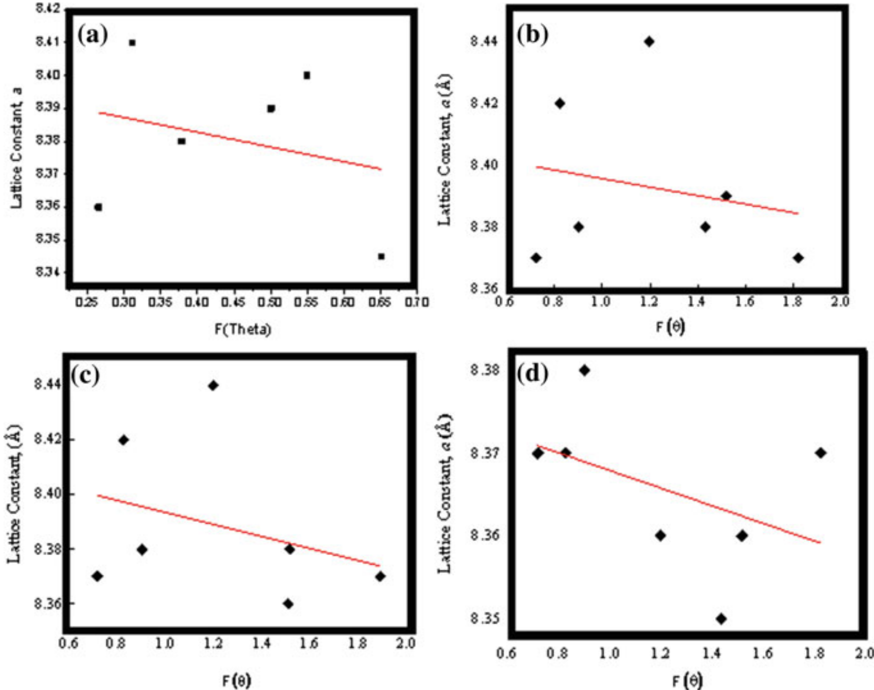

Fig. 3 Lattice constant as a function of N-R function for $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ for different cobalt contents

3.3 Crystallite Size

The lattice parameters and crystallite sizes of all NPs are shown in Fig. 4. The crystallite size of the $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ ferrite nanoparticles was increased with the increase of Co^{2+} content. This is happened because of the minimum atomic radius of the Co^{2+} ion than the Mg^{2+} ion. It is smaller for $x = 0.0$ and maximum at $x = 0.6$ because Mg is replaced completely by Co ions.

3.4 Density Measurement

Bulk and X-ray density of lattice constant were shown in Fig. 5a, b. By using lattice constant and mass–volume ratio, theoretical and bulk densities were determined. The variation of bulk and X-ray densities of $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ *(x = 0.0, 0.2, 0.4, 0.6)* can be observed from Fig. 5a. The X-ray density of nanoparticles was increased linearly with Co content except for $x = 0.4$. Due to the higher atomic mass of Co than Fe, the theoretical density was increased. The bulk density was also increased linearly for higher cobalt content. The increase of bulk density depends on

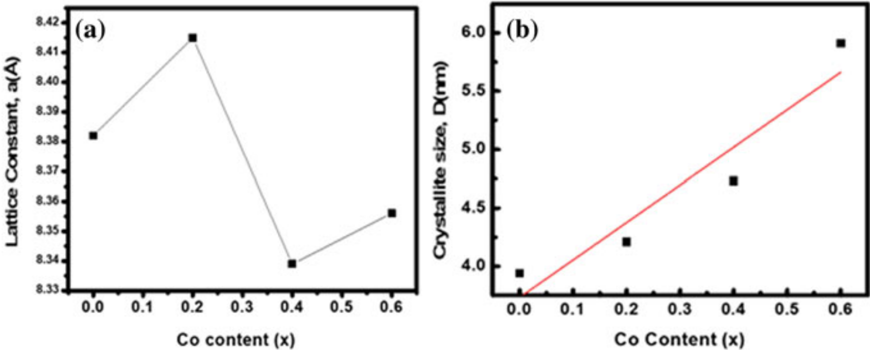

Fig. 4 **a** Lattice constant and **b** crystallite size of synthesized ferrite NPs

the structure of ferrite nanoparticles which contains intergranular porosity. Moreover, the size increases for $x = 0.4$ which may create intergranular porosity. Due to high rising growth rate of grains, the pores were entrapped by grains [8]. To the compact microstructure of NPs, the bulk density was increased for 0.2 and 0.4 values of x. Figure 5b showed that the X-ray density is higher than bulk density, and it can be stated that when magnetic ferrite nanoparticles are fabricated, few crack and pores are made and vacancies are also occurred in the lattice [8]. Thus, it can be explained that experimentally density may have these defects but when it is determined by using the volume of unit cell as well as the lattice parameter of NPs, then defects are reduced significantly.

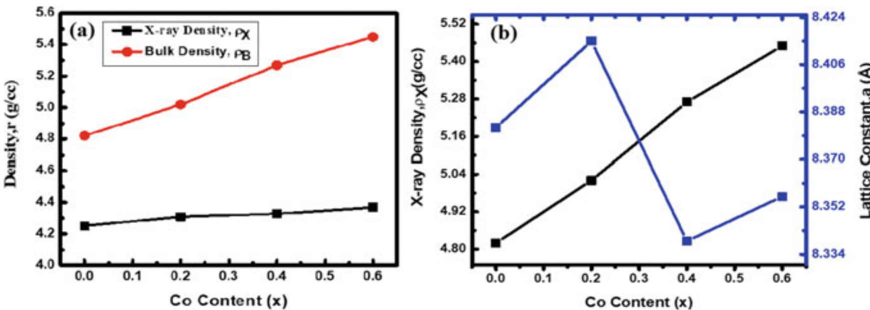

Fig. 5 **a** X-ray and bulk density with different cobalt content and **b** comparison of X-ray density and lattice constant with Co content

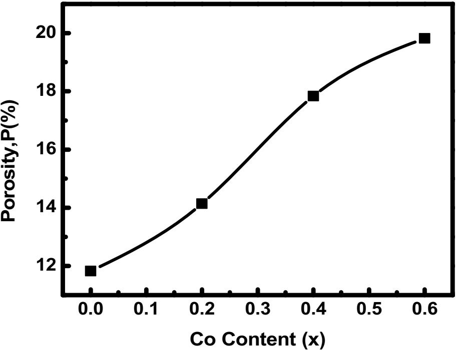

Fig. 6 Variation of porosity as function of Co content

3.5 Porosity Measurement

The porosity mainly defined the grain size of ferrite nanoparticles. The variation of the porosity for different cobalt content is observed in Fig. 6. The total porosity is calculated by the summation of inter and intra-granular porosity.

The poor magnetic and mechanical properties of ferrite nanoparticles indicated the intra-granular porosity and that may practically impossible to eliminate [4]. This might be happened due to the low oxygen pressure, high temperature, and over-sintering of NPs.

3.6 FT-IR Analysis

The absorption band of spinel ferrite phase in $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ nanoparticles was probed by the FT-IR spectroscopy at room temperature (wavenumber 400–4000 cm^{-1}). The FT-IR spectrum of all ferrite NPs is shown in Fig. 7. There are two significant absorption peaks revealed in the FT-IR spectra of spinel magnetic ferrite nanoparticles due to the intrinsically stretching vibrations between oxygen bands and metal cations [8]. Figure 7 revealed two absorption bands at around 400 cm and 535–540 cm. At the tetrahedral site, the high-frequency vibration of metal–oxygen is responsible for the peak at 535–540 cm^{-1}, and the low-frequency vibration at octahedral site is responsible for the peak at 400 cm^{-1} [1, 13, 20]. In the figure, only octahedral site stretching was observed because tetrahedral site stretching is appeared near 400 cm. Table 2 represents the peak positions at the tetrahedral site for all ferrite NPs. The table indicated that the peak position for tetrahedral site vibration is found at higher wavenumbers due to the higher concentrations of Co. On the other hand, a negligible band for the bending and stretching of hydroxyl group is associated at 1540 cm^{-1} [19].

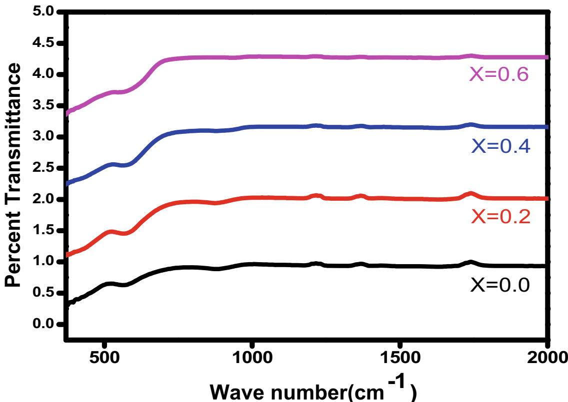

Fig. 7 FT-IR spectrum of $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ ferrites

Table 2 Structural parameters of $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ ferrites

Co content (x)	Crystallite size, D (nm)	Lattice parameter (Å)	X-ray density, ρ_x (g/cm^3)	Bulk density, ρ_B (g/cm^3)	Porosity (1-ρ_B/ ρ_x) × 100	V_2 (cm^{-1})
0.00	3.94	8.38	4.82	4.25	11.82	535
0.2	4.21	8.41	5.02	4.31	14.14	536
0.4	4.73	8.33	5.27	4.33	17.83	538
0.6	5.91	8.35	5.45	4.37	19.81	540

3.7 *Study of M-H Loop as a Magnetic Characterization*

Figure 8 represents the M-H loop for $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$. The anisotropy constant of all ferrite NPs is shown in Fig. 9a, and b represents the saturation magnetization and coercivity of NPs. All magnetic parameters were represented as a function of applied magnetic field where the variation of magnetic properties was observed for the different concentration of cobalt on NPs. The magnetic properties of ferrite NPs were decreased due to the presence of Zn^{2+}ions in magnesium (showed in Table 3). Replacement of Co ions with the Zn ions can be the reason behind the decreasing of magnetic properties of NPs. The saturation magnetization was decreased for 0.2 cobalt content, then increased for next higher cobalt contents. Moreover, the graph of coercivity shows the lowest value for 0.2 cobalt content and the highest value for 0.6 cobalt content. The coercivity can be increased due to the defect on NPs. The decrease in the coercivity with Co content may be due to a favorable microstructure in the sample. Anisotropy constant has been calculated using the equation: $K = (\mathrm{MS} \times \mathrm{HC})/2$. The saturation magnetization on doped ferrite nanoparticles is affected due to the nonmagnetic characteristics of Zn^{2+} ions [14, 15]. The MA is decreased, and Ms is enhanced due to the polarization effect of ferrite NPs and preference of

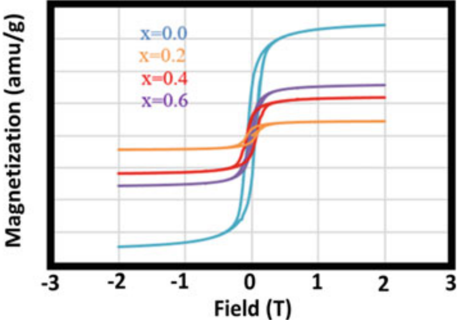

Fig. 8 M-H loop for $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$

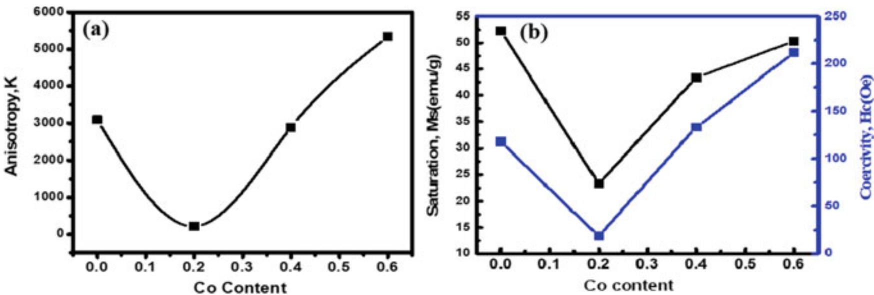

Fig. 9 **a** Anisotropy constant (K) with Co content and **b** saturation magnetization (Ms) and coercivity (Hc) with Co content

Table 3 Calculation of saturation magnetization, coercivity, and anisotropy constant

Co content, (*x*)	Saturation magnetization (emu/g)	Coercivity (Oe)	Anisotropy constant
0.0	52.29	118.00	3085.11
0.2	23.27	19.00	221.065
0.4	43.36	133.00	2883.44
0.6	50.33	212.00	5334.98

tetrahedral site. The increased value of saturation magnetization may depend on the rise of anti-parallel spin coupling due to migration of Fe^{3+}.

4 Conclusions

In this report, $Mg_{0.6-x}Co_xZn_{0.4}(Fe_{1.5}Cr_{0.5})O_4$ spinel ferrite nanoparticles with different cobalt content have been successfully synthesized. The physical and magnetic properties of NPs have been discussed. The lattice parameters of ferrite

nanoparticles were affected by the different concentrations values ($x = 0.0$, 0.2, 0.4, and 0.6). The crystallite size, X-ray density, bulk density, and porosity have been increased with the higher concentration values. It can also be explained by the way that the lattice spacing may increase due to the replacement of larger cobalt ionic radius. Since atomic mass of Co is higher than Fe, the X-ray density is increased for Co content ferrite NPs. In addition, the saturation magnetization, coercivity, and anisotropy constant were decreased for the concentration value $x = 0.2$. This study will serve as the fundamental analysis of Co-doped spinel ferrite magnetic nanoparticles which will be helpful for the future investigations of ferrite nanoparticles.

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Electrical Activities of Ginger Extract-Mediated Silver Nanoparticles in Bio-electrochemical Cell

K. A. Khan, Bithi Paul, Mohammad Abul Kashem Siddique, Monika Paul, and S. M. Zian Reza

1 Introduction

Green synthesis is a unique and cost-effective approach to synthesizing the metal and semiconductor oxide nanomaterials by using plant extract reducing agent during the reaction mechanism instead of chemical reducing agents [1, 2]. This rapid synthesis method is now widely being used to synthesize several nanoparticles such as Ag, Au, ZnO, CuO, and TiO_2 [1, 2]. The smaller particle size, uniform size distribution, good thermal conductivity, and high photocatalytic activities of nanoparticles made a great attention toward the researchers to synthesize NPs [3]. These have been using for different potential applications in various field of science like biotechnology, drug delivery, bio-imaging, photocatalysis, sensor, materials science, biomedicine, electronics, waste treatment, food industry, cosmetics, and energy [4–9]. The non-toxic green approach to synthesizing metal nanoparticles has drawn a great attention due to the multiple biological applications such as biomedicine, targeted drug delivery, cancer treatment, wastewater purification, food industry, and antibacterial activity [3, 10]. Though the plant extract-mediated NPs are now vastly used for the biological applications. In this report, NPs were used for the power generation application in bio-electrochemical cell (BEC). In BEC, various vegetative and fruit extract electrolytes are applied instead of chemical electrolyte [11–16]. Nowadays,

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rising demand and scarcity of electricity have driven researchers to develop BEC to generate the electricity. BEC offers very low-cost power supply in rural and urban areas. At present, different kind of BEC has been already developed by using various vegetables, fruits, and plant extract electrolyte, and the power generation activities of these electrochemical cell have been monitored [2, 12, 13, 16]. In this study, a pair of Zn/Cu electrodes-based BEC was developed with fresh ginger extract electrolyte solution, then the power and power density of BEC were examined. Moreover, Ag NPs was synthesized by using fresh ginger extract (reducing agent), and the effect of NPs in BEC was monitored. The internal resistance of BEC with Ag NPs was decreased, and the maximum power as well as power density of BEC was surprisingly increased. In a nutshell, silver nanoparticles showed an important role to improve the electrical activities of BEC, and these results can open a new era to the development of electronic devices.

2 Method and Materials

2.1 Preparation of Plant-Reducing Agent

Raw ginger was bought from the local market in Bangladesh. About 20 gm of cleaned ginger was washed with deionized (DI) water three times and then blended appropriately. A mixture of 100 mL DI and ginger paste was heated on a hot plate at 60 °C for half an hour. This mixture was kept aside to cool. The filtered ginger extract was kept at 4 °C before use as a reducing agent.

2.2 Green Synthesis of Silver Nanoparticles

About 99.99% pure $AgNO_3$ precursor was purchased from Sigma Aldrich for this experiment. Then, 5 mL of ginger extract was added to the 45 mL $AgNO_3$ (1 mM) solution dropwise at room temperature. The transparent $AgNO_3$ solution was becoming brownish after adding the ginger extract in it which indicated the reduction of silver ions to the silver nanoparticles. The formation of Ag NPs further confirmed by various characterizing tools. The step diagram of the green synthesis of silver nanoparticles is shown in Fig. 1.

2.3 Characterizations of Green Synthesized Silver NPs

The reduction of silver NPs was primarily affirmed by the visualization of the color change of the mixture solution. It became a dark brown color solution after the

Fig. 1 Color change of mixture solution during the bio-reduction of silver NPs

reduction of silver ions to silver nanoparticles. The nanoparticles were characterized by UV–vis spectrometer (UV-2102, China) and X-ray diffraction instrument Rigaku (Ultima IV 2036E202), and the active functional groups of ginger extract were analyzed by FT-IR measurements Shimadzu (IRPrestige-21).

2.4 Design of BEC

Two types of BEC were constructed named Cell-A and Cell-B by varying the electrolyte solution. A pair of Zn and Cu electrode plates and 150 mL of fresh ginger extract electrolyte solution were used for Cell-A and Cell-B. In Cell-B, a very slight amount of Ag NPs has been used with the ginger extract electrolyte. The experimental set-up of BEC is drawn in Fig. 2.

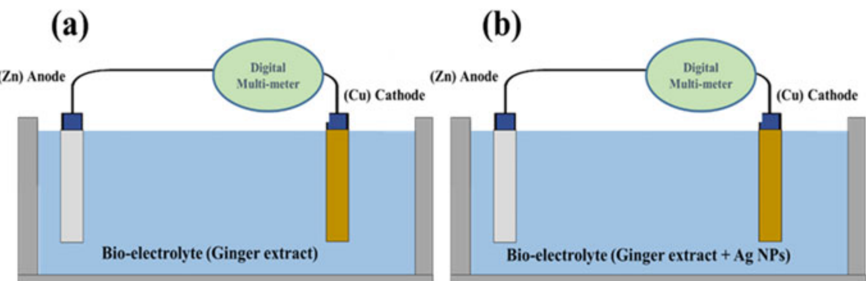

Fig. 2 Design of BEC **a** without Ag NPs and **b** with Ag NPs

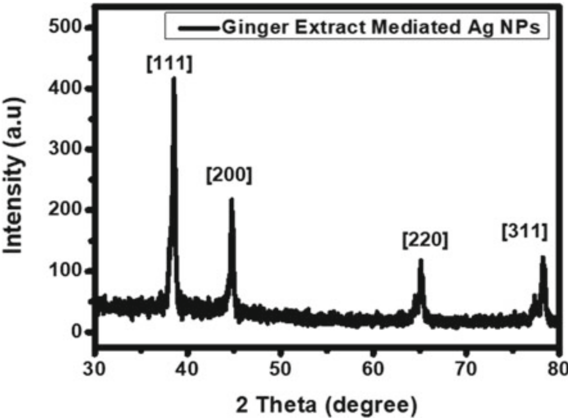

Fig. 3 XRD analysis of ginger extract-mediated silver nanoparticles

3 Result and Discussions

3.1 XRD Analysis

The crystalline structure of Ag NPs has been probed by XDR. The XRD pattern of Ag NPs is shown in Fig. 3. Spectra reveal four diffraction peaks at 2 theta angle 38.54°, 44.76°, 65.12°, and 78.24° for the corresponding planes of [111], [200], [220], and [311], respectively, which correspond to the formation of silver nanocrystal JCPDS No. 04-0783 [1, 2, 17–20].

Crystallite size of ginger extract-mediated NPs is determined by the Debye Scherrer formula, $D = 0.89\lambda/\beta\cos\theta$. Here, θ represents the Bragg's diffraction angle, λ is the X-ray wavelength (λ = 1.54056 Å), and β represents the full width at half maximum (FWHM) [21–23]. The calculated crystal size is 11.34 nm.

3.2 UV–Visible Analysis Synthesized Ag NPs

The formation of silver nanoparticles from silver ions was probed by the UV–visible spectra of Ag NPs. The reduction was performed by the bio-reducing agent ginger extract. The transparent solution of $AgNO_3$ becomes dark brownish after the reduction process. Generally, Ag NPs reveal the surface plasmon resonance absorption in between 380–500 nm and varying the particle size, shape, morphology of NPs as well as the nature of solvent [18, 24]. The absorption of surface plasmon resonance happens for the vibration of free electrons [25]. Figure 4 shows the UV–visible spectra of ginger extract-mediated silver nanoparticles. The position of maximum spectra depends on the particle size of nanoparticles [26]. Here, Ag NPs show maximum absorption at 416 nm.

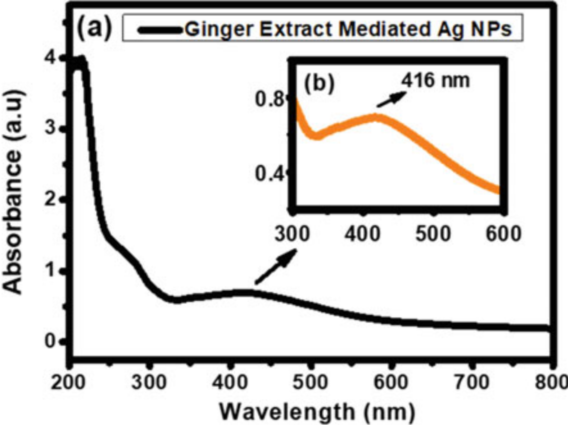

Fig. 4 UV–visible spectra of silver nanoparticles after the bio-reduction **a** full spectra **b** spectra of the range 300–600 nm

3.3 FT-IR Analysis

Figure 5 shows the FT-IR spectra of ginger extract-mediated Ag NPs. The FT-IR spectra identified the active functional groups of plant extract. The functional groups of reducing agents play important role during the reaction mechanism of the reduction process [27]. The figure shows two significant peaks around 3388 and 1638 cm^{-1} that may be appeared due to the strong stretching vibration of -OH group and C–C stretching vibration of aldehyde and flavonoid groups, respectively [28–30]. Moreover, few weak signals were also identified at 3765, 2274, 2135 and 1282 cm^{-1} that may be originated from the O–H deformation vibration of tertiary C–OH groups, and C-O stretching vibration [28, 29].

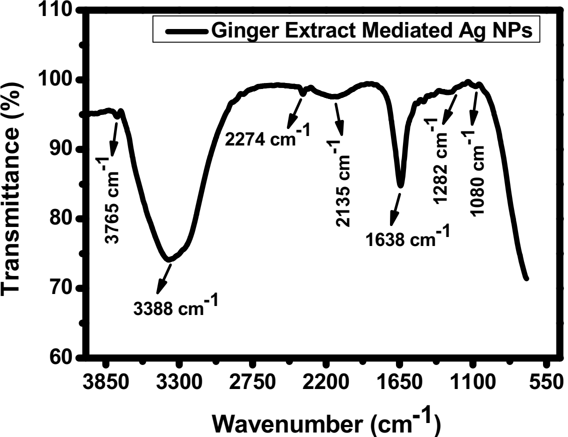

Fig. 5 FT-IR spectra of silver nanoparticles

4 Electrical Activities of BEC

The electrical activities of BEC have been evaluated by monitoring the maximum power and power density of BEC with and without NPs. Figure 6 represents the electrical performances of BEC. All of the electrical parameters have been integrated by using Ag NPs in BEC. Moreover, the average internal resistances of BEC without Ag NPs and with Ag NPs were calculated and found at 418.90 Ω and 361.16 Ω, respectively. The electrical performance of BEC depends on the internal resistance of the cell, and the performances are amplified with the decreasing of the internal resistance of the cell. The average values of electrical parameters are shown in Table 1. The voltage of BEC is determined by the equation:

$$E = E_0 - \frac{RT}{nF} \ln(Q)$$

The chemical reactions in BEC during the cell voltage generation can be described by the famous Nernst Equation which was discussed in our previous report [2, 11]. Here, Q is denoted for the quotient constant, and it is a very important parameter in developing the voltage of BEC. There are two types of ions found in BEC, and these are reactant ions and product ions. Q represents the ratio of product ions and reactant ions in the electrolyte solution. Higher cell voltage is found for the increasing of reactant ions in cell.

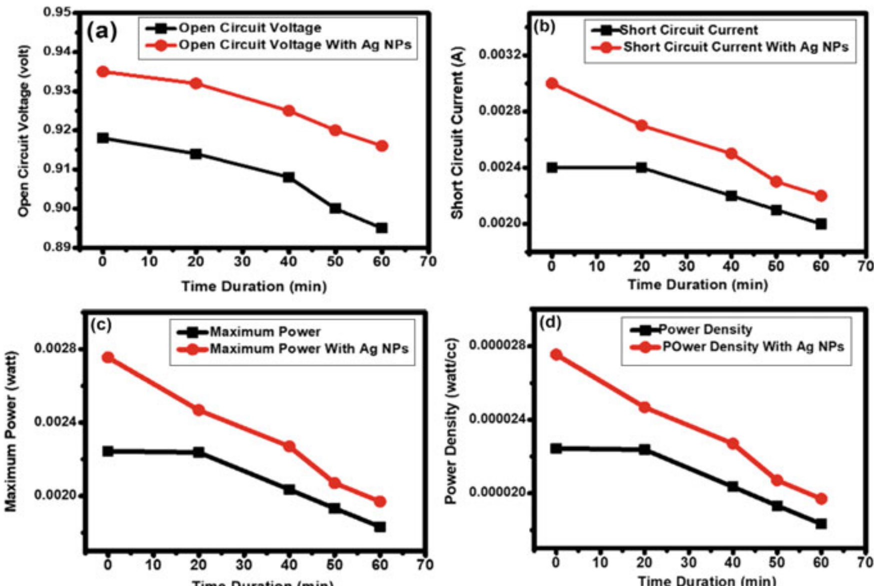

Fig. 6 Electrical performances of BEC with out and with Ag NPs **a** open circuit voltage, **b** short circuit current, **c** maximum power, and **d** power density

Table 1 Average electrical performances of BEC with and without Ag NPs

BEC	Average V (volt)	Average current (A)	Average power (watt)	Average power density (watt/cc)
Without Ag NPs	0.907	0.0018	0.002054	1.66956
With Ag NPs	0.925	0.00208	0.002306	2.30616

5 Conclusion

In this report, fresh ginger extract played an important role as a reducing agent in the synthesis of silver nanoparticles. The active functional groups of the ginger extract are responsible for reducing the silver nanoparticles from silver ions. The crystallite size of silver NPs was found at 11.34 nm. From the literature review, it is generally reported that the antibacterial, antifungal, and antimicrobial activities of green synthesized Ag NPs, but in this report, the electrical activities of Ag NPs in BEC have been examined. From the electrical performances of BEC with and without Ag NPs, it is demonstrated that Ag NPs play a significant role in the improvement of power generation. After the incorporation of ginger extract-mediated Ag NPs in BEC, the internal resistance of BEC has been decreased. Consequently, the power and power density of BEC were increased. Though it is still a challenge to generate sufficient amount of electricity by this single cell, the noteworthy results of electrical activities of BEC with Ag NPs can take a frontier forward to the fundamental development of nanotechnology in low-cost electrical device applications.

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Highly Stable Liquefied Petroleum Gas Detection of $Mn_{0.2}Co_{0.8}Fe_2O_4$ Incorporated in Polyvinyl Alcohol based Nanohybrid

Anshika Singh and Pratima Chauhan

1 Introduction

The adsorption of gases in the ambient atmosphere can change the electrical conductivity of semiconducting materials [1, 2]. This characteristic of semiconducting materials has been used in sensors to identify poisonous and combustible gases such as hydrogen and hydrocarbons [3, 4]. The explosive gas known as liquefied petroleum gas (LPG) includes several hydrocarbons. It is hazardous for people and causes various health and breathing issues [5]. Therefore, the identification of LPG leaks in the environment is a severe problem for humanity [5–7]. The lower explosive limit (LEL) and upper explosive limit (UEL) of LPG sensors have thus been the subject of extensive research. The lowest concentration of a gas at which it will ignite when in contact with any flammable material is known as the LEL [5–7]. Since LPG is a reducing gas, it reacts with n-type materials to improve conductivity while decreasing resistance. The conductivity of p-type materials diminishes and the resistivity rises when exposed to LPG [8, 9]. The most researched materials are ferrites because of their potential in areas like medicine delivery, electromagnetic shielding, water purification, gas sensing, and catalysis [10, 11]. These are determined to be n-type materials and are the subject of extensive research by the scientific community. Due to their numerous applications, hybrid nanomaterials are highly sought after today. These materials' remarkable processability, flexibility, and optical, thermal, and mechanical capabilities of polymers mixed with exceptional features like optical, electrical, and dielectric allow them to meet current and future technological demands [12–15].

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Fe_2O_3/PVP nanocomposite LPG sensor with response/recovery times of 20/23 s was recently described by Kumari et al. [6]. LPG sensor with a response/recovery time of 22/52 s was examined by A. Kabure et al. using a studied CeO_2-Fe_2O_3 nanocomposite [16]. PVA based nanohybrids are gaining popularity due to their simplicity in production, low cost, versatility, and biodegradability [16, 17]. Recently, electrospun tin dioxide decorated with cerium oxide for LPG sensing reported a response time of 45 s at 2000 ppm of targeted gas [18]. Additionally, flexible PET thin films coated with heterostructures of polyaniline and Ce-ZnO nanomaterial for LPG gas sensing demonstrated a maximum response of 80 % at 100 ppm with a response time of 157/154 s [19]. In this way, we report on the chemically and economically processed $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA in the current work that shows excellent parameters as compared to previous kinds of literature. As prepared material is used for fabrication of device and thereafter for a study on LPG gas detection.

2 Experimental Section

2.1 Materials

Iron (III) Nitrate Nanohydrate $Fe(NO_3)_3.9H_2O$, Manganous Acetate $(CH_3COO)_2Mn.4H_2O$, Cobalt (II) Nitrate Hexahydrate $Co(NO_3)_2.6H_2O$, Sodium hydroxide Pellets (NaOH), Polyvinyl Alcohol (PVA) and DI water. All the chemicals were bought from Merck-India.

2.2 Synthesis of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA

As previously reported, $Mn_{0.2}Co_{0.8}Fe_2O_{4\ is}$ synthesized by sol–gel method [20]. All the precursors were dissolved in the DI water in stoichiometric proportions and mechanically agitated continuously for two hours. Then, add 1 M NaOH dropwise to the entire solution until the pH was neutral. The solution was centrifuged at 5000 rpm, and filtrate was repeatedly washed with ethanol and DI water. The generated sample was then dried at 80 °C and calcined at 600 °C.

Additionally, 2 g PVA was dissolved in the 20 ml of DI water at 80 °C until the mixture is homogenous and dense. As synthesized nanoferrites were poured into the solution and the formation of the blend. This blend is used for the fabrication of device. Figure 1 depicts the schematic illustration for the synthesis of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA.

LPG sensing device fabrication and measurements: Spin coating techniques are used to create the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA sensing device on a glass substrate with a $1 \times 1\ cm^2$ size. In the beginning, distilled water, ethanol, and acetone were used to ultrasonically clean the glass substrate. The glass substrate was then homogeneously

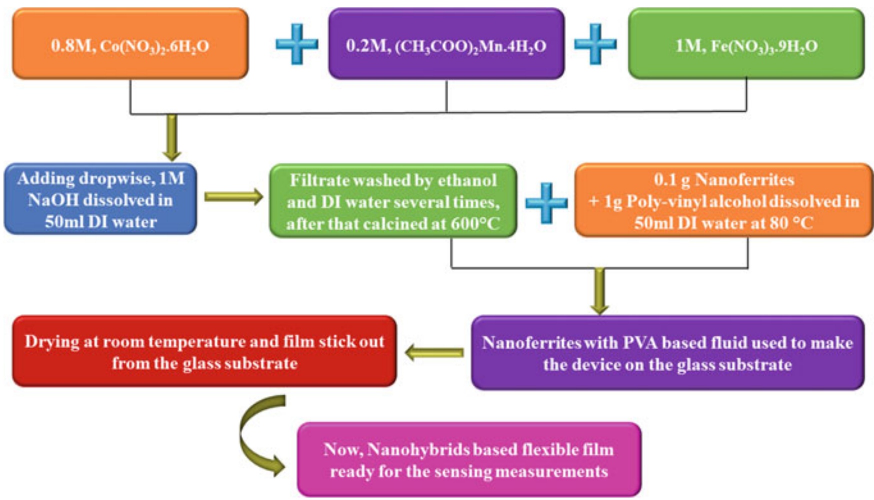

Fig. 1 Schematic illustration for the synthesis of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA nanohybrids

coated with $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA and rotated for 60 s at 1000 rpm before being dried at 50 °C for 10 min. After that, it was dried for 24 h at room temperature. Films were peeled away from the glass substrate after they had dried at ambient temperature. The flexible films were used to detect LPG. Silver paste deposits for the co-planar electrode on the sensing film. An inlet and outlet knob make up the gas sensing setup, and inverted burette method is used to measure the volume of gas. The sensing device is coupled to a current source (6221) and a nanovoltmeter (2182A) to measure dynamic resistance.

3 Results and Discussion

3.1 X-ray Diffraction Analysis

Structural analysis of as prepared sample $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA is confirmed by the X-ray diffraction (XRD). The amorphous structure of PVA is responsible for a broad peak at $2\Theta = 20°$. It can be seen in the XRD pattern, and diffraction peaks of $Mn_{0.2}Co_{0.8}Fe_2O_4$ matched with JCPDS 22–1086 data assigned to the spinel structure [20] as shown in Fig. 2. XRD analysis reveals the formation of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA nanohybrid material; their pattern confirms all the diffraction peaks of $Mn_{0.2}Co_{0.8}Fe_2O_4$, and the presence of PVA is also supported by the presented data [20].

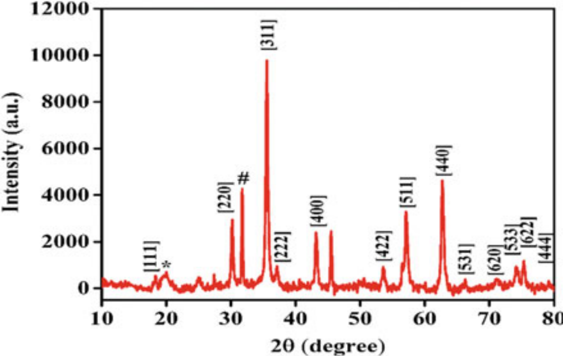

Fig. 2 X-ray diffraction pattern of the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA matched by the JCPDS 22–1086

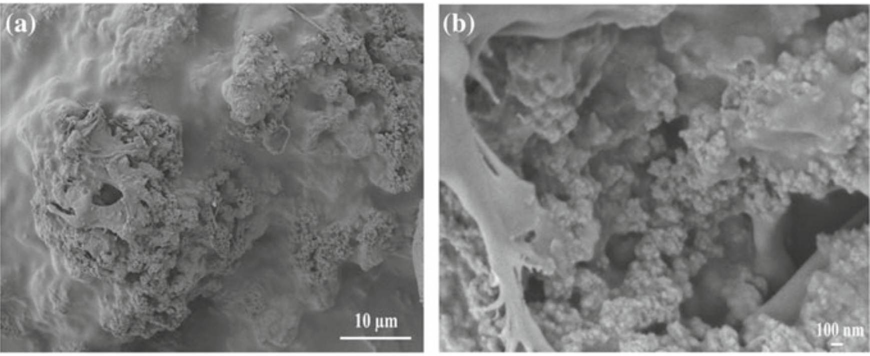

Fig. 3 FESEM micrographs of the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA at **a** 10 µm and **b** 100 nm

3.2 Field-Emission Scanning Electron Microscopy

The surface morphological analysis of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA sample is carried out by field-emission scanning electron microscopy (FESEM). The FESEM micrographs revealed that the $Mn_{0.2}Co_{0.8}Fe_2O_4$ was embedded in the PVA matrix as readily evident in Fig 3a and b.

3.3 UV–Visible Spectroscopy Analysis

According to UV–visible spectroscopy (UV), the absorbance of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA sample was measured in the range of 195–1100 cm^{-1} as shown in Fig. 4a. The broad peak of the absorbance can be seen in the visible region. The optical bandgap of the sample is calculated by Eq. (1):

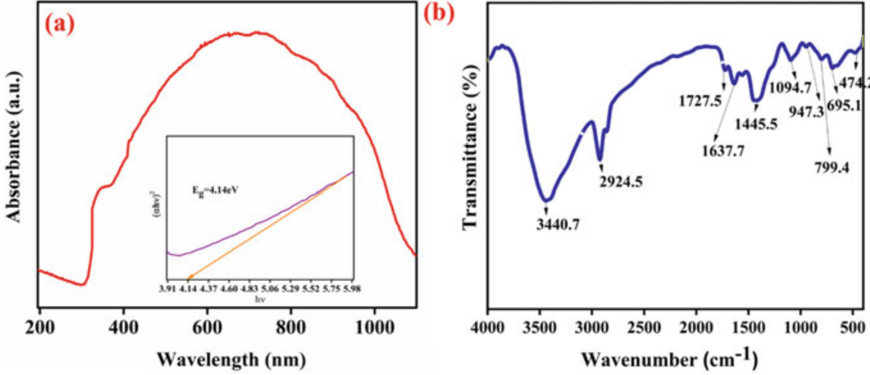

Fig. 4 **a** UV–visible spectrum and Tauc plot in the inset image **b** FTIR spectrum for the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA

$$(\alpha h\nu)^2 = A\left(h\nu - E_g\right) \tag{1}$$

The value of bandgap was obtained by extrapolating the straight-line portion of $(\alpha h\nu)^2$ to $h\nu$. The optical bandgap of the sample is found to be 4.14 eV as can be seen in the inset image of Fig. 4a.

3.4 Fourier Transform Infrared Spectroscopy Analysis

As seen in Fig. 4b, Fourier transform infrared spectroscopy (FTIR) of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA was taken in the range 400–4000 cm^{-1}. FTIR spectra analyses were performed to evaluate all organic bonds or functional groups that were present in the material [15, 20]. In $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA nanohybrid, $Mn_{0.2}Co_{0.8}Fe_2O_4$ has M–O bands at low wavenumber region between 400 and 500 cm^{-1} [15]. Other bands on the higher range of IR spectra confirm the formation of ferrites incorporated in PVA based nanohybrids [17, 21].

3.5 LPG Sensing Measurements

The development of $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA nanohybrid material based sensors for the detection of LPG gas at room temperature is now underway. It is commonly known that LPG is composed of the molecules CH_4, C_3H_{10}, and C_4H_{10} and that the reducing hydrogen species are attached to carbon atoms in these molecules. On the surface of the nanohybrids, LPG therefore dissociates less readily into reactive reducing components. The overall reaction of LPG molecules with adsorbed oxygen can be explained as follows in Eq. (2):

$$C_nH_{2n+2} + 2O^- \leftrightarrow H_2O + C_nH_{2n} - O + e^- \quad (2)$$

where C_nH_{2n+2} represents the CH_4, C_3H_{10}, and C_4H_{10} [22, 23]. When LPG gas is exposed to a nanohybrids sensing device, the change in electrical resistance over time is recorded at various concentrations [24].

When the LPG is exposed to the material, oxygen molecules readily adsorb on the surface of the material due to its high electronegative nature [1, 7]. As a result, the O_2 molecule takes one electron from the conduction band of the nanohybrids and becomes imprisoned on the surface of the material. The electron that gets trapped from the conduction band raised the potential barrier. After introducing LPG gas in the chamber, it gets interacts with the trapped electron on the surface of the nanohybrid material. It releases electrons from the adsorbed O_2, and it takes out the oxygen anions from the sensing material with interacting gas, then potential barrier lowers [24]. The schematic representation of the sensor system is depicted in Fig. 5. The Resistance of the material lowers when exposed to LPG gas at the room temperature due to the interaction of the n-type materials with reducing gas. The basic idea behind gas sensing is that the adsorption and desorption of the target gas cause a change in the physical resistance of the nanoferrite in the PVA nanohybrid material. PVA provides more active sites to the nanohybrid device which ultimately is in charge of the highly effective LPG sensor.

The dynamic resistance study of the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA LPG sensor was conducted with a range of concentration in Fig. 6a. The prepared sample also detects lower concentration of the targeted gas. The rise and decay time for a cycle is also estimated by the exponential fitting as shown in Fig. 6b. The fabricated LPG sensing device shows reproducible nature which is very necessary for the commercial sensors. Figure 6c shows LPG sensor at 0.5 vol % of the targeted gas, and Fig. 6d shows high stability of the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA based LPG sensor. Sensor response of the LPG gas sensing is defined as the ratio of the maximum value of the resistance at a

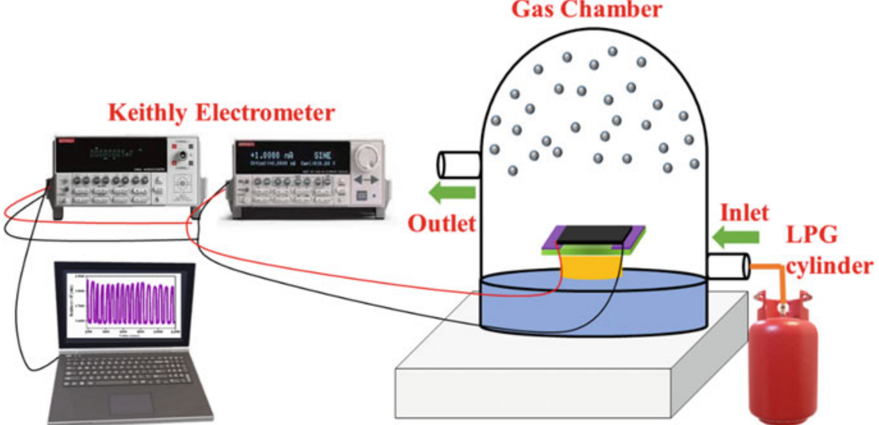

Fig. 5 Schematic diagram for the LPG sensing of the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA nanohybrids

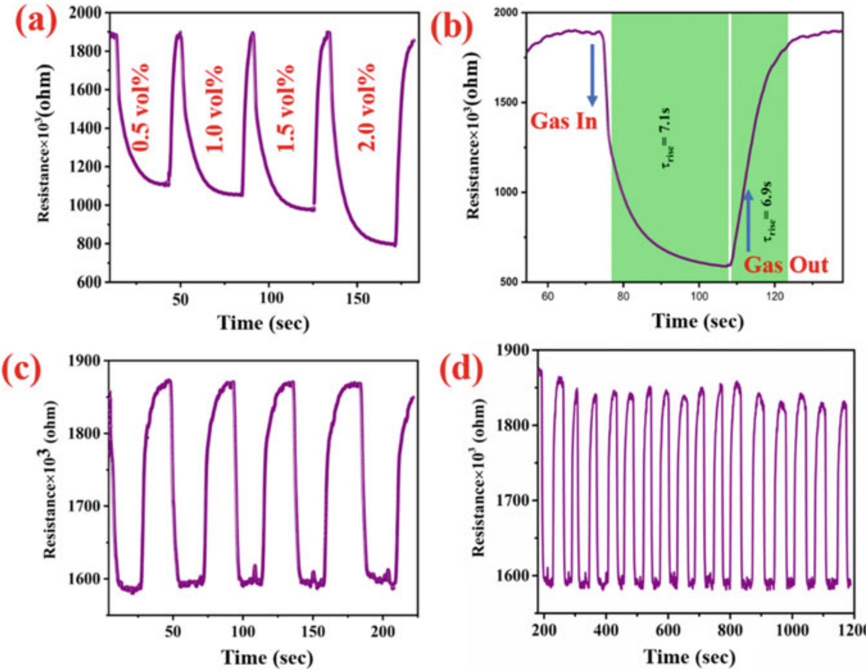

Fig. 6 **a** LPG sensing of the $Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA nanohybrids at different concentration, **b** rise and decay time for the 0.5 vol % concentration of LPG, **c** dynamic resistance study at 0.5 vol % of LPG, and **d** stability graph of the LPG sensor at 0.5 vol %

particular gas concentration (R_g) to the resistance of the gas sensing element in the air (R_a) as given in Eq. (3):

$$\text{Sensor Response\%} = \frac{R_a - R_g}{R_a} \tag{3}$$

Sensor response of the nanohybrid materials is evaluated at the various concentrations and found to be 41 %, 44 %, 48 %, and 58 % for 0.5, 1.0, 1.5, and 2.0 vol%, respectively. The sensing device shows excellent parameters as compared to the reported literature.

Active materials	Target gas	Rise/decay time	Response %	References
Fe_2O_3/PVP	LPG	20/23 s	–	[6]
CeO_2/Fe_2O_3	LPG	22/52 s	–	[16]
Ni0.4Zn0.6Fe_2O_4	LPG	34/45 s	–	[25]
ZnO	LPG	54/20 s	189	[26]
$CoFe_2O_4$	LPG	25/240 s	86	[27]

(continued)

(continued)

Active materials	Target gas	Rise/decay time	Response %	References
$NdFeO_3$	LPG	60/90 s	–	[28]
$Mn_{0.2}Co_{0.8}Fe_2O_4$/PVA	LPG	7.1/6.9 s	41	This work

4 Conclusion

In this study, we provide $Mn_{0.2}Co_{0.8}Fe_2O_4$ intercalated in the PVA matrix synthesized by chemical method. In this manner, the synthesized material employed for the fabrication of sensing device is used for the LPG detection at various concentrations of the target gases. The adsorption and desorption of the gas on the surface of the film determine the sensing performance of the nanohybrid based device. The sensor response of the device was discovered to be 41 %, and rise/decay time of one cycle was discovered to be 7.1/6.9 s at 0.5 vol % of LPG exposure. The prepared sample exhibits excellent qualities at significant lower concentration of the targeted gas and demonstrated the highly stable nature.

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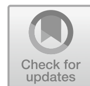
Insight into 3D Printed Eight Well Electrochemiluminescence Biosensing Platforms with Shared Cathode: Towards Multiplexed Sensing



Abhishek Kumar, Manish Bhaiyya, Satish Kumar Dubey, Arshad Javed, and Sanket Goel

1 Introduction

Electrochemiluminescence (ECL) based biosensors have shown potential for clinical diagnosis. ECL is a light emission phenomenon triggered over the electrode surface due to electrochemical reactions. The ECL process driving principle converts electrical energy into radiative energy [1–3]. The ECL process involves producing reactive species that undergo high-energy electron transfer from stable precursors, forming an excited state that emits light [3–5]. The ECL-based sensing approach has received widespread attention for clinical diagnosis, bioanalytical applications, and pharmaceutical analysis due to its numerous promising functionalities such as wide dynamic range, wide linear range, well reproducibility, high sensitivity to analyte determinations, low detection limit, low working potential, low background noise, ease to control over time, location, and ECL signal emission [6–8]. These characteristics give ECL methods the potential for rapid point-of-care detection of various biomolecules. In the field of ECL, luminol is a commonly used organic reagent for enzymatic sensing of various biomolecules. Luminol-based ECL system in the presence of H2O2 emits photons typically in the blue light range. The luminol emission

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spectrum λECL shows a maximum range of up to 425 nm per the applied potential and experimental conditions. Similarly, Ru(bpy)32+ is an inorganic reagent and is considered the gold standard for detecting proteins, toxins, and bacteria. Its co-reactant is TPrA, which serves as redox potential and emits photons in the red-light range. The ruthenium emission spectrum λ ECL shows a maximum range of up to 650 nm per the applied potential and experimental conditions.

As electrode material, ECL sensors utilize organic molecules, inorganic complexes, quantum dots, and semiconductor nanocrystals. For rapid point-of-care onsite detection, the use of carbon-based materials such as conductive carbon ink, laser-induced graphene, and carbon-based 3D printing feedstock filament has been extensively explored for bio-sensing applications. Carbon-based materials are considered an ideal candidate for the fabrication of electrodes. In addition, the induction of nanomaterials in biosensor development has improved the device sensitivity and analytical performance [9, 10]. Multiplex biosensors can perform multiple detections of multiple biomarkers at the same time. The multiplex assay concept is derived from ELISA, but instead of a single signal emission, it emits multiple signals synchronously. The simultaneous detection of various biomarkers has become a hotspot for screening disease in a single run cycle known as multiplex sensing. Compared to traditional biosensors, the multiplexed sensor has shown the potential to distinguish multiple analytes with higher selectivity, sensitivity, and accuracy [11–13].

The fused deposition modeling (FDM) based 3D printing process is a 3-dimensional part fabrication mechanism that uses thermoplastic material in feedstock filament form. It can create complex geometries by the successive stacking of material layer-by-layer fashion. Compared to other non-conventional manufacturing processes, it provides additional benefits such as rapid prototyping, easy fabrication, low cost, minimal material wastage and low material consumption etc. [14–16]. In the last decade, 3D printing has been utilized for developing biochemical sensing platforms such as electrochemistry, chemiluminescence, and electrochemiluminescence. Among all the available detection methods, since it is highly sensitive and selective, the electrochemiluminescence method is the most encouraging technique for sensing various analytes. ECL requires fewer hardware requirements and no external light source, which shows potential for becoming a micro total analysis system (μTAS) because of its capability to undergo miniaturization, among other methods [17–20].

Previously, several ECL-based detection systems have previously been reported for detecting various biomarkers, such as single electrode and Bipolar electrode configurations (open and closed. In an open bipolar electrode ECL system (OBE-ECL), the bipolar electrode and driving electrodes are placed together in the same electrolyte compartment. In contrast, in a closed bipolar electrode configuration (CBE), both electrodes (cathode and anode) are bridged from each other, and the electric current flows through the bipolar electrode only [1, 2, 21].

The work aims to develop a multiplexing ECL platform using the FDM process for sensing various analytes. Hence, herein we present an 8-well shared cathode closed bipolar electrode ECL device design, which can be used for the continuous monitoring of various analytes having different molar concentrations at the same

time. The fabricated device will have the following key benefits such as (i) The single-step detection of various analytes can be possible. (ii) Multiple detections of different analytes (seven) would be possible using a single ECL device. (iii) Compared to other detection methodologies, ECL-based systems provide numerous advantages, including zero background signal, cost-effectiveness, low response time, accurate quantification, excellent selectivity, and easy coupling with miniaturized PoC devices. The primary focus is to develop a rapid, low-cost, and portable single-step sensing platform. The presented device is tested for sensing H2O2 and TPrA, which can be extended for sensing several biomarkers in a multiplexed manner.

2 Experimental Section

2.1 Materials and Methods

For analyte and reagent preparation, Luminol, H_2O_2, tris(2,20-bipyridyl) dichlororuthenium(II) hexahydrate Ru(bpy)32+ , tripropylamine (TPrA), NaOH, NaH2PO4.2H2O and Na2HPO4.2H2O. were purchased from Sigma-Aldrich, India. The step-by-step Luminol, H2O2, TPrA, [Ru(bpy)3]2+ solution preparation procedure was performed, as detailed in our group's previous literature [2, 22]. PLA and graphene feedstock filament is used to fabricate 3D-printed ECL platforms.

2.2 Working Principle and Fabrication of 8 Well-Shared-Cathodes ECL Device

FDM 3D printer (make: BCN3D Sigma D25) was used to print eight well shared cathode closed bipolar electrode ECL platforms using PLA and graphene filament. PLA material was used as a nonconductive substrate for the ECL platform, and graphene was used as conductive material for the ECL platform. The CAD design was prepared using Solidworks™ software. STL format and imported to BCN3D Slicing software to convert. STL file in layer-by-layer file format. The sensing principle and fabricated 8-well cathode shared ECL device is illustrated in Fig. 1 a and b, respectively.

In the fabricated device, the anode and cathode of the bipolar electrode were placed in different compartments. Further, a single cathode of the driving electrode was shared with each compartment. When an electric potential is applied across both driving electrodes (cathode and anode), Triggering the redox reaction on the anode and cathode of the ECL platform results in light emission over the anode electrode surface.

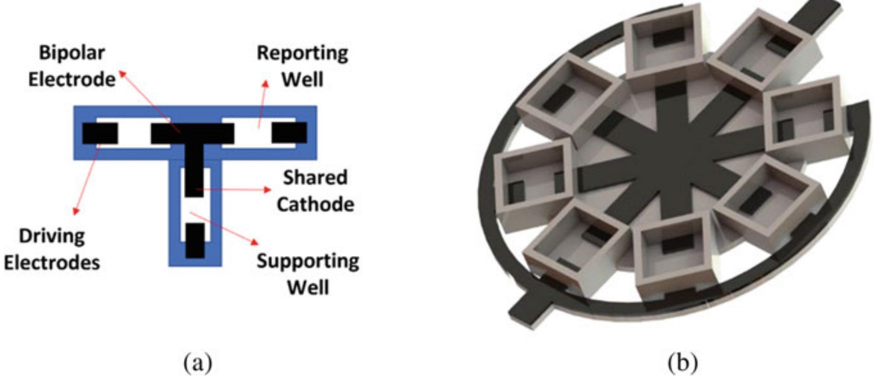

Fig. 1 **a** Working principle of shared cathode ECL system **b** schematic of 8 well-shared cathode ECL device

2.3 ECL Emission Data Acquisition and Analysis

The signal emission was acquired by fabricating a smartphone-enabled in-house 3D-printed ECL system to eliminate the dark room conditions (Fig. 2). An Android smartphone was used to capture emitted ECL signal. The fabricated ECL biosensing platform was powered directly from the smartphone using a DC-DC buck-boost converter. Further, the Data analysis was done using the Java-built android suite application previously reported by our group [1, 22].

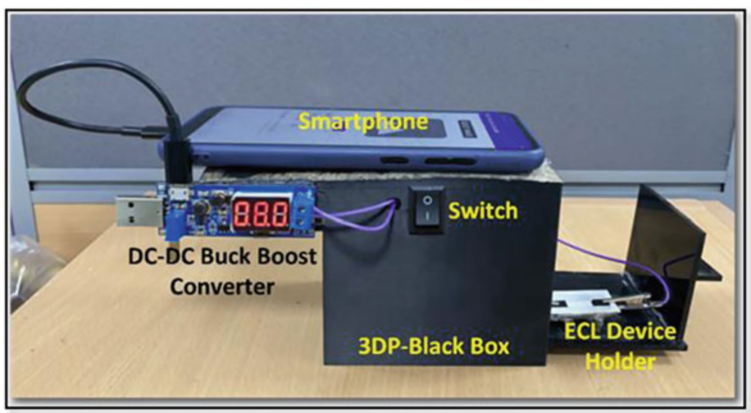

Fig. 2 ECL signal data acquisition system

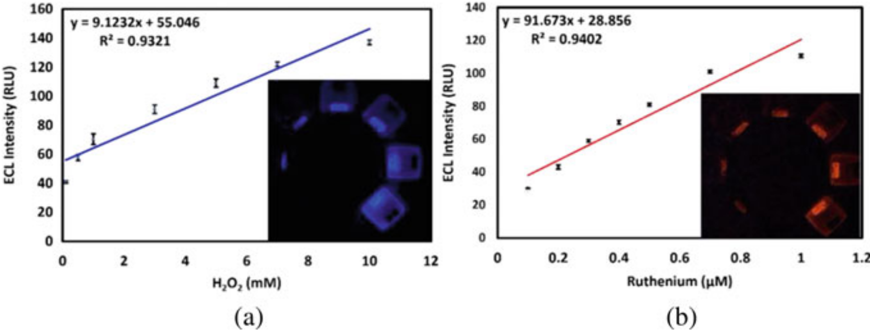

Fig. 3 Analytical performance of Eight well-Shared cathodes. **a** Sensing of H_2O_2, **b** Sensing of Ru(bpy)3^{2+}

3 Results and Discussion

Luminol/ H2O2 and Ru(bpy)32+ /TPrA chemistry have been carried out to understand the analytical performance of 8 well-shared cathodes closed bipolar electrode systems for detecting various biological samples. As ECL intensity is highly dependent on selected process parameters, previously reported [1, 22]. optimal values for luminol (4 mM) and electric voltage (7 V). H_2O_2 and ruthenium sensing was carried out. First, different concentrations of H2O2 ranging from 0.1, 0.5, 1, 3, 5, 7 and 10 mM was pipetted in seven different channels of the same device. Optimized luminol and applied voltage values were used for the H2O2 sensing study. The observed results show that H2O2 has a linear range from 0.1 to 10 mM with a limit of detection of 0.1 mM, shown in Fig. 3a. Similarly, sensing of Ru(bpy)32+ was carried out by pipetting different concentrations of Ru(bpy)32+ (0.1, 0.2, 0.3, 0.4, 0.5, 0.7 and 0.8 mM) into different channels (starting from left) with the optimized value of TPrA 25 mM and voltage 10 V. The observed results show that Ru(bpy)32+ has a linear range from 100 to 1000 µM limit of detection of 30 µM (shown in Fig. 3b).

4 Conclusion

Herein, the developed 8 well-shared cathodes closed bipolar electrode device is explored for sensing H2O2 and Ru(bpy)32. The presented device is a low-cost miniaturized multiplexing and quantitative detection solution for biological samples. In Luminol/H2O2-based sensing, the varying concentration of H2O2 has shown a linear range from 0.1 to 10 mM with a limit of detection (LOD: 0.1 mM). Similarly, in [Ru(bpy)3]2+ /TPrA sensing, the varying concentration of [Ru(bpy)3]2+ has shown a linear range from 100 to 1000 µM with a limit of detection (LOD: 30 µM). The proposed device may be abstracted for performing multiplex sensing

based on ruthenium and luminol for biological samples. The developed sensor may be used for multiple detections of various biomarkers, environment monitoring, protein detection, genotoxic compound detection, bioanalytical applications, pharmaceutical applications etc. Despite the advantages of shared cathode 3D printed eight well CBPE-ECL device, it has some limitations, and further improvements are necessary. Firstly, device sensitivity and accuracy should be measured for different biomarkers. Additionally, the ECL platform is semi-automated and requires manual data acquisition; future work may involve automated data acquisition and analysis.

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Fabrication of MEMS Cantilever: A Case Study

Sonali Biswas

1 Introduction

Cantilever is the most popular micromachined structure and finds its application almost everywhere. It can be converted into a stress sensor by depositing a thin film of certain responsive chemical on top of it. Silicon piezoresistive cantilevers are widely used for sensing force and displacement and is widely used for environmental, biological and chemical sensing applications. Microfabrication is a real boon as many ultra-thin cantilevers can be realized. Cantilever design and fabrication, both have undergone many design modifications and considerations respectively for improving its performance. Microfabrication technology enables batch fabrication [1, 2]. Also, on multiple wafers of silicon many microfabrication processes can be applied. Some of the common ones are material deposition, evaporation and etching. At a time thousands of MEMS devices can be produced by each fabrication. This helps in cost reduction. Also, another marked feature of MEMS is that before designing a whole system the individual components have to be designed first. The most important thing for designing a microsystem is that the fabrication process has to be designed too; otherwise there may be a failure in realizing the device.

Usually the fabrication of MEMS starts with a standard-size single-crystal silicon wafer of 4 inch, 8 inch or 12 inches. Silicon has excellent thermal and mechanical properties which makes it suitable for the said purpose. Moreover, there are some processes long back established for microelectronics, which can be used for MEMS either directly or by slight modification. Besides silicon, materials like silicon oxide, silicon nitride, polysilicon, gallium arsenide, aluminium, gold, etc. are also used for realizing microstructures [1]. MEMS has to its credit a large number of advantages. These being batch fabrication, it makes low cost, lightweight and small size possible.

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At the same time with this technology one can also realize some devices to reach inside human body for monitoring and cure. Moreover, the devices realized by MEMS technology have reduced power consumption and possibility of energy harvesting. In order to make a design ready for fabrication first modelling and simulation is required. The ultimate success of developing or realizing a device depends on going through all the process steps of fabrication correctly. Cantilever is the most widely used device in most of the MEMS used for varied applications. The available literatures show that the MEMS sensors of cantilever type can sense various sensitive biological and chemical parameters [3]. These microsensors have high performance with regard to sensitivity, selectivity and have a less complexity with respect to fabrication. The MEMS cantilever with different design configuration and material selection is reported in different literatures. Many researchers have designed rectangular-shaped cantilever [3–6]. The design is optimized with silicon dioxide which is the best material as there exist etching processes and makes it easy to deposit [6].

2 Methodology

The fabrication process steps in general can be given as shown in the schematic in Fig. 1 [1, 2]. The silicon substrate is chosen. Then oxidation is done and on top of the oxide layer, photoresist is deposited. Then mask is used with structures drawn and on top UV light is exposed. Then mask alignment is done and the unwanted parts are etched. Next stripping is done, the unwanted photoresist is etched away, and the desired pattern is released. The process in practical is not that straightforward and easy.

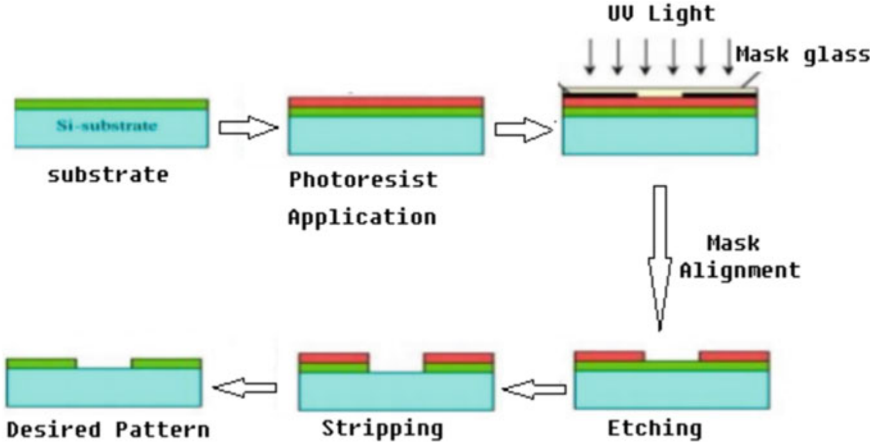

Fig. 1 Fabrication process steps in general [2]

3 Fabrication of the Cantilever Done in Clean Room (Class 100)

The MEMS cantilever is fabricated using the clean room facility of INUP Centre of IISC Bangalore. The protocols of clean room are a must to be followed for successful fabrication of the device. The process steps for the fabrication of the cantilever can be shown as in Fig. 2. Here, surface micromachining technique was adopted and the steps followed are detailed as follows:

- **Wafer detail**: A p-type silicon on insulator of 100 orientation and thickness 3 inches was chosen. The (silicon on insulator) SOI wafer used had three layers, namely the top layer called device layer, buried oxide and the bottom layer or handle wafer which supports the entire device.
- **Substrate cleaning:** At first, the SOI wafer was thoroughly cleaned in a wet etch. Here, RCA cleaning was done using the general wet bench. RCA1 is a mixture of water, H_2O: ammonium hydroxide: H_2O_2 in the ratio of 5:1:1. The substrate is dipped in RCA1 and heated to a temperature of 750 °C for a duration of 10 min. The HF dip is done and next deionized water dip is done. Then RCA2 which is a

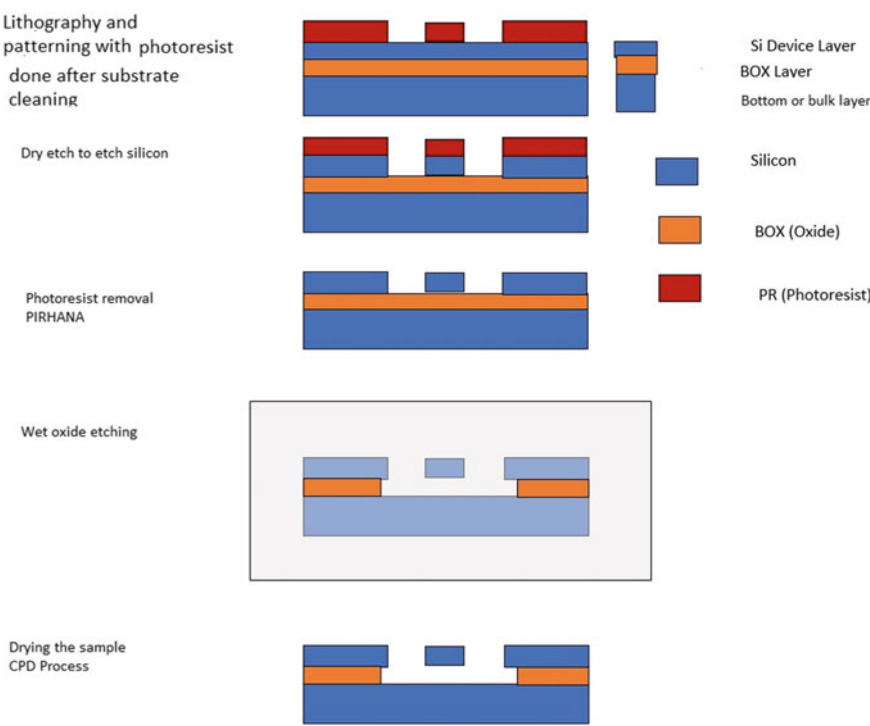

Fig. 2 Fabrication process steps followed for cantilever fabrication

mixture of water, HCL and hydrogen peroxide is done. Heating has to be done at temperature of 75 °C for 10 min followed by hydrogen flouride dip for 10 to 15 s and rinsed thoroughly by deionized (DI) water dip. The samples are then blown with nitrogen for drying.

In this step organic contaminants, metalliccontaminants and native oxide are removed.

- **LPCVD:** Low-pressure chemical vapour deposition was done by depositing 6.2 microns of 1.97 index of silicon nitride. We get here edge, depth, phase and theta. The thickness of nitride was 250 nm. The sample is then made ready for the next step called lithography.
- **Lithography:** The clean room class of lithography had a specification of 100. The sample after thorough cleaning and making it moisture free becomes ready for this process as shown in Fig. 3. In this process, the cantilever pattern is transferred from a glass mask on the cleaned wafer as shown in Fig. 4. In order to remove any moisture content dehydration is done at a temperature of 250^0C. Now, in order to form a patterned coating on the surface, positive photoresist of AZ4562 was used with the help of a spin coating technique as shown in Fig. 5. The spin coat was for 500 rpm 5 s, 4000 rpm 40 s and 500 rpm 5 s. Spin coating was done for uniform spread of photoresist as shown in Fig. 6.

The resist is exposed with ultraviolet light where the underlying material is to be removed. The chemical structure of the photoresist changes, which makes it more soluble in the developer solution. After applying the developer solution, the exposed

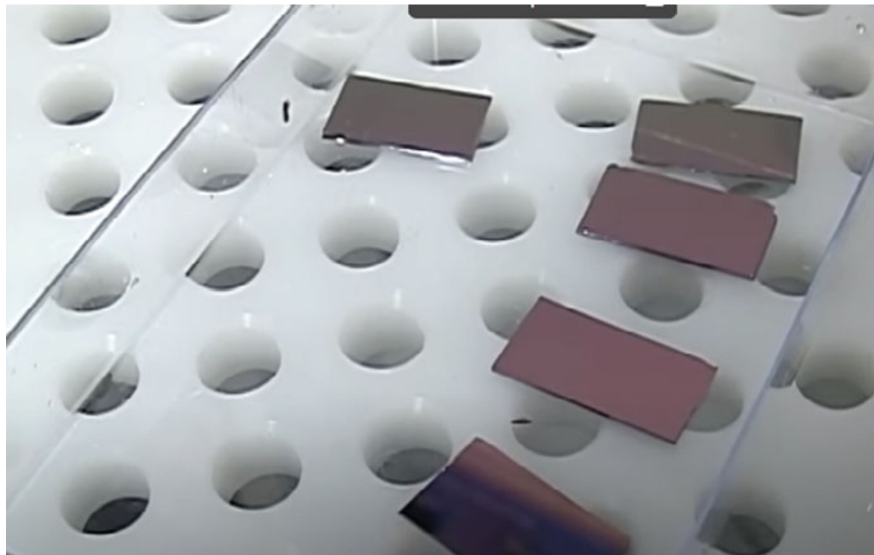

Fig. 3 Samples after cleaning and drying ready for lithography [7]

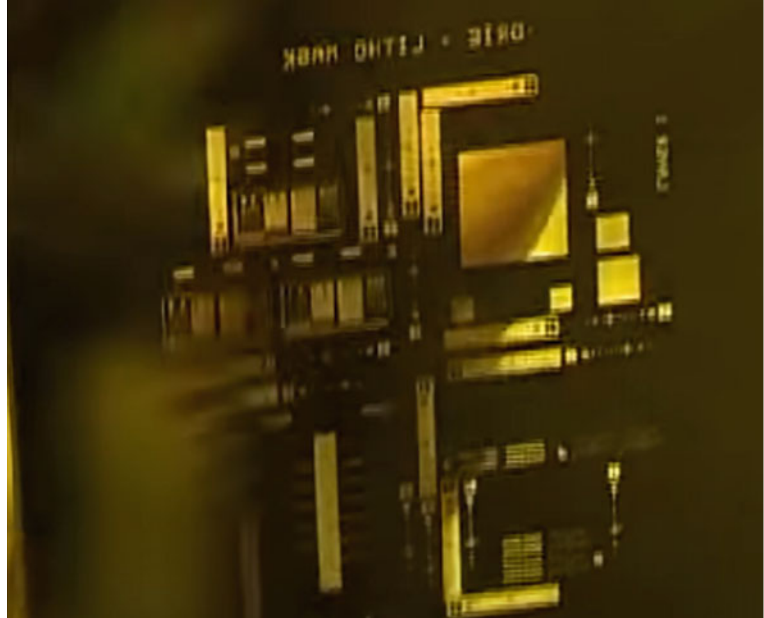

Fig. 4 Glass mask from which the pattern is transferred [7]

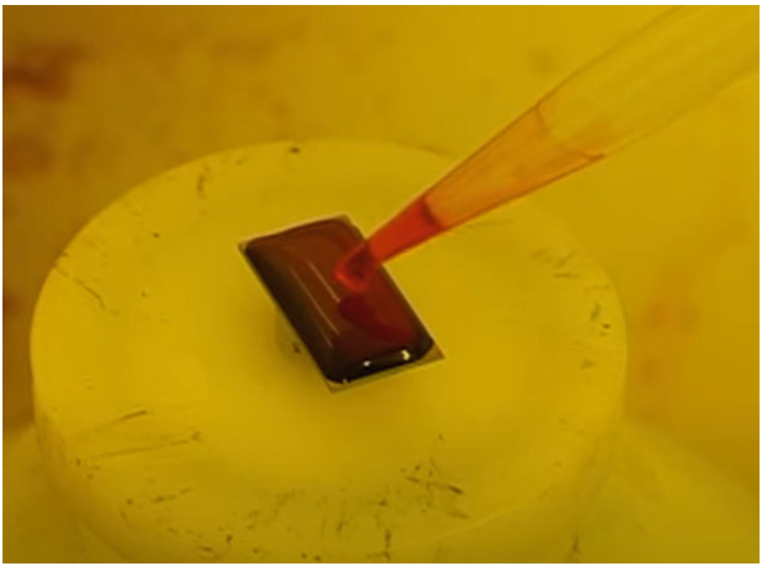

Fig. 5 Photoresist coating applied [7]

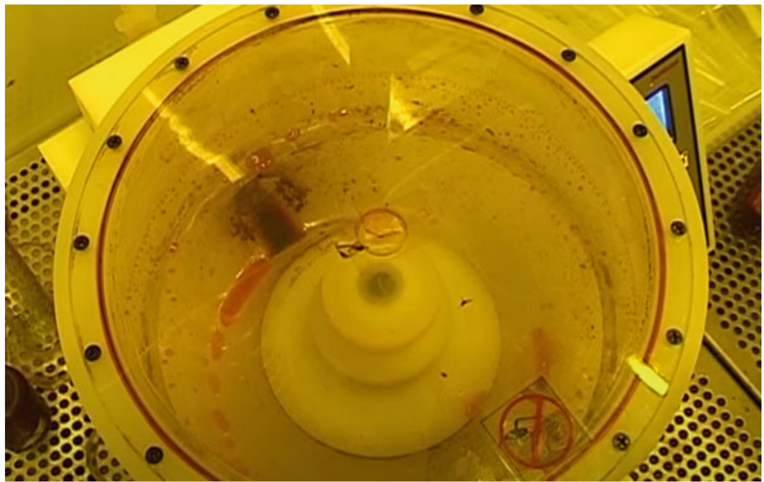

Fig. 6 Spin coating done for uniform spread of photoresist [7]

resist is washed away. The mask therefore contains the exact copy of the pattern which is to remain on the wafer. It almost behaves as a stencil for further processing.

- **Soft Bake:** To remove the solvents soft bake is done for 1 min at 110 °C. We process the entire batch of wafers in a similar way.
- **Pattern Transfer:** First masking has to be done using any software like CoventorWare, and the hard contact is the EVG detail, and there must be UV light constant dosage. This process has an EVG double-sided mask aligned. At first a prefabricated cantilever mask was taken from the mask library of INUP. The mask has both transparent and opaque parts that define a desired pattern. The resist-coated sample is taken, and the mask is placed on top of it. Then ultraviolet light exposure is done for around 2 s. We then load the samples on mask alignment tray, then UV light is exposed at predefined levels. After ultraviolet light exposure, the pattern must be developed on samples photoresist as shown in Fig. 7. Now using a specified developing solution in a petridish, the UV-exposed samples are dipped into it. The developer used was MF 26A for 100 s. The photoresist contains both exposed and unexposed parts. The exposed parts of the photoresist get soluble in the developing solution, thus leaving behind a replica of the mass pattern. The samples obtained after photolithography are as shown in Fig. 8. After this, hard bake has to be done at 110 °C for 3 min to harden the photoresist.

- **Dry Etch:** This process utilizes anisotropic plasma etching of silicon. For etching we use reactive ion etching (RIE) flourine-type tool. First on a large carrier wafer, formaline is applied to make the surface sticky. Then the samples are placed on top of the carrier wafer and loaded on a RIE station load lock chamber as shown in Fig. 8.

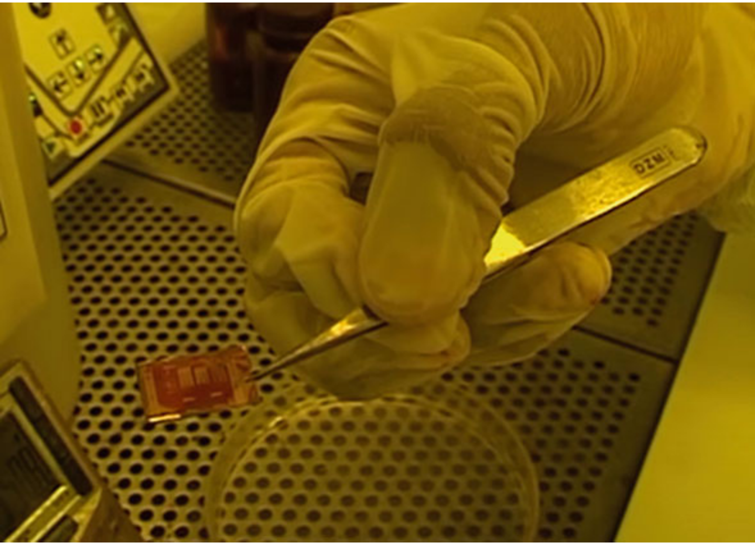

Fig.7 Pattern developed on samples photoresist [7]

Then using a graphical user interface of the station, a vacuum is created inside the load lock. Then samples are taken inside the RIE main chamber. Gases starts flowing at specified temperatures and plasma strikes on reaching the exact appropriate conditions. Flourine ions in the plasma start etching the exposed silicon, and there is a chemical reaction. After etching the samples are unloaded from the equipment and formaline at the bottom surface is wiped away. The samples obtained after dry etch are shown in Fig. 9. The samples obtained are then observed under microscope and the images of a number of beams are as shown in Figs. 10 and 11.

- **Wet Etch:** In order to remove the photoresist we need to do wet etch again using Piranha Solution. The samples are then dipped in a petridish containing the solution for around 10 min. The solution removes the photoresist from the wafer surface. Thus the patterned device layer over oxide is obtained, and there is no photoresist. The sample is then rinsed using deionized water and dried by blowing nitrogen.
- **Release of the Cantilever Using Wet Etch:** The buried silicon dioxide layer is etched out with buffered hydroflouric acid (BHF). Then the sample is rinsed with DI water and Isopropyl alcohol to get rid of the remaining silicon dioxide which may keep the beams suspended. We need to take care to avoid stiction, so the sample should be kept in liquid. The submerged samples need to be observed under the microscope in order to confirm the release. The release of the cantilever is confirmed only when the cantilever and the substrate have differential focussing. Then drying is done using critical point dryer and the cantilever beams are released with minimal stress. When both samples and the chambers are completely dry, these are unloaded and proceeded for testing.

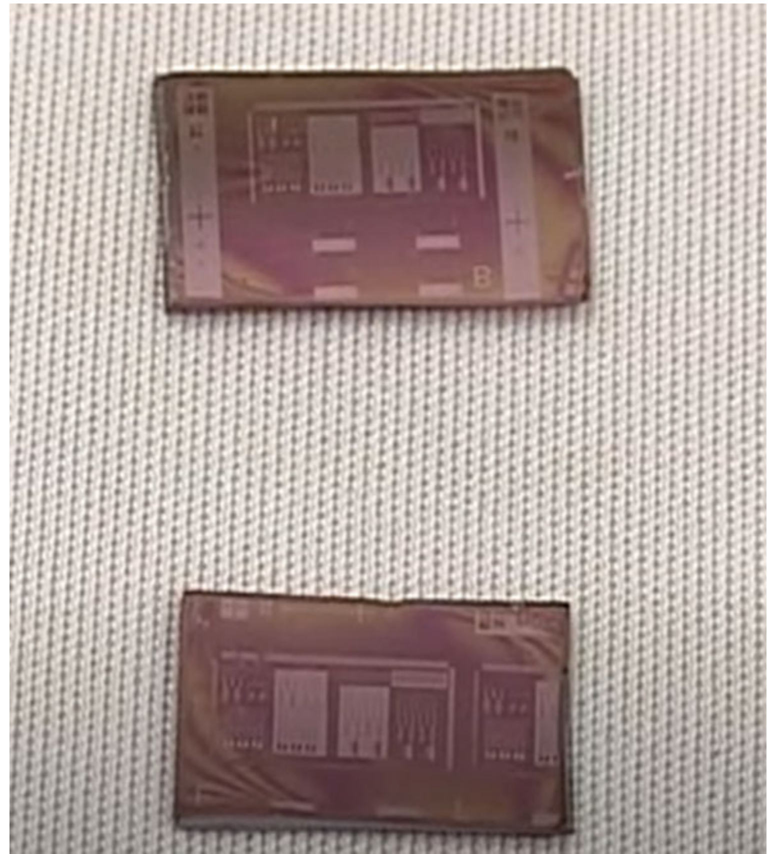

Fig. 8 Samples obtained after photolithography [7]

4 Observation

The testing was done using laser Doppler vibrometer. This step verifies if the cantilever beam released is functional or not. The cantilever beam fabricated is shown in Fig. 12. The characterization is done, and the frequency response is observed as shown in Fig. 13.

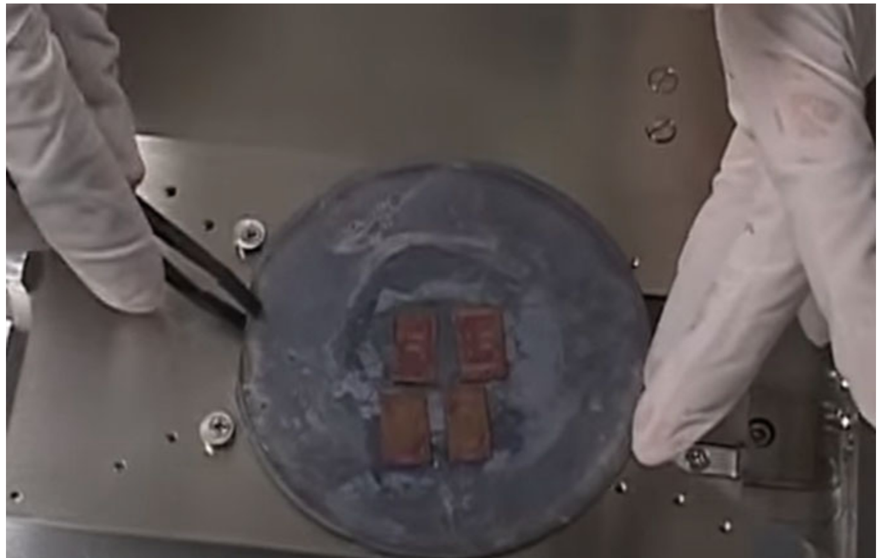

Fig. 9 Samples glued on surface of a carrier substrate [7]

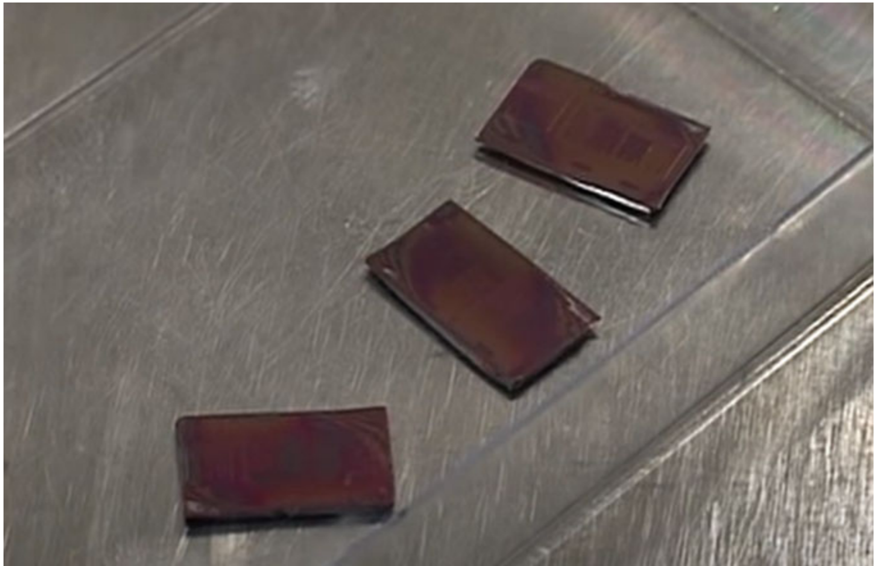

Fig.10 Sample after dry etch, taken out from RIE station [7]

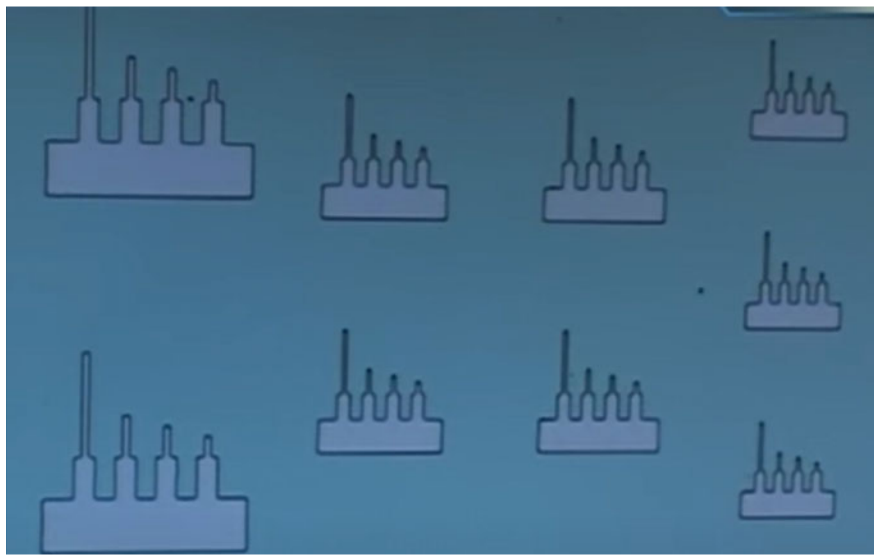

Fig. 11 Cantilever pattern observed in microscope [7]

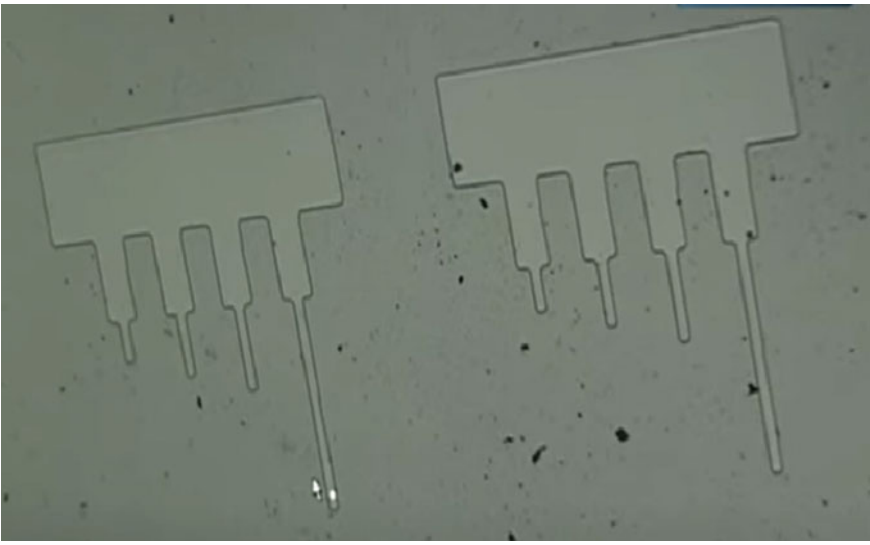

Fig. 12 Cantilever observed after release [7]

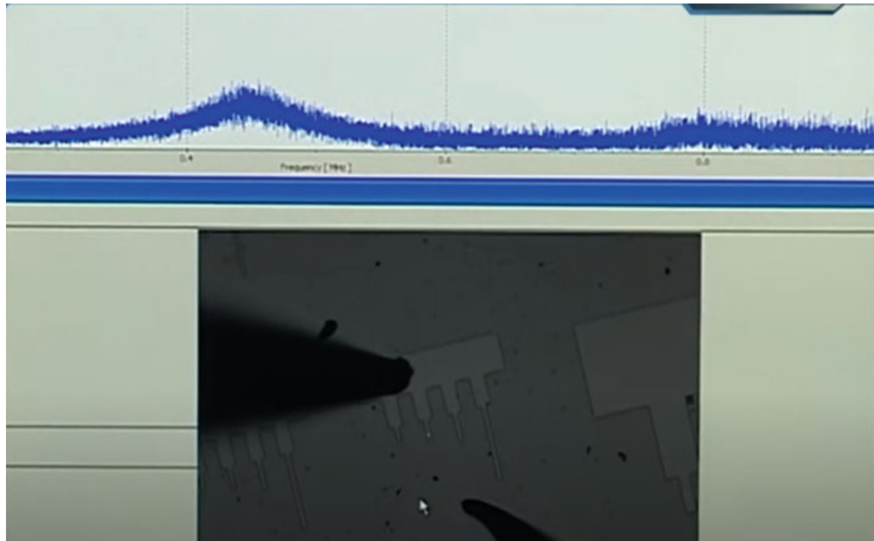

Fig. 13 Frequency response characteristic obtained [7]

5 Conclusion

This paper has brought out the step-by-step process flow of fabrication of MEMS device with a cantilever beam. The pictorial view of each step is also appended in the paper. The test methodology post-fabrication, is also brought and the results are presented. As a case study this paper provides a detailed outline of the broad steps and also provides the characterization results.

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Single Quarter-Wave Phase-Shifted Bragg Grating Modulator on SOI with Enhanced Modulation Technique

Senjuti Khanra

1 Introduction

To cope up with the ever-increasing growth for high-speed data transmission among computer chips and interconnects and also to meet the higher demand for broadband services in metropolitan areas, the use of silicon photonics technology can fill up the gaps between the existing CMOS electronics and conventional photonics technologies. The silicon photonics is making photonic integrated circuits on silicon (Si) for high levels of integration at a low manufacturing cost. The silicon-on-insulator (SOI) fabrication platform is fully compatible with the matured and well-established complementary metal–oxide semiconductor (CMOS) electronics fabrication technology [1, 2], and it provides a high refractive index contrast between Si -SiO2 system.

The optical modulator is an essential component in silicon (Si) photonic circuits, especially for datacom applications [3]. But the development of optical modulators based on Si is a real challenge. Si has insufficient electro-optic effect for modulation, and it is not useful for conventional modulation purposes. So, researchers have to find alternative approaches to produce modulation in Si. Modulation can be achieved in Si through the use of either the thermo-optic effect [4] or optical microelectromechanical systems-based structures [5]. However, these approaches are limited to lower speeds as well as lower tuning frequencies up to MHz. Another approach to achieve modulation in Si is the introduction of Pockels effect [6] by generating strain in Si waveguide. Whereas it requires very high drive voltage leads to the sufficient power consumption for modulation. Finally, it was found by researchers that the

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most promising approach to achieve low-power and high-speed modulation in Si-photonics is plasma dispersion effect [7]. The plasma dispersion effect is interrelated to the density of free carriers in a semiconductor, which was widely examined in the classical work by Soref et al. [7]. Using this technique, various modulators have been reported in the past few years, comprising the carrier-injection Si ring modulators [8, 9], the Si microdisk modulators [10], the GeSi modulators [11], the hybrid III-V modulators [12], the carrier-depletion Si ring modulators [13], and Si Bragg grating modulators [14]. Among all the modulators, the carrier-depletion Si Bragg grating modulators employing reverse bias pn junction diode have demonstrated the most. The Si Bragg grating modulator is advantageous as the device is more compact, and it provides negligible free spectral range (FSR)] with respect to ring modulators.

The modulator proposed in this paper is, quarter-wave phase-shifted Bragg grating modulator on SOI using which high-speed optical modulation can be achieved. Similar type of modulator has been proposed in [15] where maximum 0.4 nm wavelength shift can be achieved. This tuning mechanism can be enhanced by increase in local temperature of the modulator. This is typically achieved by exploiting thermo-optic effect by means of resistive heaters placed in proximity to the device structure. This is the novelty of our work where maximum tenfold of wavelength shift has been reported.

The paper is organized as follows: Sect. 2 is devoted to modeling technique of the proposed modulator. Section 3 reports the simulation results on some important characteristics of the modulator. Conclusions are drawn in Sect. 4.

2 Theory and Modeling Technique

2.1 Device Design

The configuration of the proposed modulator is given in Fig. 1 which comprises of Bragg grating (BG).

A single quarter-wave phase-shift (PS) has been added to the corrugation pattern of the proposed Bragg gratings at the center of the Bragg mirror. All the input/reflect and output/transmit ports of this device are optical. An electrical input port is required to modulate the light by radio frequency (RF), and corresponding modulated light is present in both the optical port. To apply the RF, the device is doped laterally in such a way that a p–n junction is formed along the central axis of the grating mirror over the entire length of the waveguide. To make an electrical connection to the p–n junction region for the RF input, the silicon slab of both sides of the waveguide is also doped laterally. RF is applied to the modulator as shown in Fig. 1, and the modulation performances can be employed in the device by free carrier plasma dispersion effect which will be investigated in the following sections.

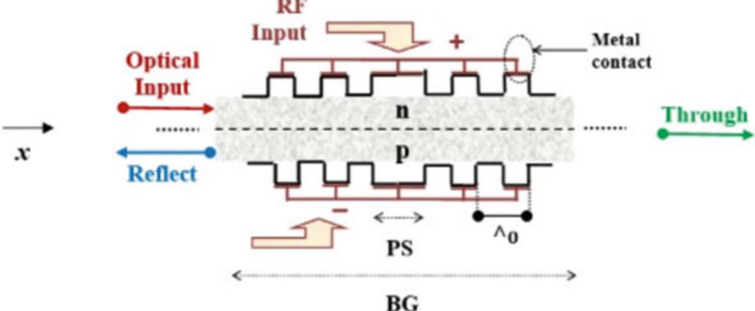

Fig. 1 Structure of integrated phase-shifted Bragg grating modulator. It comprises of single-phase shift (PS) section at the center of a laterally corrugated Bragg grating (BG) mirror on both sidewalls along a central p–n junction

2.2 Modeling of Phase-Shifted Bragg Grating Modulator on SOI

Following the design procedure given in [15], the optical output at the transmission as well as reflection port of the Bragg grating shown in Fig. 1 can be calculated as,

$$R = \frac{T_{21}}{T_{11}} \text{ and } T = \frac{1}{T_{11}} \tag{1}$$

where R and T are the reflection and transmission coefficients, respectively, and T_{11} and T_{21} are the coefficients of the transmission matrix of the Bragg grating [8]. Now, RF is applied in terms of reverse voltage V_R to the p–n junction in such a way that instantaneous charge ($\Delta\ Q$) is stored in the junction capacitance C_j of the device.

where

$$\Delta Q = C_j \Delta V \tag{2}$$

ΔV ($= V_{bi} - V_R$) is the change in applied voltage due to reverse bias V_R and V_{bi} is the built-in-potential in the p–n junction. The corresponding voltage-induced carrier density change for electrons and holes is ΔN and can be calculated from (2) as:

$$\Delta N = \frac{\varepsilon_o \varepsilon_r}{q W_d}(V_{bi} - V_R) \tag{3}$$

where ε_o and ε_r are the free space permittivity and high-frequency relative permittivity of the silicon layer, respectively, q is the electronic charge, and W_d is the depletion layer thickness which is a function of reverse bias V_R [16]. If the reverse voltage is applied, the effective refractive index ($n_{\text{eff}}{}'$) will change due to change in free carriers (ΔN_e andΔN_h) at the junction. This is plasma dispersion effect [7].

This carrier-dependent variation in refractive index of silicon can be obtained from experimental absorption spectra through Kramers–Kronig analysis [17] given by:

$$\Delta n_e = -8.8 \times 10^{-22} \Delta N_e$$

and

$$\Delta n_h = -8.5 \times 10^{-18} (\Delta N_h)^{0.8} \tag{4}$$

where carrier density variations (ΔN_e for electrons and ΔN_h for holes) are in units of cm^3. Equation (4) is valid only at 1550 nm communication wavelength. So the free carriers are extracted from the junction due to applied reverse bias, and corresponding refractive index is enhanced by an amount of Δn_e and Δn_h. The change in refractive index results in a shift of central Bragg wavelength λ_B. Now if the temperature of the junction is increased, then the amount of free carriers will also increase.

In the next subsection, we will investigate the effect of temperature on the modulation performance of the device.

2.3 Effect of Temperature on the Device Performance

The modulation performance of the proposed modulator can be improved only by increasing the carrier density variation ΔN which can be assessed easily by increasing the device temperature through Peltier cell. If temperature is increased by ΔT, corresponding corrugation period $\wedge_T$ of the Bragg grating and effective refractive index (n_{eff}) both can be varied as

$$\wedge_T = \wedge_0 (1 + \alpha \Delta T) \tag{5}$$

where α (=2.5 × 10^{-6}/K [18] is the temperate coefficient of linear expansion for silicon at room temperature.

And

$$n_{\text{eff}} = n'_{\text{eff}} (1 + \Delta n . \Delta T) \tag{6}$$

where Δn (= 4.0 × 10^{-5}/K is the temperature-dependent refractive index variation in silicon.

In case of reverse bias p–n junction, the reverse saturation current density increases by a factor of four (approximately) for every 10 °C or 10 K increase in temperature [16]. Accordingly, the change in carrier density ΔN also varies with temperature which in turn affects the refractive index variation Δn_e and Δn_h largly results in longer shift in central Bragg wavelength λ_B. In this way, higher local temperature

variation (ΔT) near the junction makes longer shifts of the central wavelength by the same RF input. This can be possible by using specifically designed heaters.

3 Simulation Results

The simulation results obtained from Sect. 2 are presented in this section. The parameter values used for the simulation of the device are listed in Table 1.

3.1 Device Output Characteristics Without RF

The passband normalized transmission spectrum obtained from (1) is plotted with wavelength in Fig. 2 for a single quarter-wave phase-shifted Bragg grating shown in Fig. 1. A single-phase shift section is inserted in between two Bragg reflectors for three different grating lengths. The length of the grating can be varied by changing the number of corrugations ($N = 200$, 300, and 700) while keeping the grating period fixed at 320 nm.

Increasing the grating length L_M in terms of the number of corrugations N causes the transmission passband in between stopband to be sharper as shown in Fig. 2, but this makes the top of the passband falls to −10 dB. To make the transmission power maximum at 0 dB, an optimized Bragg grating section length is chosen and corresponding value of corrugation number N is calculated as 300. A sharp bandpass window of width ~1 nm at the half power can be observed within a ~6 nm-wide stop-band region. Similar result was found with similar device parameter in experiment [19].

In this way, a sufficient modulated signal power can be obtained which is a desired characteristic for modulation.

Table 1 Parameter values used for the simulation

Parameters	Values
$\wedge_0$	320 nm
N	100
ε_o	8.85×10^{-12} F/m
ε_r	11.68
$N_A = N_D$	1×10^{25} m^{-3}
α_p	2.5×10^{-6}

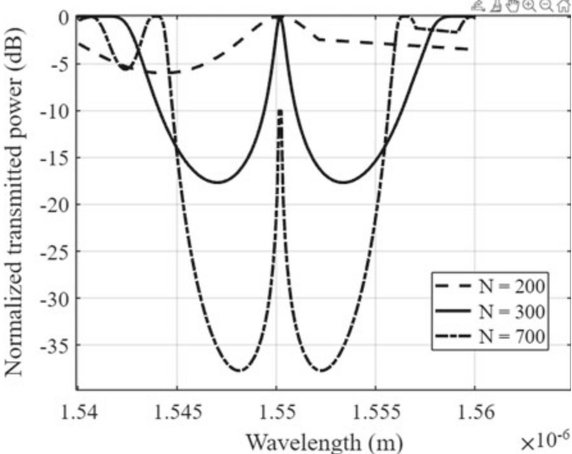

Fig. 2 Normalized transmission power versus wavelength over a 20 nm span around the Bragg wavelength. The curve is plotted for three different Bragg grating lengths

3.2 Modulation Performances with RF

The DC modulation performance of the device is characterized by changing the reverse bias voltage across the p–n junction of the modulator. Spectral responses of the through port can be obtained from Eq. (1) which is shown in Fig. 3. The through port passband peak shifts about 0.4 nm as reverse bias voltage changes from 0 V to −3 V.

The spectrum shifts by 0.4 nm shown in Fig. 3 produce a negligible static modulation extinction ratio (ER) at a wavelength of 1550 nm. This result signifies that the modulator can be operated at a very high change in drive voltages which in turn affect the grating profile of the device itself.

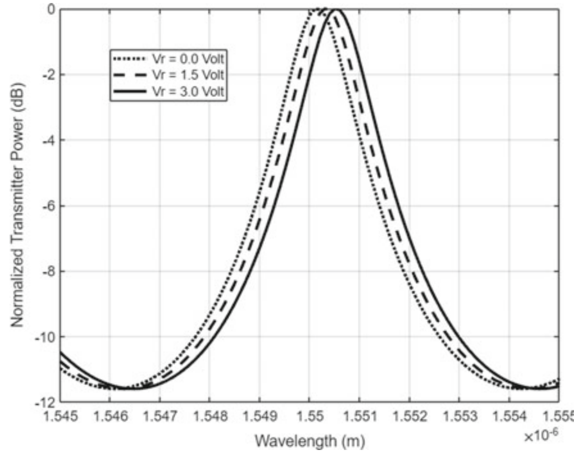

Fig. 3 Spectral response of the normalized transmission power versus wavelength over a 10 nm span around the Bragg wavelength. The result is plotted for three different reverse bias voltages

3.3 Improved Modulation Performances with Increase in Temperature

The tunability of the bandpass window of the modulator has been enhanced by increasing the local temperature near the junction. Similar results are produced with varying the similar reverse bias voltages from 0.0 V to 3.0 V at higher temperatures. The observed spectral response for two different chip temperatures is plotted in Fig. 4a and b, respectively, with corresponding typical thermal dependence of ~0.09 nm/K. The corresponding static modulation extinction ratio (ER) of 3 dB can be obtained at a wavelength of 1550.9 nm with 10 K increase in temperature of the junction. Larger local temperature variations (corresponding to larger shifts of the central wavelength) could be imposed by using specifically designed heaters. This can be assessed by varying the chip temperature through a Peltier cell.

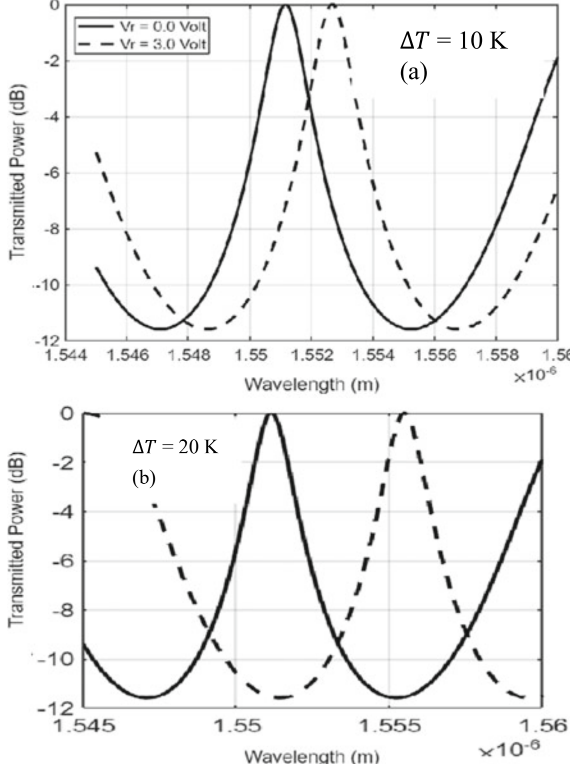

Fig. 4 Enhanced tunability of the Bragg grating modulator with increase in 10 K **a** and 20 K **b** temperature variations

4 Conclusions

In this work, the modulation performance of a single phase-shifted Bragg grating modulator is investigated. It is found that the tunability of the modulator can be enhanced by increasing the temperature variation of the junction. 1 nm wavelength can be shifted by applying −3.0 V reverse bias voltage at the modulator. So, high-speed modulation up to 100 GHz can be achieved. With further parameter optimization, the modulation speed as well as the extinction ratio can be made larger.

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