Lecture Notes in Electrical Engineering 1062

Shubhakar Kalya
Muralidhar Kulkarni
Subramanya Bhat *Editors*

Advances in VLSI, Signal Processing, Power Electronics, IoT, Communication and Embedded Systems

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Preface

This book contains research papers in the areas "VLSI, Signal Processing, Power Electronics, IoT, Communication and Embedded Systems". The research papers accepted and presented in a Two Day International Conference on "VLSI, Signal Processing, Power Electronics, IoT, Communication and Embedded Systems (VSPICE-2022)" as a part of Multi-Conference on International Conference on Emerging Trends in Engineering (ICETE- 2022) on 22nd and 23rd December 2022 were included in the book. The conference was organized by the Department of Electronics and Communication Engineering, N.M.A.M. Institute of Technology, Nitte, India. The book is dedicated to driving innovation in nearly every aspect of Electronics & Communication Engineering. The book provides a platform for researchers, professionals, executives and practicing engineers from various industries, research institutes and educational bodies to acquire knowledge. A series of technical research papers in this book, discussed new issues, tackled complex problems and found advanced enabling solutions which can shape new trends and enable the development of mankind as a whole.

A total of 43 researchers from India and abroad have contributed their research papers. Authors also incorporated suggestions provided from Reviewers from India and Abroad, Session Chairs, Conference Convenor, Organizing secretaries and Delegates.

Advances in VLSI, Signal Processing, Power Electronics, IoT, Communication and Embedded Systems pave a pathway for the development of efficient and economic systems. For making the best use of resources, expertise in multiple specializations and interdisciplinary research is gaining prominence. The research papers presented in the book will contribute as best resources for the same.

Singapore, Singapore — Shubhakar Kalya
Mangalore, India — Muralidhar Kulkarni
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About the Editors

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Prototype for Parking Shield System Using Raspberry Pi

Rai B. Rajeshwari and K. Mahaveera

Abstract The automotive industry is seen to be making a transformation from manual to semi-autonomous to fully autonomous vehicles. Advanced Driver Assistance System (ADAS) forms a major building block for the next generation of highly Autonomous Vehicles. ADAS is among the fastest-growing segments in automotive electronics and includes large number of applications like Antilock braking system, automatic speed control, Parking assistance system, lane keeping assist etc. Parking assistant system supports several functionalities like Parking line detection, object detection, pedestrian classification, parking support functions etc. These functions are mainly implemented using Surround View Camera System (SVCS) which provides real-time view of the area surrounding the car. Parking Shield System (PSS) is one such parking support function which works with the help of SVCS. PSS is used as an aid to identify the damage caused to the parked vehicle. This work proposes a prototype development for PSS using Raspberry Pi. Acceleration sensor is used to detect the movement of the vehicle and once the vehicle movement is detected, LEDs glow (indicating opening of flaps and mirrors). Immediately, USB Camera connected to Raspberry Pi captures the image and is displayed in VNC Viewer window.

Keywords Advanced driver assistance systems (ADAS) · Parking shield system (PSS) · Surround view camera system (SVCS)

1 Introduction

Driver assistance systems are electronic aids designed to offer help to drivers in certain situations. These systems are mainly intended to increase comfort and safety of the drivers in real driving situations. The evolution of automotive technology has led the Advanced Driver Assistance Systems (ADAS) to become a mainstream.

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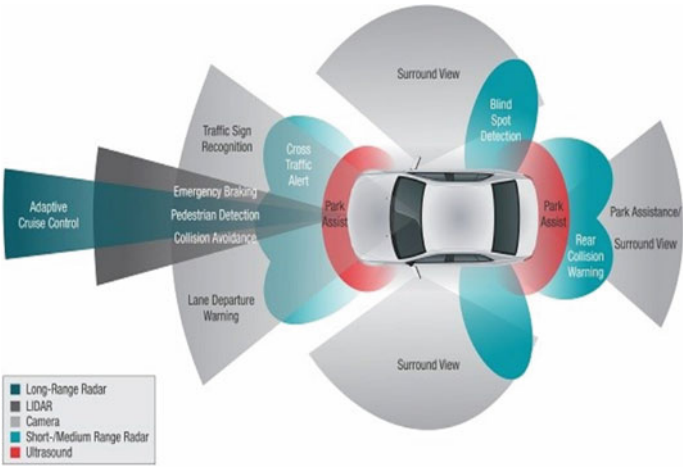

Fig. 1 Advanced driver assistant systems [6]

ADAS use automated technology, such as sensors and cameras to detect obstacles or driver errors and respond accordingly, thus reducing the risk of accidents. ADAS is among the fastest-growing segments in automotive electronics and includes large number of applications as shown in Fig. 1. Vehicles usually offer limited view of surroundings. In such cases, Parking systems such as Surround View Camera System (SVCS) come to rescue by offering better view of surroundings to the driver and thus enhancing his vision and giving him more control on the surroundings. A SVCS consists of four cameras as shown in Fig. 2 connected to Electronic Control Unit. It provides real-time view of the area surrounding the car. Four cameras consisting of wide-angle lenses are integrated in the body of the vehicle. Usually, these cameras are placed on the front grille, under the rearview mirrors on either side of the car and on the tail. The 360-degree camera technology combines the perspectives of all the four cameras placed around the vehicle into one image as a top-down view. This view is directly projected onto the dashboard hardware called infotainment system or Head Unit of the vehicle. It also shows the nearby obstacles, helping us to avoid impacts. The front and rear view camera present in SVCS is covered by camera protection Flap. These Flaps are to be opened at the time of capture. The other two cameras are placed below the rearview mirror on either side. Hence the rearview mirror on either side has to be unfolded at the time of capture.

2 Problem Definition

If a car parked in a parking lot (mall or roadside) gets damaged in the absence of the owner, it is important to know the cause for the same. If the driver who hit/damaged the parked car is not at the scene and did not leave any contact information or if the

Fig. 2 SVCS installed in car [7]

real cause of the damage is unidentified, it will be very difficult for the owner to identify the cause. In such scenario, by making use of 360^0 camera systems, images of the scenes can be captured and sent to Head unit. By making use of the images captured, owner can find out the real cause of the damage.

3 Objectives

The objective of this project is to develop a prototype for the design and validation of the Parking Shield System, such that the performance of the system can be guaranteed. The objective can be further decomposed as follows:

- Detect the vehicle movement (indicating damage) using Accelerometer sensor
- If movement is detected, following objectives are to be met
- Rearview mirrors on either side should open up
- Front and rear camera flaps should open up
- All 4 cameras should capture images
- Captured images are to be saved for future reference

4 Literature Review

A review on ADAS systems and its technologies including Adaptive speed control system, automatic brake system, collision warning system, and Lane keeping system is presented in [1]. Traffic sign detection and recognition used in ADAS systems based on Machine learning is proposed in [2], cascade Feedforward Neural Network with Random Weight (FNNRW) classifier is used for the classification of images. Rear obstacle detection is carried out in [3] using a single rearview camera. To offer

better view of the surroundings, [4] proposes a surround view solution for Embedded systems which will be useful to know the cause of damage caused to a parked vehicle, in the absence of the owner.

5 Methodology

PSS using Raspberry Pi involves vehicle movement detection indicating damage caused to the parked vehicle. Acceleration sensor continuously senses the vehicle acceleration and sends the signal to Raspberry Pi. If any movement is detected by the sensor, all four LEDs connected to Raspberry Pi glow which indicates that the front and rear flaps are open, and right and left mirrors are unfolded. Figure 3 shows the Block diagram for PSS which includes Power supply, Accelerometer and USB camera as inputs to the Raspberry Pi and LED is used as the output device for the system which indicates the status of camera flaps and mirrors. Image captured using USB camera system are displayed in the VNC Viewer window.

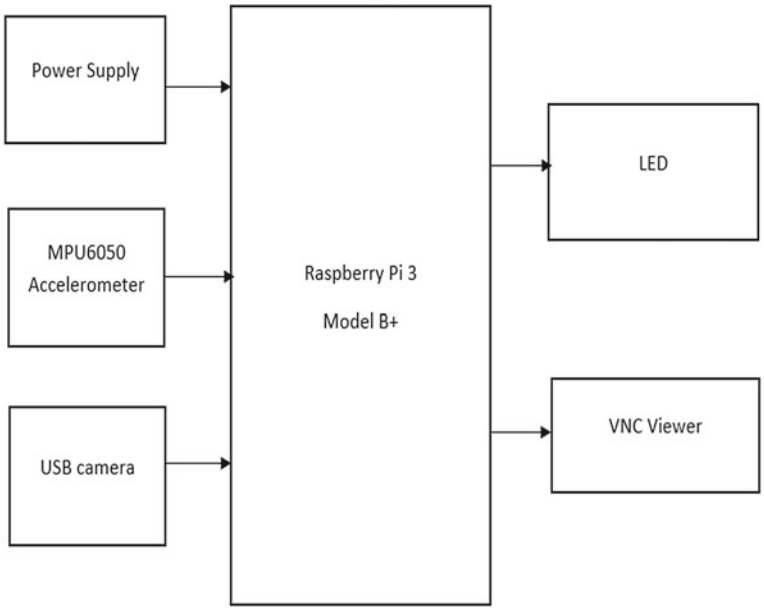

Fig. 3 Block diagram for PSS

A. Hardware Components

(1) Raspberry Pi 3 Model B +

Raspberry Pi 3 Model B + as shown in Fig. 4 is a single-board computer. It features a 64-bit quad-core 1.4 GHz ARM Cortex-A53 Broadcom processor. Provides dual-band 2.4 GHz and 5 GHz wireless LAN and Bluetooth 4.2/BLE. It offers faster Ethernet (Gigabit Ethernet over USB 2.0) and Power-over-Ethernet (PoE) capability via separate PoE HAT. It also provides Preboot Execution Environment (PXE) network, USB mass-storage booting and improved thermal management.

(2) MPU6050 Accelerometer Sensor

MPU6050 as shown in Fig. 5 consists of 3 axis (x,y and z) accelerometer used to measure acceleration along the 3 axis and with full scale ranges $\pm$ 2 g, $\pm$ 4 g, $\pm$ 8 g and $\pm$ 16 g. The module uses the I2C protocol for communication with the Raspberry Pi. It supports two separate I2C addresses: $0 \times 68_{HEX}$ and $0 \times 69_{HEX}$. The AD0 pin present in MPU6050 determines the I2C address. It has a built-in 4.7 K pull-down resistor. Therefore, when the ADO pin is unconnected, the default I2C address is $0 \times 68_{HEX}$ and when it is connected to 3.3 V(pulled HIGH) I2C address becomes $0 \times 69_{HEX}$.

Accelerometer is made up of micro-machined structure laid on silicon wafer. Polysilicon springs are suspended from this structure. When the acceleration is applied on any of the three axes, the structure deflects. Deflection results in the capacitance change between plates attached to the suspended structure and fixed plates. This capacitance change corresponds to the acceleration on that axis. This change in capacitance value is processed by sensor and converts it into an analog output voltage.

(3) Light Emitting Diode (LED)

A Light-Emitting Diode (LED) is a semiconductor light source which emits light when current flows through it. LEDs are used to depict the flaps and mirrors. Four

Fig. 4 Raspberry Pi 3 Model B + [8]

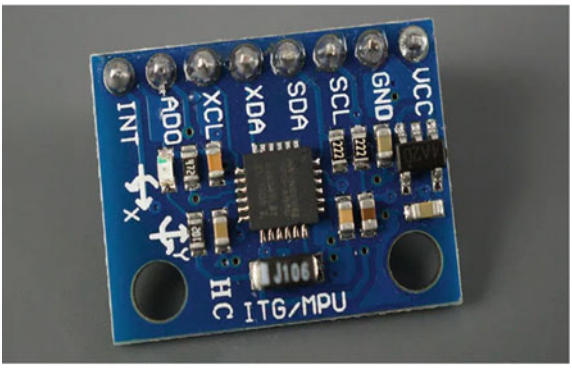

Fig. 5 MPU6050 Accelerometer sensor [9]

LEDs are used which act as Front flap, Rear flap, Right mirror and Left mirror. LED display unit indicates that flaps and mirrors are open.

(4) USB Camera

Figure 6 shows the Cable collapsive 8 Mega Pixel USB Camera. Features of this camera include 640X480 resolution, YGA/YUV2 packed formats, Retractable USB cable, USB 2.0 High speed sensor, High definition and true color images.

B. Software Component

(1) PuTTy

It is the software application used to access Raspberry Pi. It acts as the interface between the user and Raspberry Pi. This application is run on a desktop or laptop to access command line interface. Using SSH, it opens a terminal window on laptop/ desktop and sends commands to Raspberry Pi and receives data from it. Using IP address of Raspberry Pi, PuTTY can be used from a remote computer to have access on Raspberry Pi via a terminal. Putty configuration session is shown in Fig. 8.

Fig. 6. 8MP USB camera

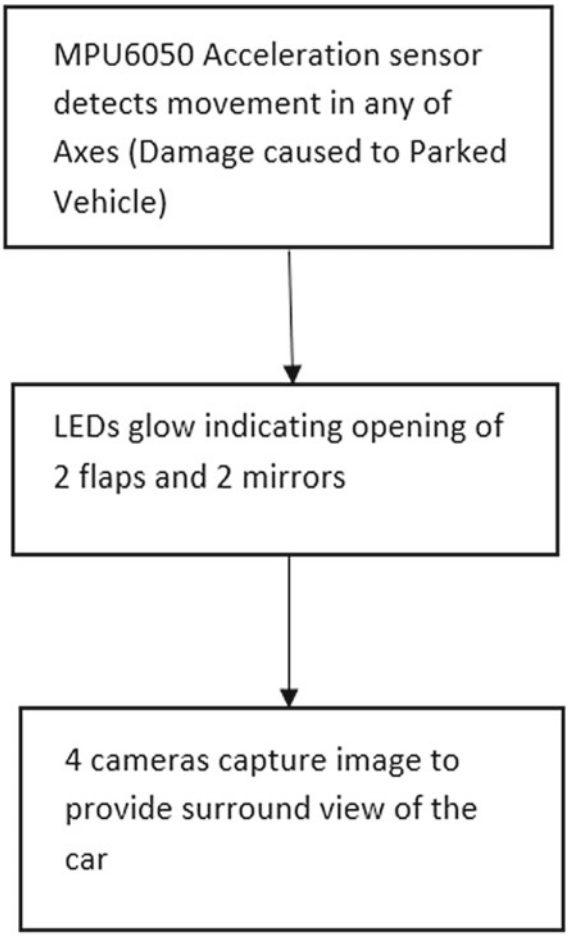

Fig. 7 Working of PSS using Flow chart

(2) VNC Viewer

Virtual Network Computing (VNC) Viewer is the graphical desktop sharing system which helps the users to remotely and instantly access any computer (Windows, Linux or Mac machine). This is used to control and view the remote computer desktop. This application uses Remote frame buffer protocol to control the computers remotely.

(3) Raspberry Pi Imager

Raspberry Pi imager application as shown in Fig. 9 is used to install Operating system on SD card. This application automatically installs the OS on to the SD card.

Steps followed during installation are:

- Connect SD card reader with SD card inserted in it, to a Laptop/PC.
- Open Raspberry Pi imager application and choose the OS required from the list

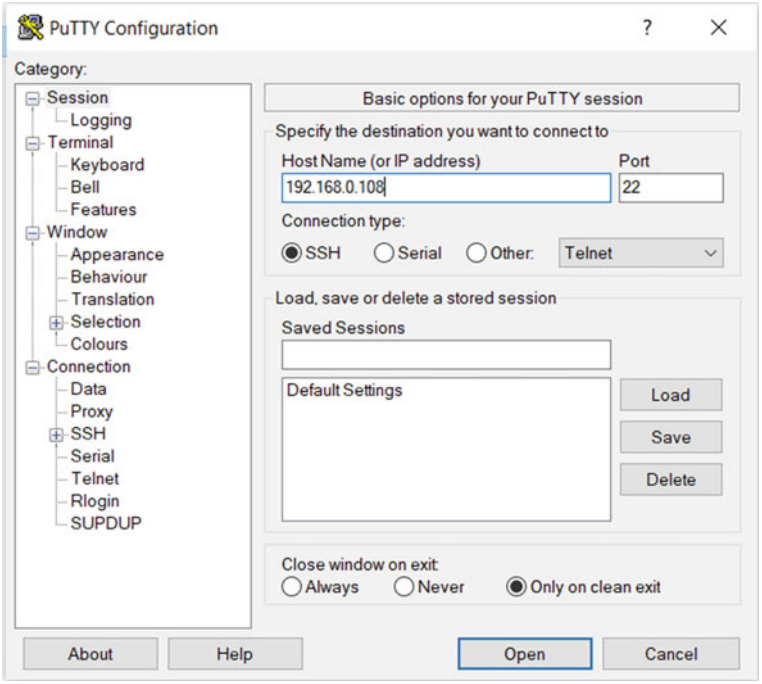

Fig. 8 PuTTy configuration session

Fig. 9 Raspberry Pi imager

```
$ cd /opt

/opt$ git clone https://github.com/Itseez/opencv.git

/opt$ git clone https://github.com/Itseez/opencv_contrib.git
/opt$ cd opencv

/opt/opencv$ mkdir release

/opt/opencv$ cd release

/opt/opencv/release$ cmake -D BUILD_TIFF=ON -D WITH_CUDA=OFF -D ENABLE_AVX=OFF -D
WITH_OPENGL=OFF -D WITH_OPENCL=OFF -D WITH_IPP=OFF -D WITH_TBB=ON -D BUILD_TBB=ON
-D WITH_EIGEN=OFF -D WITH_V4L=OFF -D WITH_VTK=OFF -D BUILD_TESTS=OFF -D
BUILD_PERF_TESTS=OFF -D CMAKE_BUILD_TYPE=RELEASE -D
CMAKE_INSTALL_PREFIX=/usr/local -D
OPENCV_EXTRA_MODULES_PATH=/opt/opencv_contrib/modules /opt/opencv/

/opt/opencv/release$ make -j4

/opt/opencv/release$ make install

/opt/opencv/release$ ldconfig

/opt/opencv/release$ exit

/opt/opencv/release$ cd ~
```

Fig. 10 Commands used to build and install OpenCV [5]

- Choose the SD card from the given list
- Click on Write button to write the OS on to SD card.

4. OpenCV

Open Source Computer Vision library (OpenCV) is the Open source library which includes computer vision and machine learning software. This programming function library mainly aims at real-time computer vision. Its applications include Facial recognition, object detection, camera capture, Motion understanding, Motion tracking, Segmentation etc. The commands used to build and install OpenCV are shown in Fig. 10.

6 Tests and Results

C. Test Setup

Acceleration sensor values read by MPU6050 are sent to Raspberry Pi using I2C communication. Test setup for PSS prototype is shown in Fig. 11. By manually moving the acceleration sensor, the damage detection for the vehicle is tested. If there is any acceleration change occurred at any axis (i.e. movement of the sensor

from its standstill position) immediately the flaps and the mirrors are to be opened up for further processing. In this case change in the acceleration results in glowing of LED, indicating the opening of flaps and mirrors.

D. Observation

Acceleration values at all 3 axes of accelerometer is displayed on Putty as shown in Fig. 12. Considering the sensor placed on the plane surface, Fig. 12 corresponds to the acceleration values when the sensor is at standstill position (i.e. no damage caused). Sensor placed on any surface will have its axes values corresponding to X:0, Y:0, Z:1. These axes values are in terms of acceleration gravity(g). In Fig. 12 X axis values slightly varies from 0, since it depends on the surface on which it is placed and sensitivity of the sensor. These variations are reduced to an extent possible by calibrating the sensor. Z values at the standstill of sensor almost equals 1 g, this is because of acceleration due to gravity acting on it (1 g = 9.8 m/s^2).

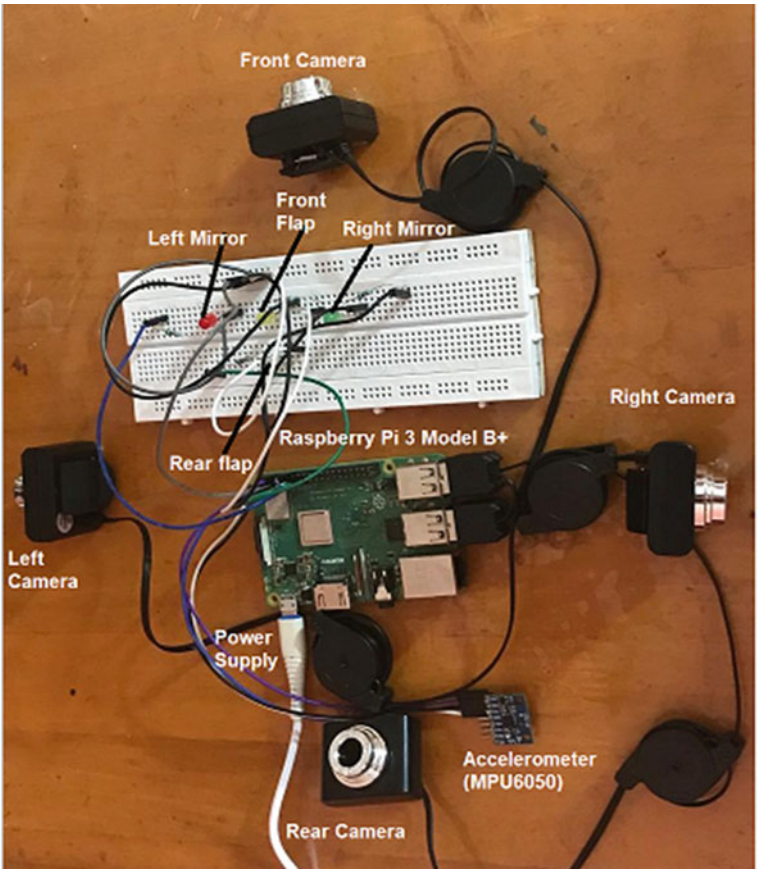

Fig. 11 Test setup for PSS prototype using Raspberry Pi

```
pi@raspberrypi: ~/pdd/fold
pi@raspberrypi:~/pdd/fold $ ./Example
Accelerometer Readings: X: 0.124, Y: 0, Z: 1.01
Accelerometer Readings: X: 0.116, Y: 0, Z: 1.004
Accelerometer Readings: X: 0.121, Y: 0, Z: 1.01
Accelerometer Readings: X: 0.112, Y: 0, Z: 1.008
Accelerometer Readings: X: 0.117, Y: 0, Z: 1.002
Accelerometer Readings: X: 0.122, Y: 0, Z: 1.004
Accelerometer Readings: X: 0.112, Y: 0, Z: 1.012
Accelerometer Readings: X: 0.137, Y: 0, Z: 1.007
Accelerometer Readings: X: 0.122, Y: 0, Z: 1.004
Accelerometer Readings: X: 0.129, Y: 0, Z: 1.013
Accelerometer Readings: X: 0.126, Y: 0, Z: 1.007
Accelerometer Readings: X: 0.135, Y: 0, Z: 1.003
Accelerometer Readings: X: 0.135, Y: 0, Z: 1.009
Accelerometer Readings: X: 0.134, Y: 0, Z: 1.007
Accelerometer Readings: X: 0.143, Y: 0, Z: 1.003
Accelerometer Readings: X: 0.137, Y: 0, Z: 1.01
Accelerometer Readings: X: 0.148, Y: 0, Z: 1.005
Accelerometer Readings: X: 0.142, Y: 0, Z: 1.01
Accelerometer Readings: X: 0.106, Y: 0, Z: 1.008
```

Fig. 12 Acceleration values as displayed on Putty

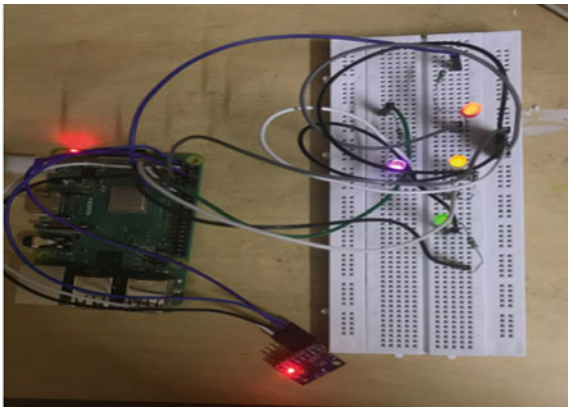

Fig. 13 LEDs glown when sensor moved manually

Once the acceleration values at all 3 axes exceed the acceleration value corresponding to standstill mode of the sensor as shown in Fig. 12, all LEDs are made to glow as in Fig. 13 indicating that the damage is caused to the vehicle, and the flaps and mirrors are opened. Once all the LEDs are glown, USB camera connected to Raspberry Pi captures the image. The image captured by all four USB cameras is displayed on VNC Viewer window as shown in Fig. 14.

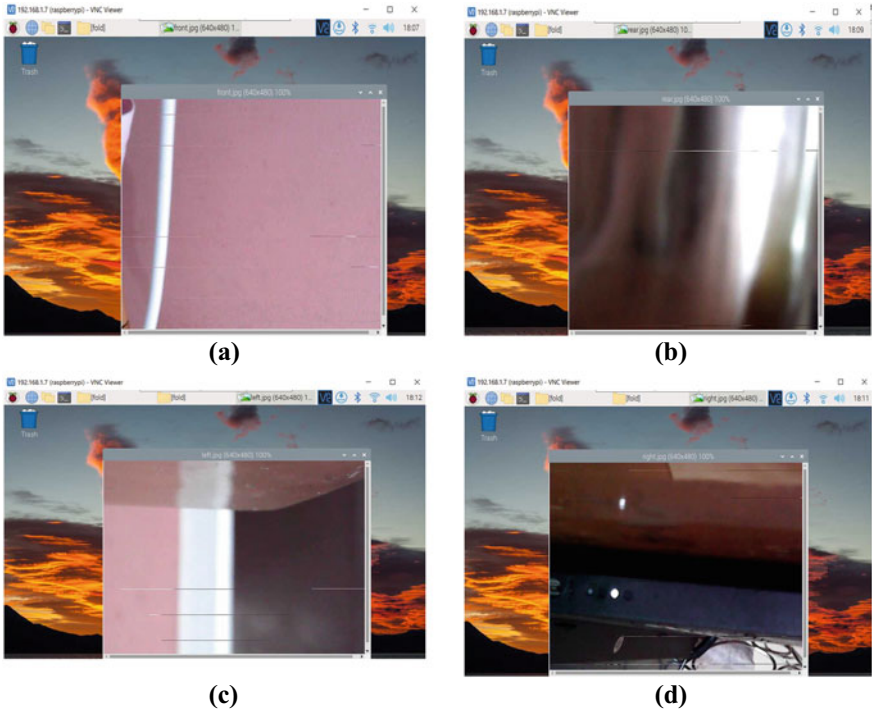

Fig. 14 Images captured by USB camera as seen from Raspberry Pi **a** Front camera capture, **b** Rear camera capture, **c** Right camera capture, **d** Left camera capture

7 Conclusion

PSS is one of the Parking Assist functions which is used to detect any kind of damage caused to the parked vehicle. Prototype for PSS is implemented using Raspberry Pi. Using MPU6050 accelerometer sensor, movement is detected and the LEDs are made to glow indicating the opening of flaps and mirrors. Immediately after mirrors and flaps open up, USB camera captures the image and is displayed in VNC Viewer window. Future scope of this work includes stitching and projecting images as a top-down view, Identifying Camera defects and alerting the driver instantaneously using user application.

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Design and Implementation of Smart Waste Management System

S. Krishnapriya, Binu Manohar, M. N. Ameena, Ankitha Arun, M. S. Rabiya Nasnin, and Yedudev K. Nair

Abstract In our technologically advanced period, where urbanization is fast rising, waste accumulation is also increasing steadily. Making cities smart has become the need of the hour in order to tackle this problem. Though literature shows several methods for the implementation of smart cities, the problem still remains. One general issue while designing a system for waste management is the segregation of different types of waste. Manual segregation is still being followed in most of the cities. This paper proposes a smart waste management system that can differentiate and store biodegradable and non-biodegradable waste separately using a set of sensors such as ultrasonic, IR, moisture and inductive sensors. The proposed system also does segregation of the non-biodegradable waste as plastic, wood, and metal.

Keywords Segregation · Ultrasonic sensor · IR sensor · Moisture sensor

1 Introduction

Waste management is a crucial feature of municipal administration, particularly in urban regions. Without a smart waste management system, a smart city would be incomplete. A city consists of a mix of small and large-scale houses and communities, as well as markets, offices, and institutions. The most common source of garbage is household waste. Organic and inorganic waste products are produced by commercial and home activities. A trash can is the only way to collect residential waste while waiting for municipal services [1–3]. Due to the daily growth in waste, dustbins in public places or in front of homes/societies in cities are frequently overflowing. When garbage management goes wrong, it has serious implications for society.

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Inadequate waste management is a serious health risk, as it causes infectious diseases to spread and pollutes the environment. Hazardous gases such as methane are created if specific biodegradable waste combinations stay neglected for several days and thus leading to immediate intervention. The primary challenge of maintaining a healthy environment in a city with a constantly growing population requires daily separation and management of biodegradable and non-biodegradable waste [4–6]. There must be a mechanism in place for the timely detection of trash can filling and to notify the concerned authority, allowing the bin to be cleared in time and the environment to be safeguarded. A city can also be smart if the community is clever when it comes to trash management.

Sensing technology has various advantages, including predictive and preventative maintenance. They not only speed up the transfer of measured data but also improve accuracy, allowing for better process management and asset health. As a result, various sensors can be used based on their uses to properly segregate trash as biodegradable and non-biodegradable.

2 Literature Survey

Rapid urbanization, industrialization, and increase in population have resulted in a waste management catastrophe over the last two decades in India [5]. According to the World Bank, municipalities spend 20 to 50 percent of their total budget on trash management. The Integrated Solid Waste Management (ISWM) plan in some of the Indian metro cities includes baseline data, proposed targets, concern issues, management system responses, implementation strategy, monitoring, and system feeding [7, 8]. When the trashcan is completely filled, the system sends an SMS to the supervisor, allowing the system to summon a waste collection truck. The supervisor receives another SMS notification of the trash collection [9].

Machine learning is a strong and useful tool for making judgments, utilizing certain patterns, and evaluating large amounts of data from sensors in IoT devices, and smart waste management technologies. Machine learning is considered as a feasible tool for taking data-driven actions. Agarwal et al. gave extensive knowledge of India's waste management strategies for human health [3, 8]. The author revealed the potential for waste management to be improved for the benefit of society. Waste management is crucial for smart city development, but it is more than just collection and disposal.

For waste management to be complete, garbage should be segregated into biodegradable and non-biodegradable types, and biodegradable waste can be used to create compost. Harmful gases released by household items are causing environmental issues. This inspires us to create a system that can sort household waste into two categories such as biodegradable or non-biodegradable, and issue alert messages

based on data collected from sensors using a machine learning technique. Once segregated, biodegradable garbage is utilized to make compost, while non-biodegradable waste is collected by the Municipal Corporation following additional segregation at the society level [8, 9].

3 System Description

The whole system for smart waste management can be modeled as shown in Fig. 1. The various levels of working of the system are explained in the following sections.

A. Automatic Opening and Closing of the Waste Bin

For implementing the automatic opening and closing of dustbin, servo motor, ultrasonic sensor and Arduino AT Mega 2560 are used. Ultrasonic sensor detects the person approaching the dustbin and enables the servo motor to open the dustbin via Arduino. The Arduino Uno is an open-source microcontroller board based on the Microchip ATmega328P microcontroller and developed by Arduino.cc. The Arduino IDE employs the program avrdude to convert the executable code into a text file in hexadecimal encoding that is loaded into the Arduino board by a loader program in the board's firmware.

After detecting a person, the lid remains open for 5 s and closes afterwards. Soon after the dustbin opens, a message will be displayed on the LCD to place the waste on a platform of bin one at a time.

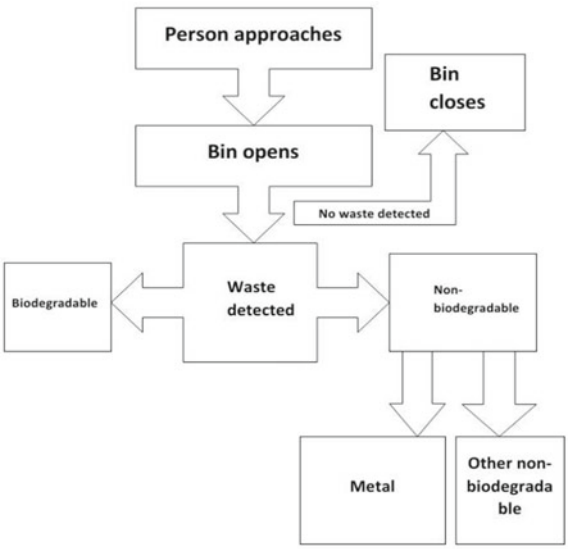

Fig. 1 Waste segregation system model

The implementation setup of the smart bin, automatic opening and closing of the bin when a person is sensed and LCD display showing instructions and status for the smart bin are shown in Figs. 2, 3 and 4.

B. Waste segregation

Once the waste is deposited in the dustbin, initially it falls on a platform where the IR sensor is placed in order to detect the presence of waste. After the detection of waste, primary segregation takes place. The primary segregation makes use of moisture sensors to differentiate the waste as biodegradable and non-biodegradable.

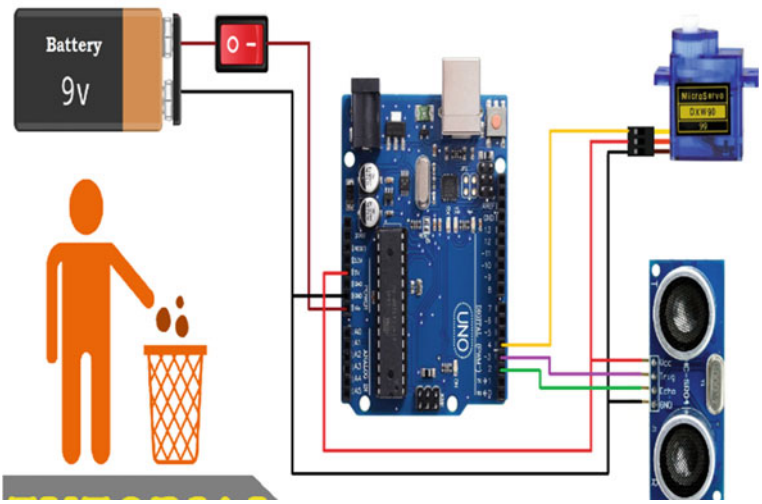

Fig. 2 Set up of smart waste bin

Fig. 3 Automatic opening of the bin

Fig. 4 LCD display showing instructions and status for the smart bin

The segregation of waste as biodegradable and non-biodegradable is based on the value of moisture content in the waste. If the value is less than 500, then the waste is considered as biodegradable and non-bio degradable otherwise.

For further segregation of non–biodegradable waste into plastic and metal, an inductive sensor is used. Inductive sensor is basically used for the detection of metal. Inductive sensor uses the digital value to segregate the same. The digital value '0' represents the detection of metal waste. Paper waste is segregated into a separate compartment with the help of a fan.

C. Level Sensing and Message Alert

Ultrasonic sensor is installed in each compartment to detect the level of waste. Once the level of waste has reached 90% of total capacity, a message will be sent to the respective authority via Blynk app. Blynk is specially designed for the Internet of Things and can control hardware remotely, display sensor data, store data, and visualize it. It is a digital dashboard to build a GUI for projects by simply dragging and dropping widgets. Blynk Library can connect any hardware over Ethernet, WiFi, or GSM, 2G, 3G, LTE, etc. It has got a flexible firmware API.

4 Results and Discussions

Automatic opening of the bin is tested by checking the Ultrasonic sensors within a sensor to object distance of 5 cm to 1 m. Also, level sensing using ultrasonic sensors is verified by allowing the garbage to be filled above 90% of the total bin capacity. The alert messages in the Blynk app and LCD display of the bin are shown in Figs. 5 and 6 respectively.

As the segregation of waste as biodegradable and non-biodegradable is based on the value of moisture content, trials are conducted by putting paper, vegetable cuttings, wood chips and metallic wastes. The results are verified with the help of a serial monitor as shown in Figs. 7 and 8.

As per the nature of the waste detected, it is directed into respective compartments enabling proper segregation of the same. If the waste is detected as non-biodegradable, it is further segregated into plastic, wood, and metal compartments as per the type of the waste.

Fig. 5 Alert shown in Blynk app when the bin is full

Fig. 6 Alert message shown on the bin

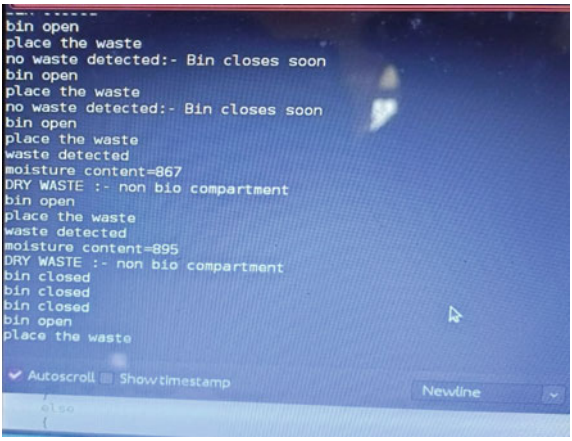

Fig. 7 Output of Arduino in serial monitor during dry waste detection

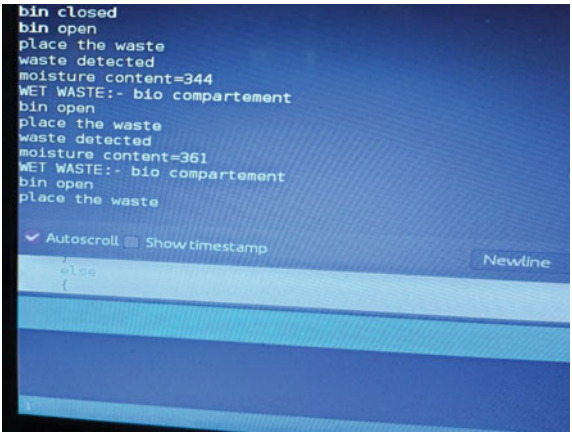

Fig. 8 Output of Arduino in serial monitor during wet waste detection

5 Conclusion

The Smart Bin allows effective and clean disposal of the waste. The automatic door opening system ensures that garbage disposal by humans is completely hands-free, and therefore, extremely hygienic, since there is no contact established with the bin. Waste deposited in the bin is initially sorted into biodegradable and non-biodegradable waste followed by further classification under non-biodegradable waste. Also, the level of waste in the dustbin is determined with the help of ultrasonic sensors and the corresponding alert message is sent to the respective authority via the Blynk app.

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Multiplier Design for the Modulo Set $\{2^n - 1, 2^n, 2^{n+1} - 1\}$ and Its Application in DCT for HEVC

P. Kopperundevi and M. Surya Prakash

Abstract The Residue Number System (RNS) is a non-weighted number system. Because of its inherent parallelism, it has been extensively studied and used in Digital Signal Processing (DSP) systems. A key arithmetic operation in residue-based real-time computing system is modulo multiplication. For small moduli, ROM-based structures are better at realizing multipliers. Implementations with arithmetic components are more for medium and large moduli due to the exponential growth of ROM sizes. The new modular multiplier introduced in this paper is capable of easily handling medium and large moduli. The multiplier unit is proposed in this paper using shift and add, followed by the modulo operation. The implementation results show that our proposed design outperforms existing architectures in terms of area and power consumption when using the TSMC-180 nm CMOS Technology. When compared to existing works, our proposed multiplier saves 86% to 93% of area and 65% to 83% of power. The proposed multiplier improves the existing DCT architecture by 18% in terms of area.

Index Terms Residue number system · Multiplier unit · Hardware architecture · ASIC

1 Introduction

The Residue Number System (RNS) is a non-weighted parallel numerical representation system, which divides the integers into multiple independent ones through modular operations. Thus, the bit-width of each channel is greatly reduced. As a result, RNS-based systems can achieve high calculation speed and low complexity. In simple words, RNS or residue of moduli set $\{m_1, m_2, \ldots m_n\}$, simply depicts a,

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represents a large integer number as a smaller set of integers. The r is said to as the residue of a with respect to m if Q and R are the quotient and remainder of an integer division of a by m. Accordingly, r = a mod m which is represented by r = |a| Accordingly, r = a mod m which is represented by r = |a|| Accordingly, r = a mod m which is represented by r = |a| Accordingly, r = a mod m which is represented by r = |a|| Accordingly, r = a mod m which is represented by $r = |a|_m$. Let A be the least common multiple, or if all the moduli are relatively prime, just the product of all of them m_i. Any integer X smaller than A can be uniquely represented by a residue set $\{x_1,x_2,x_3....x_n\}$ of the modulo $\{m_1,m_2,...m_n\}$, where $x_i = |X|_{mi.}$ A is the dynamic range of the system. The Chinese remainder theorem (CRT) describes the relationship between the integer X and its RNS representation $\{x_1,x_2,x_3....x_n\}$ as follows:

$$X = |\sum_{i=1}^{N} w_i x_i|_A \tag{1}$$

where $w_i = A_i|A_i^{-1}|_{m_i}$, $A_i = |A|_{m_i}$, and $|A_i^{-1}|_{m_i}$ is the inverse of A_i's multiplicative component with regard to m_i. This reduced residue set can be used to perform operations like addition, subtraction, and multiplication because the propagation of carriers between these residues is not necessary for RNS i.e., $X \odot Y = Z \Leftrightarrow x_i \odot y_i = z_i \mod m_i$.

The symbol $\odot$ represents the basic operation of RNS such as addition, multiplication and subtraction. The fundamental operation of RNS multiplication is described as follows. If A, B and C have RNS representations given by, $A = a_1,a_2,...a_n$, $B = b_1,b_2,...b_n$, $C = c_1,c_2,...c_n$, then denoting * to represent the RNS multiplication operation then, the RNS version of C = A*B satisfies (2) and (3).

$$C = \left\{\langle a_1 * b_1\rangle_{m_1}, \langle a_2 * b_2\rangle_{m_2}, ..., \langle a_n * b_n\rangle_{m_n}\right\} \tag{2}$$

Take an simple a {3,5,7} RNS module as an example. If.
A = 23 = {2,3,2} and B = 40 = {1,0,5} then,

$$\begin{aligned} C_{prod} &= \langle A * B\rangle mod\ m \\ &= \{\langle 2 * 1\rangle_3, \langle 3 * 0\rangle_5, ..., \langle 2 * 5\rangle_7\} \\ &= \{2, 0, 3 = \langle 23 * 49\rangle_{105} = \langle 920\rangle_{105} = 80\} \end{aligned} \tag{3}$$

Due to its high-speed parallel operation and the simultaneous multiplication that may be performed on N residues within N parallel channels, the RNS is appealing. It is essential to perform the modular multiplication in each and every RNS application. Consequently, developing an effective modular multiplier is a big challenge. In the literature, there are numerous multipliers based on RNS [1–4]. Sign detector for the extended four-moduli and one diminished modulo was introduced in [5, 6] respectively. Chen [7] proposed an efficient modulo $2^n + 1$ multiplier. Zimmermann [8]

proposed a joint implementation of the modulo 2^n-1 multiplier. Hiasat [3] presented a generic multiplier for any modulo. For small moduli, ROM-based multipliers are used in [9–12]. Memory size in ROM-based multipliers typically increases as n's value increases. A modulus of n = 16 bits, for example, would require two read only memory of size ((217)*16) and one inverse index read only memory of size ((216)*17), in addition to some additional logic, based on the multiplier in [11]. As a result, ROM structure-based implementation seems impractical for large moduli. By utilizing a special technique based on isomorphic transformation, it is possible to translate the modular multiplication in RNS into a more simple modular addition [13]. The only acceptable numbers for ROM-based isomorphic multiplier units are prime values. In this work we present a novel simple modulo multiplier specifically for the modulo set 2^n-1,2^n, and 2^{n+1}–1. The proposed algorithm suits all numbers regardless of whether the number is prime or not.

2 Proposed Multiplier Unit and Its Implementation in FPGA

In this section, modulo multipliers for modulo set belonging to the type $\{2^n\text{-}1,2^n,2^{n+1}-1\}$ are discussed. Variable n represents the input number of bits for example if n is eight bit, then $m_1 = 255$, $m_2 = 256$, $m_3 = 511$ for the modulo set $\{2^n\text{-}1, 2^n, 2^{n+1}-1\}$. The general block diagram for the multiplier unit is shown in Fig. 1. The proposed design multiplier unit consists of shift and add unit followed by the modulo operation unit. Here X is the multiplicand, Y is the multiplier and a represents the product of X and Y. Finally after the modulo operation r represents the modulo of the product with respect to m. Most of the existing architectures designed the multiplier using direct multipliers [10]. Here, we implemented multiplier using shift and add operations to reduce hardware cost. The proposed modulo multiplier consists of carry save adder, subtractor and a multiplexer for modulo 2^n-1, 2^{n+1}–1. For the set 2^n, the modulo operation is carried out by calculating bit wise AND operation of the product with n value. The module which performs modulo operation for 2^n-1, 2^{n+1}–1 is shown in Fig. 2 and the working principle of it is described below.

Step 1: Output product value a is right-shifted by n bit denoted as A.

Step 2: Perform a bit wise AND between a and the value m labeled as B in Fig. 3. m is number of bits for example for mod255 the value of m is 8.

Step 3: With the carryin set to zero (C), add the outcomes of steps 1 and 2.

Step 4: Subtract m from C, which is represented as D.

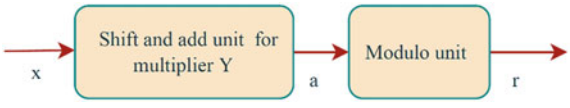

Fig. 1 General block diagram for the multiplier unit

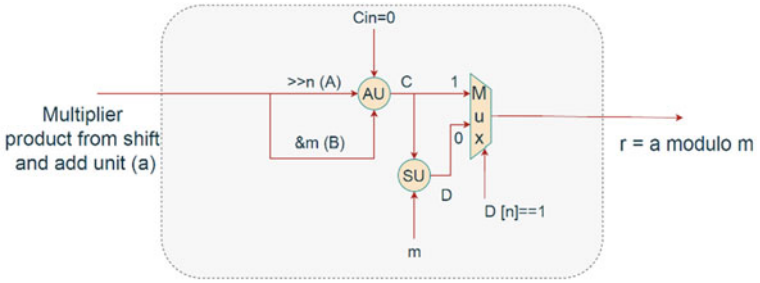

Fig. 2 Block diagram represents modulo operation for $\{2^n\text{-}1, 2^{n+1}\text{–}1\}$

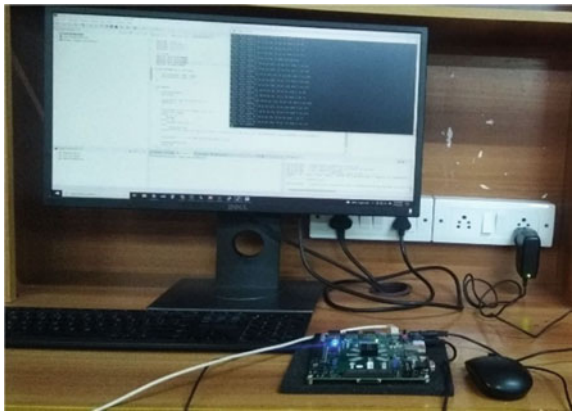

Fig. 3 FPGA implementation setup for the proposed multiplier unit

Step 5: Finally, the Value D serves as a select line to the multiplexer, which selects C or D based on the MSB of D, which is either 1 or 0, to achieve the modulus result of a multiplicand multiplied by a number

Table 1 shows the hardware consumption of proposed multiplier in detail. To reduce hardware consumption, the proposed design uses shift and add instead of direct multiplier as in architectures of [3, 14]. Along with the multiplexer, an N bit subtractor and adder are used, where N refers to the number of bits used to represent the residue of a number. Table II shows a comparison of our design to existing work in terms of area. It depicts the consumption of cell area for modulo multipliers in μm^2. With the TSMC 180 nm library, the design is evaluated in cadence Genus. It shows that for modulo $2^n\text{-}1$, 2^n, our design takes up sixteen and eight times less area than existing architecture respectively. Because the proposed modulo $2^n\text{-}1$ multiplier does not require the generation of partial products as required in [3, 14], our design achieves less area than [3, 14]. Table 2 also depicts the power consumption of proposed design for modulo multipliers in μW. Our architecture consumes 87% and 65% less power than the existing architecture for modulo 2^n and $2^n\text{-}1$ respectively.

The proposed design is evaluated in Field Programmable Gate Array (FPGA- ZED board-xc7z020clg484-1). Our architecture consumes 1.72% of slice LUT, 1% of slice

Table 1 Hardware comparison results

	Multiplier [13]	Multiplier [14]	Proposed
(nxn) Multiplier	1.25	2.5	Shift and add
CSA	2	2	1
CPA	1	0	0
Subtractor	0	0	1
Other combinational logic	Yes	Yes	Yes

Table 2 Comparison of proposed adder in terms of power and area with existing work

Power (μW)			Area (μm^2)	
[1]	Existing (n = 8)	Proposed (n = 8)		
2^n	374.409	45.47	12,464.02	768.398
2^n-1	938.349	326.12	17,866.10	2368.397
2^{n+1}–1	–	600.35	–	4277.750

registers, 1.61% of LUT as logic, and 0.36% of LUT as Memory. Output of the design is verified with the help of Universal Asynchronous Transmitter Receiver (UART) communication. Figure 3 depicts the FPGA experimental setup for the proposed multiplier unit.

3 DCT Architecture for HEVC

Transform coding is an important feature of the High Efficiency Video Coding (HEVC) standard. Detailed overview of DCT architecture is presented in [15]. The fact that HEVC supports DCT in a variety of sizes, including 4, 8, 16, and 32, is one of its key features. In order to compute DCT of any of these lengths, the hardware architecture should be adaptable enough. The 32 × 32 matrix of DCT contains up to 31 unique numbers as follows.

$$\begin{aligned} d_{i,0}i = 1, ...31 = (&90, 90, 89, 88, 87, 85, 83, 82, 80, 78, 75, 73, 70, \\ &67, 64, 61, 57, 54, 50, 4643, 38, 36, 31, 25, 22, 18, 13, 9, 4) \end{aligned} \tag{4}$$

One of the preliminary component of DCT architecture when implementing in RNS is the multiplier unit. The proposed design suits well for implementing DCT architecture as it leads to reduce area consumption while exploiting the maximum redundancy of DCT. As it has the least delay in reverse conversion and is effective in modulo additions and multiplications of moduli sets [5, 16], a three mutually-prime moduli set $m_1, m_2, m_3 = \{2^n\text{-}1, 2^n, 2^{n+1}\text{–}1\}$ is chosen for this application. Having a dynamic range of 3n bits, where n is set to 8 to allow for the hardware's largest range

of values. How the proposed multiplier is modified to implement multiplication unit in DCT architecture for HEVC is explained as follows.

In multiplier unit design, the Multiple Constant Multiplication (MCM) technique is used. One of the multiplier numbers in DCT is 90, as can be seen in (4). An architecture designed for a constant multiplied by ninety is discussed here as an example and shown in Fig. 4. Multiplier units for all other multiplier values are designed using the same procedure as Multiplier unit ninety. For moduli of 255, 256, and 511, the RNS value is 90 for a constant positive number of 90. For modules of 255, 256, and 511, the RNS value of negative number 90 is 165, 166, and 421. We first designed the shift and add unit (SAU) for a set of (90, 165), (90, 166), and using the MCM method (90, 421). Let us refer to SAU 90 and 165 as Block-A, SAU 90 and 166 as Block-B, and SAU 90 and 421 as Block-C. The output of Block-A is the result of multiplying the multiplicand number by 90 or 165 using a multiplexer and inverse is the control unit's select signal indicating whether the multiplicand number is to be multiplied by 90 or 165 (-90). By performing a bitwise AND operation with the output of Block-B and the number 255, the modulo 256 result is obtained.

Step 1: Block-A (Block-C) output is right-shifted by eight bit (nine bit), denoted as A.

Step 2: Perform a bit wise AND between the result of Block-A (Block-C) and the value 255 (511) labeled as B in Fig. 4.

Step 3: Add the results of steps 1 and 2 with the carryin at zero (C).

Step 4: Subtract 255 (511) from C, which is represented as D.

Step 5: Finally, the Value D serves as a select line to the multiplexer, which selects C or D based on the MSB of a multiplicand multiplied by a number 90 with modules 255 (511).

Figure 5 illustrates the verification of proposed multiplier unit in FPGA via UART communication.

The DCT architecture proposed in this work has been implemented using Verilog HDL and evaluated in Cadence Genus with 90 nm library file. Results from Table 3 clearly indicate that DCT architecture designed using proposed multiplier consumes less gate count compared to the design which uses LUT for multiplication purposes. In comparison to the architecture that uses LUT for the multiplication process in RNS design, our proposed method uses nearly 3.2 times fewer gates for a 32 point DCT. The power consumption of the DCT algorithm is also presented in Table III. It demonstrates that the architecture we've suggested uses 69% less energy than the one that makes use of a LUT as a multiplier unit.

4 Conclusion

A new multiplier architecture for the modulo set $\{2^n\text{-}1, 2^n, 2^{n+1}\text{–}1\}$ and its application in DCT are presented in this work. The proposed multipliers offer significant power and area savings over the current multipliers, and they can be used in DCT architecture to consume less space. These RNS multipliers can be used in a variety of

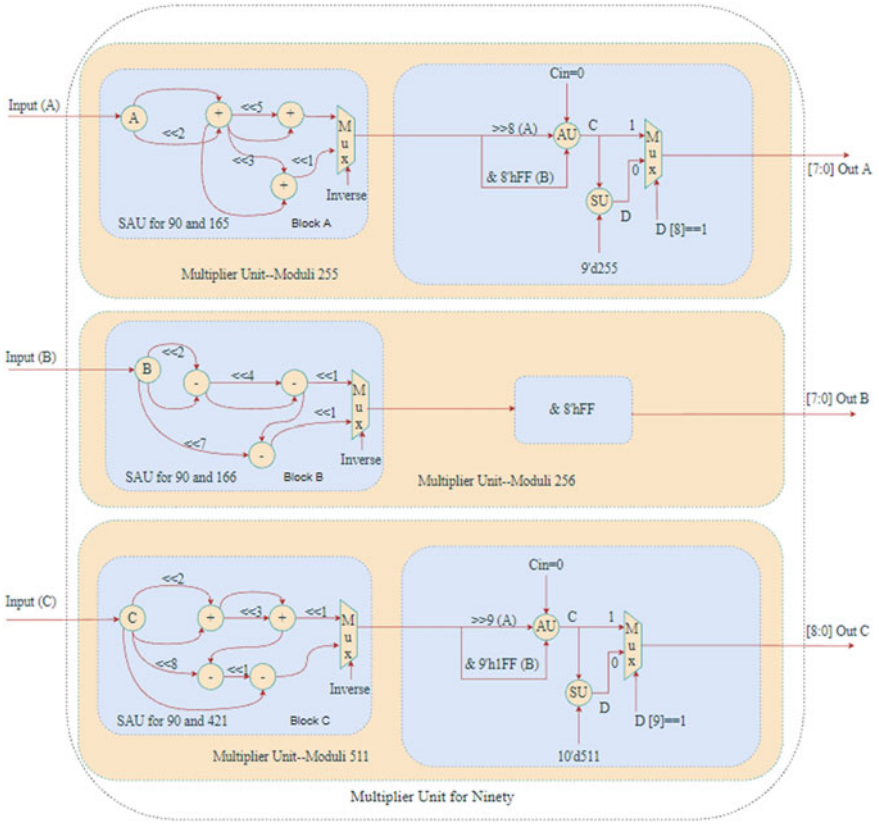

Fig. 4 Multiplication unit for ninety in DCT achitecture

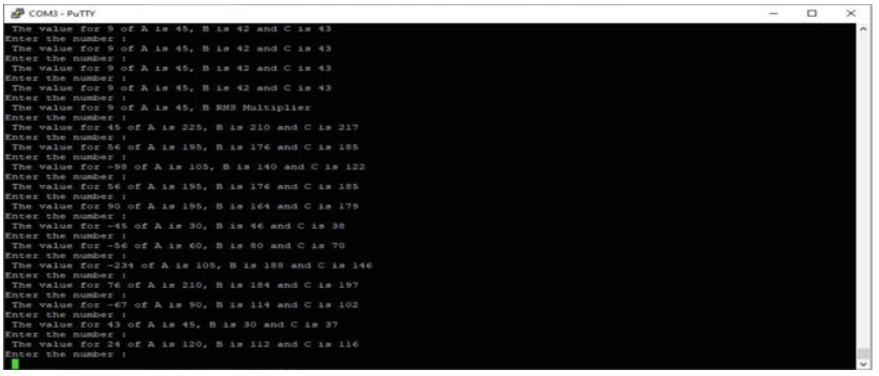

Fig. 5 Screenshot for UART Communication-based Verification of the Proposed Multiplier Unit on putty platform (A = (24*90)mod255 = 120, B = (24*90)mod256 = 112, C = (24*90)mod511 = 116 and A = (45*165)mod255 = 30, B = (45*166)mod256 = 46, C = (45*421)mod511 = 38)

Table 3 Comparison of DCT architectures in terms of gate count and power consumption

Gate count (K)			Power (mW)	
DCT	Using proposed multiplier	Using LUT for multiplication	Using proposed multiplier	Using LUT for multiplication
4 × 4	2.5	27	1.2	8.2
8 × 8	8.3	42	2.09	14.9
16 × 16	24	84.5	7.8	32.3
32 × 32	48.6	155.8	18.2	59.5

RNS applications, including computer security (cryptography), speech recognition, picture enhancement, embedded software, and more.

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Modelling Performance Analysis in VLSI Testing Methodologies

K. Karthikeyan, S. Maragathasundari, M. Kameswari, R. Vanalakshmi, and C. Swedheetha

Abstract In order to improve the quality of devices before they are delivered to customers, VLSI testing processes have been created to detect damaged devices using automated test equipment. To characterize a chip and identify manufacturing issues that must be resolved before full production, a variety of devices must be tested. This testing methodology for services includes a time-consuming and error-prone planning process. Through the use of a queuing strategy, the performance level of the process used in these testing approaches is investigated and examined. In order to utilize the concept of queuing, the process of VLSI testing procedures is transformed into a mathematical problem. The supplemental variable approach is then used to resolve this mathematical queuing problem. A simulation process is used to create performance measurements for this type of queuing system of VLSI testing techniques using the MATLAB and R tools. Results are as anticipated. A specific discussion of how to prevent or minimize disruptions so that the system can run effectively is included in the analysis section.

Keywords VLSI testing methods · Stage of services · Service interruption · And supplementary variable method

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1 Introduction

Before shipping to clients, VLSI testing techniques have been developed to detect faulty devices using automatic test equipment (ATE). A variety of devices must be reviewed in order to define a chip and identify manufacturing issues that should be fixed before the chip is fully produced. Since the characterization and production testing must be completed quickly and efficiently, each item is tested utilizing automated test equipment. Since the first integrated circuit was developed in 1958, Very Large-Scale Integrated Circuit (VLSI) technology has improved significantly. Because even the smallest fault can render an entire integrated circuit (IC) worthless, fabrication-related problems cannot be disregarded. In order to increase the quality of devices before they are delivered to customers, VLSI testing procedures have been created to effectively detect defective devices using automatic test equipment (ATE). From the initial design to the finished product, a device may be tested at different points during the manufacturing process. Using a range of various test methods on integrated circuits is necessary to detect a variety of defects, such as bridging failures and stuck at issues (ICs) (Fig. 1).

The main test objectives are to ensure product quality, diagnosis, and repair. The system is tested by exercising it and analyzing the response to see if it responds as expected after production.

2 Queuing Strategy in VLSI Testing Methodology of Services

With regard to the VLSI testing methodology of service systems, comprising maintenance work, stages of service, setup time stage work, Reneging, interruption, and repair process, the current study offers a stacking strategy to handle the critical issue. The insulating device is sensitive to probability movement at several VLSI testing levels. Testing VLSI has completely evolved into a line problem. It entails offering a range of administrative services.

Figure 2 presents an illustration of the architecture of an n- port output queuing router.

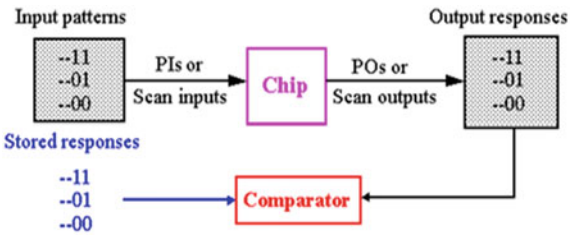

Fig. 1 VLSI circuit

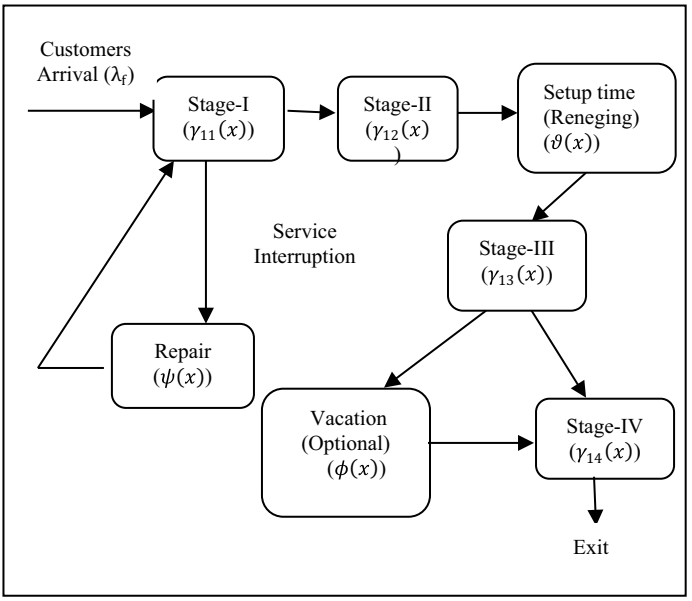

Fig. 2 Queuing model of the process in VLSI testing

Description of Fig. 2:

- *Customers*: Devices to be tested
- *Stage 1*: DC Parametric test—Interruptions arise during this test and the repair process is carried out immediately
- *Stage 2*: AC Parametric test
- *Reneging*: Sometimes it takes longer time because the malfunctioning component was being tested. As a result, the procedure no longer includes the additional devices that were in the line to test the components. This circumstance is known as the Reneging. Here, a stuck at fault model is employed in conjunction with a structural test approach. This specifically occurs during the AC Parametric test process since it takes longer than the other tests.
- *Setup time stage*: Before the actual happening of functional tests, the basic characterization is to be carried out in prior.
- *Stage 3*: Functional tests
- *Optional vacation*: Here vacation means maintenance work which helps the system to detect the flaws or to minimize the interruption which arises during the time of service- Burn in test
- *Stage 4*: Productivity test

Below is a more thorough explanation of how the queuing parameters work in this kind of testing.

The variables that are significantly weighted in this testing approach are service levels, pauses, repair processes, defaulting, and optional maintenance activities.

These elements are used to develop the queuing architect, and the supplemental variable technique of queuing theory is used to describe and address the system's issues. The findings of the performance analysis of the system used in the services testing methodology are then determined.

A. *Stage 1: DC Parametric Test*

In this stage, input and output voltage, leakage current, and other device DC parameters are tested to see if the measured values comply with the electrical requirements. To find accurate input threshold voltages and output driving voltages, a margin search test is employed. Then, a limited set of variables are used in production testing. The gross IDD current test, static IDD current test, dynamic IDD current test, and power supply bump test are the most common power supply current tests. To find out how much current a device uses when it is turned on, perform a power supply current test. This test can find specific physical flaws inside the chip, like those brought on by under-etching or photo mask misalignment.

B. *Interruption During the Process of DC Parametric Test and Repair Process*

Interruption: In this situation, a system may halt as a result of a straightforward physical issue. During the DC parametric test, also known as stage 1, the measurement tool for the system's physically proper operation needs to be assessed. To check for issues with power dissipation and power supply, utilize the basic specifications.

Fault: A physical defect within a circuit or a system– may or may not cause a system failure.

In order to simulate a manufacturing flaw in an integrated circuit, fault simulators and automated test pattern generation (ATPG) tools require a specific fault model called a stuck-at fault. It is believed that specific signals and pins are stuck at the logical values "1," "0," and "X." The input might also be connected to a logical 0 to simulate the behaviour of a malfunctioning circuit that is unable to switch its output pin. Digital circuits employ the failure model known as the single stuck line. Not for design testing, but for post-manufacturing testing. According to the model, one line or node in the digital circuit is permanently set to logic high or logic low. A fault is when a line becomes trapped. The two types of digital circuits are sequential circuits, which have storage, and gate level or combinational circuits, which just have gates like NAND, OR, XOR, etc. This failure model includes the gate level circuits that can be separated from the storage components. The stuck at fault model assumes that only one input on one gate will be problematic at a time; if several are defective, it is thought that a test that can easily identify any one issue should be able to identify multiple faults.

C. *Repair Process*

A failure that leads to a defective output happens when a line is consistently connected to ground; this should be prevented. Any gate may use this line as an input or output. This issue may also be accompanied by one or more stuck defects. In order to recover from this kind of disturbances, a design method known as BIST (Built-In Self-Test)

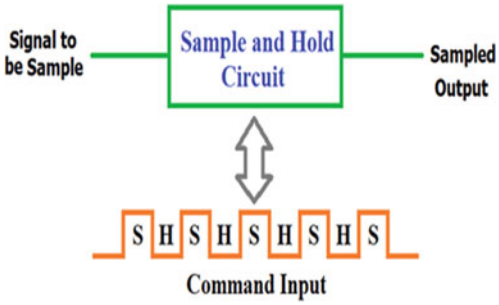

Fig. 3 VLSI sample and hold circuit

uses a circuit's individual components to evaluate the circuit as a whole. A short between two uncoupled logic gate signal lines can also result in bridging. Even while an inter-gate short between disconnected lines might not seem dangerous, a multiplexer bridge defect could result in logical oscillations.

D. *Stage 2: AC Parametric Test*

Sample and hold test: An analogue input signal is sampled by a sample and hold circuit, which then outputs the sampled portion of the input signal after holding the samples for a set period of time. Only a few microsecond-long input signals can be sampled with this device. A sample and hold circuit consists of an operational amplifier, a capacitor, and switching components. The capacitor in the Sample and Hold Circuit serves as the device's central processing unit, storing the sampled input signal and sending it to the output in response to input commands. His circuit is mostly utilised in Analog to Digital Converters to reduce input signal fluctuations that could negatively impact the conversion process (Fig. 3).

An analogue signal with a variable frequency is frequently used as the input voltage signal. The input signal is sampled and held when a command is input. The sampling and holding procedure are carried out in accordance with the command input. When the switch is open, the output signal is kept in the circuit; when it is closed, it is sampled.

E. *Reneging*

The others queuing in line to test the components were impatient while the flawed component was being tested. Here, a stuck at fault model is employed in conjunction with a structural test approach. The logic of digital circuitry governs how Fixed at Fault Models operate. An input or output could become stuck at zero or one. As an illustration, think about the three digital circuits NAND, NOR, and inverter. The majority of logic operations in CMOS technology use these logic gates. A stuck at fault logic gate produces an inaccurate response when a pattern is applied to its inputs. Let's start by discussing the inverter.

- *Error*: Manifestation of a fault that results in incorrect circuit outputs or states—Caused by faults.

- *Failure*: Deviation of a circuit or system from its specified behaviour—Fails to do what it should do—Caused by an error
- Fault → Error → Failure.

F. *Stage 3: Functional Tests*

Setup time stage: A design is fully functionally and parametrically evaluated on a couple of the early fabrications before it is put into production to make sure it works as intended. A characterization test's objective is to determine the highest device parameters at which it will operate.

Functional tests: A functional test's main goal is to identify stuck at problems or other flaws that impact a device's logic states. This kind of testing looks to determine if each application feature operates in accordance with the demands of the product. Each function is compared to the corresponding requirement to ascertain whether its output meets the end user's expectations. Some specific input test vector sequences may result in device failures. It is easy to pinpoint problems with the fabrication process and the chosen test constraints by closely examining these failures. A device must be diagnosed if it fails an initial test to determine the true cause of the failure. Characterization testing will be followed by the deployment of a device into full-scale production. To distinguish between defective and good devices, production tests are utilized. Additionally, gadgets must be tested using automatic testing equipment (ATE). The creation of effective tests is necessary because this step involves testing a significant number of devices at once.

G. *Optional Vacation: [Burn in Test]*

This procedure is used to identify defects or problems in manufacturing. This method generates test patterns using the automatic test pattern generation (ATPG) tool that allow the test engineer to discern between the proper circuit behaviour and the incorrect circuit behaviour. The packaged die in this instance must pass the burn-in stress test. An early-stage problem that manifests in a product is intended to be found and eliminated using a temperature/bias reliability stress test. As a result, burn-in testing is commonly carried out to reduce a device's lifespan such that certain unit's breakdown before being delivered to users.

H. *Stage 4: Production Test*

The SoC test, sometimes referred to as a manufacturing test or production test, is a procedure to confirm that the design is correctly built. This is mostly because chips have imperfections as a result electrical excitation to the wafer's dies. Typically, a wafer probe of the fabrication process' regrettable imperfections. The SoC test, which incorporates wafer sorting, is a procedure for evaluating the manufactured chips. Wafer testing comes first in the manufacturing test process. In this stage, test patterns are applied to all dies while they are still on the wafer in order to test them for flaws. It is carried out using evaluation techniques such the electronic die sort, circuit probe, and wafer final test (WFT) (EDS). Wafer testing has finished, and it is then ready for manufacturing.

In the following part, the aforesaid method of VLSI testing is described in terms of a mathematical study (a queuing system-issue), and in Sect. 3.1, the problem is approached using a supplementary variable technique. As a result, the system's performance metrics are derived, and Sect. 3.2 goes into great depth about the results. In addition to that, Sect. 3.3 provides a detailed explanation of the analysis's findings and studies.

3 M/G/1 Modelling and Study of Solving

Mathematical study: The distribution of customers entering the system is Poisson. Devices line up for the second stage of service after finishing the first stage of administration. The study's other metrics, including service time, all have a broad distribution. If no users are waiting for the first two levels of service when all arriving users have received the second phase of service, the server takes a brief setup time stage of service before completing the necessary server third stage of duty. Vacations in this context refer to the optional system maintenance work that is carried out once stage 3 servicing is complete. This maintenance effort helps the system provide a flawless service to the greatest extent possible. This is optional. The final bit of work for the VLSI testing approach of services will be completed before the server enters a fourth level of service after the vacation. Similar to this, stage 1 service will inevitably experience server failure. In fact, the server immediately begins the repair process. Service is restored after the problem has been fixed. Users wait in line to obtain stage 2 of the service once the first phase of service is complete. Customers finally exit the system after completing all servicing procedures. In software development settings, early and rapid performance monitoring of enterprise, high-traffic apps is essential. As a result, more performance modelling efforts are being used to help anticipate system performance parameters early in the lifetime. Many performance testers mistakenly think queuing theory is too difficult and outsource it to key efficiency modelling professionals because they are afraid of mathematics. However, analyzing system performance can be made easier by grasping the foundations of mathematical queuing theory. Performance testers need to be aware of the relationships among performance metrics like response time, throughput, and server utilization in order to identify performance-, scalability-, and capacity-related problems rapidly.

The queuing theory is a useful tool for assessing the common occurrence of standing in line. It is the mathematical analysis of how waiting lines or queues arise, operate, and get congested. A queuing model is an abstract representation of a scheduling process that utilizes certain presumptions on the discipline and organization of the queue, the quantity and sort of servers, the inter arrival and service procedures, and their probabilistic character. There are infinite different variations, but we will concentrate on a Predominant non markovian bulk queuing model in this paper because they are more frequently employed. There are equations available for such models, along with many others, that enable the quick computation of

numerous performance measurements that can be utilized to assist in the design of a new regime. The non-Markovian queuing model has been described by many writers with a variety of parameters. Barbe [1] studied a Very large-scale integration (VLSI): fundamentals and applications. Chen et al. [2] displayed an investigation of swarm intelligence techniques in VLSI routing problems. Vanalakshmi et al. [22] performed a Queuing system in the study of VLSI physical design and derived the queue performance measures based on the effect of various queue parameters. Maragathasundari and Dhanalakshmi [10] considered a queuing approach in Mobile adhoc networks problem. Raheel Ahmed Memon et al. [18] reported on Simulation Model for Blockchain Systems Using Queuing Theory. An MX/G/1 G-queue with Single Vacation, Setup Times, and Working Breakdown was explored by Li and Li [5]. Maragathasundari [9] examined a test on the general service distribution queuing system using an established time and a second discretionary administration. Mary Florida et al. [15] discussed about the optimized Meta-Heuristic Queuing Model in VLSI Physical Design. Mirabella et al. [16] suggested a Testing single via related defects in digital VLSI designs. Performance Modelling of Fault-Tolerant Machining System with Working Vacation and Working Breakdown was the subject of a report by Jain et al. [3]. Maragathasundari et al. [19] made a Queuing Analysis in Robotic Process Automation. A study on the performance metrics of the non-Markovian model of optional forms of service with extended vacation, reneging process, and service disruption followed by phases of repair process was provided by Maragathasundari and Manikandan [11]. The queuing model of optional kind of services with service stoppage and revamp procedure in web hosting was examined by Maragathasundari and Joy [12]. Vanalakshmi et al. [23] prepared a Queuing system behaviour in thermo pack process. Jayapradha [4] studied the Detection and Diagnosis of Faults in VLSI Testing. Manikandan et al. [10] gave a report on a mathematical model on VLSI circuit partitioning. Scholze et al. [20] discussed about the Optimized queue-based communication in VLSI. Picker and Fellman [17] studied about the VLSI priority packet queue with bequest. Maragathasundari et al. [13] prepared a report on the investigation of mathematical modelling in non markovian queue. Manikandan et al. [6] investigated the specific issues in VLSI physical design the Analysis of non-Markovian batch arrival queuing model with many phases of service of restricted admissibility, feedback service, and three optional vacations in manufacturing and production was optimized by Maragathasundari and Srinivasan [14]. Maragathasundari et al. [8] studied about the phases of services with multi-vacation policies. Chakravarthy et al. [21] examined the queuing model with server breakdowns, repairs, vacations, and backup server.

All of the queuing literature described above contains very detailed information on the vacation time. The perspectives of many authors regarding the Vacation approach as a required step have been expressed in a wide range of publications. As part of the VLSI design study in between the services, no mandatory vacation was required. Additionally, the break doesn't start until all service steps are complete. However, no author has yet added a vacation to their work during the intervals in between services. In many real-life scenarios, a pause during the service is essential. In this case, a multi-vacation plan is also helpful. In this study, the concepts of flexible

vacation, Reneging, phases of services, interruptions, and fixation process have all been introduced together with the investigation of queuing technique.

To the highest possible standard, this is the very first queuing article in the operation of VLSI testing techniques of services that clearly illustrates the performance analysis of all the system's numerous parameters Quantity of input, optional vacation, reneging, interruption and repair process.

The scheduling algorithm used in VLSI testing methodologies for services is applied in this work in the most complex manner possible.

3.1 Conventions, Nomenclature, and Model Assumptions

Clients enter the framework in groups of varying sizes and follow a Poisson distribution with an arrival rate $\lambda_s > 0$. The service is distributed in a general manner.

Notations	Description	Distribution function	Density function
$A_n^{(1)}(x)$	First stage of service: (Service Interruption) The chance that there are $n \geq 1$ customers in the line ahead of the one being served and the amount of time that has passed since this customer was last served is x when there are n customers in the first stage of service The conditional probability that a stage 1 service will be completed is denoted by $\gamma_{11}(x)$ and it is given by $\gamma_{11}(x) = \frac{j_1^*(x)}{1-j_1^*(x)}$, $j_1^*(x) = \gamma_{11}(x)e^{-\int_0^x \gamma_{11}(t)dt}$	$J_1^*(x)$	$j_1^*(x)$
ζ	Service Interruption: A service interruption is a transmission interruption that completely eliminates the service's signal, making the service inoperable. The service will be "Available" if there isn't a service interruption	–	–
$A_n^{(2)}(x)$	Second stage of service: This is similar to the stage 1 service $\gamma_{12}(x) = \frac{j_2^*(x)}{1-j_2^*(x)}$, $j_2^*(x) = \gamma_{12}(x)e^{-\int_0^x \gamma_{12}(t)dt}$	$J_2^*(x)$	$j_2^*(x)$
$R_n(x)$	Repair Process: The process of restoring a damaged or malfunctioning object to good working order is referred to as the repair process $\psi(x) = \frac{j_3{}^*(x)}{1-j_3{}^*(x)}$, $j_3{}^*(x) = \psi(x)e^{-\int_0^x \psi(t)dt}$	$J_3{}^*(x)$	$j_3{}^*(x)$

(continued)

(continued)

Notations	Description	Distribution function	Density function
$G_n(x)$	Setup time stage of service: (Reneging) The amount of time needed to configure a machine so that it is prepared to handle a job is known as setup time $\vartheta(x) = \frac{j_4^*(x)}{1-J_4^*(x)}$, $j_4^*(x) = \vartheta(x)e^{-\int_0^x \vartheta(t)dt}$	$J_4^*(x)$	$j_4^*(x)$
χ	Reneging: Reneging is the act of a customer leaving a queuing system without obtaining service	–	–
$A_n^{(3)}(x)$	Third stage of service: $\gamma_{13}(x) = \frac{j_5^*(x)}{1-J_5^*(x)}$, $j_5^*(x) = \gamma_{13}(x)e^{-\int_0^x \gamma_{13}(t)dt}$	$J_5^*(x)$	$J_5^*(x)$
$L_n(x)$	Vacation: (Optional) In a working vacations queuing paradigm, the server operates at a varied rate throughout the vacation period rather than remaining fully idle. The arrival rate varies based on the server's condition $\phi(x) = \frac{j_6^*(x)}{1-J_6^*(x)}$, $J_6^*(x) = \phi(x)e^{-\int_0^x \phi(t)dt}$	$J_6^*(x)$	$J_6^*(x)$
$A_n^{(4)}(x)$	Fourth stage of service: $\gamma_{14}(x) = \frac{j_7^*(x)}{1-J_7^*(x)}$, $j_7^*(x) = \gamma_{14}(x)e^{-\int_0^x \gamma_{12}(t)dt}$	$J_7^*(x)$	$J_7^*(x)$

Using the birth and death process, the governing equations for the defined queuing frame work and its corresponding bounding conditions are framed.

Next, we employ the supplemental variable technique to calculate the probability of the queue length for the server's idle time, which serves as the foundation for determining all the performance measures of the defined queuing frame work.

By calculating the linear combination of the number of consumers already present and the projected remaining time for the client being serviced, the size of the line-up and the waiting time are determined. We also determine how long queues typically are for embedded processes.

The combined distribution of the peak time duration and the total number of clients serviced during a busy period is the final result of our method.

Using the supplementary variable technique in the governing equations and boundary conditions, the probability generating function of queue size $T_q^*(z)$, which serves as a foundation for determining the other queue performance measures of the defined VLSI testing methods of services is derived

$$\mathrm{T}_{\mathrm{q}}^*(\mathrm{z}) = \mathrm{A}_{\mathrm{q}}^{(1)}(\mathrm{z}) + \mathrm{A}_{\mathrm{q}}^{(2)}(\mathrm{z}) + \mathrm{R}_{\mathrm{q}}(\mathrm{z}) + \mathrm{G}_{\mathrm{q}}(\mathrm{z}) + \mathrm{A}_{\mathrm{q}}^{(3)}(\mathrm{z}) + \mathrm{L}_{\mathrm{q}}(\mathrm{z}) + \mathrm{A}_{\mathrm{q}}^{(4t)}(\mathrm{z}) \quad (1)$$

where $A_q^{(1)}(z), A_q^{(2)}(z), R_q(z), G_q(z), A_q^{(3)}(z), L_q(z)$ and $A_q^{(4)}(z)$ represents the parameters which is explained in the Table of Notations.

$$T_q^*(z) = \frac{\lambda_f H(E(z)-1)\left[\frac{1-J_1^*(s)}{s}\right]\left\{1+\zeta z J_2^*(u)\left[\begin{array}{c}1+J_3^*(u)+J_3^*(u)J_4^*(g)+J_3^*(u)J_4^*(g)J_5^*(u)\\ +rJ_3^*(u)J_4^*(g)J_5^*(u)J_6^*(u)(1+J_7^*(u))\end{array}\right]\right\}}{z-\zeta z J_2^*(u)\left[\frac{1-J_1^*(s)}{s}\right]\left(1+rJ_3^*(u)J_4^*(g)J_5^*(u)J_6^*(u)J_7^*(u)\right)} \tag{2}$$

Execution measures of the queuing architecture of VLSI testing methods

All of the queue performance indicators in this section are then computed using the probability generating function of the queue length, which was determined in the portion before.

(i) *Idle time and factor of utilization of the server*

Normalization condition $T_q^*(z) + H = 1$ is used in order to determine the idle time H.

$T_q^*(z)$ becomes indeterminate as $z \to 1$, L. Hospital's rule is applied.

$$\text{Hence, we get } H = \frac{D'(1)}{N'(1)+D'(1)} \tag{3}$$

$$\text{Utilization factor } \rho \text{ is calculated using } \rho = 1 - H \tag{4}$$

(ii) *The total number of inputs waiting in line* (L_q)

L' Hospital's rule is used to calculate the steady-state average queue length.

$$L_q = \lim_{z\to 1} \frac{D'(z)N''(z) - N'(z)D''(z)}{2\left(D'(z)\right)^2} \tag{5}$$

$$\text{where, } N'(1) = \lambda_f\left[\frac{1-J_1^*(s)}{s}\right] \tag{6}$$

$$\begin{aligned} N'(1) = 2\lambda_f\Bigg[\Bigg[\frac{1-J_1^*(\zeta)}{\zeta}\Bigg]\lambda_f E(S_1) - J_1^{*\prime}(\zeta) + E(R)\zeta\Bigg[\frac{1-J_1^*(\zeta)}{\zeta}\Bigg] \\ + E(S_2)J_1^*(\zeta) + E(G)J_1^*(\zeta) + E(S_3)J_1^*(\zeta) + rE(V)J_1^*(\zeta) \\ + E(S_4)J_1^{*\prime}(\zeta) + \left(1-J_1^*(\zeta)\right)E(S_4)\Big] \end{aligned} \tag{7}$$

$$\begin{aligned} D'(1) = 1 - \zeta\Bigg[\Bigg[\frac{1-J_1^*(\zeta)}{\zeta}\Bigg] + (1+\lambda_f E(S_1)) - J_1^{*\prime}(\zeta) \\ -\lambda_f\left(J_1^{*\prime}(\zeta) + J_1^*(\zeta)(E(S_2)+E(S_3)+E(G)+rE(V)+E(S_4))\right)\Big] \end{aligned} \tag{8}$$

$$
\begin{aligned}
\mathrm{D}'(1) = (\lambda_{\mathrm{f}})^2\big[\mathrm{J}_1^{*\prime}(\zeta) &+ \mathrm{E}\big(\mathrm{S}_2^2\big) + \mathrm{E}\big(\mathrm{S}_3^2\big) + \mathrm{E}\big(\mathrm{S}_4^2\big) + \mathrm{E}\big(\mathrm{G}^2\big) + \mathrm{E}\big(\mathrm{V}^2\big) \\
&+ 2\mathrm{J}_1^{*'}(\zeta)(\mathrm{E}(\mathrm{S}_2) + \mathrm{E}(\mathrm{S}_3) + \mathrm{E}(\mathrm{G}) + \mathrm{rE}(\mathrm{V}) + \mathrm{E}(\mathrm{S}_4)) \\
&+ 2(\mathrm{E}(\mathrm{S}_2)\mathrm{E}(\mathrm{S}_3) + \mathrm{E}(\mathrm{S}_2)\,\mathrm{E}(\mathrm{S}_4) + \mathrm{E}(\mathrm{S}_2)\mathrm{E}(\mathrm{G}) + \mathrm{rE}(\mathrm{S}_2)\mathrm{E}(\mathrm{V}) \\
&+ \mathrm{E}(\mathrm{G})\mathrm{E}(\mathrm{S}_3) + \mathrm{rE}(\mathrm{G})\mathrm{E}(\mathrm{V}) + \mathrm{E}(\mathrm{G})\mathrm{E}(\mathrm{S}_4) + \mathrm{rE}(\mathrm{S}_3)\mathrm{E}(\mathrm{V}) \\
&+ \mathrm{E}(\mathrm{S}_3)\mathrm{E}(\mathrm{S}_4) + \mathrm{rE}(\mathrm{V})\mathrm{E}(\mathrm{S}_4))] - 2\zeta\lambda_f\mathrm{E}(\mathrm{S}_2)\mathrm{E}(\mathrm{G})(-\lambda_{\mathrm{f}} + \chi) \\
&- 2\lambda_f\mathrm{J}_1^{*\prime}(\zeta)\mathrm{E}(\mathrm{G})(-\lambda_{\mathrm{f}} + \chi) - 2\zeta\lambda_{\mathrm{f}}\mathrm{E}(\mathrm{S}_3)\mathrm{E}(\mathrm{G})(-\lambda_{\mathrm{f}} + \chi) \\
&- \zeta\mathrm{E}\big(\mathrm{G}^2\big)(-\lambda_{\mathrm{f}} + \chi)^2 - 2\mathrm{r}\zeta\lambda_{\mathrm{f}}\mathrm{E}(\mathrm{G})\mathrm{E}(\mathrm{V})(-\lambda_{\mathrm{f}} + \chi) \\
&- 2\zeta\mathrm{E}(\mathrm{G})(-\lambda_{\mathrm{f}} + \chi)\mathrm{E}(\mathrm{S}_4)
\end{aligned}
\tag{9}
$$

(iii) *Performance measures for the waiting time*

The length of the system, the average wait time of a customer in the framework, and the average wait time of a consumer in line may all be determined using Little's method.

$$\mathrm{W}_{\mathrm{q}} = \frac{\mathrm{L}_{\mathrm{q}}}{\lambda_{\mathrm{c}}} \tag{10}$$

$$\mathrm{W} = \frac{\mathrm{L}}{\lambda_{\mathrm{c}}} \tag{11}$$

$$\mathrm{L} = \mathrm{L}_{\mathrm{q}} + \rho \tag{12}$$

3.2 Measured Approach to the VLSI Testing Methods' Queuing Structure

R software used in the suggested VLSI architecture analyze the impact of different settings on queue execution metrics. The assumption in this situation is that the service time will be dispersed exponentially. We gathered the following values.

A. Study on the effect of various parameter implementation in R software:

$$\lambda_f = 2,\ \ \zeta = 3,\ \ \chi = 4,\ \ r = 0.1,\ \ \vartheta = 5,\ \ \gamma_{11} = 2.5,\ \ \gamma_{12} = 4.5,$$
$$\gamma_{13} = 5.5,\ \ \phi = 6,\ \ \psi = 6.5,\ \ \gamma_{14} = 7,$$

$$\mathrm{E}(\mathrm{S}_2) = \frac{1}{\gamma_{12}},\ \ \mathrm{E}(\mathrm{S}_3) = \frac{1}{\gamma_{13}},\ \ \mathrm{E}(\mathrm{G}) = \frac{1}{\vartheta},\ \ \mathrm{E}(\mathrm{L}) = \frac{1}{\phi},\ \ \mathrm{E}(\mathrm{R}) = \frac{1}{\psi},$$
$$\mathrm{E}(\mathrm{S}_4) = \frac{1}{\gamma_{14}},\ \ \mathrm{E}\big(\mathrm{S}_2^2\big) = \frac{2}{(\gamma_{12})^2},\ \ \mathrm{E}\big(\mathrm{S}_3^2\big) = \frac{2}{(\gamma_{13})^2},\ \ \mathrm{E}\big(\mathrm{G}^2\big) = \frac{2}{(\vartheta)^2},$$
$$\mathrm{E}\big(\mathrm{L}^2\big) = \frac{2}{(\phi)^2},\ \ \mathrm{E}\big(\mathrm{R}^2\big) = \frac{2}{(\psi)^2},\ \ \mathrm{E}\big(\mathrm{S}_4^2\big) = \frac{2}{(\gamma_{14})^2}.$$

In Table 1, it is seen that the queue's length grows as the number of customers does. As a result, the work is moving along very slowly and the passive component is growing. Last but not least, the length of the line and the wait time grow as the number of consumers rises.

In Table 2, it is shown that reneging shortens both the line and the waiting time by lengthening the line. The utilization factor declines and the passive factor rises as customers leaves the line.

Table 3 indicates that a breakdown is what results in a service interruption. The malfunction occurs while the server is not in use. While the server is inactive, the variables for idle time and utilization remain constant. But the wait time also increases as additional devices are added to the line.

Table 4 shows the relationship between the increase in idle time and the optional maintenance rate. As a result, the server's awake time is cut down. The length of the queue and wait times will be less if the server does not insert during its own optional vacation.

Table 5 demonstrates how the server has been operating faster than the utilization factor while simultaneously prolonging the waiting time following setup. The size of the queue and the waiting durations will both go down once the server has concluded the setup process.

B. *Graphical portrayal of the performance measures*

Using the values from the Table 5, the implementation metrics of the different indicators are examined in this section using **MATLAB**.

Table 1 The impact of arrival rate

λ_f	H	ρ	L_q	L	W_q	W
2	0.3827	0.6173	0.7903	1.1730	0.3952	0.5865
2.8	0.4617	0.5383	2.4535	2.9152	1.2268	1.4576
3.6	0.4972	0.5028	3.6819	4.1791	1.8409	2.0896
4.4	0.5175	0.4825	4.5178	5.0353	2.2589	2.5177
5.2	0.5307	0.4693	5.2329	5.7635	2.6164	2.8818

Table 2 The impact of reneging

χ	H	ρ	L_q	L	W_q	W
4	0.3827	0.6173	0.7903	1.1730	0.3952	0.5865
4.5	0.3895	0.6105	0.5907	0.9802	0.2953	0.4901
5	0.3989	0.6041	0.3989	0.7948	0.1995	0.3974
5.5	0.4023	0.5977	0.2175	0.6198	0.1087	0.3099
6	0.4085	0.5915	0.1058	0.5472	0.0861	0.2740

Table 3 The impact of breakdown

ζ	H	ρ	L_q	L	W_q	W
3	0.3827	0.6173	0.7903	1.1730	0.3952	0.5865
3.1	0.3827	0.6173	1.4289	1.8116	0.7145	0.9058
3.2	0.3827	0.6173	3.5564	3.9391	1.7782	1.9695
3.3	0.3827	0.6173	5.9004	6.2831	2.9502	3.1415
3.4	0.3827	0.6173	8.4608	8.8435	4.2304	4.4217

Table 4 The impact of optional vacation

ϕ	H	ρ	L_q	L	W_q	W
0.1	0.3827	0.6173	0.7903	1.1730	0.3952	0.5865
0.3	0.4022	0.5978	0.7621	1.1643	0.3811	0.5822
0.5	0.4205	0.5795	0.6612	0.8171	0.3062	0.4085
0.7	0.4377	0.5623	0.5447	0.7545	0.2584	0.3772
0.9	0.4539	0.5461	0.3985	0.6254	0.2087	0.2231

Table 5 The impact of completion of setup time stage

ϑ	H	ρ	L_q	L	W_q	W
5	0.3827	0.6173	0.7903	1.1730	0.3952	0.5865
6	0.3619	0.6381	0.7145	0.9825	0.3206	0.5120
7	0.3461	0.6539	0.6450	0.9061	0.2757	0.4731
8	0.3338	0.6662	0.5841	0.8682	0.2021	0.3412
9	0.3239	0.6761	0.4150	0.7518	0.1411	0.2371

The study's above-mentioned parameters' effects are examined, and the results are represented graphically by the usage of MATLAB software as follows Figs. 4, 5, 6, 7 and 8.

4 Summary and Conclusion

Numerous methods and approaches can be used when approaching testing. The applicability of the most popular techniques is assessed in this study. Today, testing is a significant design constraint, and selecting the best test strategy is a difficult issue. This argument does not favour or single out any one test approach in particular. Instead, it will make an effort to assess and contrast various approaches in the various testing phases of production, the study's methodology, and the findings of simulations on the testing burden, frequency of verification and validation, and test efficacy. This study investigates the VLSI testing procedure utilizing a queuing

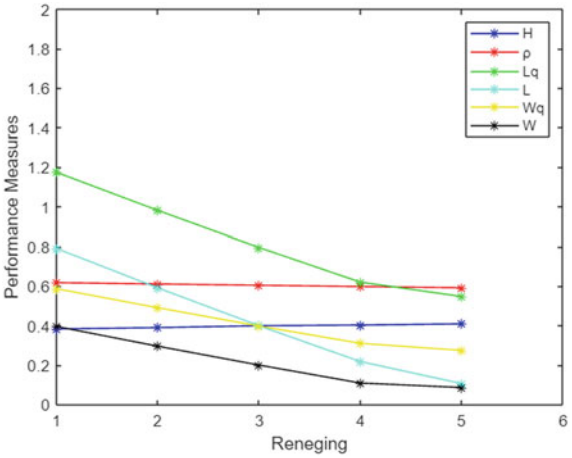

Fig. 4 Graphical depiction of the outcome of arrival rate (Table 1)

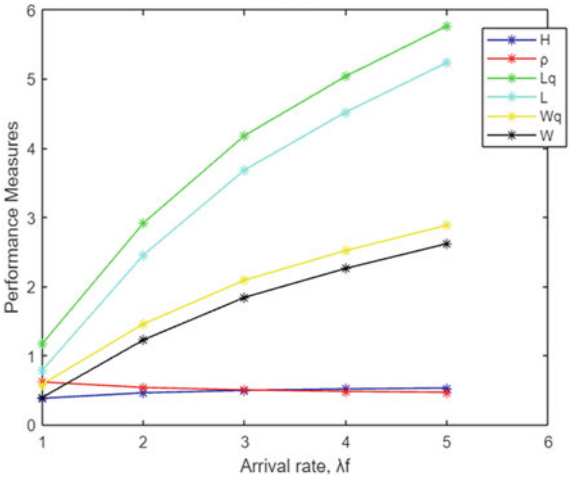

Fig. 5 Graphical illustration of the effect of reneging (Table 2)

technique and makes performance measurements. Additionally, the model is fully supported by mathematical formulation, and the inquiry is carefully conducted using techniques for graphic depiction. In-depth descriptions of the earlier articles are provided, and it is made clear how this study differs from earlier ones. The pictures are a true representation of the indicated model. Additionally, the model is supported by numerical findings, and the study is conducted thoroughly using visual portrayal techniques. This makes it much simpler to identify issues and make additional system enhancements when a particular identified queue issue occurs during testing. The method described here differs from the majority of the research on quick diagnosis or rule-based decision theory in that it necessitates an estimate of the signal position.

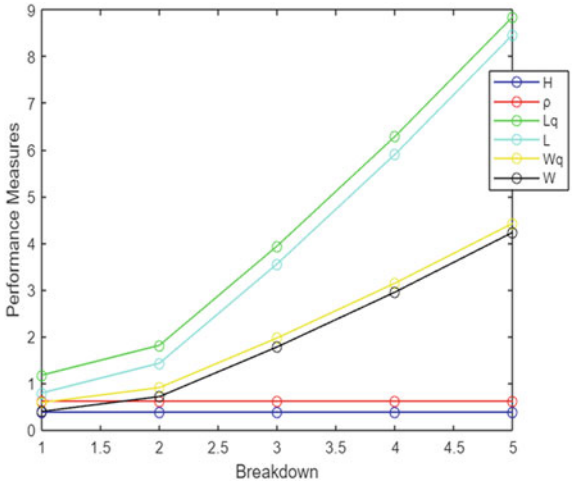

Fig. 6 Image of the upshot of breakdown (Table 3)

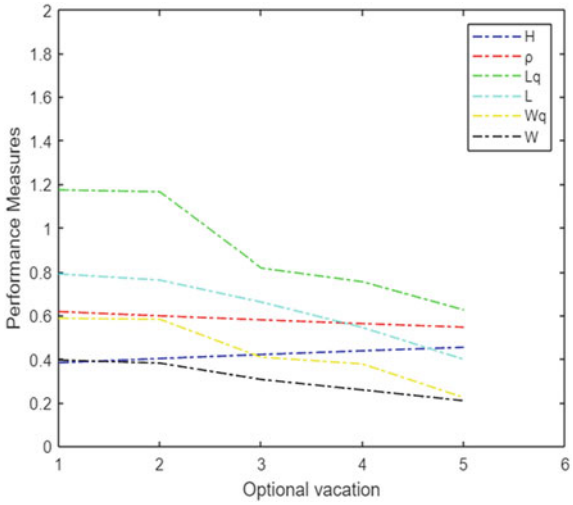

Fig. 7 Graphical depiction of the conclusion of optional vacation (Table 4)

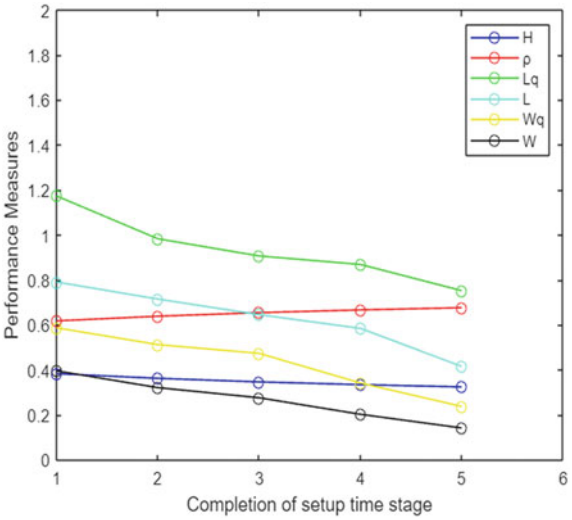

Fig. 8 Picture of the result of completion of setup time process (Table 5)

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Verification of AHB2APB Bridge Protocol Using UVM

Saroja V. Siddamal, Suneeta V. Budihal, and Apoorva Narode

Abstract It is vital to update tools and methodologies in pace with technological innovation in order to handle the problems posed by the changing verification environment. The authors propose a verification of AHB2 APB bridge protocol using Universal Verification Methodology (UVM). It is the intention of this study to discuss the benefits of using the Universal Verification Methodology for AHB2APB verification. This work focuses on creating a standard AHB2APB Bridge protocol architecture that is efficient and on enhancing the authentication environment utilizing a System Verilog UVM implementation. An automated authentication platform developed by UVM will produce an AHB2APB Bridge debugging test for any given DUT. UVM-based performance verification adds randomized test scenarios to ensure high-performance by covering all potential cases. On the other hand, Verilog cannot be used to examine the active cover model in a typical verification location. System Verilog is used for coding, while Questasim is the simulation tool of choice. The code coverage for RTL design is acquired, and 98.81 percent of the code coverage and 100 percent of the functional coverage are recovered.

Keywords AHB2APB bridge · UVM · Code coverage · Questasim

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1 Introduction

To implement the AHB2APB bus protocol, multiplexers are a connecting technique. In this technique, the master and arbitrator communicate as follows: The address and control signals driven by the bus master decide whether a transfer is a read or write transfer. The address is sent to the chosen slave when the arbitrator selects the master that possesses its control signal. The data read and signal response multiplexer, which selects the pertinent signals from the slaves needed for the transfer, are primarily under the control of the central decoder.

The AHB bus is for high clock frequency system for providing:

- It offers the High-performance, high bandwidth and pipelined operation
- AHB protocol supports Split transactions, burst transfers, and multiple bus masters.
- It has outstanding latency and uses little power.

The advanced peripheral bus (APB): It is a straightforward, non-pipelined protocol that enables reading and writing from or to a bridge or master to a number of slaves via a common bus. The same sets of signals are used for both reads and writes. The transfer of bursts is not supported.

2 Related Works

Several works on the verification of communication protocols are contributed to its development and overall performance. In paper [2] authors have worked on the AMBA AHB for system modules with high-performance and high clock frequencies. The high-performance backbone system bus is the AHB. The effective connectivity of processors is supported by AHB. The AMBA APB is designed to use less power and have a simpler interface to support peripheral operations. Functions of the AHB2APB Bridge protocol are implemented in this project by writing the code in VERILOG and simulating it in XILINX ISE. In this work, we write UVM verification code and use several test cases to validate all Bridge protocol functionalities.

Authors in their [3] work explain that an open System-on-Chip bus protocol called Advanced Microcontroller Bus Architecture (AMBA) allows high-performance buses and low-power devices to interface with one another. The AHB and APB buses are connected by a bridge that is also present. Bridges are common bus-to-bus interfaces that enable standardized communication between IPs linked to various buses. In order to develop, implement, and test the AHB2APB bridge, Verilog and UVM were used, and the results are described in this work The AHB2APB Bridge is a sophisticated interface bridge between AHB and APB that has been designed as a synthesizable RTL code.

Authors in [4] worked on the fast time-to-market requirements, the rising expense of testing makes producing a highly integrated SoC a significant strain. An effectively

tested design with on-chip peripherals technique is presented in this study. Utilizing the bridge function to its fullest extent allows for effective functional and structural testing. By adding more test channels and condensing the test-control protocols, the testing time can be greatly decreased. According to experimental findings, both functional and structural test modes significantly minimize testing durations and area overhead. The suggested method can be applied to many on/off-chip bus bridge types.

In paper [9] the AMBA is widely adopted connectivity standard and on-chip-bus-architecture is used to increase the reusability-of-IP core (SOC). It is difficult to analyze embedded systems that use AMBA. The authors have synthesized and simulated the AHB2APB Bridge, which is a complex-interface-bridge between the AHB and APB. Here, a list of Bridge modules is constructed using the Paper Synthesized Net. To perform functional and timing simulation Xilinx and Modelsim tools are used.

Authors in the paper [10] have designed and verified the AMBA-APB Protocol. AHB, ASB, and AXI, for example, are high-performance bus components that are utilized as interfaces with APB, a low performance bus, and other components of the AMBA Bus. APB connects to slaves such as UART, TIMER, Keypad, INTERRUPT CONTROLLER, etc. using minimal peripheral bandwidth. Simulation-based verification is the conventional approach. The complexity of ICs has risen as technology has advanced. As a result, verification time has also increased. The design of the APB protocol in Verilog and verification in two languages—System Verilog and Universal Verification Methodology—are the primary topics of this work (UVM).

3 Methodology

All the high-performance peripherals will be connected to an AHB bus, while the low power peripherals will all be connected to an APB bus.

Bridge transforms AHB transferals to APB transferals; it is both an AHB slave and an APB master; it serves as an interface-between-high-performance IPs and low-power peripherals. For building high-performance embedded microcontrollers, AMBA specification-defines-an on-chip communications standard.

In the AMBA Structure there are two buses AHB and APB. High-performance is needed for the CPU (ARM) cores, DMA, and high bandwidth memory, even though the low bandwidth peripherals are connected through the APB bus. An AHB to APB bridge connects AHB with APB. While all peripherals linked to the APB act as slaves, the AHB-APB bridge, also referred to as the APB bridge, serves as the Master and initiates all transactions.

This paper discusses the architecture of the AMBA APB bridge protocol and offers a design verification strategy for creating an AMBA APB bridge verification IP with a UVM-based custom test bench. It also looks at the outcomes.

A. Advanced High-Performance Bus (AHB)

AHB is a high-performance and high-clock-frequency system modules which acts as the system's high-performance-backbone bus. Low power peripheral microcell operations can be successfully coupled with CPUs, on-chip memories, and off-chip-external memory-interfaces with the help of AHB.

AHB also makes use of automated test methodologies and synthesis to ensure usability in an efficient design flow.

Any internal memory, the APB bridge, and the external memory interface are the most often used AHB slaves. The following components are present in an AMBA AHB system architecture that is typical: 3 AHB master A bus master can begin read and write operations by providing an address and control information. There can only ever be one active bus master driving the bus at a time. AHB employee A bus slave responds to a read or write operation within a particular address-space range.

The bus slave notifies the active master of the data transfer's success, failure, or waiting status. Decide for AHB The bus arbitrator makes it possible for just one bus master to initiate data transfers at once. The arbitration protocol is established, however, any arbitration–procedure, such as highest priority or fair access, may be employed depending on the needs of the application. An AHB would only have one arbiter, even though this would be superfluous in systems with a single bus master. The AHB decoder, decodes each transfer's address and communicates a chosen signal to the participating slave. A single centralized decoder must be used by all AHB implementations.

B. Advanced Peripheral Bus (APB)

There is APB for low-power peripherals. The interface is made to be as simple as feasible to facilitate peripheral operations while consuming the least amount of power possible. APB is compatible with both system bus iterations. The APB bridge acts as a slave module for the local peripheral bus and controls bus handshake and control signal retiming. In an AMBA APB implementation, an APB bridge is frequently included and is required to convert AHB or ASB transfers into a language that the slave devices on the APB can understand.

The Architecture of AHB to APB Bridge is as shown in Fig. 2.

APB Finite State Machine and AHB Slave Interface are the bridge's primary components (FSM). This bridge generates a signal for each connected device and manages the peripherals map to memory addresses.

State machine representation of the process is as shown in Fig. 3. The "Hreadyout" signal governs all AHB transactions. All APB output signals are generated under the control of the bridge as well.

PWDATA is continuously driven by the bridge, the only master aboard the bus. When the slaves are chosen by the bridge during APB read transfers, PRDATA is only driven.

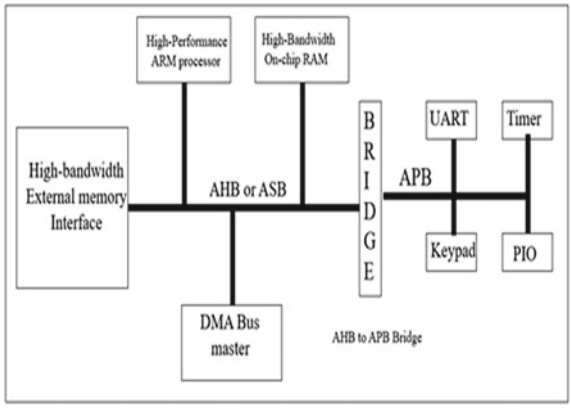

Fig. 1 AMBA system

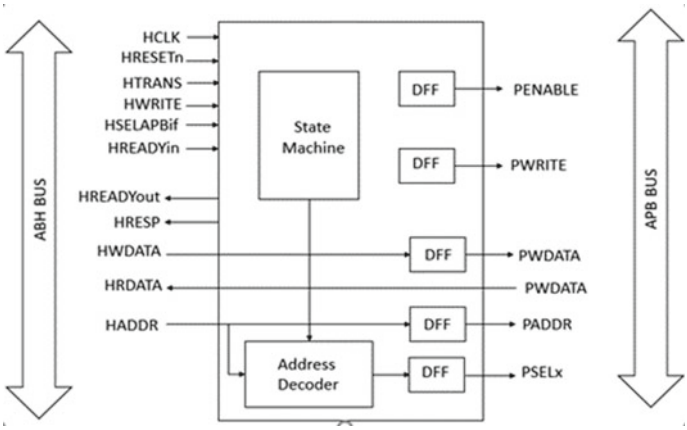

Fig. 2 AHB to APB bridge architecture

Verilog HDL is used to create the AHB-APB bridge.

The APB FSM controller and AHB slave module are the two submodules that make up the bridge module. It is created as a Register-Transfer-Level module so that it can be physically realized and synthesized. To ensure that the bridge complies with the protocol, two extra modules have been constructed. Bus functional is the realization of AHB Master and APB Slave modules.

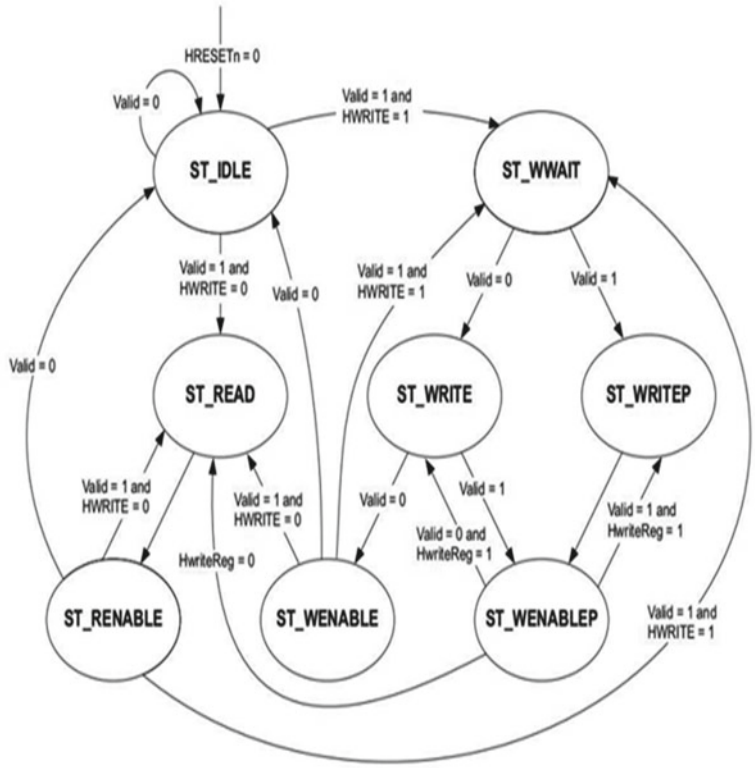

Fig. 3 FSM of AHB to APB bridge

4 Implementation Details

. The foundation of the Open Verification Methodology is used by UVM. Version UVM 1.0 EA was made available by Accellera on May 17, 2010. A strong verification strategy is frequently used to support a design's high quality. AHB2APB bridge is incorporated into the project's design. Functional verification of the integrated device is carried out utilizing a verification test bench built using UVM and System Verilog (SV). A good verification strategy should test the Design Under Test (DUT functioning)'s in all conceivable situations. An engineer should create an organized, automated test bench to do this. A good verification plan should be created before building a test bench, taking all potential outcomes into consideration.

A. Assertion based Verification Plan

The predicted behavior of the DUT under specific circumstances or events is tested using assertions. The assertions will stop the test and indicate an error if the device doesn't operate as expected. The assertions are among the most potent components

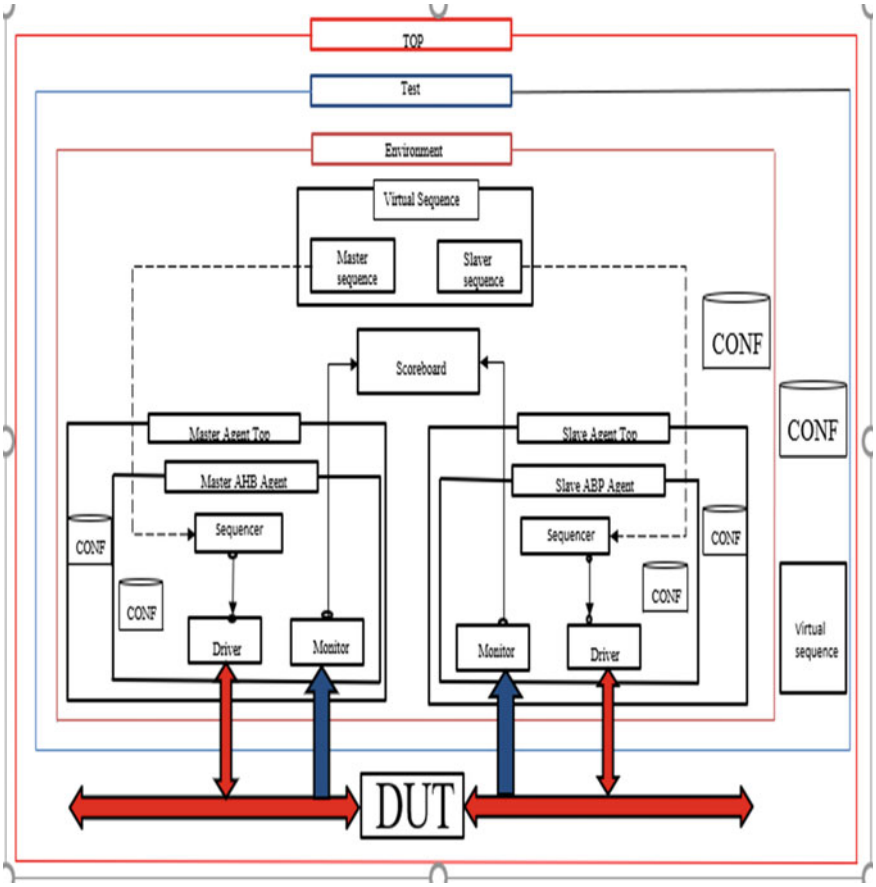

Fig. 4 AHB to APB bridge verification TB architecture

of the verification strategy. A condition and a message to be displayed upon test termination make up an assertion. More DUT features are tested the more claims there are. Assertions shorten the test's simulation runtime because they operate in parallel. It is possible to write coverage for assertion. This will determine how frequently the case relevant to the assertion condition appears. Assertions and coverage groups both belong in a good verification test bench.

Building test scenarios that feed inputs of various formats into the DUT in accordance with protocol and then verify output allows for the correctness of the AHB2APB bridge to be validated. In Chap. 4.2, the scenarios that were created to test the functions are mentioned.

B. Assertion based Verification Plan

For verification of design testbench is built using system Verilog/UVM. This test bench is a setting that provides stimuli for the design being tested (DUT). The

verification is done using a reference model that implements the DUT capability, and whose outcomes are considered as expected output for any given set of inputs. The DUT's results are contrasted with those of the reference model.

Establishing a directed test bench is the conventional method of the aforesaid verification methodology. Verification engineers can only attempt to validate the design using this directed test bench by sending a small number of essential sets of inputs to the DUT. Random stimuli are required in order to take into account all the unlikely-corner cases as well. Some kind of automated test bench environment that can generate random stimulus is required in order to employ random-stimuli. A group of semiconductor companies came up with the UVM standard verification approach as a result of this.

The main elements of the UVM test bench environment include a driver, monitor, sequencer, and scoreboard.

UVM provides a basic class for each component with standardized functions, allowing us to customize the test bench environment to meet our needs. Every part of the UVM test bench relies on data that is constantly flowing through the surrounding environment to function. This information is referred to as a sequence item, and it is essentially dynamic in nature. Reusability will be one of UVM's standout qualities. Any verification engineer with a solid grasp of the UVM approach may quickly comprehend the established test bench and make changes in accordance with his requirements.

Any test scenario can be verified using a variety of techniques, such as creating inputs, driving them at the correct clock cycle, obtaining outputs, and lastly comparing the inputs from the previous cycle with the output. The building of the appropriate test bench will enable these events to take place sequentially.

C. UVM-Based Test Bench Architecture

Test bench Top: The UVM test bench includes the interface instantiation that connects the DUT with the UVM test bench as well as the design instantiation that needs to be verified. Transaction Level Modeling (TLM) techniques are used in UVM to connect components. A UVM test that compiles the test bench all at once and performs several tests linked to it is called during runtime.

Bridge Test: UVM Test is the top-level component class that is located under the UVM test bench. In this class, UVM sequences are called to provide the design under test with the necessary stimuli. Value configuration is possible using configuration classes.

Bridge Environment: This container component class contains all verification components, such as scoreboards and agents, organized according to hierarchy. This environment class aims to encompass all design-focused lower-level verification components. UVM test allows you to modify the UVM environment's default settings.

AHB Agent: Agent comprises of low-level class like sequencer, driver, and monitor.

APB Agent: The UVM class hierarchy's lowest and most basic level is the sequence item class. This class adds the ability to define transaction items with

or without limitations to the UVM object class. In order for the sequencer class to communicate the defined transactions to the driver, this class is essential.

The UVM object class, which is intended to produce and randomize a set or collection of transactions as defined by the sequence items class, is extended by the bridge sequence class. To the UVM sequencer, which subsequently delivers it to the driver, are sent the created transactions.

AHB Sequencer: The sequencer makes the UVM component longer. The sequence and the driver communicate with one another through the sequencer. By adhering to the handshake procedures between the sequence and the driver, it passes transaction items.

Driver for UVM: The UVM component is expanded by the UVM driver. By transforming the transaction into a pin signal, it forces the transactions into the DUT. Get next item (), item done (), and other methods are used to receive transaction items.

AHB Monitor: The UVM monitor extends the UVM component. It converts the output pin signals of DUT into a transaction item and sends it to the scoreboard component for comparison with golden responses.

5 Results and Optimization

This session presents the findings of the functional simulation of the AHP2APB bridge module. The AHP2APB bridge top-level module and all of its submodules were created in Verilog-Hardware Description Language (Verilog-HDL), and they were all tested first on a conventional Verilog-HDL test bench and then on a UVM test bench. Having constructed a test bench in UVM. Using UVM approaches, the Bridge is implemented for the functional verification for both read and write operations.

The RTL design's functional verification by the Bridge results in complete code and functional coverage. Bridge Functional Verification Using UVM because verification methodology is a crucial part of circuit design. For the RTL design, the read operation of the Bridge is completed in XILINX, and the verification techniques are completed in Questasim Verilog is used for the design, and UVM is used for the verification. The Bridge is configured as a DUT and functional verification, and 100 percent code coverage are attained. From the Fig. 5 the signal HRESETn is the reset, it is the only active LOW signal in AMBA AHB, and it is the primary reset for all the bus elements. The reset may be asserted asynchronously but deserted synchronous with the rising edge of HCLK. HTRANS indicates the type of transfer. Every transfer can be classified into four different types that are Ideal, busy, Sequential, and non-sequential. The HSIZE indicates the size of the transfer.

A. UVM-Based Test Bench Architecture

Scoreboard is a class that extends from UVM Component, where we obtain inputs and outputs from Input monitor and Output monitor respectively, and then compare the output.

```
#Width = 32, size 16 bits
#-----------------------------------------------------------------------------------------------------------------------
# Name                          Type Size Value          Size          Value
# ----------------------------------------------------------------------------------------------------------------------
  #   req                       ahb_xtn   -   @1094
  #       begin time            time      64  1060
  #       end_time              time      64  1060
  #       depth                 int       32  `d2
  #       Parent sequence (name) string   7   wr_seqs
  #       parent sequence (fullname) string 49 uvm_test_top.env_h.ahb_agt_top.agent.sr_h.wr_seqs
  #       sequencer             string    41  uvm_test_top.env_h.ahb_agt_top.agent.sr_h
  #       HRESETn               integral  1   `d0
  #       HTRANS                integral  2   3
  #       HBURST                integral  3   5
  #       HSIZE                 integral  3   `d1
  #       HWRITE                integral  1   1
  #       HADDR                 integral  32  `h80002e4
  #       HWDATA                integral  32  `hfcb73cd2
  #       HRDATA                integral  32  `h0
#-----------------------------------------------------------------------------------------------------------------------
```

Fig. 5 Test bench topology

```
#-----------------------------------------------------------------------------------------------------------------------
# Name                          Type       Size   Value
# ----------------------------------------------------------------------------------------------------------------------
  #   xtn                       ahb_xtn    -    @1216
  #       HRESETn               integral   1    `d0
  #       HTRANS                integral   2    3
  #       HBURST                integral   3    `d0
  #       HSIZE                 integral   3    `d1
  #       HWRITE                integral   1    1
  #       HADDR                 integral   32   `h80000268
  #       HWDATA                integral   32   `hfda8eb57
  #       HRDATA                integral   32   `h0
  #-----------------------------------------------------------------------------------------------------------------------
  #UVM_INFO ../ahb_master_agent/ahb_monitor.sv(84) @1100: UVM_test_top_env_h.ahb_agent_top.agent.mr_h [AHB
#MONITOR] addr=2147484264 ,write data = 4255705943, read data = 0
#UVM_INFO ../tb/bridge_scoreboard.sv(113)  @1180:uvm_test_top.env_h.sb [SB] Inside run phase
```

Fig. 6 Scoreboard result

Data from monitor class is received into scoreboard. Inputs and Outputs are printed in the transcript. Here the Input fed to the DUT in the first cycle is stored in the register. The write-transfer-from AHB to APB can occur with zero wait-states. The initial transfer is the start of a burst and therefore is non-sequential. The bridge is responsible for sampling the address, transfer of data from AHB to peripherals through APB, and holding the value for the duration of APB write transfer. Initially when HADDR gets the address value. Hwrite signal is 1 then HWDATA is broadcasted on the data bus. The above Fig. 5.1 is the packet generated at the AHB bus. Initially, reset signal will reset the bus and the HTRANS transfer type will be sequential. Burst is set for a single transfer. The HWRITE signal is set to 1 so that write single is enabled for write operation. And HADDR is the address broadcasted on the address bus. HWDATA is the write data bus, driven by the bus-master during write transfers. HRDTAT is the read data bus driven by the appropriate slave during read transfers. The generated data HWDATA = 'hfcb73cd2 is transferred from AHB to APB through Bridge.

Figure 7 represents the packet received by APB. Whenever the data transfer is to be done PSELX signal indicated the slave selection for data transfer. PSELX is 0, and PENABLE is asserted. During the state transition from SETUP to enable the address, write and select–signals are maintained stable. For APB write access the PWRITE is maintained to High. The data and the address from the APB are same as the data and address in AHB. So transaction is successful.

After running the test cases for multiple times and if the test gets passed in all the iterations, then TEST CASE PASS message will be displayed as shown in Fig. 5.3 else TEST CASE FAIL message will be displayed.

```
#width 32, size 16 bits
#UVM_INFO ../apb_slave_agent/apb_monitor.sv(100) @1180: UVM_test_top_env_h.apb_agent_top.agent.mr_h [APB
#MONITOR] APB TRANSFER RECEIVED BY APB MONITOR IS
#--------------------------------------------------------------------------------------------------------
# Name                    Type        Size  Value
#--------------------------------------------------------------------------------------------------------
  #  xtn                  ahb_xtn     -     @1220
  #      PSELx            integral    3     `d1
  #      PENABLE          integral    1     1
  #      PWRITE           integral    1     1
  #      PADDR            integral    32    `h80000268
  #      PWDATA           integral    32    `hfda8eb57
  #      PRDATA           integral    32    `h0
  #--------------------------------------------------------------------------------------------------------
Transaction Successful
ahb monitor write/read  add 00000268
apb monitor write/read  add 00000268
ahb monitor write/read  data 0000eb57
apb monitor write/read  data 0000eb57
```

Fig. 7 Transaction packet in AHB

```
#  UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 647: reporter [TEST_DONE] 'run' phase is
   ready to proceed to the 'extract' phase
#  UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 647: reporter [TEST_DONE] 'run' phase is
   ready to proceed to the 'extract' phase
#  -- UVM Report Summary ---
#
#  ** Report counts by severity
#  UVM_INFO : 14
#  UVM_WARNING : 0
#  UVM_ERROR :0
#  UVM_FATAL :0
#  * Report counts by id
#  [AHB MONITOR] : 3
#  [APB MONITOR] : 3
#  [APB DRIVER] : 1
#  [Quest UVM] : 2
#  [RNTST] : 1
#  [SB] :3
#  [TEST DONE]  1
#  ** Note: $finish : C:/questasim64_10.7c/win64/../verilog_src/uvm-1.1d/src/base/uvm_root.svh(430)
#  Time: 580 ns Iteration: 69 Instance: /TOP
#  Saving coverage database on exit
```

Fig. 8 Base test result

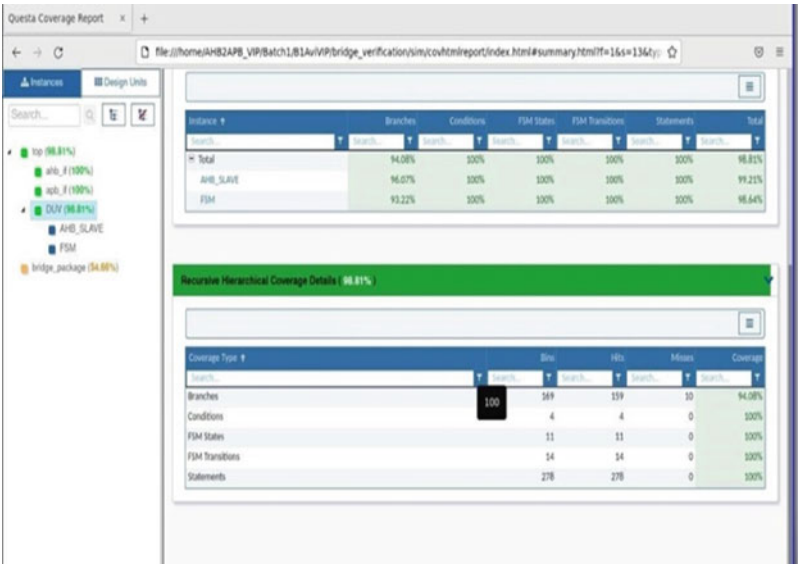

Fig. 9 Code coverage

Coverage Report

The overall code coverage is 98.81 percent while the branches, conditions, FSM states, FSM branch and statements are 94.08 percent. Hence, this proves the design of an AHB2APB bridge is tested for all cases.

6 Conclusion

The proposed work shows the methodologies to construct and test the AHB2APB Bridge. The code coverage for RTL design is acquired, and 98.81 percent of the code coverage and 100 percent of the functional coverage are recovered. The methodology offers full RTL design coverage in order to produce a bridge protocol design that is error-free. Therefore, it can be integrated into a real-time system. Additional implementation of this is possible for SOC and ASIC applications. Future work will involve implementing an interface between various AMBA protocols and APB.

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Design and Verification of AMBA AHB Protocol Using UVM

Spoorthi Kumari and Prabha Niranjan

Abstract SOC's have multiple blocks integrated on a single chip, to interact between these blocks, on-chip bus architecture is required. ARM's AMBA (Advanced Microcontroller Bus Architecture) is one of the extensively used on-chip architecture used in the VLSI industry. AHB (Advanced High-Performance Bus) is an AMBA Bus protocol with high-performance, supports multiple masters and multiple slaves and has wider bandwidth; as a result of these features, AHB is generally used in SOC's. Previously, AHB design was verified using either Verilog or system Verilog, where the time spent on verification was more than the time spent on design. A more effective verification methodology, like UVM (Universal Verification Methodology), must be adopted to reduce the average time spent in verification and increase efficiency. An AHB protocol with one master and three slaves is designed in ModelSim using Verilog and verified in QuestaSim using UVM, and a coverage report is generated. QuestaSim and ModelSim are the EDA tools developed by Mentor Graphics for design and verification purposes.

Keywords SOC · AMBA · AHB · Verilog HDL · UVM

1 Introduction

ARM established the open standard bus architecture known as AMBA, which is commonly utilized for on-chip bus systems. The purpose of AMBA is to reduce the design by enabling the usage of replaceable parts inside the SoC. The AMBA includes bus types like APB (Advanced Peripheral Bus), ASB (Advanced System Bus), AHB (Advanced High-performance Bus) and AXI (Advanced Extensible Interface).

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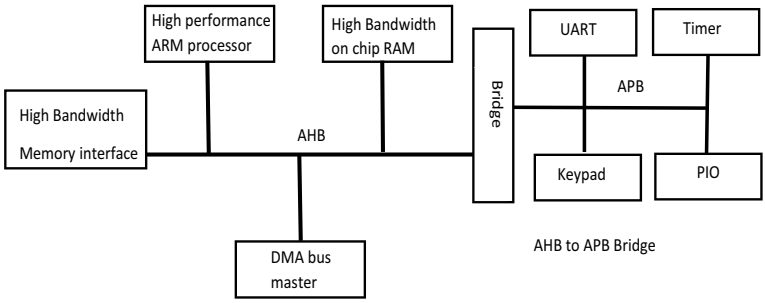

Fig. 1 AMBA AHB block diagram [1]

AHB is designed to address the requirements of high-performance, high bandwidth synthesizable systems [1].

AMBA AHB includes the following characteristics:

- Burst operation
- Split transaction
- Single-cycle bus master handover
- Single-clock edge operation
- Non-trivial implementation
- Supports up to 128-bit bus configuration

Figure 1 shows the AMBA AHB block architecture, which comprises of high-performance devices like on-chip RAM, memory interface and DMA (Direct Memory Access) all connected through an AHB Bus. On the other side, APB (Advanced Peripheral Bus) connects the low bandwidth peripheral devices like UARTs, PIOs, keypads, and timers. A central bridge connects the high-performance bus to the peripheral bus, allowing signals from on-chip devices to be transmitted to peripheral devices.

The work aims to design an AMBA AHB Protocol with one master and three slaves using Verilog HDL and verify the design using UVM.

The paper is structured as follows. Section 2 includes a literature survey on different AMBA AHB verification methodologies. Section 3 describes the design methodology. Section 4 explains the verification methodology. Section 5 describes the simulation results, and Sect. 6 concludes the work with the final analysis.

2 Literature Review

AHB system with three masters and four slaves designed and verified in ModelSim using system Verilog assertions. Where AHB attributes and corner case properties were evaluated, yielding a total coverage report of 80.3% with 20 system Verilog assertions [2].

AHB Single Master Single Slave, Single Master Multi slave, and Multi Master Single Slave were designed and verified in ModelSim using System Verilog [3]. By developing a Verification environment, a comparison was made between Verilog and System Verilog verification methodologies. The comparison revealed that the System Verilog Verification approach produced more accurate results than Verilog.

An AHB protocol was designed using Verilog and verified using system Verilog in QuestaSim [4]. Where the design under test was verified, and coverage report of nearly 65% was generated.

Using a Xilinx simulator, AMBA AHB was designed and verified for simple write and read operations with basic examples using Verilog [5].

AHB system with three masters and four slaves was designed and implemented in Verilog HDL using Xilinx ISE 14.6 [6]. Random combinations of masters and slaves were given to incremental burst operations of four, eight, and sixteen beats.

UVM was used to verify the AHB Protocol, which was built for three masters and four slaves. According to the UVM study conducted, the results obtained were more precise [7].

A single master single slave and multi master multi slave AHB system was designed and verified in ModelSim using UVM (Universal Verification Methodology) [8]. By interfacing STM32 controller, the performance latency of the AHB bus and the baud rate of the USART peripheral were measured which provided 100% functionally corrected output for UVM verification.

To speed up the verification process, a generic and reusable verification environment for SoC buses was developed. When compared to previous methodologies, the recommended methodology reduced verification costs and speeds the verification process [9].

AMBA AHB system was designed with three masters and three slaves, and was verified using both system Verilog and UVM (Universal Verification Methodology) in QuestaSim. Both verification approaches generated coverage reports, with UVM yielding a higher level of coverage than System Verilog [10].

The majority of the relevant work done in the preceding review is on Verilog hardware descriptive language and System Verilog. Along with the design, more work needs to be done in the verification process by using improved verification methodologies.

3 Design Methodology

AMBA AHB architecture with one master and three slaves is shown in Fig. 2, where the master is provided with the bus address, control information and data. The master sends the address to the decoder through the HADDR signal; the decoder broadcasts this address to all of the slaves in the system. The slave with this address will respond to the decoder by turning on its HSELx signal.

Once the HSELx signal is HIGH, the master will begin transferring data to that slave based on the HTRANS signal, which determines the mode of transfer as shown

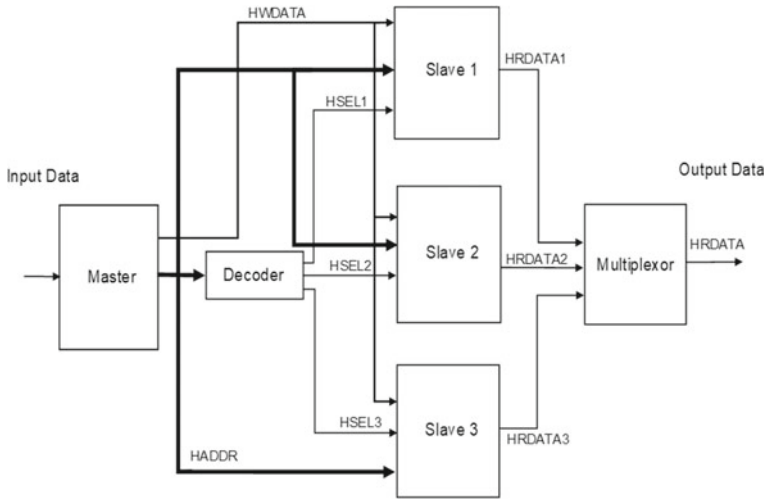

Fig. 2 AMBA AHB with one master and three slaves

in Table 1, where there are four data transfer modes IDLE, BUSY, NON-SEQ, and SEQ. The SEQ mode data transfer is dependent on burst operations, like incrementing or Wrapping burst. Once the transfer mode is selected HWRITE signal is used to execute the Write or Read operation.

When the HWRITE signal is HIGH, data is written to the slave, and when the HWRITE signal is LOW, data is read from the slave. After completing the Write or Read, the response, i.e., the HRDATA signal from all slaves, is received and sent to the multiplexer. The multiplexer will multiplex these signals and transmit the HRDATA along with the HRESP signal to master, stating that the data transaction has been completed.

Table 1 Transfer modes of AHB

HTRANS [1:0]	Type	Description
00	IDLE	Master is given access to the bus but does not intend to execute any data transfer. IDLE transfers will be rejected by slaves
01	BUSY	Master includes IDLE state between transfer of burst, indicating that master is already processing bursts of data and is unable to handle the next data immediately
10	NON-SEQ	Initial transfer in a burst or single transfer
11	SEQ	The succeeding transfer in a burst, where the address is the previous transfer's address plus the size (in bytes)

4 Verification Methodology

In VLSI industry large number of chips are being produced every year with a greater number of features. As all features in a chip must be verified before the specified Time to Market, the verification speed has to be increased. This is achieved through the use of a better verification language and a faster verification methodology.

UVM is an IEEE 1800.2 standard since 2017 which was developed by Synopsis in 2010. It is a hybrid of two methodologies: OVM (Open Verification Methodology) and VMM (Verification Methodology Manual). UVM is basically a set of classes defined in the System Verilog language. UVM is a new technology used for verification that is supported by the majority of EDA vendors and extensively accepted in the VLSI industry. UVM minimizes the work of constructing a standard testbench, and also verification components of UVM could be reused across multiple designs.

A. Components of UVM

Figure 3, illustrates a UVM verification environment that includes an interface connected to a DUT with a testbench, agent, generator, driver and monitor forming the subcomponents of the test bench.

(1) Generator: It generates a set of randomized data (where range of random data is specified by the *use of assertions) for randomization test or a single data which will be sent to the driver.*
(2) Transaction: moves data from generator to driver and also from monitor to scoreboard. Generated by extending UVM_Sequence_item.
(3) Driver: Driver produces stimulus and sends to DUT (Design under Test) through the interface. This is generated by extending UVM_component class.

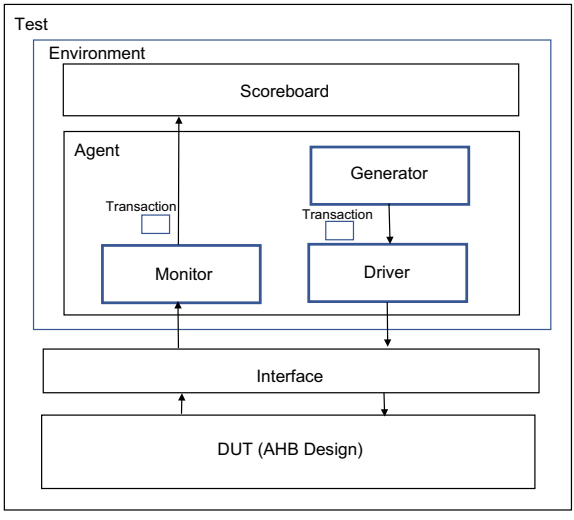

Fig. 3 UVM verification environment

(4) Agent: The agent consists of the verification components like driver, monitor, and generator which are connected using TLM (Transaction Level Modeling) connections. This is generated by extending UVM_ component class.
(5) Interface: It connects driver and monitor to DUT.
(6) Monitor: Receives random or single output from DUT. Derived from UVM_component class.
(7) Environment: Generator, agents, driver and monitor are together placed inside the environment.
(8) DUT (Design Under Test): DUT is the actual design which has to be verified.
(9) Reference Model: This is constructed in case of randomization test to determine whether the random output from DUT is valid.
(10) Scoreboard: It collects the DUT output from the monitor and the output from the reference model and compares both the outputs to check whether DUT outputs are valid.
(11) Testbench: It consists of the test cases. It is generated by UVM_component class.

B. Verification Flow:

The verification can be done in two ways,

1. Directed Test.
2. Randomization Test.

In directed test, single input data is generated and given to the DUT, to obtain respective output. If we have multiple testcases, it is time consuming to check the output for each input data given. So, a set of random data is given as input, and output is determined, this process is called as randomization. As shown in Fig. 4, random data is generated from the generator, this random data is then passed to the driver through transactions, this is called as transaction level modeling (TLM). The driver will send this data along with the instructions to be performed through the interface to the DUT. In DUT, the data is executed and random output is obtained and this is sent to the monitor. To verify the result, a reference model is constructed, which has the same functionality as of the DUT, reference model also takes the random data and produces output. The output from monitor and reference model is given to scoreboard to check whether the results are matching. If it matches, the data has been successfully transferred from slave to master.

The scoreboard results contain the following.

(1) Checker: Where assertions are inserted to check whether design is functioning proper or not.

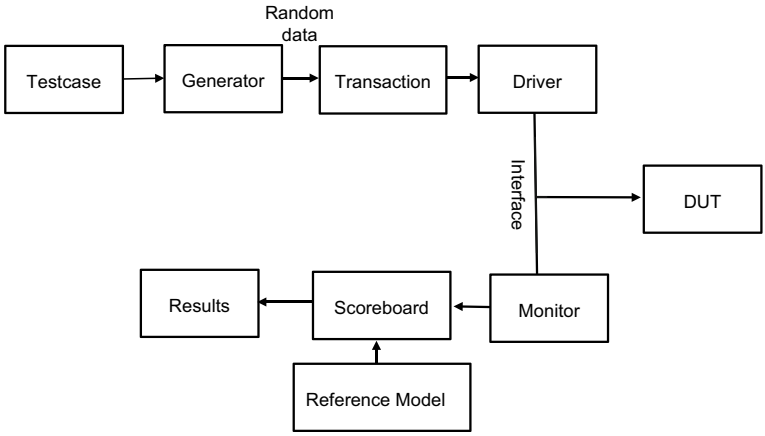

Fig. 4 Verification Flow

(2) Coverage: Coverage is classified into two categories.

- *Code coverage:* The percentage of code that was generated during verification. It can help in locating dead code and false paths, that are not generated for any given combination of inputs.
- *Functional coverage*: Indicates the percentage of successful transactions.

5 Results and Discussion

A. Decoding:

In the first case, the address given by the master is 32' h0034, the slave 1 has this address in its memory so the slave 1 is activated by making its HSEL1 signal HIGH as shown in Fig. 5.

In the second case the address 32'h0054 given by the master matches with address present in slave 2, Hence slave 2 is activated by making HSEL2 signal HIGH and Slave 3 will be having the address 32'h0094 in its memory list, so it is activated by making HSEL3 as HIGH.

B. Data Transfer from Master to Slave 1:

When the HWRITE signal goes HIGH, the data 05 h given by the master, is written to the address 34 h present in the memory of slave 1 as shown in Fig. 6. When the HWRITE signal goes LOW, the data which was written into the slave memory is read back which is shown in Fig. 7.

C. Verification Results

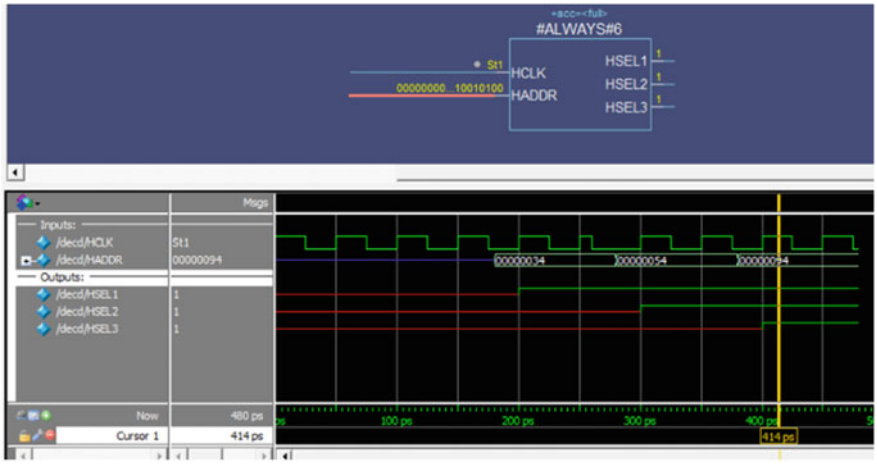

Fig. 5 Decoder Output

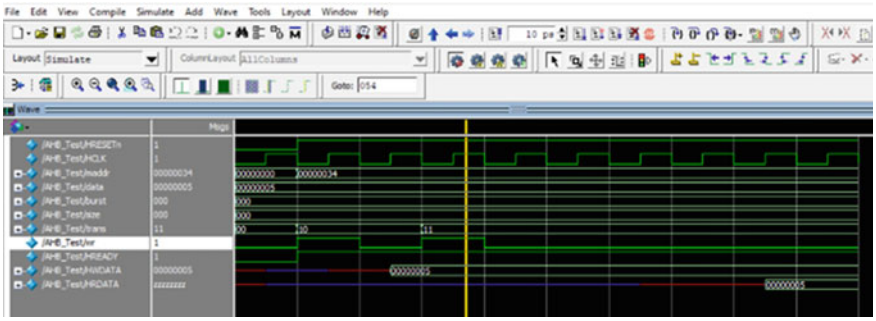

Fig. 6 Output of AHB write and read

The verification results obtained from the scoreboard shown in Fig. 8 show that the output obtained from the DUT and reference model for a random input data is matching, this indicates that the design is generating 100% functionally corrected output.

Figure 9, shows the coverage report where Coverage obtained around 96.8%, which shows that most of the test cases are being covered by this method.

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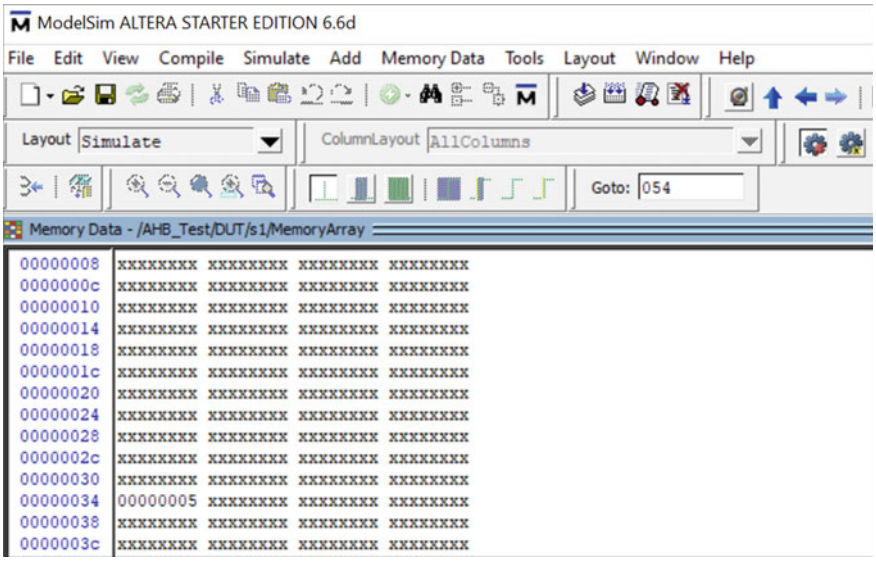

Fig. 7 Internal Memory of Slave 1

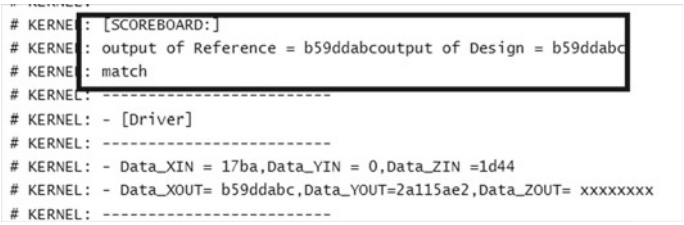

Fig. 8 Scoreboard Results

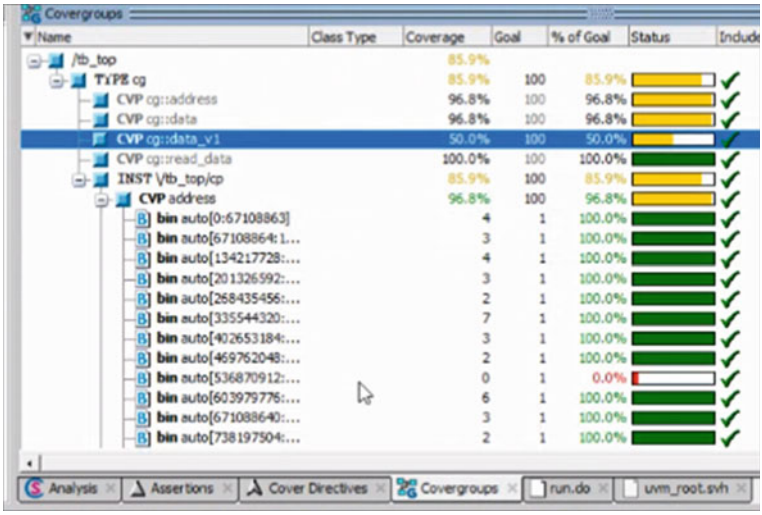

Fig. 9 Coverage Results

6 Conclusion

This work gives an overview of the AMBA AHB bus protocol, designed with one master and three slaves. The AHB design is implemented in ModelSim tool using Verilog and verified in QuestaSim using Universal Verification Methodology. To verify the exact working and functionality of the design, the entire design is tested under all possible cases in accordance to its specification. The coverage report of 96.8% is obtained from this verification methodology which gives better coverage compared to that of other verification methodologies. In the present work conducted AHB is designed, with one master and three slaves. In future one can design an AHB with 16 masters and 16 slaves and also UVM methodology could be used to verify other buses like APB, AXI, DMA etc.

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Dictowriter: Speech to Text Plotter

G. K. Dayanad, Akshatha G. Baliga, I. R. Manjunatha, and Bharath H. Kamath

Abstract People with impairments struggle harder in both daily life and academic settings. Students who are physically or visually challenged find it challenging to navigate an increasingly complicated world. Understanding the requirements of students with disabilities and the ways in which technology might be used to assist them is crucial. They can overcome obstacles and achieve better outcomes in both education and daily life with the aid of assistive technologies, which comprise both software and hardware. In this paper, a solution for physically disabled persons, a voice-activated plotter, which recognizes the speech and writes down the spoken content on the paper at a speed closer to average human writing speed is developed. This work on a speed of 10 WPM, which is closer to the Average human speed i.e. 13 WPM is archived.

Keywords Phython · G-Code · Arduino IDE · Raspberry Pi · WPM (words per minute) Raspbian OS

1 Introduction

This paper focuses on the problems faced by visually impaired and physically disabled students and the need for the development of assistive devices like this to tackle these problems. It is aimed at building a Raspberry Pi based voice-activated plotter capable of recognizing speech, converting it to G-code and write down the spoken content on paper with increased speed and improved user experience.

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2 Literature Survey

In paper [1], the authors discussed developing Speech to Text Machine. This machine is a portable machine, that operates in two axis of motion i.e., X–Y axis. It uses a pen to plot on a flat surface. Its output is obtained with the help of stepper and servo motors, G-Code plays a major role in the successful operation of the CNC machine. The only code which understands the CNC machine. With the help of 'Bluetooth to G-code App' this conversion became easy through the Bluetooth module this code conversion is sent to the Arduino Uno controller which sends the commands or instructions to the motor drivers to perform the movement. And according to the task the data is plotted with the help of pen or chalk.

Implementation of 2D Plotter was presented in Ref. [2]. This paper presents demand for plotter machines in Educational Institutions such as blind student educational institutes. Affordable model of a plotter machine with the ability to write down spoken content was built. The Implementation method used here is appreciable because the spoken content needs to be converted into text file and sent to PC using Bluetooth. Later the text file was converted to G- code manually using Inkscape software and sent to the plotter. Hence this project does not automate all the processes involved and is difficult to be used by visually impaired.

Computerized Numerical Control (CNC) machines are used to design mechanical parts and draw anything in accordance with the design program that is given into their controller unit. Computers and microcontrollers are both examples of controller units. Stepper and servo motors are used by CNC machines to draw the design in accordance with the fed program. A programming language called G-code is used to instruct machines where and how to move. A compact, low-cost CNC plotter machine that can draw figures or pictures on a little sheet of paper is to be developed in Ref. [3]. It employs a servo motor on the Z-axis in addition to two stepper motors on each X and Y axis as linear drives. These three axes' proper synchronization with one another when printing or drawing is managed by the Arduino Uno microcontroller.

3 System Design

3.1 Software Overview

i. *Python 3.7*

A popular, all-purpose, high-level, interpreted dynamic programming language is Python. Programmers can convey concepts in less code and appreciate to its syntax when compared to languages like C++ or Java, which emphasize readability in code. Programming paradigms supported by Python include procedural, imperative, and object-oriented programming. It features an automatic memory management system,

a sizable standard library, and a dynamic system. We utilize Python 3.7 to create the software for our project.

ii. *G-Code*

A CNC programming language called G-code tells machines where to go and how to move. The G-code used by CNC machine manufacturers varies depending on the kind, make, and model. An instruction manual for each computer includes the particular machine code for each function. Geometric code, or "G-code," uses a variant of the alphanumeric model.

iii. *Arduino IDE*

Integrated Development Environment, or Arduino IDE, is a recognized program created by Arduino. cc that is primarily used for creating, compiling, and uploading code into Arduino hardware. The Arduino IDE has specific code organization guidelines to support the languages C and C++. The core code, sometimes referred to as a sketch, created by the IDE platform is delivered and downloaded to the board controller as a hex file. The two main elements of the IDE environment are the editor and compiler. The required code is created using the compiler after being written in the editor and then uploaded to the designated Arduino module.

iv. *Raspbian OS*

For the Raspberry Pi, Raspbian is an operating system that is based on Debian. It has been the primary operating system for the Raspberry Pi single-board computer family since 2015, according to the Raspberry Pi Foundation. Operating system development is still ongoing. The low-performance ARM CPUs of the Raspberry Pi family are well suited to Raspbian. Since the most recent release, Raspbian has used PIXEL, Pi Improved Xwindows Environment, and Lightweight, as its main desktop environment. It comprises of an altered version of the Openbox stack window manager and the LXDE desktop environment. The distribution comes with the most recent version of Chromium, a lightweight version of the computer algebra tool Mathematic, and a version of Minecraft dubbed Minecraft Pi.

v. *PyAudio Python Library*

PyAudio provides a Python binding for the PortAudio cross-platform audio I/O module. In order to use the Speech Recognition API, PyAudio must be installed. PyAudio makes it simple to play and record audio in Python on a variety of operating systems, including GNU/Linux, Windows, and Apple Mac OS X/macOS.

vi. *Speech Recognition Python Library*

A popular, all-purpose, high-level, interpreted dynamic A Python library called Speech Recognition is used to do speech recognition. It supports a number of online and offline engines and APIs. It utilizes speech recognition APIs including IBM Speech to Text, SnowboyHotword Detection (offline), CMU Sphinx (offline), Google Speech Recognition, Google Cloud Speech API, Wit.ai, Microsoft Bing Voice Recognition, Houndify API, and Google Speech Recognition to achieve outstanding results.

Fig. 1 Raspberry Pi 3

3.2 Hardware Overview

3.2.1 *Raspberry Pi 3B+*

The Raspberry Pi is a single-board computer the size of a credit card that runs Linux and has a set of GPIO pins for controlling electronic devices to explore the Internet of Things (IoT) (Fig. 1).

3.2.2 Motion Control Mechanism

The plotter has to move in both X and Y directions, mainly there are three travelling mechanisms: H-bot, T-bot and core XY. For this project we are implementing a core XY control mechanism to achieve the motion. Core XY is a technique of motion control in 2D axis using a single continuous belt for both the axes. The advantage of the core XY mechanism is that both the Y-axis motor as well as the X-axis motor are placed on the main chassis, which keeps the center of gravity closer to the chassis and reduces weight on X-axis mechanism as it need not carry heavy Y-axis stepper motor on it (Fig. 2).

3.2.3 X-Axis Assembly

Assemble X-axis carriage by placing 8 LM8UU bearings into the slots present in the 3D printed carriage mount and by placing 624ZZ hinged bearings into the screws mounted onto the carriage mount. Complete assembly of the X-axis by inserting the bottom part of carriage into the smooth rods and by inserting the X-axis mount at the other end. Finally mount the stepper motors at the two ends of the X-axis mount (Fig. 3).

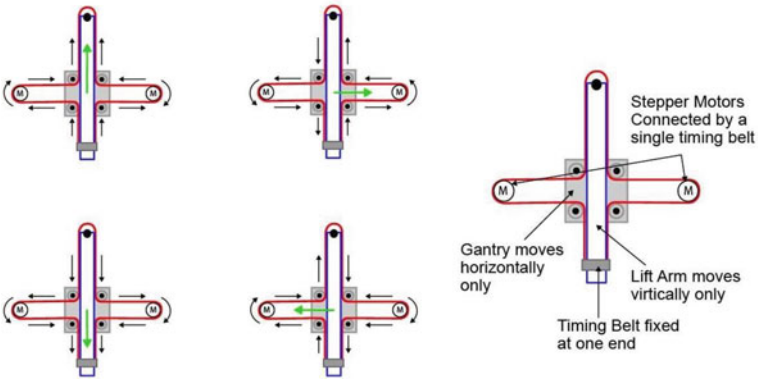

Fig. 2 Core XY motion control mechanism

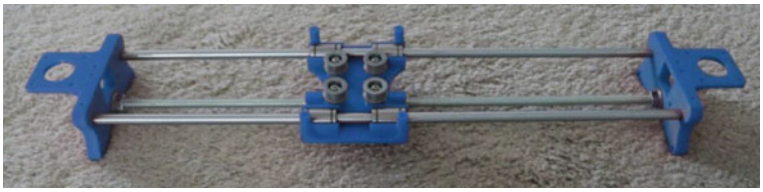

Fig. 3 X-axis assembly

3.2.4 Y-Axis Assembly

Insert 62ZZ bearings at one end of Y-axis mount by inserting a screw. Finally insert the belt through all the bearings running between bearings present in the carrier mount and Y-axis mount and lock the belt at the other (Fig. 4).

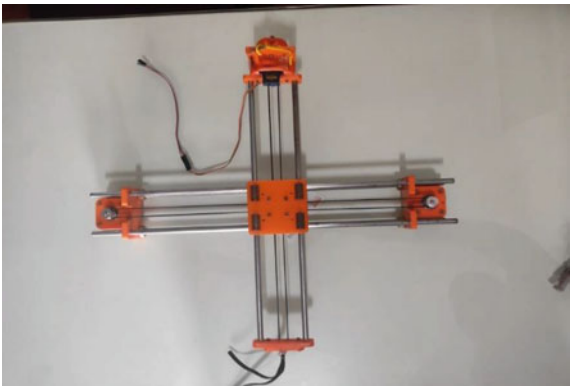

Fig. 4 Complete X-axis and Y-axis assembly

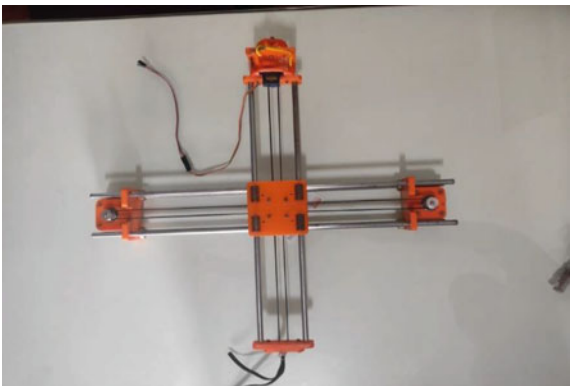

Fig. 5 Z-axis pen mount

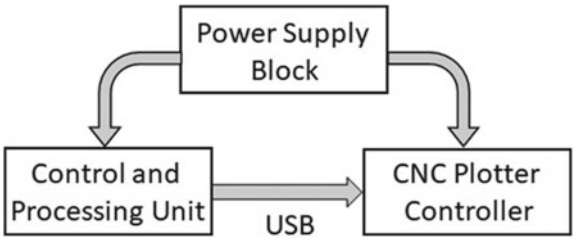

Fig. 6 Abstract block diagram of the system

3.2.5 Z-Axis Assembly

See Fig. 5.

4 Implementation

4.1 Hardware Implementation

Hardware implementation of the project is divided into three main blocks which are power supply block, control and processing unit and CNC plotter control unit. Abstract level block diagram of the system is shown in Fig. 6.

4.2 Control and Processing Unit

Raspberry Pi is the main component of the control and processing unit which receives user inputs and processes them in order to produce the outputs. Raspberry Pi accepts speech input from USB microphone, it also accepts inputs from user buttons to control

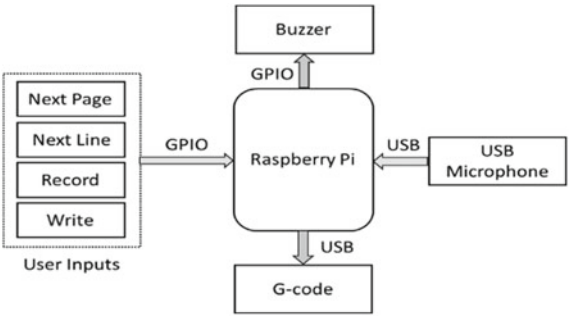

Fig. 7 Block diagram of control and processing unit

various actions of the system. USB microphone accepts the speech input from the user and sends it to Raspberry Pi which in turn processes the input to obtain the text. The text is converted to G-code and sent to Arduino via USB cable in order to control the CNC plotter. System accepts input from a user, process it and starts writing on paper. System also beeps the buzzer whenever a page is full which indicates the user to insert a new page and start writing (Fig. 7).

4.3 CNC Plotter Controller

The CNC plotter controller which receives G-code as input from Raspberry Pi and interprets the G-code to control the motion of CNC plotter. To achieve the motion in X-axis and Y-axis two stepper motors are used which are controlled by two A4988 stepper drivers and a servo motor is used to achieve the lifting action of the pen in the Z-axis (Fig. 8).

5 Results and Discussion

The proposed system ensures about starts recording speech once the user activates record button. If user pauses for 5 s in between speech gets uploaded to Google speech to text API and output text is appended into a file. Once text file gathers 40 characters (one line) G-code is generated for that line using the hf2gcode library and stored into a separate file. If write is activated the G-code is sent serially to the plotter and text is written on paper. The image of final setup of the proposed system in action is shown in Fig. 9.

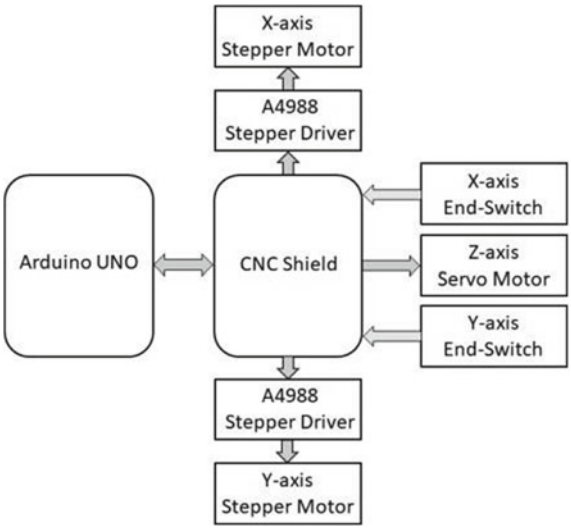

Fig. 8 Block diagram of CNC plotter controller

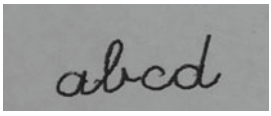

Fig. 9 Speech to text result plotted by the Dictowriter

5.1 Accuracy

System is checked for accuracy by dictating several sentences and the results have been tabulated in Table 1. Here speech to text module of the system is checked for the correctness of the text generated. Random text with random number of words has been dictated and tabulated against number of errors generated and percentage errors. However, we are using google speech to text API hence percentage error is quite low (Fig. 10).

Table 1 Results of accuracy test

Total words	Output errors	Percentage errors
254	15	6.0
78	4	5.0
156	9	5.5
312	15	5.0
213	11	5.0

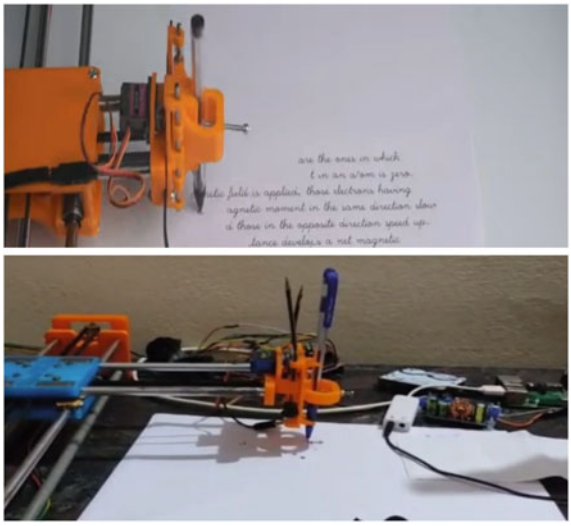

Fig. 10 Proposed system in action

5.2 Speed

The speed of the plotter plays an important role in actual implementation of the prototype into a product. Random text is dictated to the machine and tabulated versus writing time, words per minute. Average writing speed of an adult is around 68 letters per minute which is around 13 words per minute. The range of writing speed may vary between 5 and 20 words per minute in humans. Through this is initial stage of the prototype we have dared to compare the speed of this machine with human writing speed. The results have been shown in Table 2.

However, the results obtained from comparison have achieved around 50% efficiency when compared to human writing speed the speed can be increased by using high-quality stepper motors with greater seeds, by increasing the federate of the plotter and by using simple fonts (Table 3).

Table 2 Results of speed test

Total words	Output errors	Percentage errors
254	25	10.1
78	7	11.2
156	13	12.0
312	30	10.4
213	20	10.6

Table 3 Results of z-axis (movement)

Total words	Movement (z-axis)
10	20
7	10
5	16
15	33
12	28

6 Conclusion

A speech to text plotter has been proposed and a prototype has been developed. This project describes a detailed implementation of Raspberry Pi based speech to text plotter that has been built and tested. The output is obtained with the help of Arduino based X–Y plotter using the core XY motion control mechanism. Speech to text conversion is first step in designing this plotter which is achieved by using Speech Recognition library. Finally, the proposed system is tested for its speed and various steps have been followed to improve the writing seed of the system.

The font and feed rate play an important role in determining the speed of the system. If we increase the feed rate, then the text tends to be illegible but feed rate can be increased to achieve greater speeds. There are various single line fonts specially designed for CNC plotters. This project uses hf2gcode 0.3.0 library, which consists different fonts such as cursive, futural, futuram, gothgbt, gothgrt, gothiceng, gothicger, rowmand, rowmans, rowmant, script, scripts, symbolic, timesg, timesib, timesi, timesrb, timesr. But one of the limitations here, is that it is not possible to interface the symbols spoken during speech into symbols in the text file. Instead, if symbols are written manually, it can be plotted on the paper. Also, the starting letter of the sentence cannot be capitalized while spoken but can be done so manually.

Further this system finds applications in blind schools and schools for physically disabled children. This system can also be used to write examinations on behalf of physically disabled students.

Future Scope of this project can be done, by upgrading it to a wireless system wherein it works on a custom-built PCB which can be controlled/commanded.

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Classification Performance Analysis of CART and ID3 Decision Tree Classifiers on Remotely Sensed Data

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Abstract Classification is one of the most commonly employed techniques in remote sensing studies. The thematic maps generated by the RS data classification are employed in a diversity of socio-economic applications. With the advent of space technology, new diverse and advanced RS data are generated at a very high rate. In this study, we implement two decision tree based classification techniques; classification and regression trees (CART) and iterative dichotomizer (ID3), in classifying heterogenous multispectral RS data. The study uses two Landsat-8 study areas; the North Canara District boundary and Kumta Taluk boundary, in Karnataka India. We selected seven level-1 and level-2 LULC classes from Anderson's (Anderson, A land use and land cover classification system for use with remote sensor data, vol. 964. US Government Printing Office, 1976) classification system for each study area. Class separability is measured between each class pair using the Euclidean distance metric and severely overlapping classes are identified on each data. The paper also discusses different types of decision trees and their attribute selection measures. The results obtained indicate that CART and ID3 are excellent choices for separating severely overlapping spectral class pairs.

Keywords CART · ID3 · Remote sensing · Classification · Thematic map

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1 Introduction

Image classification, in the remote sensing (RS) viewpoint, is the method of allotting a land-use land-cover (LULC) identifier to each pixel on the image to generate a thematic map. A range of image classification algorithms is presented in the literature ranging from pixel-based, object-based, and scene-based techniques. Image classifiers are further categorized into supervised, unsupervised, and hybrid techniques. Among the plethora of algorithms presented, supervised classification techniques are the most generally employed techniques in RS studies.

An expert system classifier is a technique that involves the collection of information about the land surface of study in terms of hypothesis, conditions, and rules. These are then used to create a knowledge base that is then used to classify an RS image. One of the best ways to represent an expert system classifier is by building a decision tree structure. Decision trees are one of the normally used data mining techniques [2]. The objective is to create a target variable using one or more input variables. A decision tree is created by splitting the data that forms the root node into subsets that form the branches. The partition made follows a finite set of rules consisting of classification features [3]. By using recursive partitioning, data splitting is reiterated until convergence. The splitting is complete when a subset at a node is equal to the target variable's value. This is referred to as the Top-Down Induction of Decision Trees (TDIDT) [4].

A decision tree takes an object or image described by a set of rules, conditions, and hypotheses as input and returns a decision [4]. The attributes of input and output may be discrete or continuous. Learning a function that is discrete-valued is called classification learning. Learning a continuous-valued function is called regression [5, 6].

Decision trees are broadly categorized into two types: classification trees and regression trees. When the prediction result is a class to which the data belongs, classification tree analysis is employed. On the other hand, when the predicted result is a real number, regression tree analysis is employed. CART technique defined by Briemann et al. [7], is used to refer to both regression and classification. Although trees used for classification and regression have some resemblances, they vary in the technique used to decide where to divide the data.

When a decision tree is constructed for expert systems, data form the tree trunk, rules form the limbs of the tree, and conditions form the leaves. This construction is referred to as a hierarchical decision-tree classifier [8, 9]. Building decision trees as a hierarchical structure permit relating classes within the study area at different scales and different levels of detail [8, 10].

In the past 50 years, a diversity of approaches has been developed for constructing decision trees. For RS applications, where the data are well understood, classification trees may be defined based on the analyst's knowledge. Running et al. presented this approach in 1995 for classifying vegetation based on NDVI [11]. The data are split based on the training data. Such techniques are also referred to as learning algorithms [12]. This would demand the requirement of high-quality training data. One of the

examples of such an approach is the CART model presented by Briemann et al. [7]. At each node, CART repetitively splits the data using a selection attribute measure in such a way that, the homogeneity of the training data is increased in the resulting nodes. With such an approach, decision trees are shown to perform as well as the maximum likelihood classifier [13].

Based on the nature of the dataset and the test employed, a variety of factors are to be considered for constructing a tree [14]. These factors include how different data are handled by the estimation procedure [15], metrics used for measuring the quality of split [16], how mining data are handled [4], and the algorithm used for feature selection at internal nodes [17]. Generally, a decision tree will correctly classify all of the training data. If the training data itself contains errors, decision trees cause overfitting of the data and lead to poor results. Therefore, a suitable technique to correct the overfitting of the decision tree may be employed. This is called pruning the trees. This type of pruning can reduce classification errors. Different methods of pruning classification trees are discussed in [18, 19].

This study has a two-fold objective: (i) To classify Landsat-8 RS imagery using CART and ID3 decision tree based algorithms, and (ii) To assess the classification results of CART and ID3 algorithms in separating spectrally overlapping LULC classes. The rest of the article is structured as follows. Section II presents and explores the Landsat-8 RS data over its LULC class cover and their overlapping. Section III reviews the decision trees and their features. Section IV examines the decision tree attribute selection measures. Section V presents the methodology employed in this study. Section VI discusses the results of the classification studies conducted. Section VII presents the conclusions drawn from the results attained.

2 Study Areas

This study employs two Landsat-8 derived study areas for testing the selected classifiers. The primary study area, as shown in Fig. 1, is the boundary of North Canara District, Karnataka, India, and the secondary study area, as shown in Fig. 2, is the boundary of Kumta Taluk, Karnataka, India. To ensure both study areas exhibit similar LULC classes, the secondary study area is selected in such a way that, it is encompassed within the boundary of the primary study area.

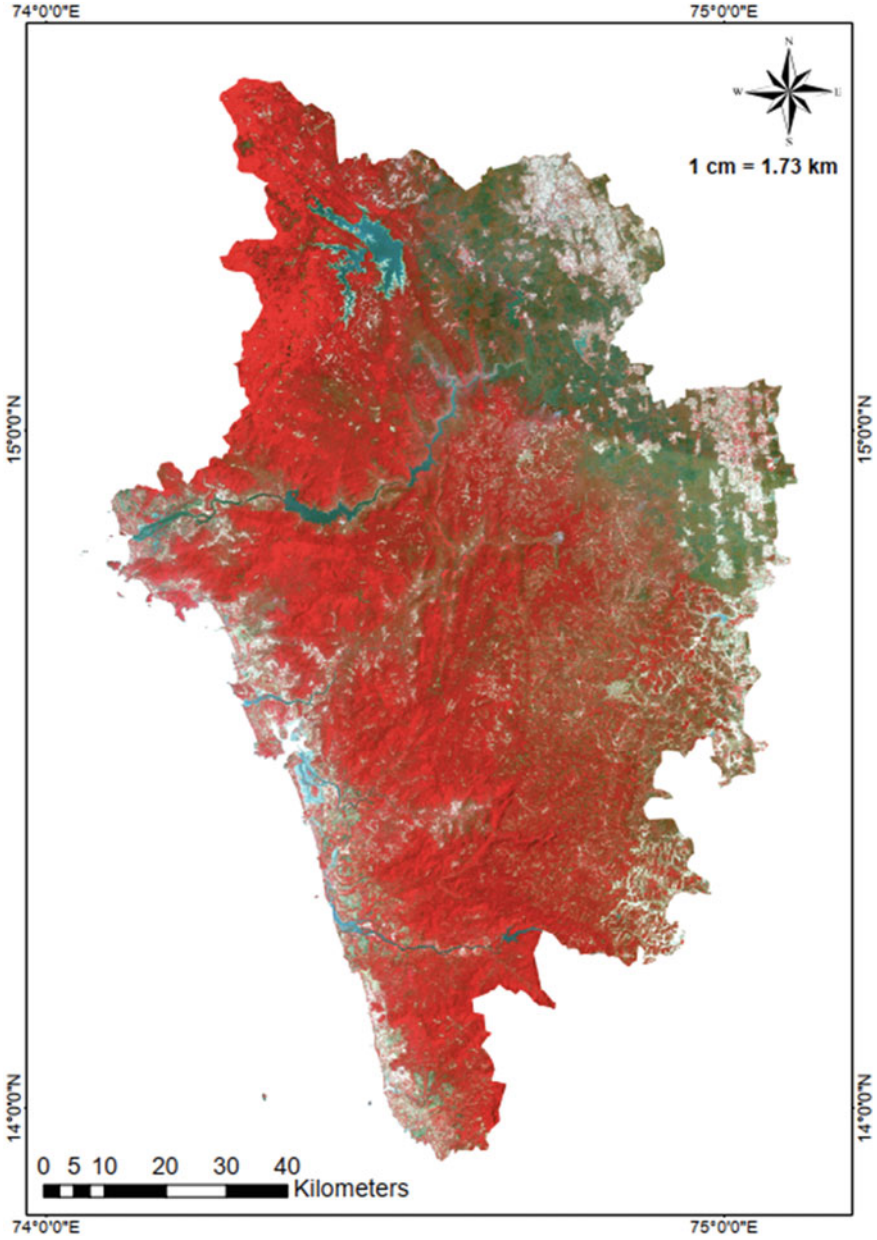

Fig. 1 Composite map of the North Canara District study area (Data courtesy: United States Geological Survey [20])

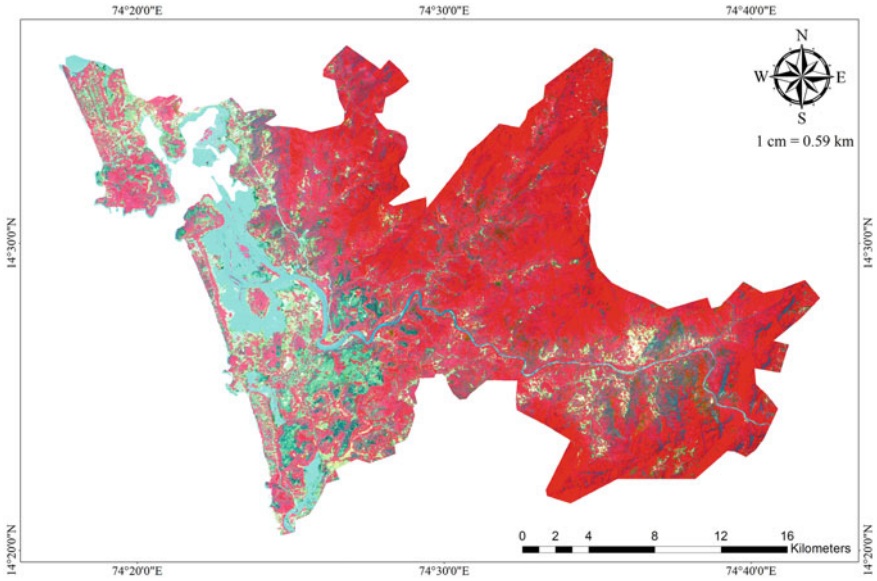

Fig. 2 Composite map of the Kumta Taluk study area (Data courtesy: United States Geological Survey [20])

3 Decision Trees

In this section, a brief overview is provided on the decision tree categorization followed by a discussion on attribute selection measures for the same. The section also analyses the CART and ID3 classification techniques employed in this study.

A. Decision Tree *Categorization*

Decision trees are divided into three types based on the features used and the feature selection methods applied. These are discussed as follows.

- *Univariate Decision Trees (UDTs):* UDTs are those that generate a tree at each node based on a single feature of the input data [21]. Until a leaf node is reached, the data is separated into subsets depending on a single input feature in this method. The class value of this leaf node is then assigned to that pixel or observation vector [12]. Breiman et al. [7] gave an example of such a technique for designing CART. This process for identifying LULC classes using Band 1 is shown in Fig. 3.
- *Multivariate Decision Trees (MDTs):* MDTs are those that split data using two or more input features. A set of linear discriminant functions is estimated at each node using the training data [12]. MDTs are generally more compact than UDTs while also being more accurate [14]. To estimate splitting rules at each node, MDTs can use a variety of techniques, including the pocket algorithm [22], explicit impurity reduction [7], recursive least squares [23], and thermal

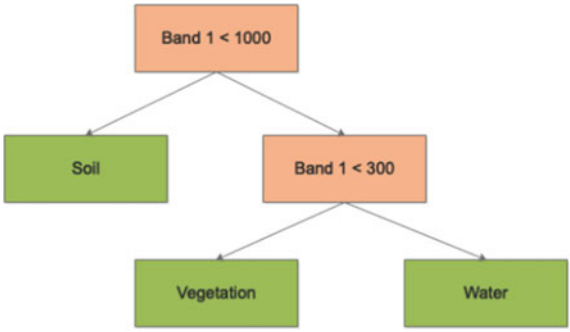

Fig. 3 An example of univariate decision tree

training [24]. These methods may yield variable results depending on the nature of the data and the classification task. Depending on the nature of the data and the classification job, these methods may produce varying outcomes. Due to the use of different splitting criteria at each node, MDTs are also more difficult to comprehend than UDTs [12].

Since MDTs use more than one feature to split data at each node, different feature selection algorithms can be used such as the sequential backward elimination (SBE) [17]. MDT is said to do feature selection at a local level rather than a global level in this situation [12]. Figure 4 shows a simple example of a multivariate decision tree.

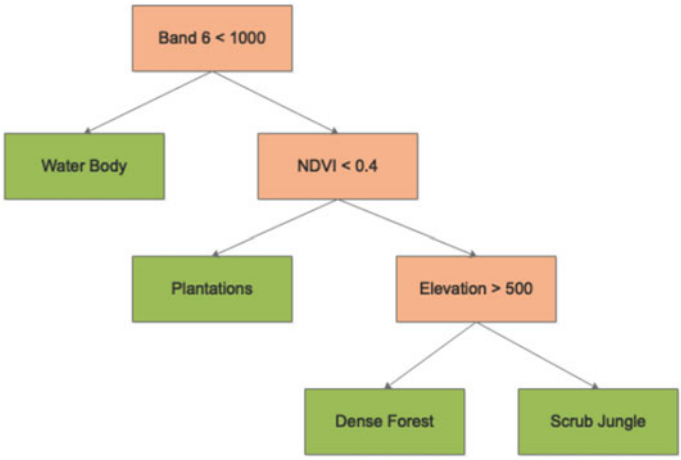

Fig. 4 An example of multivariate decision tree

- *Hybrid Decision Trees (HDTs):* HDTs can employ different classification techniques for different subtrees of a larger tree. Brodley [14] demonstrated the Model Class Selection (MCS) system, which can generate a hybrid classifier by combining up to three classifiers. HDT can take advantage of certain algorithms' inherent superiority in terms of performance [14].

B. Attribute Selection Measures

Attribute selection measures are used to split the data into subsets in the best possible way. The general idea would be to split the data at each node in such a way that the partition is pure i.e., all the pixels belonging to a partition are from the same class [25]. Such a partition will create the best splitting criteria. Attribute selection measures will determine how the data is split at each node and hence are also called splitting rules. The most frequently used attribute selection measures are; Gini index, Entropy (information gain), and information gain ratio. These measures are discussed in the following sections.

- *Gini Index*. Assume that the data $|T|$ is to be split into K target categories at node T. The Gini index at node T for some random variable X is defined as,

$$Gini(T) = \sum_{i=1}^{K} P_T(i)(1 - P_T(i)) = 1 - \sum_{i=1}^{K} P_T^2(i) \tag{1}$$

If the probability of occurrence of the class at node T is equal, the Gini index achieves the maximum value of (1 – 1/K). On the other hand, if there is only one class at node T, the Gini index achieves its minimum. The Gini index has a property that its value increases with impurity. To lower the impurity level, subnodes can be added [26]. For example, if subnode S is added to node T, the Gini index can be defined as,

$$Gini(S, T) = Gini(T) - p_L Gini(T_L) - p_R Gini(T_R) \tag{2}$$

where, p_L and p_R represent the proportion of cases in node T classified to T_L and T_R, respectively.

- *Information Gain*: The inclusive information at node T is given by [26],

$$Info(T) = -\sum_{i=1}^{K} P_T(i) log_2(P_T(i)) \tag{3}$$

The decision tree at node T is divided into two or more subnodes. Then the inclusive information can be expressed as,

$$Info(X, T) = \sum_{i=1}^{n} \frac{|T_i|}{T} Info(T_i) \tag{4}$$

Combining Eqs. (3) and (4) produces the information gain and is defined as,

$$Gain(X, T) = Info(T) - Info(X, T) \tag{5}$$

- *Information Gain Ratio:* To improve the application of the information gain concept, the information gain ratio was put forward [247] and is defined as,

$$Gain\ Ratio(X, T) = \frac{Gain(X, T)}{Split\ Info(X, T)} \tag{6}$$

where,

$$Split\ Info(X, T) = -\sum_{i=1}^{n} \frac{|T_i|}{T} log_2\left(\frac{|T_i|}{T}\right) \tag{7}$$

Information gain ratio was shown to be more preferable for continuous variables. Therefore, information gain ratio for a continuous variable with n distinct values is expressed as [27],

$$Gain(X, T) = Info(T) - Info(X, T) - log_2 \frac{(n-1)}{|T|} \tag{8}$$

C. Classification and Regression Trees (CART)

Breiman [7] introduced CART in 1984 and showed that it can be used for creating both classification and regression trees. The CART model uses a binary tree representation to build the decision tree. The root of the decision tree is the input variable (X) and represents the split point. Splitting the root node creates leaf nodes that represent the output variable (Y), which is used for making the prediction. The prediction making is rather straightforward for the CART model thus described. The decision tree is passed for new input by evaluating the same input started at the tree's root node. Every input parameter on the p-dimensional space can be viewed as a dimension. This space is divided into rectangles (for $p = 2$) or some sort of hyper-rectangles (for $p \geq 2$). When fresh data is entered into the decision tree, it is processed through the tree until it reaches one of the rectangles, where the output value for that rectangle represents the model's prediction. A greedy algorithm is used to pick the optimal input variable and define the split-point. This role is done by the greedy algorithm by reducing the cost function. A predetermined stop condition, such as a minimum number of training cases allotted to each tree leaf node, can be used to end the decision tree construction.

Advantages of CART include: handling missing data values using surrogate splits, automatic feature selection, using any combination of continuous/discrete variables, establishing interactions among variables, and is not affected by the monotonic transformation of predictive variables [28].

- Greedy Splitting: CART uses a recursive method of binary splitting to divide the input space of each node. This algorithm selects the best split point at each node in a greedy way. The minimized cost function to identify split points for recursive problems is the cumulative squared error across all rectangle training samples. Gini index is used as the value function of classification problems. The recursive binary splitting method works down the tree and needs to be told about the stop criterion. The most common stop criterion is to assign the minimum number of training instances to each leaf node. If at a node, the number of training instances is less than the minimum number, that node is considered to be the final leaf node and there is no splitting.
- Pruning the Tree: The number of splits within a decision tree is used to determine its complexity. Simpler trees are recommended because they are less likely to overfit the data and are easier to comprehend. Pruning can be performed to boost CART's performance. The easiest and simplest pruning strategy is to work through each leaf node in the tree with a hold-out test set and evaluate the effect of eliminating that node. If and only if the full test set results in a drop in the overall cost function, a leaf node can be eliminated. This process will be repeated until no additional improvements can be made.

D. Iterative Dichotomiser 3 (ID3)

Ross Quinlan [32] is the developer of ID3. ID3 is a top-down technique in which each node's attribute is chosen to create the optimal data classification [33]. ID3 divides the data at each node using information gain as the selection attribute measure and selecting the characteristic that generates the most information gain. ID3 is preferred when constructing smaller decision trees and is a heuristic algorithm. Decision trees constructed based on ID3 only accept categorical attributes. To produce accurate results, ID3 requires the data to be preprocessed and is sensitive to noise [29]. The ID3 algorithm starts with the original set S at the root node. On each iteration of the algorithm, it iterates through every unused attribute of the set S and calculates the entropy H(S) or information gain IG(S) of that attribute. The property with the lower entropy value is then chosen (or the greatest gain of information). Then after, the set S will be split to create subsets of the data based on the chosen attribute. A node, for example, can be split into child nodes depending on sub-population ages of under 50 years, 50 to 100 years, and over 100 years. The algorithm iterates over each subset, taking into account only attributes that have never been chosen before.

Recursion on a subset may stop in one of the following cases;

- Each subset element belongs to the same class; in this instance, the node is marked with the class of examples and becomes a leaf node.

- There are no more attributes to pick from, but the samples are not yet in the same category. In this situation, the node is labeled with the most common class of instances in the subset and becomes a leaf node.
- When no occurrence of a given value of the specified attribute is found in the parent array, there are no instances in the subset. Then, in the set of the parent node, a leaf node is created and labeled with the most prevalent class of samples.

The decision tree is formed throughout the procedure, with each non-terminal node (internal node) reflecting the selected attribute on which the data was divided and terminal nodes (leaf nodes) providing the class tag of the branch's final subset. Advantages of ID3 include [30]: use of training data to create understandable prediction rules, builds trees faster, builds short trees, the entire data set is used for constructing the tree, reducing the number of tests by enabling pruning of test data, computation time is the product of node number and characteristic number. Disadvantages of ID3 are [31]: data may be over-classified or over-fitted by a small sample, decision making consumes greater time since only one attribute is tested at a time, difficulty in classifying continuous data, and sensitive to features with a large number of values.

4 Methodology

The overall methodology of the study is divided into three segments as discussed below.

A. Pre-processing

Two tiles of Landsat-8 data are acquired from the United States Geological Survey's Earthexplorer website [20]. The bands 1 to 7 are used to perform layer stacking to create a 30 m multispectral imagery. This image along with band-8 of the data are then used in the resolution merge process to create a 15 m multispectral image. The boundary of each study area is then extracted using a subset operation. These preprocessing operations are executed on ERDAS IMAGINE v14.0® RS and GIS software.

Using an on-screen selection of polygons, lines, and pixels, training sites for seven LULC classes are selected in each study area. This operation was performed using IDRISI Selva v17® RS and GIS software. The LULC classes identified on the data are; Evergreen Forest (EGF), Deciduous Forest (DF), Water Body (WB), Scrub Land (SL), Kharif (KH), Double Crop (DC), and Built-Up (BU). By employing statistical measurement metrics, the distance between each class pair is computed. The LULC classes are categorized based on these metrics as spatially and spectrally dominant and subservient classes. This categorization is indicated in Table 1. Table 2 specifies the separability between each LULC class pair in terms of Euclidean and Normalized Euclidean distances.

Table 1 Lulc class information on primary and secondary study areas

North Canara study area				Kumta Study Area			
Spatially dominant	Spatially subservient	Spectrally dominant	Spectrally subservient	Spatially dominant	Spatially subservient	Spectrally dominant	Spectrally subservient
Evergreen Forest	Kharif	Water Body	Kharif	Evergreen Forest	Kharif	Water Body	Kharif
Deciduous Forest	Double Crop	Deciduous Forest	Double Crop	Water Body	Double Crop	Evergreen Forest	Double Crop
Water Body	Scrub Land	Evergreen Forest	Scrub Land	Scrub Land	Deciduous Forest		Deciduous Forest
	Built-Up		Built-Up		Built-Up		Built-Up
							Scrub land

Table 2 Class separability for each class pair in terms of Euclidean distance for North Canara study area (from least to most)

North canara study area						Kumta study area					
Class Pair	ED	NED	Class Pair	ED	NED	Class Pair	ED	NED	Class Pair	ED	NED
EGF-DC	1134.93	0.08	WB-DC	7248.91	0.51	EGF-DC	7204.13	0.10	KH-DF	45,907.39	0.63
DF-SL	1774.70	0.12	DC-SL	7958.55	0.56	KH-BU	17,726.09	0.24	WB-KH	48,870.09	0.67
BU-KH	3281.39	0.23	EGF-SL	8412.13	0.60	SL-BU	24,119.57	0.33	SL-DC	52,694.96	0.72
BU-SL	4325.80	0.30	KH-DF	8638.07	0.61	SL-DF	25,162.78	0.34	EGF-SL	54,706.30	0.75
WB-DF	4460.88	0.31	WB-BU	9060.46	0.64	SL-KH	26,804.24	0.37	KH-DC	60,398.94	0.83
BU-DF	5785.29	0.41	DC-BU	10,647.23	0.76	WB-BU	33,834.54	0.46	EGF-KH	63,239.82	0.87
WB-SL	6025.09	0.43	EGF-BU	11,408.05	0.81	DF-DC	35,120.83	0.48	BU-DC	65,437.28	0.90
DC-DF	6852.19	0.49	WB-KH	12,240.93	0.87	EGF-DF	36,571.65	0.50	WB-DC	68,628.12	0.94
KH-SL	6961.23	0.49	DC-KH	13,140.97	0.94	WB-SL	38,520.13	0.53	EGF-BU	68,990.16	0.95
WB-EGF	7120.97	0.50	EGF-KH	13,978.37	1.00	DF-BU	44,430.49	0.61	WB-EGF	72,974.51	1.00
EGF-DF	7145.00	0.51				WB-DF	44,661.80	0.61			

ED: Euclidean distance, NED: Normalized Euclidean distance, EGF: Evergreen Forest, DF: Deciduous Forest, WB: Water Body, SL: Scrub Land, KH: Kharif, DC: Double Crop, BU: Built-Up

By analyzing the class-pair distances in Euclidean space, we identify that some of the class pairs overlap each other by large proportions. For example, the EGF-DC class pair on the North Canara study area form the most overlapping class pair of the lot. The spatial region where these classes overlap will constitute mixed pixels, which contain information on more than one class. The challenge in such RS classification studies is to classify these mixed pixels to the correct LULC class.

B. Classification

Classification of the two study areas was implemented using IDRISI Selva v17® RS and GIS software. Information gain ratio is used as the attribute selection measure for CART and Entropy is used as the attribute selection measure for ID3. The decision trees are set to auto-pruning for leaves with proportion $\leq 1\%$.

C. Post-Classification Processing

The thematic maps obtained after classification are subjected to a rigorous accuracy assessment process. Each thematic map is verified for its accuracy by comparing the same with Google Maps, Wikimapia maps, Government census documents, and previous research outputs. For the primary study area and secondary study area, a total of 1098 and 1000 pixels were selected for the accuracy assessment process, respectively. These pixels were selected by employing a stratified random technique so as to consider the proportion of each LULC class of the study areas. The thematic map accuracy is depicted using several accuracy assessment measures; producer's accuracy (PA), user's accuracy (UA), omission error (OE), commission error (CE), class Kappa coefficient, overall classification accuracy (OCA), overall Kappa value (OKV), quantity disagreement (QD), and allocation disagreement (AD). For more information on these metrics, please refer to [32].

5 Results and Analysis

This section presents the results obtained during this study.

(A) CART Results

CART successfully extracted all seven LULC classes in the North Canara study area. Among the seven LULC classes, CART extracted Kharif and Water Body classes excellently with User's Accuracy (UA) values of 89.61% and 84.62%, respectively. Further, CART extracted Evergreen Forest and Deciduous Forest classes with good UA values of 78.50% and 72.61%, respectively. CART extracted the remaining LULC classes poorly. CART also separated spectrally overlapping classes with good effectiveness. EGF-DC class-pair forms the most severely overlapping class-pair in the North Canara study area. Yet, CART separated them with UA values of 78.50% and 43.33%, respectively. The same can also be said about the DF-SL class-pair, which forms the

second most severely overlapping class-pair in the North Canara study area. This performance by CART is considerably better than the conventional hard classifiers tested previously on the same data [33]–[38]. The OCA and OKV attained by CART for North Canara study area are 73.91% and 0.6009, respectively. The accuracy assessment results of CART for North Canara study area are indicated in Table. 3.

For Kumta study area, CART extracted Evergreen Forest, Water Body, and Kharif classes excellently, with greater than 85% UA values. CART also extracted Built-Up, Double Crop, and Scrub Land classes with reasonable accuracies. Deciduous class was the only poorly extracted class of the lot. For the Kumta study area, CART separated the spectrally overlapping class pairs very efficiently. This can be seen by the way EGF-DC and KH-BU classes are separated. Even though these class-pairs for the two most severely overlapping class-pairs in the Kumta study area, CART separated them very efficiently. CART produced the best classification results in separating spectrally overlapping class-pairs compared to our previous studies on the same area [33]–[38]. The OCA and OKV produced by CART for Kumta study area are 79.40% and 0.6482, respectively. The accuracy assessment results of CART for Kumta study area are shown in Table. 4.

(B) ID3 Results

For the North Canara study area, ID3 extracted Evergreen Forest and Kharif classes with excellent user accuracy values (greater than 80% UA values). The only other class that was extracted with greater than 50% UA value is the Deciduous Forest class. All other LULC classes were extracted poorly (less than 50% UA values). ID3 also failed to separate the spectrally overlapping classes in the study area. As a result, the classification results of ID3 for North Canara

Table 3 Accuracy assessment results of CART for North Canara study area

Class name	RT[a]	CT[b]	NC[c]	PA[d]	OE[e]	UA[f]	CE[g]	Kappa
Evergreen forest	529	642	504	95.27	04.73	78.50	21.50	0.5852
Deciduous forest	244	241	175	71.72	28.28	72.61	27.39	0.6479
Water body	24	26	22	91.67	08.33	84.62	15.38	0.8427
Scrub land	132	71	28	21.21	78.79	39.44	60.56	0.3116
Kharif	115	77	69	60.00	40.00	89.61	10.39	0.8839
Double crop and plantations	46	30	13	28.26	71.74	43.33	56.67	0.4086
Built-up	8	11	1	12.50	87.50	9.09	90.91	0.0842
Totals	1098	1098	812					
Overall classification accuracy				73.91%	Overall Kappa value			0.6009
Quantity disagreement				118	Allocation disagreement			168

RT[a]: Reference totals, CT[b]: Classification totals, NC[c]: Number correct, PA[d]: Producer's accuracy, OE[e]: Omission error, UA[f]: User's accuracy, CE[g]: Commission error

Table 4 Accuracy assessment results of cart for Kumta study area

Class name	RT[a]	CT[b]	NC[c]	PA[d]	OE[e]	UA[f]	CE[g]	Kappa
Evergreen forest	600	645	560	93.33	06.67	86.82	13.18	0.6705
Deciduous forest	29	78	28	96.55	03.45	35.90	64.10	0.3398
Water body	79	82	75	94.94	05.06	91.46	08.54	0.9073
Scrub land	112	114	67	59.82	40.18	58.77	41.23	0.5357
Kharif	76	57	49	64.47	35.53	85.96	14.04	0.8481
Double crop and plantations	89	17	10	11.24	88.76	58.82	41.18	0.5480
Built-up	15	7	5	33.33	66.67	71.43	28.57	0.7099
Totals	1000	1000	794					
Overall classification accuracy				79.40%	Overall Kappa value			0.6482
Quantity disagreement				99	Allocation disagreement			107

RT[a]: Reference totals, CT[b]: Classification totals, NC[c]: Number correct, PA[d]: Producer's accuracy, OE[e]: Omission error, UA[f]: User's accuracy, CE[g]: Commission error

study area are found to be considerably poor. The OCA and OKV produced by ID3 for North Canara study area are 71.31% and 0.5805, respectively. The accuracy assessment results of ID3 for North Canara study area are shown in Table. 5.

For the Kumta study area, ID3 extracted Water Body, Evergreen Forest, and Kharif classes excellently (with greater than 80% user accuracy values). ID3 also extracted Double Crop, Scrub Land, and Built-Up classes with reasonable

Table 5 Accuracy assessment results of id3 for North Canara study area

Class name	RT[a]	CT[b]	NC[c]	PA[d]	OE[e]	UA[f]	CE[g]	Kappa
Water body	24	61	22	91.67	08.33	36.07	63.93	0.3464
Evergreen forest	529	574	476	89.98	10.02	82.93	17.07	0.6705
Scrub Land	132	66	31	23.48	76.52	46.97	53.03	0.3972
Kharif	115	82	73	63.48	36.52	89.02	10.98	0.8774
Deciduous forest	244	221	161	65.98	34.02	72.85	27.15	0.6509
Double crop and plantations	46	83	19	41.30	58.70	22.89	77.11	0.1952
Built-up	8	11	1	12.50	87.50	09.09	90.91	0.0842
Totals	1098	1098	783					
Overall classification accuracy				71.31%	Overall Kappa value			0.5805
Quantity disagreement				122	Allocation disagreement			193

RT[a]: Reference totals, CT[b]: Classification totals, NC[c]: Number correct, PA[d]: Producer's accuracy, OE[e]: Omission error, UA[f]: User's accuracy, CE[g]: Commission error

accuracies. Deciduous Forest was once again extracted with poor class accuracy values. Further, ID3 separated the spectrally overlapping class-pairs with considerably better user accuracy values. This is once again seen for EGF-DC and KH-BU class pairs. For Kumta study area, ID3 produced OCA and OKV of 78.60% and 0.6350, respectively. This is closely comparable to the CART classification results for the same data. The accuracy assessment results of ID3 for Kumta study area are shown in Table. 6.

(C) Observations

The North Canara study area is 6–8 times larger than the Kumta study area. Both CART and ID3 have produced better classification results for the smaller sized data i.e., Kumta study area. This indicates that both CART and ID3 generalize well for smaller data sizes. Both CART and ID3 have performed excellently in separating the spectrally overlapping class-pairs on the data and thereby avoiding overfitting of the dominant classes. This performance is one of the best among the other classifiers we have tested previously.

Both CART and ID3 have also extracted the spatially subservient classes on the Kumta study area with the best accuracies attained among all the classifiers tested by us till date. This characteristic is seen only in the decision tree classifiers. The overall classification performance of CART and ID3 on the more complicated Kumta data indicates the algorithms' capability in handling heterogeneous data.

Table 6 Accuracy assessment results of id3 for Kumta study area

Class name	RT[a]	CT[b]	NC[c]	PA[d]	OE[e]	UA[f]	CE[g]	Kappa
Water body	79	83	76	96.20	03.80	91.57	08.43	0.9084
Evergreen forest	600	644	557	92.83	07.17	86.49	13.51	0.6623
Double crop and plantations	89	18	9	10.11	89.89	50.00	50.00	0.4512
Scrub land	112	111	65	58.04	41.96	58.56	41.44	0.5333
Kharif	76	55	47	61.84	38.16	85.45	14.55	0.8426
Deciduous forest	29	82	28	96.55	3.45	34.15	65.85	0.3218
Built-up	15	7	4	26.67	73.33	57.14	42.86	0.5649
Totals	1000	1000	786					
Overall classification accuracy				78.60%	Overall Kappa value			0.6350
Quantity disagreement				101	Allocation disagreement			113

RT[a]: Reference totals, CT[b]: Classification totals, NC[c]: Number correct, PA[d]: Producer's accuracy, OE[e]: Omission error, UA[f]: User's accuracy, CE[g]: Commission error

6 Conclusions

Classification of thematic maps has several important socio-economical applications such as change detection, mapping, forestry, etc. In this paper, we employed CART and ID3 decision tree-based classifiers for classifying heterogenous multispectral RS data. Seven LULC classes were selected in each study area and analysed for their separability using Euclidean distance. The results obtained indicate that both CART and ID3 are excellent choices for extracting spectrally overlapping classes. In doing so, both classifiers have also avoided overfitting the data. From the obtained results, we observe that CART and ID3 classifiers are data size-dependent. We obtained excellent results for the smaller study area, even though it was the more heterogeneous one. From these observations, we conclude that CART and ID3 classification algorithms are more suitable for data that exhibit large spectral overlapping in the study area. It should be noted that, in this study, we have measured spectral separability between two class pairs at a time. In future work, we intend to analyse the same for more than two classes at a time and analyse the impact on classification results.

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Spectral Splitting of Speech Using Time Varying Comb Filters to Improve Speech Perception in Sensorineural Hearing Loss Subjects

Aparna Chilakawad and P. N. Kulkarni

Abstract Persons with Sensorineural Hearing Loss (SNHL) experience a decrease in speech perception because of masking in a noisy environment. Spectral splitting of speech using time varying comb filters with complementary magnitude responses for binaural dichotic presentation is helpful in decreasing the effect of frequency masking of spectral components. Thus, there is an improvement in speech perception. FIR time varying comb filters with complementary magnitude responses of order 512 are designed using a frequency sampling method with 22 one-third octave bands ranging from 0 to 11 kHz. and the continuous shift in magnitude responses with time shifts selected below just a noticeable difference (JND), so that gap detection ability improves without offsetting the advantage of the spectral splitting technique. Filter performance is assessed by objective tests using PESQ (Perceptual Evaluation of Speech Quality), spectrographic analysis, and by subjective tests using Mean Opinion Score (MOS) for quality. Subjective test is investigated on normal hearing subjects by adding white noise at different SNRs. Test materials used for the evaluation are VC (Vowel Consonant) nonsense syllables and vowels. The results showed an improvement in the perception of processed speech in a noisy environment.

Keywords Time varying comb filter · Spectral splitting · Masking · PESQ · MOS

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1 Introduction

Sensorineural deafness occurs because of damage in hair cells of the cochlea of the inner ear or the nerve path from the inner ear to the brain. One of the characteristics of Sensorineural Hearing Loss (SNHL) is frequency masking [1] which can be reduced by splitting the spectrum of speech into two parts having complementary spectral components for binaural dichotic presentation using pair of FIR comb filters with complementary magnitude responses [2]. The scheme helped to improve speech perception. The focus of the work was to compare different types of comb filters and concluded that filters with 1/3 octave band and auditory critical band (ACB) are better than filters with constant bandwidth. All filters were designed with a sampling frequency of 10 kHz. The methodology was assessed on normal hearing subjects.

In work [3], 18 ACB ranging from 0 to 5 kHz FIR filter bank summation approach with sampling frequency 10 kHz to split the speech spectrum for binaural dichotic presentation followed by frequency compression with factor 0.4–1, the strategy was discussed to boost speech perception for sensorineural deafness subjects. The scheme was tested on normal hearing subjects. Reported that the algorithm worked significantly under adverse listening conditions.

The objective of the paper [4] was to decrease both frequency and temporal masking for SNHL listeners for better speech intelligibility using a pair of time varying comb filters having a set of pre-calculated coefficients (256 coefficients FIR filters) with complementary magnitude responses to split the speech signal spectrum for binaural dichotic presentation. Magnitude responses were cyclically swept within 20 ms time period. The investigation was done with sets of 2, 4, 8 and 16 filters which were helpful in enhancing speech perception of place and duration for subjects using a binaural hearing aid. The sweep cycle in FIR time varying comb filters to split the speech spectrum was optimized for binaural dichotic presentation in SNHL [5]. Conducted the experiment for different sweep cycles for 8–16 shiftings on normal subjects. The finest outcome was for a sweep cycle of 50 ms.

In the paper, Wang et al. [6] for multichannel digital hearing aid sub-band noise reduction technique was proposed to reduce mainly the computational complications and compared the proposed algorithm with spectral subtraction, adaptive Wiener filtering, modulation frequency-based algorithms, and found that Perceptual Evaluation of Speech quality (PESQ) [7] improvement was 0.94 and 0.59 for SNR 5 and 10 dB respectively, but the algorithm was not assessed in adverse listening conditions.

The speech signal was split into two complementary spectra for binaural dichotic presentation using temporal splitting, spectral splitting and combined splitting processing methods [8]. Spectral splitting was done with perceptually balanced comb filters. Temporal splitting was achieved with fading functions of 20, 40, and 80 ms inter-aural switching periods. Time varying comb filters with 20 40, and 80 ms, cyclically swept magnitude responses with 4, 8, and 16 shiftings were implemented for combined splitting and binaural filtering was done with an adjustable gain filter. Phonetically balanced monosyllables were used to test for speech recognition and

speech perception was improved in persons with moderate to severe sensorineural loss and in normal listeners.

18 fixed bandwidth and ACB comb filters having complementary magnitude responses were designed to split the speech spectrum for binaural dichotic presentation to improve speech perception for moderate bilateral sensorineural hearing loss subjects and to evaluate the sound localization. Subjective measures were carried out on normal subjects with different SNRs as well as on moderate bilateral sensorineural loss subjects. Speech recognition was increased for both kinds of subjects [9].

To reduce the noise in speech for hearing aid, the supervised sparse coding strategy was proposed [10] and was implemented in the time domain. The algorithm was evaluated by comparing it with Wiener filtering and spectral substation. The Evaluation was made by objective (PESQ) and subjective (for intelligibility tests using BKB (Bamford-Kowal-Bench) sentences. PESQ values were best for positive values of SNRs. For SNR of −5 db, Wiener filtering was better.

People with sensorineural hearing loss benefited from a cascaded device of noise control and multiband compression [11]. The input signal (with multiband compression) was segmented into 18 frequency bands from 0 to 5 kHz using auditory critical bandwidths (ACB). To reduce the spectral masking effect, all spectral energy was condensed at the center of each band. To reduce the noise wiener filter was used. The scheme was assessed for quality (PESQ, MOS) on normal hearing persons and for intelligibility on hearing-impaired persons. Results showed an improvement in speech perception.

Even though the earlier studies have been successful in reducing the effects of spectral masking the capacity to identify gaps is affected by step changes in the magnitude responses with a constant number of distinct time shifts in time varying comb filters. The current study suggests the continuous shift in magnitude responses with time shifts chosen below just detectable difference (JND), in order to increase gap detection ability without offsetting the advantage of the spectral splitting approach.

The main objective of the present work is to split the speech spectrum using time varying filters having complementary magnitude responses to improve speech perception in sensorineural hearing-impaired subjects, as this impairment cannot be medically cured. Magnitude response H_m (f) and impulse response h_m (n) of a time varying filter are dynamic and hence are functions of time 'm'. By using this characteristic of the filter, we proposed the continuous shift in magnitude responses with time shifts selected below just noticeable difference (JND) for binaural dichotic presentation, and also gap detection ability is improved in the speech without offsetting the advantage of spectral splitting technique. Hence speech perception gets improved.

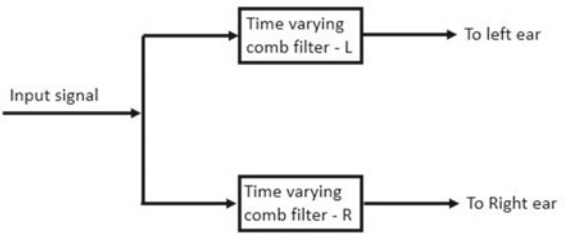

Fig. 1 Signal processing with time varying filter

2 Designing

Figure 1 is the block diagram of signal processing. A speech signal is split into two signals having complementary spectral components to present dichotically i.e., to left and right ears using a pair of FIR time varying filters with order 512 having magnitude responses complementary to each other. Filters are implemented with MATLAB software using the frequency sampling method of designing of filter [12]. Designed filters have 22 one-third octave bands with a sampling frequency of 22 kHz. 1/3-octave bands have narrow bands at lower frequencies and wider bands at higher frequencies. For lower frequencies crossover gain is maintained from −4 to −7 dB and for higher frequencies, from −6 to −6.5 dB. Transition bandwidth is adjusted between 70 and 80 Hz for higher frequencies. Pass band ripple is maintained below 1 dB. Complementary magnitude responses of time varying comb filter pairs at different instants of time are shown in Fig. 2. The continuous shift in magnitude responses with a time shift of 5 ms is considered, which is below JND.

3 Results

The scheme of spectral splitting of speech signal using a time varying comb filter with the continuous sweep with a time shift of 5 ms is assessed for speech quality by using objective measures (PESQ and spectrographic) and subjective measures on six normal listeners by using vowel /aa/, nonsense VC syllable /aa_b/ as test signals.

Figures 3 and 4 are the narrow band spectrograms for unprocessed and processed signals respectively for SNR value of infinity. Figures 5, 6, 7, 8 and 9 are spectrograms of processed signals with SNR values of 6, 3, 0, −3, −6 dB respectively. The energy of unprocessed signal is distributed between left and right signals. When these signals are presented to both ears, they get added in the center level of the auditory system. Pitch information is maintained in all the spectrograms. The spectrograms show significantly reduction in noise. These findings are in conformity with PESQ values and MOS test.

Improvement in PESQ (ΔPESQ) values is shown in Table 1. PESQ value is decreased by 1.1406 for clear test material /aa_b/ and for clear vowel /aa/ by 0. 445. For SNR values from 6 to −6 dB in steps of 3 dB for /aa_b/ ΔPESQ values are

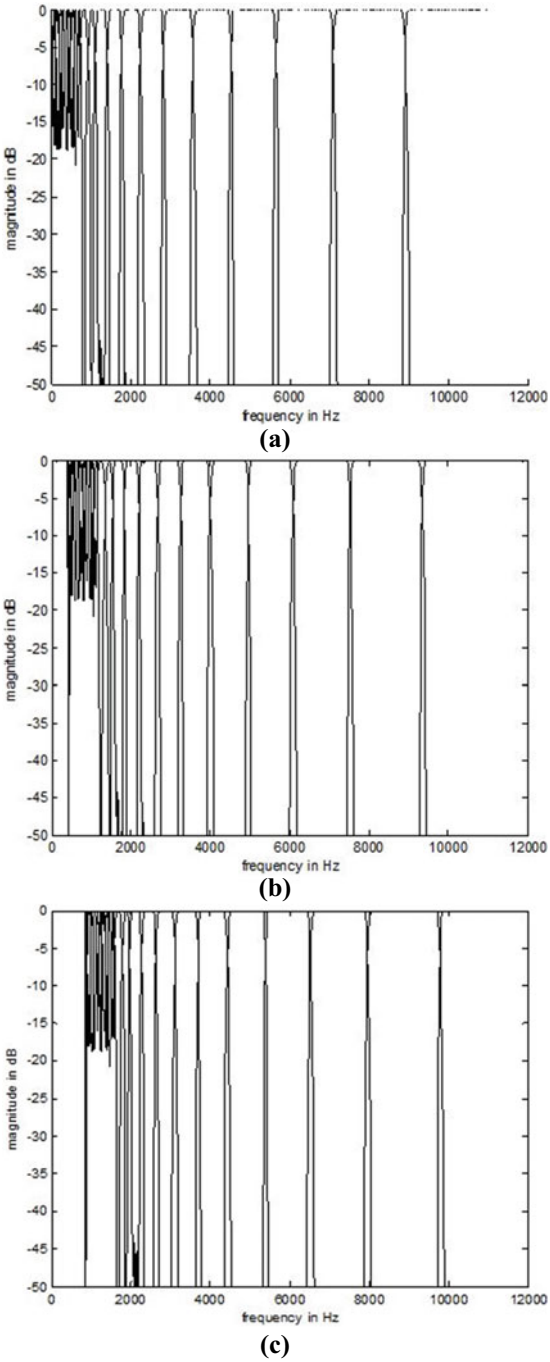

Fig. 2 Overlapped complementary magnitude responses **a**, **b** and **c** for left and right channels of time varying comb filter pairs at different instants of time

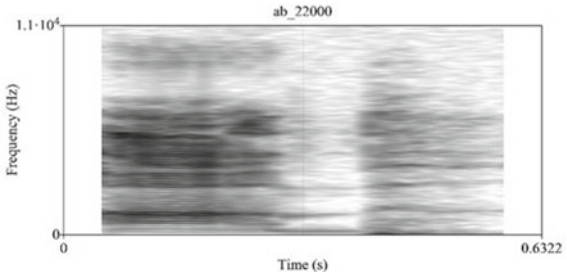

Fig. 3 Unprocessed VC syllable

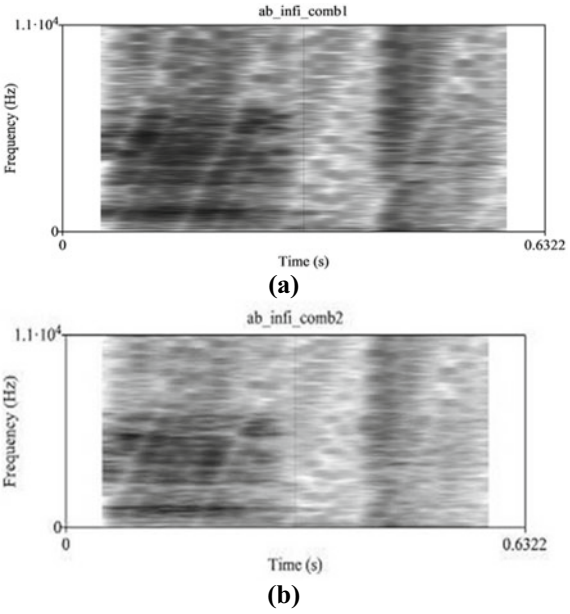

Fig. 4 Processed signals **a** for left **b** for right ears

1.6717, 1.7028, 1.7203, 1.8405, and 1.8932 respectively, and for vowel /aa/ 0.6108, 0.8643, 1.2127, 1.2821, 1.3556 respectively.

It is observed that improvement in the PESQ values is more for lower SNR conditions.

The proposed work is advantageous for the noisy environment for persons with SNHL. Subjective evaluation is carried out on normal subjects (2 male and 4 female) with ages from 18 to 45 using Mean Opinion Score (MOS) measure for speech quality. MOS assessment is listed in Table 2. The scores for processed nonsense VC test signal /aa_b/ are 2.92, 3.38, 3.17, 3.47, 3.52, 3.43 for SNR ∞, 6 to -6 in steps of 3 dB respectively. Similarly, speech quality is tested for vowel /aa/ on the same subjects using MOS, and scores obtained are better in the case of a stimulated noisy signal than the noise-free signal.

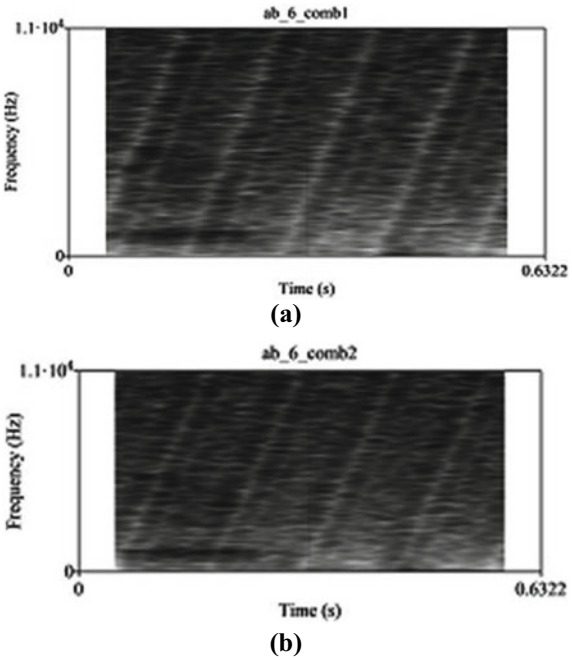

Fig. 5 Processed signals **a** for left **b** for right ears with SNR 6 dB

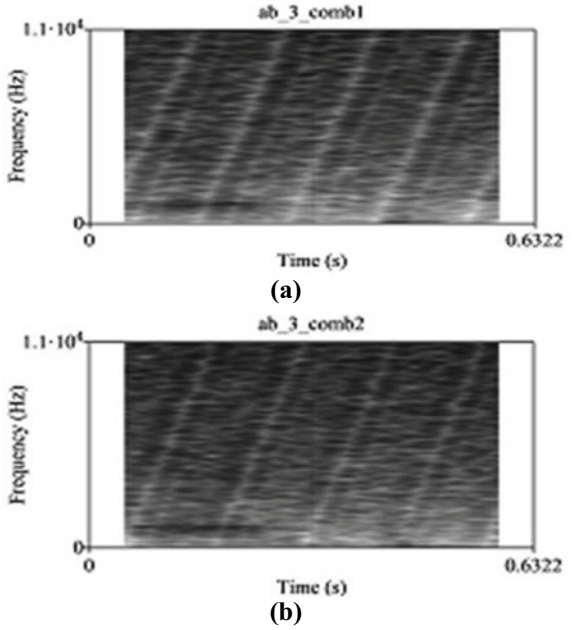

Fig. 6 Processed signals **a** for left **b** for right ears with SNR 3 dB

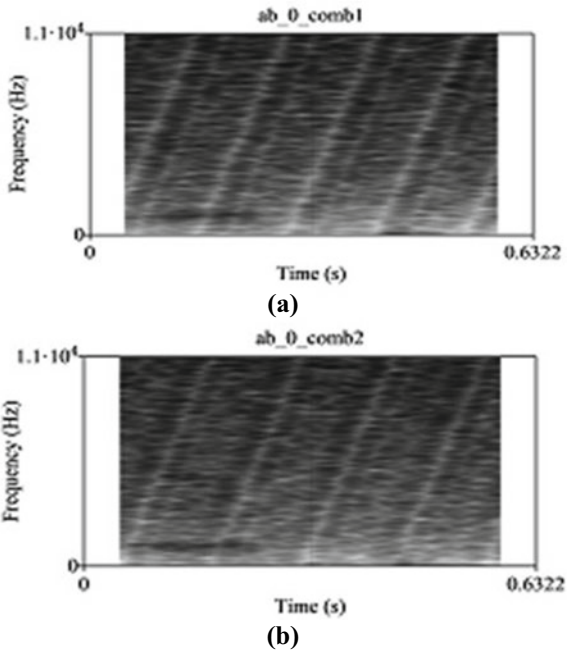

Fig. 7 Processed signals **a** for left **b** for right ears with SNR 0 dB

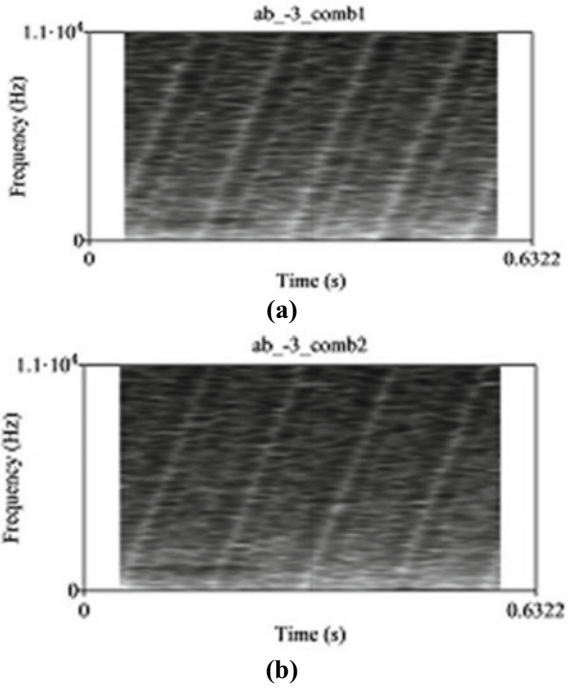

Fig. 8 Processed signals **a** for left **b** for right ears with SNR −3 dB

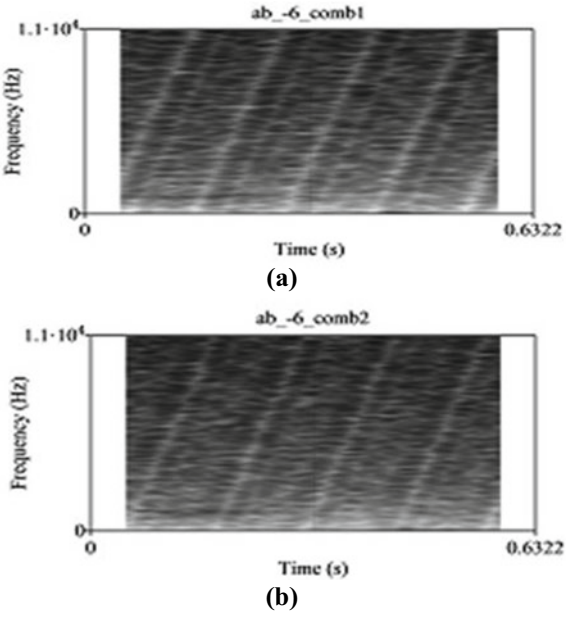

Fig. 9 Processed signals **a** for left **b** for right ears with SNR −6 dB

Table 1 Improvement in perceptual evaluation of speech quality (Δpesq) values with different SNR

SNR values in dB	ΔPESQ values for /aa_b/signal	ΔPESQ values for /aa/signal
∞	−1.1406	−0.445
6	1.6717	0.6108
3	1.7028	0.8643
0	1.7203	1.2127
−3	1.8405	1.2821
−6	1.8932	1.3556

Table 2 Mean opinion score test scores for unprocessed and processed signals at different snr values

Subjects with sex, age	SNR values in dB											
	∞	6	3	0	−3	−6						
	*unprcd	**procd	unprcd	procd	unprcd	Procd	unprcd	procd	unprcd	procd	unprcd	procd
S1, [F, 22]	4.5	3	2	3	1.5	3	1	3.5	1	3.5	1	3.8
S2, [M, 25]	4	2.5	2	3.5	1	3	1	3	1	3	1	3
S3, [F, 21]	4	3	2.5	3.5	1	3.5	1	3.5	1	3.5	0.5	3
S4, [F, 39]	4	2.5	2	3.8	1.5	3.5	1.5	3.5	1.5	3.8	1	3.5
S5, [F, 45]	4	3.5	1	3.5	1	3	1	3.5	1	3.5	0.5	3.8
S6, [M, 18]	4	3	2	3	1.5	3	1.5	3.8	1.5	3.8	0.5	3.5
MOS	4.08	2.92	1.92	3.38	1.25	3.17	1.17	3.47	1.17	3.52	0.75	3.43

*unprcd: unprocessed
**procd: processed

4 Conclusion

The splitting of a speech signal into two complementary spectra for binaural dichotic presentation using 22-band time varying comb filters having a continuous shift in magnitude responses with time shifts selected below just noticeable difference (JND), is helpful in reducing the effect of frequency masking and hence provides better speech perception. The proposed technique is evaluated using objective tests (PESQ, spectrographic analysis) and subjective tests (MOS) investigated on normal listeners. The objective test outcomes indicated an improvement in the quality of speech (ΔPESQ values) for signals with lower SNR conditions. Subjective tests showed better MOS for noisy signals than the noise-free signal. The performance of the proposed scheme is found to be better in a noisy environment. It contributes a scheme of splitting the speech signal using time varying comb filters with the continuous shift in magnitude responses in the improvement of speech perception for SNHL subjects.

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Soil Erosion Studies of Mangaluru Coastal Region Using Satellite Imageries and Machine Learning Algorithms

Subramanya Bhat

Abstract Coastal erosions usually cause drastic disasters in the ecosystems and the human lives in coastal zones. Change over time and identifying the location of the shoreline is the most important aspect of managing coastal areas and this requires frequent monitoring of the shoreline using satellite imageries over time. The effectiveness of filed-based study and image processing techniques for computing soil erosion or accretion rate are considered and the proposed method gives the precise results for soil erosion studies. In the proposed method, first principal component analysis (PCA) is applied, then image processing techniques are applied and finally, the model is developed using Machine Learning algorithms. Firstly PCA has been used for separating land and water bodies in satellite imageries, then image processing technique is used to compute soil erosion or accretion rate and finally, the model is developed using Machine Learning Algorithm. The proposed method is applied to satellite imageries, between 2014 to 2019, of the Mangaluru coastal region to attain erosion and accretion rate. The results showed that the erosion rate is comparatively high in Talapady, Someshwara, and Ullal Regions in the year 2014–2015. Also, for the years 2016–2018, there has been an erosion in these regions. Other regions of Mangaluru Coast are subjected to both erosion and accretion but there are no significant changes. As compared to field-based study and image processing technique-based soil erosion or accretion rate computation, the proposed method predicts the soil erosion or accretion for future years also. The model developed in the proposed study can process satellite imageries of several years and predicts soil erosion or accretion for future years. If the erosion rate is high then the government can take necessary action plans such as stopping sand mining, industrial and development activities and, planting more trees near the seashore.

Keywords Remote sensing · ERDAS imagine · ArcGIS · Image segmentation

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1 Introduction

Soil erosion is a serious environmental issue in many parts of the world. Erosion is a potential environmental problem, as the topsoil that is rich in nutrients is usually washed away by erosion. Erosion is mainly caused by water. As the water level of the sea increases, it tends to overflow onto the land. As the water level increases, the soil is over-saturated with water. Since water can pass more rapidly over eroded soil it causes flash-flood damage. Soil erosion is a major environmental problem, particularly in economically agricultural-dependent regions [1]. Recently NASA published reports indicating that the sea level is rising and there is a likelihood that the coastal region of Karnataka will submerge in water [2]. Because of such a warning from NASA scientific reports, it became very essential to monitor the soil erosion taking place in the Dakshina Kannada and Udupi regions of Karnataka. The soil erosion should be monitored regularly and the satellite imageries can be used. Soil erosion study is critical and very complex, as multiple variables including climate, cropping systems, and topography, influence the degree of risk of erosion. Identifying the riskiest landscapes and factors is an important step in targeting and developing localized management approaches. All of this creates a constant need for accurate data. In addition, any analysis of erosion and deposition and their causes must be focused on accurate monitoring of their characteristics over at least several years [3].

The method of detecting the changes that have occurred in the coastal area over time is called change detection of the coastal area. Change detection can be performed using conventional approaches or remote sensing techniques. Ground surveying or Filed-based studies is one of the conventional approaches. However, Ground surveying is not an effective method, due to the vast size of coastal areas and the irregular sides of coastal regions for the shoreline-plotting tasks [4]. Also, Filed-based studies are time-consuming, costly, and not accurate, while the remote sensing techniques do not face any of these issues. Using various remote sensing techniques, change detection of coastal regions is carried out effectively [5].

Remote sensing is a method of detecting and tracking an area's physical characteristics by measuring its radiation reflected and emitted at a distance. The data obtained from the remote sensing system are in the form of satellite images, aerial photographs, and other information. Using remote sensing, data can be collected about inaccessible areas. Remote sensing has found its applications in coastal applications, hazard assessment, natural resource management, agricultural applications, etc. due to the availability of a large amount of data. Since all the radiations that the sensors record have to pass through the atmosphere, the atmospheric constituents affect the radiation and cause scattering and absorption of radiation. As a consequence of this, data quality is degraded. To extract valuable data from the images, image processing is to be performed on the collected images, thereby improving the image and leading to better visual perception. If the image is exposed to blurring, geometric distortion, or degradation then it is corrected and restored by image processing [6].

In terms of radiometric, spatial, temporal, and spectral resolutions data products produced by remote sensing provide a brief and constant view of the earth. To monitor coastal areas, Remote Sensing data on a temporal basis can be used, and also soft computing methods such as Fuzzy Logic, Support Vector Machine, and Genetic Algorithm can be used. These algorithms are also used in the study of coastal susceptibility by categorizing the images of remote sensing [7]. The review of the application of these algorithms was carried out; however, these algorithms are not applied to coastal satellite imageries. The SVM is computationally interactive compared to other algorithms such as Fuzzy and GA. The results show the development and relocation of barrier-spits and also erosion and accretion of beaches. In the coastal zone, an evaluation of sediment and erosional sites indicates that the area covered by sedimental characteristics slightly surpasses those under erosion [8]. The total accretion recorded is about 29 acres in 1987–1997 and about 10 acres in 1997–2001 and total erosion recorded is about 3 acres in 2001–2005. The maximal prograde and recession are found in Thannirbhavi to Bengre and Kotepura to Ullal respectively since these were the beaches that are exposed to continuous erosion since 1997 [9]. The total erosion during the period of 1989 to 2015 in the regions of Nethravathi-Gurupur is almost 0.47 sq.Km and in the Ullal region a severe erosion has occurred. The conclusion obtained by studying the change analysis on coastal regions of Mangaluru for 33 years is that the deviation in the position of coastline has mostly occurred in Talapadi to Sashihithlu of Mangaluru coast. There is a substantial deviation in the erosion and accretion process all along the coastal regions of Mangaluru [10]. During the period 1969–1999 in Ovari zone accretion was predominant and from 1999 onwards experienced erosion frequently on the coastal zones but Tiruchendur coast has undergone both accretion and erosion. Inappropriate and in-sustainable sand mining is one of the causes of significant erosion issues in the coastal region. Unplanned mining will result in significant erosion problems due to net loss of sand or from the formation of erosional “hot spots” arising from the concentrating of wave energy on different points alongside a coastline region [11]. PCA can be used as a technique to sense variations in remote sensing imageries. Compared to a classification approach for change detection in this region, PCA was discovered to be advantageous in specifying where change had occurred, although it was difficult to interpret the changes without reference to the input data [12]. PCA to data from the Compact Airborne Spectral Imaging System and discovered that to produce the best results PC2, PC3 and PC4 have to be combined for the categorization of vegetation and sediment [13]. PCA is used to spot the volcanic ash cloud data from Moderate Resolution Imaging Spectroradiometer images. The sensitivity of thermal infrared bands is analyzed and calculated by Principal Component Images (PCIs) and then reprocessing the suitable bands with the PCA [14]. The soil erosion models, where Support Vector Machine (SVM) is used to classify coastal surface area are developed. Then the secondary image is generated by congregating water and land classes. The improvement of the secondary image is completed by morphological filtering and the coastline is extracted to compute the soil erosion [10]. Digital Shoreline Analysis System version 4.217 was used to compute the coastline rate of change of data from a time series of many coastline positions. For long-term

shoreline analyzes, Laminated Root Rate and Weighted Least Squares Regression has opted as they are the most statistically robust quantitative approaches when an inadequate number of coastlines are accessible. Weighted Least Squares Regression statistical technique is used for long-term change analysis because it accepts ambiguity fields into consideration to calculate the long-term rates of coastline change. Temporarily, the Electron Paramagnetic Resonance process is adopted [5]. The result of supervised classification using ERDAS IMAGINE software obtained states that during the last five years, there is an increase in the water body, open land or barren, forest, and wasteland by 0.55%,0.48%, 2.26%, and 0.23% respectively and there is a reduction in agriculture or other vegetation, river and habitation by 3.22%, 0.26% and 0.04% respectively [15]. However, in many papers, researchers used Filed-based soil erosion studies and image processing-based techniques for soil erosion studies. A very little work has been reported on using Machine Learning algorithms for satellite imageries. For training and testing the model with more years of satellite data, Machine Learning algorithms are efficient. The PCA, image processing techniques together with Machine Learning algorithms are not used in the literature. In the proposed study, PCA, image processing technique together with Machine Learning algorithms such as K-fold cross validation techniques are used for computing soil erosion studies.

In the proposed study, Principal Component Analysis (PCA) is the change detection technique used to identify the rate of soil erosion in coastal areas. Image Processing Techniques such as Segmentation, Erosion, and Dilation operations are used. For training and testing satellite imageries, a K-fold cross validation algorithm is used. The Linear Prediction approach is used to validate outcomes and the estimation is also verified using the same mathematical model. The major contributions of the proposed work are highlighted as:

- Firstly, pre-processing of satellite imageries. Images are collected during the summer season as they are free from cloud cover. Pre-processing such as segmentation, erosion, and dilation are implemented for satellite imageries. Morphological operations are also performed on satellite imageries.
- Furthermore, Sea soil erosion studies along the Mangaluru Coastal region during the last 05 years.
- Furthermore, Machine Learning Algorithms application for satellite imageries. Machine Learning algorithm K-fold cross validation technique is applied. The results are verified with Field-based studies. Machine Learning algorithms are able to produce better results in comparison with image processing-based techniques.
- Furthermore, a Mathematical Model is developed for soil erosion studies. These models can predict soil erosion in future years and government agencies can plan necessary actions to be prepared in advance. The model developed is compared with the state-of-the-art literature in which Field-based studies or image processing-based techniques are discussed.
- The developed model can be used to study sea soil erosion in other parts of the world. Since the model developed gave promising results, the developed model can be used to predict the soil erosion rate and to take necessary actions.

- Furthermore, the developed model can be used to monitor soil mining activities that are happening and causing damage to shores.
- Finally, the developed model can also be used for river soil erosion studies. Soil erosion is also a major problem on river banks. The developed model can be enhanced to predict soil erosion happening on the river banks. The prediction helps to protect the people and their properties, crops, etc.

The proposed system implementation is discussed in Sect. 2. The methodology is discussed in Sect. 3. The application of PCA and Image processing algorithms is discussed in Sect. 4. Application of Machine Learning Algorithms and development of Mathematical model is discussed in Sect. 5. Results and Discussions are presented in Sect. 6. The conclusion drawn on the proposed work is presented in Sect. 7.

2 System Implementation

In the proposed work, PCA is used for determining soil erosion rate. In Satellite imageries, data bands are highly correlated because similar spectral regions are occupied. PCA identifies the duplicate data over multiband datasets. PCA aggregates only essential information into groups known as Principal Component. This creates a new dataset with essential information which is smaller in size. The advantages of PCA are a reduction in redundancy and fast processing time. To perform PCA data is collected and the mean is subtracted from each data dimension. This produces the dataset whose mean is zero. The next step is to calculate the covariance matrix and then find the eigen values and eigen vectors. Eigen vectors indicate the spread of data. From eigen vectors the lines can be extracted which characterize the data. Also, the image processing techniques used in the proposed work are Segmentation, Erosion, and Dilation. The Segregation of digital images into multiple regions can be referred to as Segmentation and the main purpose of segmentation is to simplify so that it is more significant and easier to evaluate. It is more convenient to discover objects and boundaries in an image. Pixel data is reduced to region-based information in the image segmentation method. Thresholding is one of the simplest methods of image segmentation. Thresholding is a process of conversion of a gray scale image into a binary image. When multiple values are selected the essential factor for this method is to set a threshold value. Quadtree segmentation where the image is split into quadrants based on homogeneity criterion. If the image is not homogeneous, then the image is divided into four squares and so on. If the four squares are homogeneous then images are fused as numerous linked components. The nodes present in the tree are called segmented nodes and the procedure lasts until no further splits or merges are possible.

3 Methodology

Data is collected for the last five years from Landsat 8 from Earth Explorer (EE) which is a user interface developed by the United States Geological Survey (USGS). Landsat 8 has two sensors, Operational Land Imager (OLI) and Thermal Infrared Scanners (TIRS). A Landsat 8 image scene size is 185 km × 180 km. The Operational Land Imager (OLI) generates 9 spectral bands (bands 1 to 9) with a resolution of 15 m, 30 m, and 60 m. Landsat 8 bands of the OLI sensor are cirrus, coastal, red, green, blue, Short Wave Infrared-1 (SWIR-1), Short Wave Infrared-2 (SWIR-2), and Near Infrared (NIR). All of these bands have a ground resolution of 30 m. Then the panchromatic band (band 8) has a fine resolution of 15 m. The Thermal Infrared Sensor (TIRS) consists of 2 thermal bands (bands 10 and 11) with a spatial resolution of 100 m. The TIRS consists of 2 thermal bands (bands 10 and 11) with 100 m spatial resolution. It measures the thermal energy of the Earth. Both TIRS bands are long-wavelength infrared with a resolution of 100 m.

Summer season satellite images were chosen because these images are free from cloud cover, as compared to satellite images recorded during monsoon. To evade change detection error due to seasonal differences it is important to use imageries from the same time of year. In the proposed study, data is collected during the summer season. PCA is implemented using ERDAS Imagine 2014 software. The source image is shown in Fig. 1 and Pan sharpened image is shown in Fig. 2. The Principal Component Analysis is applied to the Pan Sharpened image of the different periods and the result is shown in Fig. 3. PCA is done by setting the Principal Component value as 2. The resultant image is with two Principle Components, Land and Water.

Further processing such as thresholding, erosion, and dilation are performed using MATLAB. Figure 4 shows the result after applying thresholding. Erosion and Dilation are the two fundamental Morphological operations used to remove clouds in the image. The addition and removal of pixels to the boundaries of the object in an image are known as Dilation and Erosion respectively. Depending on the size and structuring element used to process the image the number of pixels added or removed from the objects in an image. The Spatial model used for thresholding is as shown in Fig. 5.

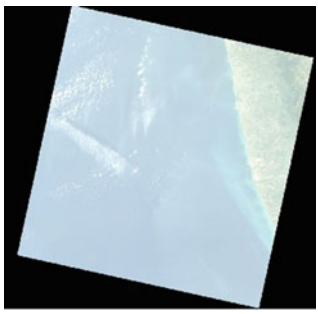

Fig. 1 Source image

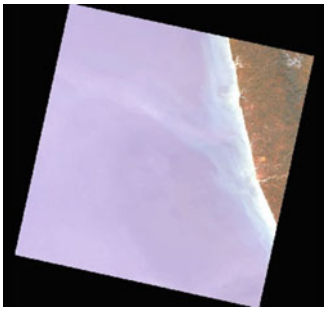

Fig. 2 Pan sharpened image

Fig. 3 Output of PCA

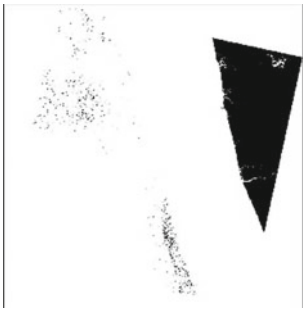

Fig. 4 Thresholding output image

To find the exact location where the erosion and accretion have taken place, the original large image is sub-divided into smaller images and then logical operations are applied to the sub-images in MATLAB. The latitude and longitude coordinate position in the original image will be compared to pixel value using ERDAS IMAGINE 2014. The coordinates of the regions of Mangaluru are given in Table 1.

Fixing reference points in a thresholded image and by calculating the pixel numbers from the reference points to the foreground pixels by applying the Euclidean distance formula, the erosion and accretion rate that occurred can be obtained. For a two-dimensional image, subtracting the x and y coordinates of the first point $(q1, q2)$ from the x and y coordinates of the second point $(p1, p2)$ and adding the squares

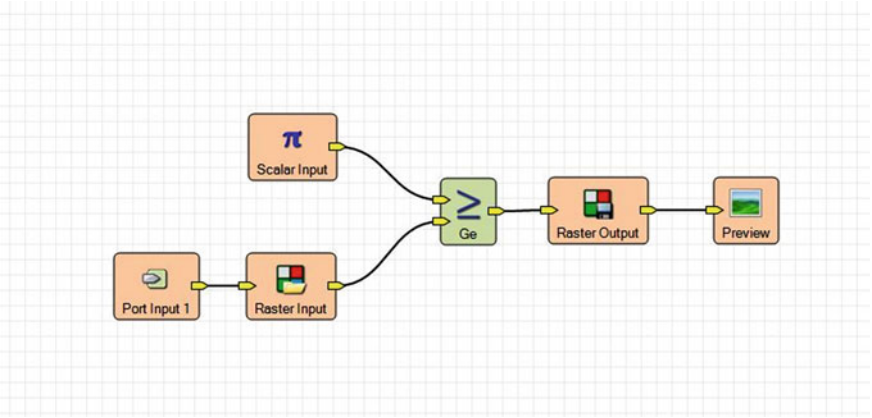

Fig. 5 Spatial model for thresholding

Table 1 Coordinates of Mangaluru region

Location	Coordinates
Talapady	12.764°N 74.88°E
Someshwara	12.7862°N 74.8535°E
Ullal	12.8076°N 74.8423°E
Kudroli	12.8770°N 74.8317°E
Sulthan Bathery	12.8897°N 74.8411°E

of the difference of both x and y coordinates, and then taking the square root of that sum to find the distance.

$$D(p,q) = \sqrt{(q1 - p1)^2 + (q2 - p2)^2} \tag{1}$$

The reference points fixed for all the images are the same and the image of the year 2014 is placed as a baseline. Comparing it with other images of the different periods will give the changes that occurred in the images of the different periods. Masking of an image is done to extract the Area of Interest. Setting some of the pixel values in an image to zero, or some other background value is known as Masking. Masking can be done in one of two ways: (1) Using an image as a mask or (2) Using a set of Region of Interest (ROI) as the mask. This method uses the second way, using ROI as the mask.

4 PCA and Image Processing

The Principal Component Analysis is carried out in ERDAS Software for the last five years of data of the same area but of a different period. Since the proposed method uses two components as Principal Components, it produces a grayscale image that separates land and water bodies. Each Principal component output of a different period is given to the thresholding separately to produce a binary image [16, 17]. The threshold value varies for each image. Applying Mask to the binary image so that only the Area of Interest will be highlighted. The pixel values of the highlighted area are obtained. Image Segmentation is done to divide the large image into smaller sub-images. First, the grid is applied to the image and then the image is divided into smaller sub-images. Taking each sub-image and performing logical operations will give the location where erosion and accretion have taken place. Figure 6 shows the image after applying the grid.

The process is repeated for every image of different periods. Taking the image of the year 2014 as the base reference and comparing the distance of every row will give the erosion and accretion rate. If the distance is more than the erosion occurred and otherwise there has been accretion occurred during that particular year. The results show that in the year 2015, there is more accretion compared to the rest of the years and in the year 2016, there is erosion. By applying logical XOR operator on two images it will give erosion and accretion locations. Consider two images, Image A of the year 2014 and Image B of the year 2015 as shown in Figs. 7 and 8 respectively. Applying logical operator $X=\overline{A} \cdot B$ will give areas where erosion has taken place and $Y=A \cdot \overline{B}$ will give areas where accretion has taken place. Figure 9 shows Erosion taking place during the year 2014–2015 and Fig. 10 shows Accretion taken during the year 2014–2015. By applying XOR operation $Z= \overline{A} \cdot B + A \cdot \overline{B}$ will give both erosion and accretion prone areas. Figure 11 shows Output obtained after applying XOR operation for Image A and B. Figure 12 helps for fixing a reference point and calculation of Euclidean distance.

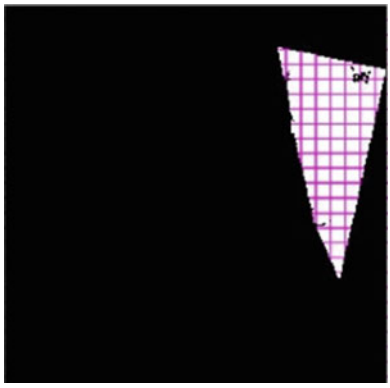

Fig. 6 Applying grid to the image

Fig. 7 Sub image A year 2014

Fig. 8 Sub image B year 2015

Fig. 9 Erosion taken place during the year 2014–2015

Fig. 10 Accretion taken during the year 2014–2015

Fig. 11 Output obtained after applying XOR operation for Image A and B

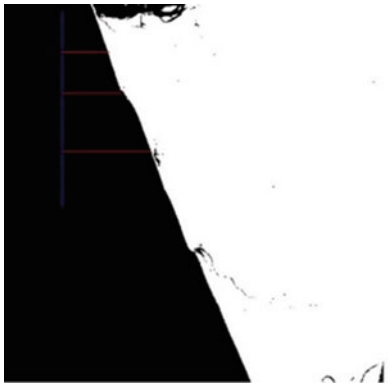

Fig. 12 Fixing a reference point and calculating the Euclidean distance

Table 2 Erosion and accretion rate details

Year Place	2014–2015	2015–2016	2016–2017	2017–2018	2018–2019
Talapady	120 m Erosion	45 m Erosion	75 m Erosion	30 m Accretion	120 m Erosion
Someshwara	135 m Erosion	45 m Erosion	75 m Erosion	30 m Accretion	135 m Erosion
Ullal	135 m Erosion	60 m Erosion	60 m Erosion	30 m Accretion	135 m Erosion
Kudroli	NIL	15 m Accretion	30 m Erosion	30 m Erosion	NIL
Sulthan Bathery	NIL	NIL	15 m Erosion	NIL	15 m Erosion

After applying logical operations to the image, the edges of the image are not clear. To enhance the image and remove the noise smoothening filter is applied. This smoothens the edge, gives an improved quality image, and produces a less pixelated image. The unwanted details can be eliminated using a Morphological operator Erosion. The white patches due to cloud are removed using the erosion and dilation method. To count the change in the number of pixels, a reference line is fixed and by applying Euclidean distance pixels were counted till the pixel value changes.

Table 2 shows the pixel count calculated after applying Euclidean distance. The reference point is fixed for the 160th column and Euclidean distance is calculated from the fixed point till the point where the pixel value changes in a particular row. It is repeated for different rows and images every year. The erosion and accretion rate of different regions of Mangaluru is graphically represented in Figs. 13, 14, 15, 16, 17, and 18. These results are also cross verified with the Field-based studies. In Field-based studies, people living in these areas are consulted and the results are verified.

5 Machine Learning Algorithm and Mathematical Model

The preprocessed images are trained and tested using the Machine Learning algorithm K-fold cross validation technique. The mathematical model is developed using Linear prediction. The linear predictor model predicts the signal amplitude at time m, $x(m)$, using a linear combination of past P samples $[x(m-1), x(m-2), \ldots\ldots.., x(m-P)]$ as follows

$$\hat{x}(m) = \sum_{k=1}^{P} a_k x(m-k) \tag{2}$$

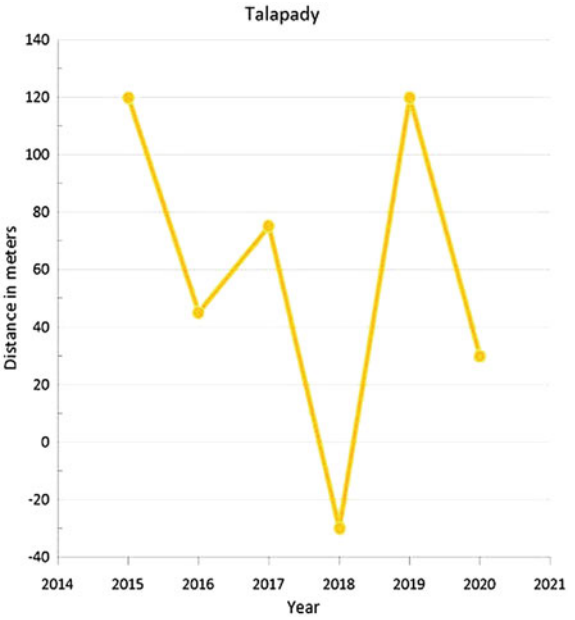

Fig. 13 Rate of erosion and accretion in Talapady region

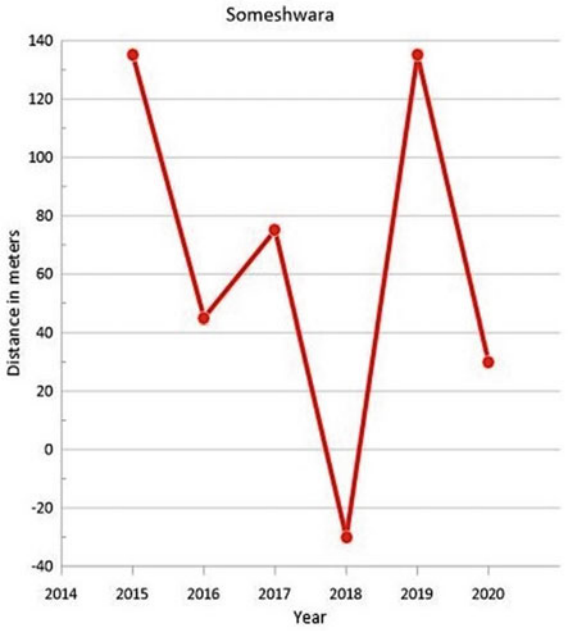

Fig. 14 Rate of erosion and accretion in Someshwara region

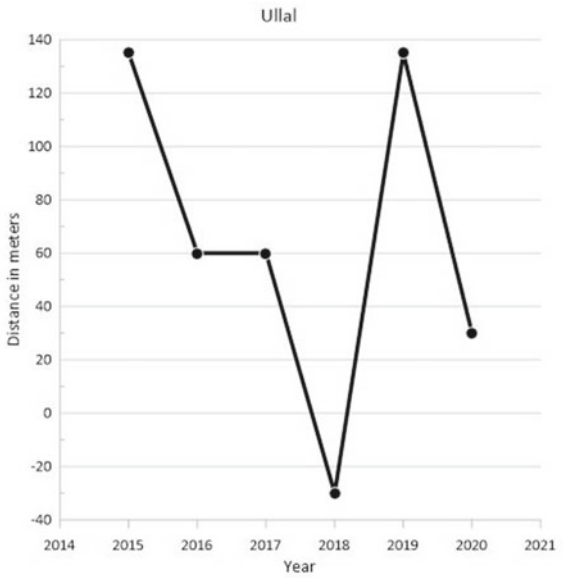

Fig. 15 Rate of erosion and accretion in Ullal region

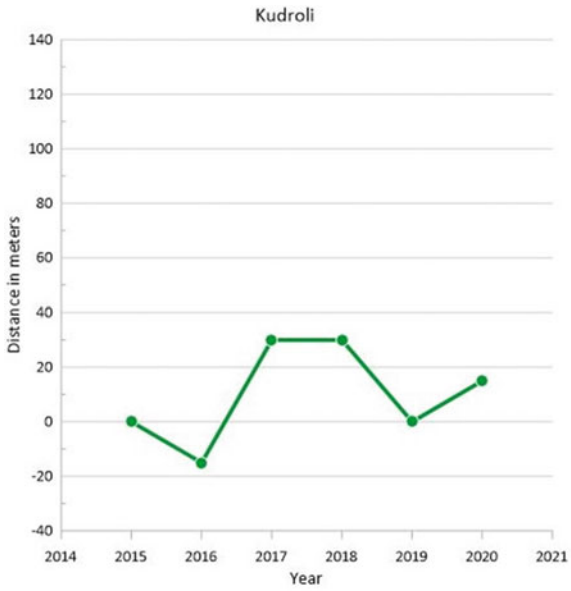

Fig. 16 Rate of erosion and accretion in Kudroli region

where integer variable m is the discrete-time index, $\hat{x}(m)$ is the prediction of $x(m)$, and a_k are the predictor coefficients. The prediction error $e(m)$ is described as the variance between both the actual sample value $x(m)$ and its predicted value $\hat{x}(m)$

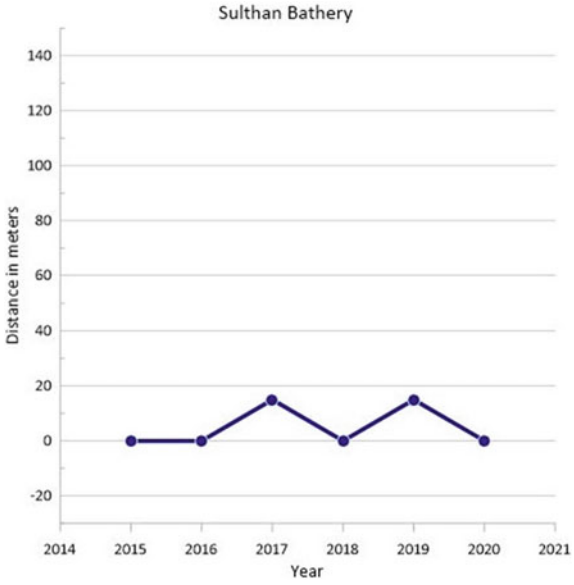

Fig. 17 Rate of erosion and accretion in Suthan bathery region

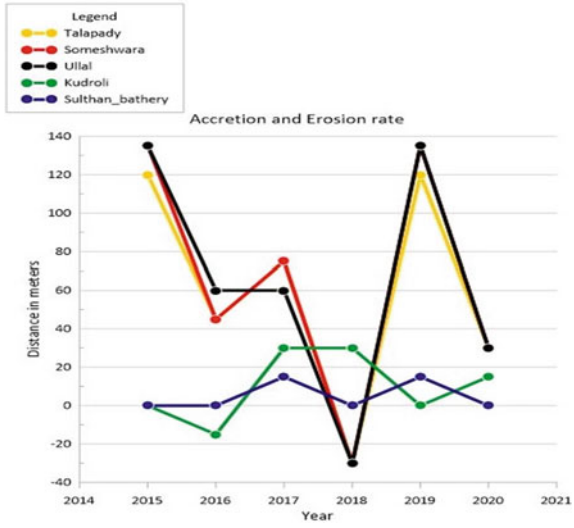

Fig. 18 Accretion and erosion rate of different regions of Mangaluru coast

$$
\begin{aligned}
e(m) &= x(m) - \hat{x}(m) \\
e(m) &= x(m) - \sum_{k=1}^{P} a_k x(m-k)
\end{aligned}
\tag{3}
$$

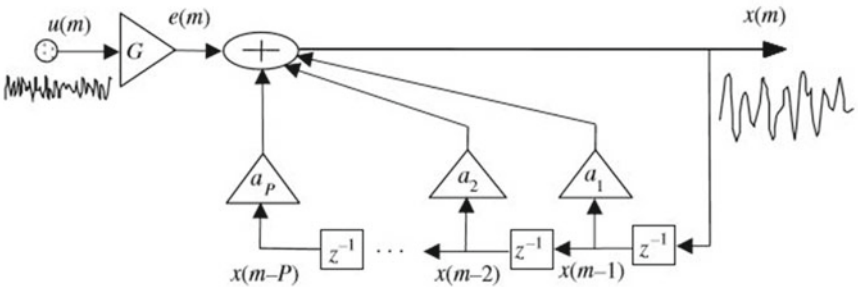

Fig. 19 Linear predictor model of a $x(m)$ signal

In a signal carrying information, $e(m)$ is the content of the sample $x(m)$, also known as prediction error which can also be considered as data. From Eq. (3), the following feedback equation can describe a signal generated by a linear predictor as

$$x(m) = \sum_{k=1}^{P} a_k x(m-k) + e(m) \tag{4}$$

Figure 19 depicts a linear predictor model of an $x(m)$ signal [20]. The prediction error in this model is $e(m) = Gu(m)$, where the zero-mean, unit-variance random signal is denoted as $u(m)$, and a gain term denoted by G, is the square root of the $e(m)$ variance

$$G = \left(E\left[e^2(m)\right]\right)^{1/2} \tag{5}$$

where $E[\cdot]$ is an operator of averages or expectations. The result of the z-transform of Eq. (5) shows that the linear prediction model is an all-pole digital filter with a z-transfer function

$$\boldsymbol{H}(z) = \frac{\boldsymbol{X}(z)}{\boldsymbol{U}(z)} = \frac{\boldsymbol{G}}{1 - \sum_{k=1}^{P} \boldsymbol{a}_k z^{-k}} \tag{6}$$

The best predictor coefficients are usually achieved by minimizing the mean square error criterion described as

$$\begin{aligned} E\left[e^2(m)\right] &= E\left[\left(x(m) - \sum_{k=1}^{P} a_k x(m-k)\right)^2\right] \\ &= E\left[x^2(m)\right] - 2\sum_{k=1}^{P} a_k E[x(m)x(m-k)] \\ &+ \sum_{k=1}^{P} a_k \sum_{j=1}^{P} a_j E\left[x(m-k)x(m-j)\right] \\ &= r_{xx}(0) - 2r_{xx}^T a + a^T R_{xx} a \end{aligned} \tag{7}$$

where $R_{xx} = E\left[xx^T\right]$ is the autocorrelation matrix of the input vector $x^T = [x(m-1), x(m-2), \ldots\ldots x(m-P)]$, $a^T = [a_1, a_2, \ldots.., a_P]$ is a predictor vector and $r_{xx} = E[x(m)x]$ is the autocorrelation vector. From Eq. (7), the gradient of the mean square prediction error for the predictor coefficient vector a is given by

$$\frac{\partial}{\partial a} E\left[e^2(m)\right] = -2r_{xx}^T + 2a^T R_{xx} \tag{8}$$

where the vector of the gradient is defined as

$$\frac{\partial}{\partial a} = \left(\frac{\partial}{\partial a_1}, \frac{\partial}{\partial a_2}, \ldots\ldots \frac{\partial}{\partial a_P}\right)^T \tag{9}$$

Setting Eq. (8) to zero, the least mean square error solution is obtained

$$R_{xx} a = r_{xx} \tag{10}$$

The predictor coefficient vector from Eq. (10) is given by

$$a = R_{xx}^{-1} \cdot r_{xx} \tag{11}$$

Equation (11) is also known as the Yule-walker equation and may also be written in an expanded form as

$$\begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ \vdots \\ a_P \end{pmatrix} = \begin{pmatrix} r_{xx}(0) & r_{xx}(1) & r_{xx}(2) & \cdots & r_{xx}(P-1) \\ r_{xx}(1) & r_{xx}(0) & r_{xx}(1) & \cdots & r_{xx}(P-2) \\ r_{xx}(2) & r_{xx}(1) & r_{xx}(0) & \cdots & r_{xx}(P-3) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ r_{xx}(P-1) & r_{xx}(P-2) & r_{xx}(P-3) & \cdots & r_{xx}(0) \end{pmatrix}^{-1} \begin{pmatrix} r_{xx}(1) \\ r_{xx}(2) \\ r_{xx}(3) \\ \vdots \\ r_{xx}(P) \end{pmatrix} \tag{12}$$

The Levinson–Durbin algorithm is an efficient method for solving Eq. (11) [20].

6 Results and Discussions

The Satellite imageries for the last 5 years are collected. Land and Water are differentiated as two main principal components using PCA with ERDAS Imagine software. The work showed that the PCA approach was a useful technique to compress the data for the study site. The PCA method differentiates land and water by providing the boundary line which can be considered as a good approach to calculate the soil erosion rate. Thresholding operation is performed using MATLAB. Erosion and Accretion rate are obtained by applying logical operation on images. For the last five years in regions of Talapady, Someshwara, and Ullal erosion rate is more compared to other regions of Mangaluru Coast. In the year, 2014–2015 the erosion rate is up to 135 m and in the year 2015–2016, the erosion rate was reduced to 45 m. In the year 2016–2017, the erosion rate increased up to 75 m and in the year 2017–2018, it reduced to 30 m. In Other regions Kudroli and Sulthan Bathery there has been an accretion of 15 m in the year 2015–2016 and in the year 2016–2017, there has been an erosion of 30 m. The major affected areas are Talapady, Someshwara, and Ullal regions where continuous erosion has beentaken place and the erosion rate is also high in these areas as compared to other regions of Mangaluru Coast. The developed work is compared with the state-of-the-art literature as follows. Ateeth Shetty et al. [18] used low tide images and topo maps of 1967 and satellite images of 1991, 2001, 2005, 2009, and 2013 and used image processing techniques. To compute shoreline changes, vector layers were created above the topo maps and satellite imageries are used. The government agencies constructed sea walls to protect against erosion; however, this resulted in the shifting of erosion from one place to another. In this paper, Machine Learning Algorithms are not implemented to predict soil erosion. However, in the proposed study, Machine Learning Algorithms are implemented to predict soil erosion and the developed model predicts soil erosion for the future years.

Rahisha et al. [4] discussed the application of image processing techniques for the detection of seashore using satellite imageries and GIS. The coastline changes over the last 33 years were studied. Topo maps of the Mangaluru coast are scanned and opened in ERDAS Environment. Landsat Images from 1989 to 2013 were used. Soil erosion was studied only during these years. Also, the prediction of soil erosion for

future years is not possible with the techniques developed. However, in the proposed study data till 2019 is considered and Machine Learning Algorithms are used to predict soil erosion for future years.

Olusola et al. [19] discussed the effects of increasing temperature on soil erosion in Nigeria. The different GIS and RS methods are used for the computation of soil erosion. Climate change has affected ecosystems and resulted in soil erosion. The development of various remote sensing techniques helped to compute soil erosion in the Ibadan coast of Nigeria. However, Machine Learning based techniques for the computation of soil erosion are not implemented. Using Machine Learning algorithms techniques, satellite imageries of the same region can be trained and a reliable model can be developed to predict soil erosion for future years.

The results of PCA, K-fold cross validation algorithm, Linear Predictor model are compared and discussed. The results of the PCA and K-fold cross validation algorithm are tabulated in Table 3. The results of PCA, K-fold cross validation algorithm, and Linear Predictor model are compared and discussed.

7 Conclusion

From the results, it has been found that the major affected areas are Talapady, Someshwara, and Ullal regions where continuous erosion has been taken place and the erosion rate is also high in these areas as compared to other regions of Mangaluru Coast. Also, for next the next five years, the same areas will have the same effect.

In future work, other Machine Learning algorithms such as Artificial Neural Networks and Support Vector Machines can be applied to the satellite imageries to produce more accurate shoreline changes. Also, deep learning using Convolutional Neural networks, Recurrent Neural Networks can be applied to the proposed work to obtain better results. The model can be developed by taking more than 15 years of data. Increasing the number of input datasets will help to obtain more accurate and better results.

Table 3 Comparison of K-fold cross validation (ML algorithm) and Linear prediction model (Mathematical model)

Place	K-fold cross validation algorithm results						Linear prediction model results					
	2019–20	2020–21	2020–22	2020–23	2020–24	2020–25	2019–20	2020–21	2020–22	2020–23	2020–24	2020–25
Talapady	110 m Erosion	50 m Erosion	70 m Erosion	25 m Accretion	125 m Erosion	110 m Erosion	130 m Erosion	55 m Erosion	85 m Erosion	32 m Accretion	122 m Erosion	130 m Erosion
Someshwara	130 m Erosion	40 m Erosion	70 m Erosion	35 m Accretion	130 m Erosion	130 m Erosion	145 m Erosion	55 m Erosion	78 m Erosion	35 m Accretion	145 m Erosion	145 m Erosion
Ullal	145 m Erosion	75 m Erosion	60 m Erosion	25 m Accretion	130 m Erosion	145 m Erosion	145 m Erosion	65 m Erosion	65 m Erosion	33 m Accretion	145 m Erosion	145 m Erosion
Kudroli	10 m Erosion	20 m Accretion	35 m Erosion	30 m Erosion	10 m Erosion	10 m Erosion	15 m Erosion	25 m Accretion	35 m Erosion	32 m Erosion	15 m Erosion	15 m Erosion
Sulthan Bathery	05 m Erosion	05 m Erosion	15 m Erosion	05 m Erosion	15 m Erosion	05 m Erosion	10 m Erosion	10 m Erosion	15 m Erosion	10 m Erosion	15 m Erosion	10 m Erosion

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Denoising of ECG Signal Using Optimized IIR Filter Architecture—A CSD-Based Design

Kunjan D. Shinde, Darshan Khanapure, Neha Shetti, Juveriya Athavani, and Nikhil Hattiholi

Abstract Signal Processing is a primary and important task in most of the applications involving signal acquisition and digital processing. Signal conditioning can be thought of as a process of removing unwanted information and preserving the required feature of the signal. Denoising can be similarly correlated with signal conditioning in this regard. The presented work is gives an IIR filter architecture that is optimized for area and speed metric for an end application of ECG signal processing. The proposed IIR filter uses Canonic Signed Digits (CSD) for representing scaled version of filter coefficients and then the IIR filter is designed. It is observed that by using CSD-based IIR filter architecture gives an efficient approach to denoise the ECG signals, demonstrates the area reduction by 90%, and improves the speed of operation by 60% when compared with conventional design. The Matlab and Xilinx Vivado platform is used to validate the designed IIR filter and further the post-synthesis implementation details are obtained for Xilinx Virtex-7 series XC7VX485T-2FFG1761C FPGA, Verilog HDL coding is employed to develop the design and stimulus environment for the work.

Keywords Digital filters · IIR filter · ECG signals · Bio-medical signal processing · FPGA · Filters · Verilog HDL coding · Digital signal processing

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1 Introduction

Signal processing has a wide range of applications that go far beyond its origins; it has created a platform to explore things around us with a mathematical perspective. Digital signal processing is the process of analyzing and modifying the signals in order to improve their efficiency or performance as desired by end applications. DSP includes a number of techniques for increasing the accuracy and reliability of bio-medical, multimedia signal processing, and more. Filtering removes particular frequencies to minimize background noise and attenuate interfering signals. Digital filtering is one of the most basic and important signal processing techniques. Filters may be of analog or digital types; Digital filters can be more precise and are used in applications like bio-medical signal processing, speech and image processing, data transmission, digital audio, telephone echo cancellation, etc.

Finite impulse response (FIR) and infinite impulse response (IIR) filters are the two main forms of digital filters. FIR filters are simple to design, operate, and are stable. But FIR filters require large computation power as the required filter order is large to implement the described frequency response. On the other side, IIR filter uses feedback operates at lower filter order, and is complex to design and implement the filters, With lower filter order and the use of advanced methods the IIR filter architecture can be improvised for applications involving lower sample rates.

Advantages of using IIR filters are not limited to less storage space and fewer coefficients are needed, but additionally, IIR filters offer better magnitude responses and are more analog model-likelier filter which is less expensive to implement. Because of the feedback channels, IIR are less numerically stable than their FIR counterparts. IIR filters' stability is a serious challenge to be addressed, as they frequently suffer from quantization errors. Few IIR filter coefficients can produce a steep filter response, which makes filtering faster than FIR. As a result, compared to FIR filters, IIR filters require fewer multiplier units to implement. IIR filters are therefore commonly employed in high-speed systems.

Bio-medical signals are quite sensitive to the environmental changes and are easily distorted by various noises in the process of signal capturing and storing. Electrocardiogram (ECG) signal processing has been a popular research issue since it depicts the vitals of human heart and its status is a direct impacting on human health. Heart rhythm, electrical activity, and heart rate are all shown by the ECG signal. An ECG signal contains both physiological and pathological data that are crucial for the diagnosis of cardiac diseases. There are several uses for ECG monitoring and the analyses that follow in the medical field. The morphological characteristics and interval components of the ECG signal can be distorted by various noises, which could result in a mistaken diagnosis and ineffective patient care [1].

The ECG signal's morphological characteristics include P-waves, QRS complex, T-waves, and U-waves. Interval features include PR-segment, ST-segment, PR interval, ST interval, RR interval, and others. ECG-based biometrics identification, seizure detection and monitoring, real-time electrocardiographic rhythm analysis, heart-rate variability analysis utilizing a smart electrocardiography patch, and the

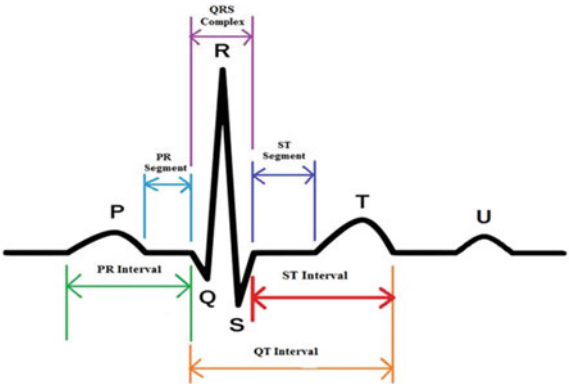


Fig. 1 A typical waveform of ECG signal

investigation of cardiac ischemia are just a few medical uses for ECG signals [1]. These applications demand an accurate determination of the morphological and interval aspects of the recorded ECG signal, which are susceptible to a variety of types of dominant noises, such as base-line wander (BW), muscle artifacts (MA) or electromyogram (EMG) noise, channel noise (additive white Gaussian noise, AWGN), power-line interference (PLI), and miscellaneous noises, such as composite noise (CN), random noise, and electrode motion artifacts. Estimating the latent, clean ECG signal from its noisy observation is the technique of ECG signal processing [1]. There are several approaches for reducing noise contamination from ECG signals, the IIR and FIR digital filters are frequently used to eliminate noise from ECG signals. A typical ECG waveform is shown in Fig. 1.

With the advent of technology, digital processing is employed in most of signal processing applications and availability of reconfigurable platform gives an opportunity to develop hardware efficient filters suitable for portable devices with moderate stability. Implementing digital filter on an FPGA has several advantages, including higher sampling rates than typical DSP processors, cheaper costs than an ASIC for modest volume applications, and greater flexibility than alternative approaches. Implementing an IIR filter on a field programmable gate array (FPGA) allows for high throughput while maximizing hardware efficiency, flexibility, and calculating accuracy at a fast rate. In this case, implementing a digital IIR architecture on an FPGA is quite beneficial in achieving high performance.

The following are existing research carried out on digital filters and have been referred to develop the presented work.

In [1], the detailed study on the ECG signal and various noises being influenced is analyzed in detail along with best-suited methods to remove the noise. The sample of ECG signals from MIT-BIH database is referred [2] and used for analysis in the presented work (Sample information: Person 1, record 1). In [3], design and implementation of IIR filters on an FPGA device is carried out on Virtex-5 XC5VLX50T-3 FPGA board, and synthesis is performed with Xilinx ISE Design Suite 14.7. Three different types of IIR filters are discussed Loss integrator-based look-ahead IIR filter, two-level parallel-pipeline IIR filter, and suggested FIR-based IIR filter. The study

gives an possible architecture for IIR filter design and opportunity to explore CSD in them. In [4] FIR-based IIR filter is designed with a maximum operating speed of 285.105 MHz, optimization is achieved in terms of critical metric considered for FPGA-based implementations. The targeted FPGA is Altera EP4CE115F29C7 and validation is carried using Quartus II synthesis tool. In [5], various FIR filter architectures are compared and the critical path evaluation is considered to find out the bottleneck of the FIR filter design. In [4] FIR acts as an important block and hence we have gone through the [5] to understand the design and implementation details of FIR filter. RTL implementation of various architectures is focused while justifying the critical path and the computation complexity involved. The use of symmetric coefficients (SC) is a key in reducing the area constraints of the filter, and further use of data representation for the coefficient is addressed with CSD, and its impact is discussed. In [6] the filter is designed using two architectures which are parallel and programmable multiplexing. The fixed-point number representation is used to represent the data and filter coefficients; VHDL RTL coding is employed to design the filter and implemented on SPARTAN3E XC3S500EFG320-4 FPGA. In [7], a new FPPE architecture is used to create an IIR filter, and partially folded arithmetic function architecture is modeled. Register allocation is done using the pipelined register design (PRD) algorithm. The modules are developed in Verilog and run on Xilinx Virtex 6 FPGA. The FPPE method results in efficient area architecture with fewer registers and logical components owing to the PRD algorithm and folding operations. In [8] IIR filter is constructed and simulated using VHDL coding on a FPGA platform. The MAC algorithm, which uses multiple operations, is used to achieve the design. The use of a parallel pipelined structure allows for full utilization of the lookup table on the target device. The multiplier function is implemented using DSP48E and DSP48 slice-based FPGAs. The IIR filter is synthesized for Virtex-5-based XC5VLX330 FPGA and Spartan 3DSP-based XC3SD1800 FPGA to test the speed and resource utilization. The Virtex-5-based system can function at an estimated frequency of 81.5 MHz, whereas the Spartan 3 ADSP-based design can only operate at 40.1 MHz. Yadav and Nandi [9] describes a technique for increasing the IIR filters' occupied area and delay by utilizing various registered adders and a shift mechanism. Registered additions and hardwire shifts are two different types of multiplications. A Canonical Signed Digit representation of the filter coefficients is used. For hardwired shifts, a barrel shifter is used, and high performance RCA and parallel prefix adders are compared for addition. Verilog HDL coding is used to model and synthesize. Various parallel prefix adders and conventional adders are referred for the work. In [10] a 64-tap IIR filter was implemented on FPGA using Fully Parallel and Partial Serial designing architectures. Fully parallel architectures are commonly employed in design because of the speed with which they operate. The serial form is easier to implement than the parallel form, but the speed suffers since it follows a step-by-step formation in which the result of one stage becomes the input of the next, and so on. The design is simulated and implemented using HDL code on the Spartan3E XC3S1200E FPGA. The partially serial architecture is a better design because it requires fewer LUTs on chip and fewer multipliers, reducing the overall area occupied while some impact can be observed on speed metric. In [11], design of

a low pass IIR Elliptic filter for high frequency noise reduction in an ECG signal is performed using a MATLAB Simulink model and Xilinx system generator blocks. The Elliptic approximation exhibits an equiripple response. MATLAB FDA Tool was used to design the filter, while XSG was used to generate the Simulink model. The implementation was made on Xilinx ISE 14.2 on SPARTAN 3E device. In [12–14] the optimization in performance of adder unit is discussed and various adders are compared. It is observed that the kogge-stone adder out performs the conventional adders and the same analogy can be referred for future work.

The purpose of this research is to increase the performance of the IIR filter architecture while comparing it to the conventional IIR filter architecture. Due to the diverse FPGAs used in the literature for various end application, the IIR filtering concept and possible architectures for the study are undertaken.

2 Design of Digital Filter

2.1 Requirements of Digital Filter—Application Perspective

In the previous sections, we have understood the various architectures and methods involved in the design process of IIR filter and also looked into FIR filters as some reference work used FIR filter as one of the building blocks in IIR filters. As the merits of IIR and FIR filters are discussed early, in the presented work we have chosen the IIR filter for the design and analysis purpose due to its lower filter order and opportunity to explore IIR filter architecture on a reconfigurable platform.

An ECG signal typically has a dynamic range of 1–10 mV and a frequency range of 0.05–100 Hz. The letters P, Q, R, S, and T are used to identify the five peaks and valleys that make up the ECG signal (ref. Fig. 1). In the ECG signal, there is a U wave that has very small amplitude or, more frequently, is not present at all. A P wave (atrial depolarization), a QRS complex (ventricular depolarization), and a T wave are the three main electrical entities that make up an ECG trace (ventricular repolarization). The ECG signal is impacted by various sounds while it is being acquired and transmitted. In the ECG signal, there are primarily two types of sounds. Electromyogram noise, additive white Gaussian noise, and power-line interference are examples of high frequency noises [1]. Baseline wandering is one type of low frequency noise. The ECG signal may be misinterpreted due to noise contamination. The ECG signal obtained from physionet database [2] was captured for 10 s and digitized at 2000 Hz with 16-bit resolution.

In the presented work we have considered the end application to be bio-medical signal processing. The objective of the work is to develop IIR filter to meet the requirements to denoise the ECG signals and to develop an environment to test and validate the designed filter with real-time ECG signals being read and written back.

To denoise the ECG signals, it is suggested to use a low pass filter, we have chosen a low pass filter designed with chebyshev type II method, cutoff frequency

to be 100 Hz, and sampling rate to be 2000 Hz, attenuation in stop band to be 60 dB and introduced a noise component of type AWGN measured to 10. With these requirements for the ECG signal denoising the IIR filter coefficients are required.

2.2 IIR Filter Realization Using Difference Equation

The functionality of the filters can be described in many different ways; An IIR filter's z domain transfer function has a non-trivial denominator that describes the feedback terms and provides information on the filter's frequency and magnitude properties, whereas the filter described using difference equation gives the implementation details on the filter to be designed. Magnitude and frequency response is important while obtaining the filter coefficients and implementation details obtained through difference equation is necessary while developing RTL code for the filter.

A system such as IIR filter that depends on both present and previous inputs as well as on past outputs is defined using the following difference equation.

$$y[n] = \sum_{l=1}^{N} a_l y[n-l] + \sum_{k=0}^{M-1} b_k x[n-k] \tag{1}$$

where

$y[n]$ = output signal

$x[n]$ = input signal

a_l = feedforward filter coefficient

b_k = feedback filter coefficient

N, M = iterations of samples being processed.

From Eq. 1, we can observe that the difference equation gives the implementation required in terms of delay element, adder/subtractor and multipliers. Expanding Eq. 1 and implementing the same results in direct form representation.

Figure 2 shows direct form I representation of IIR filter this method of signal flow is known as filter architecture. The IIR filter is a recursive filter since the output is calculated using the input, outputs from previous iterations, and current input. A discrete-time filter's structure typically produces an infinite impulse response when there is feedback.

The IIR filter architecture, as shown in Fig. 3. is based on Direct Form II architecture. A two-pole filter section is followed by a two-zero filter section, in this case. In terms of delay, it is canonical. This occurs as a result of common delay components between the two-pole and two-zero portions. The poles and zeros are susceptible to round-off errors in the coefficients, as is the case for all direct form filter designs,

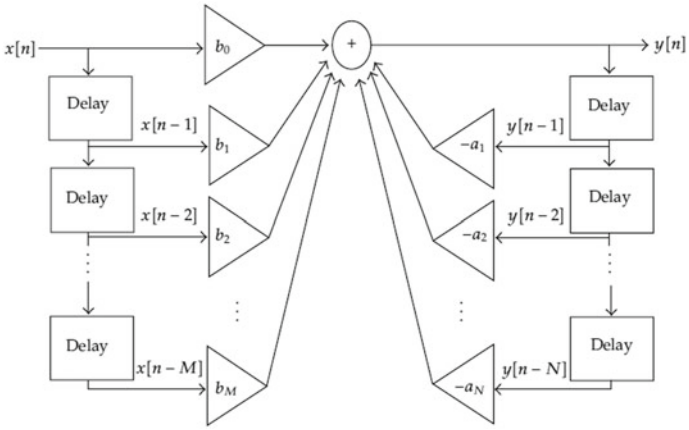
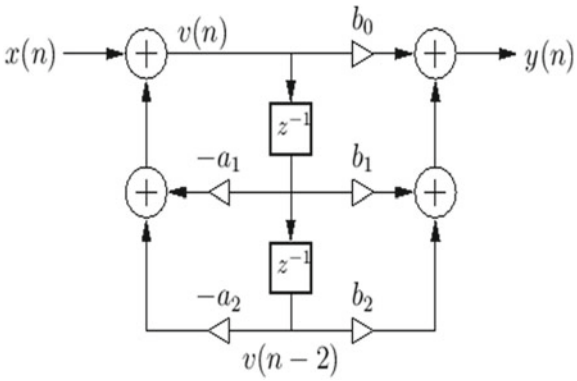


Fig. 2 Block diagram of IIR filter using direct form I architecture

Fig. 3 Block diagram of direct form-II IIR filter architecture



particularly for large transfer-function orders. Using ladder or lattice filter architectures, or series low-order sections (like second order), one can get lower sensitivity [3–6].

3 Proposed IIR Filter Design

The conventional approach to implement the IIR filter is discussed in the early sections, in the presented work we will be using the direct form I representation and the proposed architecture uses a constant multiplication approach where the input and its delayed version are multiplied using shift-and-add method and similarly at the output side also as indicated in Fig. 4.

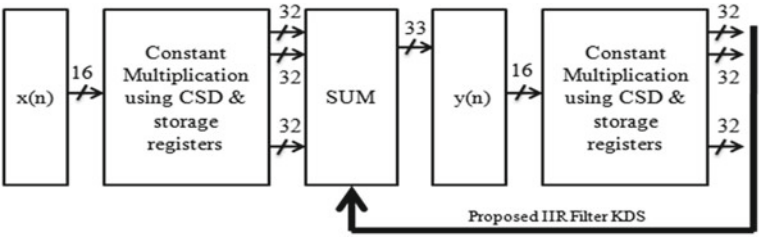


Fig. 4 Block diagram of proposed IIR filter architecture

3.1 Proposed IIR Filter Design

The block diagram of the proposed IIR filter architecture is given in Fig. 4; here the multipliers are replaced by shift-and-add method-based multiplier. In such DSP algorithms used to denoise the ECG signal, the filter under study is important and how it is being implemented also matters, as in the IIR filter architecture the multiplier is a critical block that directly impacts the filter performance, optimizing this block will yield in better filter design and hence the CSD-based constant multiplication is realized as it eliminates the multiplier from the design and realizes the multiplications operation with series of sift and add based multiplication. Further, the impact of CSD-based constant multiplication is elaborated, and thereby using CSD approach we have reduced the number of addition/subtraction required for respective constant multiplication. In the later stage horizontal and vertical sub-expression elimination methods can be applied to further reduce the resources required for constant multiplication. The sum block adds the data flowing within the setup and output of full precession is obtained from y(n). Due to the constant multiplication unit, both at the input side and at the feedback loop, the critical path is limited to the maximum of largest delay associated with single shift-and-add method represented for largest coefficient multiplication each on both the sides and hence the fast computation in proposed work while reducing the area used to implement the multipliers.

3.2 Canonic Signed Digit (CSD) Representation

Digital filtering algorithms for digital signal processing necessitate a huge number of multiplications [9]. It is possible to design coefficient memory to take advantage of coefficient properties. CSD representation is an elegant way to make digital multipliers work more efficiently. It is used to simplify hardware construction due to its properties. The CSD code approach reduces the amount of addition/subtractions and shift registers used to implement multiplication designed with shift-and-add method and also speeds up the calculation process and achieves hardware simplification.

The CSD representation requires that no adjacent digits are non-zero. The reduction of non-zero digits in this scheme allows replacing full multipliers with ones

using shift-and-add, resulting in more efficient implementations of multiplication. As a result when compared to binary representation, CSD representation is more efficient and uses 33% fewer non-zero bits [9]. The following is a generalized CSD representation notation format

$$X_{1,0} = \sum_{r=0}^{B-1} x_r 2^r \tag{2}$$

$$\text{where } x_r = \text{can take the values as } 0,\ 1,\ -1$$

Let's consider an example, an integer 15 in binary is written as 01111 when multiplied by an input $\boldsymbol{x}$ it will require three adders with three shifted versions of the input signal $\boldsymbol{x}$ i.e., $\boldsymbol{x \ll 3 + x \ll 2 + x \ll 1 + x}$, here the symbol $\ll$ represents right shift operation by a number of positions mentioned to the right. Whereas the same number 15 in CSD is represented as 1000 $\bar{1}$ ($\bar{1}$ is the subtraction of the input quantity) which becomes $\boldsymbol{x \ll 4 - x}$ and we can observe that this process requires only a single subtractor. Hence using CSD techniques we use fewer resources to implement multiplication and further it gives better performance.

3.3 Resource Requirements for IIR Filter

To understand the impact of resource utilization, let us analyze the implementation hardware required for the IIR filter with the end application considered above and with details of filter design as mentioned in Tables 1 and 2.

From Table 1, it is observed that the proposed FIR filter architecture uses only delay elements and adders to realize the IIR filter and there is a zero need for multipliers as the multiplication is implemented using shift-and-add method. Comparing resource requirements of direct form I and II architecture, there is not much difference that can be identified apart from the delay elements being reduced to half in direct form II when compared with direct form I.

Table 1 Resource requirements of IIR filter architectures

Filter type		Resources required IIR filter order 7 with given filter design specifications		
		Delay Elements	Multipliers (size)	Adders/Subtractor (size)
Conventional IIR filter	DF-I	16 (16 bit)	16 (16 × 16)	15 (32 bit)
	DF-II	8 (16 bit)	16 (16 × 16)	15 (32 bit)
Proposed IIR filter		**58 (32 bit)**	**0**	**52 (32 bit)**

Table 2 IIR filter specifications

Filter structure	Direct form I
Number of sections	1
Filter stability	Yes
Linear phase	No
Design algorithm	Chebyshev type II
Sampling frequency	2000 Hz
Filter order	7
Filter response	Low pass
Passband edge	100 Hz
Stopband edge	200 Hz
Pass band ripple	1
Stop band attenuation	60 B

4 Results and Discussions

In this section we will elaborate on the presented work, the following sub-sections are made to provide clarity on the simulations and design specifications used in the IIR filter design and ECG signal referred for the work.

4.1 Experimental Setup

The digital filter specifications are given in Table 2, using these specifications we have obtained IIR filter coefficients.

4.2 Resources and Tools Used

i. **ECG Signal**: The sample ECG signal is captured from the website called *physionet* which is a standard database for bio-medical signals and the recorded ECG signal is considered for the presented work. The platform physionet is a large collection of recorded physiological signals that are accessible for free through *PhysioNet*, along with accompanying open-source software *PhysioToolkit*. Refer sample number with details mentioned in [2].

ii. **Filter Coefficients**: In Matlab platform, we can design filters and obtain filter coefficients using Filter Design and Analysis Tool (FDATool) using keyword *filterDesigner* on the command line. It is an effective user interface for quickly constructing and analyzing filters. By entering filter specifications as shown in Table 2, *fdatool* enables you to create digital FIR or IIR filters. The coefficients

of the desired filter can be employed depending on its magnitude and frequency response. The magnitude response obtained is shown in Fig. 5.

iii. **RTL Coding**: With the help of Xilinx Vivado 2018 environment, Verilog HDL coding is used to develop design and stimulus for the IIR filters and to develop a stimulus, a test environment is created to read and write the ECG signals from Matlab R2018.

iv. **FPGA for Implementation**: The designed IIR filter is synthesized Xilinx FPGA Virtex-7 XC7VX485T-2FFG1761C and after the post-synthesis/Device implementation process, the resource utilized are captured and tabulated in Table 3.

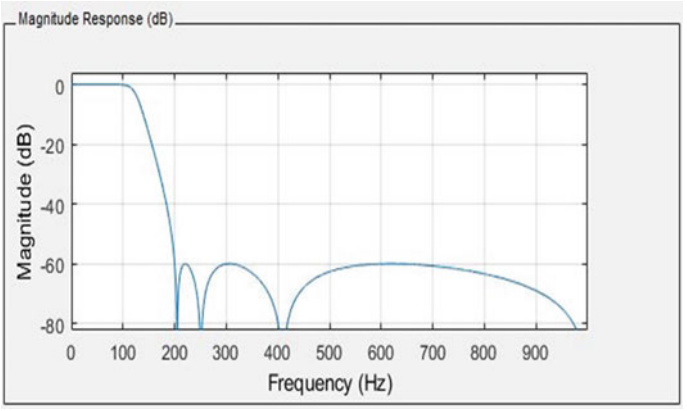


Fig. 5 Magnitude versus frequency response of the IIR filter of order 7

Table 3 Device utilization summary without DSP48 slices on Xilinx Virtex-7 XC7VX485T-2FFG1761C FPGA

Logic utilization	Available	IIR filter using conventional method used	Proposed IIR filter using CSD coefficients used
Number of LUTs	303,600	1499	13
Number of flip flops	607,200	769	22
BRAMs	1030	0.00	0.00
URAM	0	0	0
DSP	2800	0.00	0.00
Path delay	–	10.805 ns	4.09 s

4.3 Simulation Results

i. **Magnitude Versus Frequency Response**: With the given specification for filter design, we can see that the transition band is from 100 to 200 Hz and the 1st side lobe is at 200–250 Hz with attenuation of 60 dB and no attenuation is observed in pass band from 0 to 100 Hz. With this nature of magnitude response we have considered the chebyshev type II to be more suitable for the filter design mentioned.

ii. **Plotting ECG signal on Matlab environment**: Executing the raw ECG signal data obtained from MIT-Physionet Arrhythmia database is in the .mat and plotATM file which are readable on Matlab. From the files extracted we can observe the ECG signal in Fig. 6, there are two versions of the ECG signal provided in Fig. 6, i.e., with noise and filtered version as indicated. In the presented work we have extracted the filtered version of the signal and introduced measure noise AWGN of 10 and then the noisy version of the ECG signal is given to Xilinx environment. The original noisy signal obtained from the source [2] dose not consist of information on the noise present and hence we have introduced the known amount of noise in the filtered version of the original signal.

iii. **Simulation on Xilinx Vivado 2018**: The designed IIR filters are called as a component in the stimulus environment. This is the test bench where the design block is passed with a set of values obtained from Matlab environment and the filtered version from the designed IIR is displayed as shown in Fig. 7. This validates the Denoising of ECG signal for the introduced noise of type AWGN and validates the functionality of IIR filter for the said so end application. Identical results are obtained for the IIR filters considered in the presented work as direct form I and proposed CSD-based IIR filter architecture.

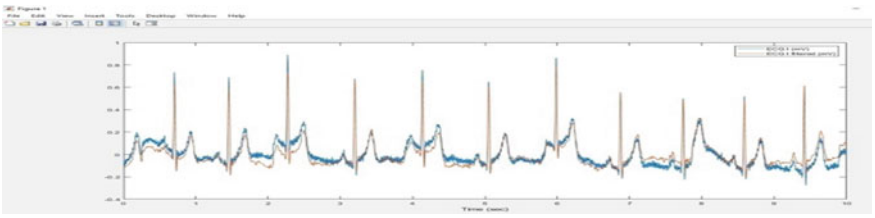


Fig. 6 ECG signal waveform in MATLAB

Fig. 7 Denoised ECG signal on Xilinx Vivado 2018 platform

4.4 Comparative Analysis

Table 3 gives a summary of utilization of all logic elements like number of LUTs, Flip Flops, DSP slices, and Path delay, these are the performance metric to be observed in the case of FPGA, where the LUT, Flip Flop, and DSP slice gives the area implications of the IIR filter design and path delay gives the maximum allowable frequency for the design. Comparing the conventional IIR filter with the proposed CSD-based IIR filter, it is observed that the proposed work is area efficient and uses less path delay to compute the results. In other terms, the CSD-based IIR filter design is faster and optimized for identified end applications.

4.5 Implementation Details

Figure 8 gives the implementation details of CSD-based IIR filter developed for denoising of ECG signals. The region under X0Y0 highlighted gives the implemented IIR filter. The device implementation is captured for Virtex-7 XC7VX485T-2FFG1761C FPGA.

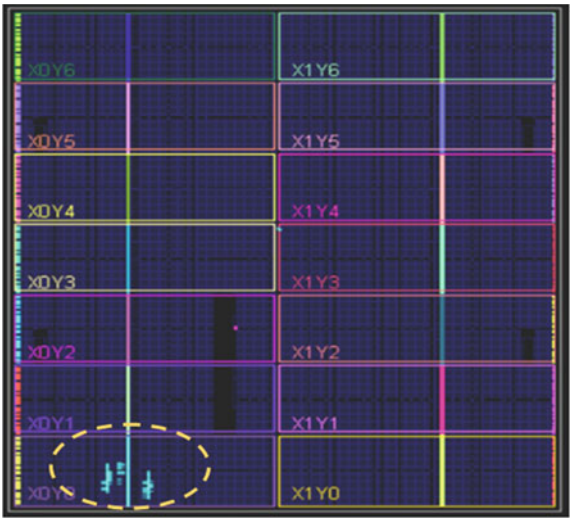


Fig. 8 Implementation details of CSD-based IIR filter on targeted FPGA

5 Conclusion

The presented work gives a detailed study on bio-medical signal processing using IIR Filter; the noise component that is present in ECG signals must be removed since it corrupts the signals in many different ways. The proposed IIR filter architecture uses CSD notation to implement constant multiplication of filter coefficients and improve the performance of the IIR filter under study. As CSD is an elegant method to implement digital multipliers in a more efficient way. From the tabulations and comparative study presented in this paper the IIR filter designed with CSD technique gives optimized implementation for IIR filter. Such techniques are best suited for time critical and area efficient portable ECG signal processing units.

Further optimization in CSD can be introduced in terms of horizontal and vertical sub-expression elimination and block level optimization/improvement can also be made possible with the help of retiming techniques and use of high-speed adders. The presented work can be treated as a reference to evolve the work described.

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Conflict of Interest We the authors would like to declare that there is NO Conflict of Interest on the research work presented.

NO data sets were generated or created in the process. ECG signal of record mentioned in [2] is used for the presented work.

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Deep Learning Analysis for Skin Cancer Detection

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Abstract In the present world, skin cancer is the most widely recognized reason for death among people. Skin malignancy is an unusual development of skin cells. Frequently created on the body part exposed to the sunlight; however, it can happen on any place on the body. The majority of the skin malignancy is treatable at the beginning phase. So an early and quick identification of skin disease can spare the patient's life. With the new innovation, early identification of skin malignancy is conceivable at the introductory stage utilizing picture handling. The skin cancer detection using image processing is based on the detection of skin cancer types at its earliest stage. There are many types of skin cancers found. It is difficult to identify the type of skin cancer at the earlier stage, manual identification can often be time consuming and inaccurate. Doctors are able to identify the symptoms of skin cancer but are unable to identify the type of skin cancer in the initial stage. So the doctors will wait until it gets blotted but by that time the disease will become out of control. So a software is developed to help the Skin Cancer Detection at its earliest stage by passing valid input images. So this chapter explains about a method to identify and classify the skin cancer using images using Convolutional Neural Network (CNN) algorithm. The accuracy obtained by using the proposed method is 89%.

Keywords Skin cancer · CNN · Accuracy · Malignancy · Classify

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1 Introduction

Skin is a peripheral layer of the human body that shields our body against outsider particles. There are a few maladies which influence the skin. One among them is skin malignancy. Skin malignancy ought to be perceived in earlier or probably it may prompt passing managing circumstances. Skin malignant growth starts when changes happen in the DNA of skin cells [1, 2].

There are various kinds of skin malignant growth to be specifically melanocytic nevi, melanoma, benign keratosis-like injuries, basal cell carcinoma, actinic keratosis, vascular sores, and dermatofibroma. The beginning phases of skin malignancy can be agonizing sores that tingle or consumes, or even cause expanding on the skin and so on. Roughly 50 percent of individuals disregard it thinking of it as a smear, which is dangerous. And furthermore, the primary issue is to distinguish which kind of malignancy it is. So a program is developed which can naturally identify the sort of skin malignant growth. Among different organization models utilized in profound learning, Convolutional Neural Networks (CNN) are generally utilized in picture recognition. CNNs have been utilized for the recognition of Skin Cancer at the beginning stage.

CNNs comprise convolutional layers, which are sets of picture channels tangled to pictures or highlight maps, alongside other (e.g., pooling) layers. In picture grouping, include maps are extricated through convolution and other preparing layers dully and the network inevitably yields a mark showing an expected class. Given a training dataset, CNN upgrades the loads and channel boundaries in the shrouded layers to produce high lights reason able to tackle the characterization issue. On a basic level, the boundaries in the network are upgraded by back-propagation and inclination plunge ways to deal which limit the classification error.

Lau and Al-Jumaily [3], the work is directed on automatically early identification of skin malignant growth study dependent on neural network classification. In light of the investigation, BNN shows the general aftereffect of high precision than ANN. Jafari et al. [4], a profound Convolutional Neural Network (CNN) design for extraction of sore locale from skin pictures is proposed and precision is appeared in the test result. Vijayalakshmi [5], the work is directed on Melanoma Skin Cancer Detection utilizing Image Processing and Machine Learning. In this paper, Support Vector Machine (SVM) is utilized to order the dangerous and benevolent skin disease pictures. Jayalakshmi and Kumar [6], performance analysis of convolutional neural organization (CNN) based harmful skin sore identification framework focuses on distinguishing the sort of skin disease whether it is threatening or benevolent dependent on the characterization of dermoscopic pictures. For the investigation of a skin sores these dermoscopic pictures give profound knowledge. Here initially we utilize the Convolutional neural organizations model to arrange the dermoscopic pictures and to distinguish the sort of malignant growth. This model will be prepared well. To improve precision of order we further utilize the bunch standardized Convolutional neural organization [7, 8].

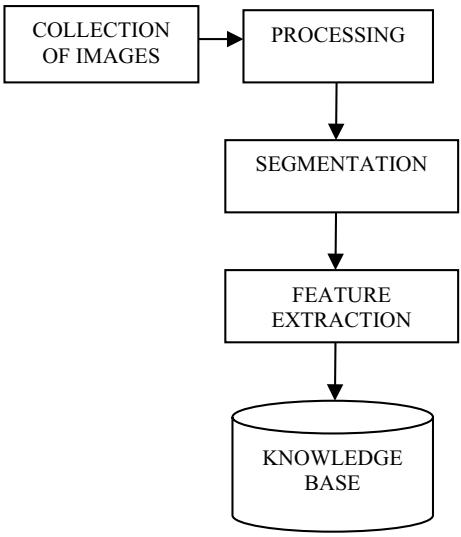

Fig. 1 Testing phase 1

2 Proposed Methodology

The proposed work will help people and doctors also to identify the type of Skin Cancer at the initial stage.

2.1 Training Phase

A set of types of skin cancer images is collected from KAGGLE and is pre-processed using Convolutional Neural Network (CNN) algorithm [9]. Further these images are segmented for feature extraction as depicted in Fig. 1. These features are stored in the knowledge base.

2.2 Testing Phase

The image to be tested is given as an input by the user which is then pre-processed and segmented similar to training phase depicted in Fig. 2. The feature extracted is matched with the knowledge base obtained by the training phase and the result is displayed [10].

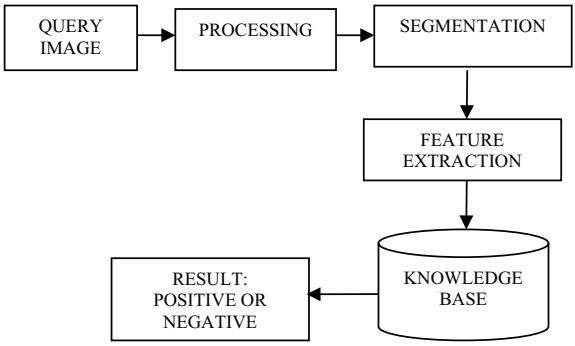

Fig. 2 Testing phase 2

2.3 Detailed Design and Methodology

Here there are four main entities, i.e., considering an input image, pre-processing, feature extraction, and classification using CNN. First, the input data has to be loaded. Goal of the next step is to make the collected image more suitable for subsequence processes, i.e., pre-processing so in the feature extraction step the features of the data set are extracted. Later, for classification purpose Convolutional Neural Network (CNN) algorithm is used as depicted in Fig. 3. Then the features in skin cancer types of the training phase are compared with the testing phase and required results are generated [11, 12].

The proposed system involves the following steps. First step involves pre-processing of captured images. The pre-processed image undergoes feature extraction, where various features of the Skin Cancer types are extracted and certain algorithms are applied. The data that is stored is compared with the pre-processed image and an approximate result is generated [13].

A computer reads an image in the form of RGB for colored images. Here RGB is the three channels. Each of these channels will have their own pixel values. When we say, the size of an image is BxAx3 it means that the pixel values of the image have B rows, A columns, and 3 channels. This is how a computer reads an image [14].

In fully connected network when an image is read usually a large image it often leads to overfitting. For example, consider an image with size $200 \times 200 \times 3$ that is with 200 rows, 200 columns, and three channels. The number of the weights in the first hidden layer itself will be nearly 1,20,000 which is a huge number and will lead to overfitting. This is the main reason that the fully connected layer is not used when it comes to image classification. The reason for using CNN for image classification is that here the neuron in each layer will be connected to only few neurons in the next layer which decreases the number of weights and also uses a smaller number of neurons. Convolutional neural network are the special type of feedforward artificial neural network in which the connectivity between the layers is inspired by the visual cortex. Here is how exactly the CNN works. Basically, the convolutional neural network shave 4 layers that are the convolutional layers, ReLU layer, pooling layer,

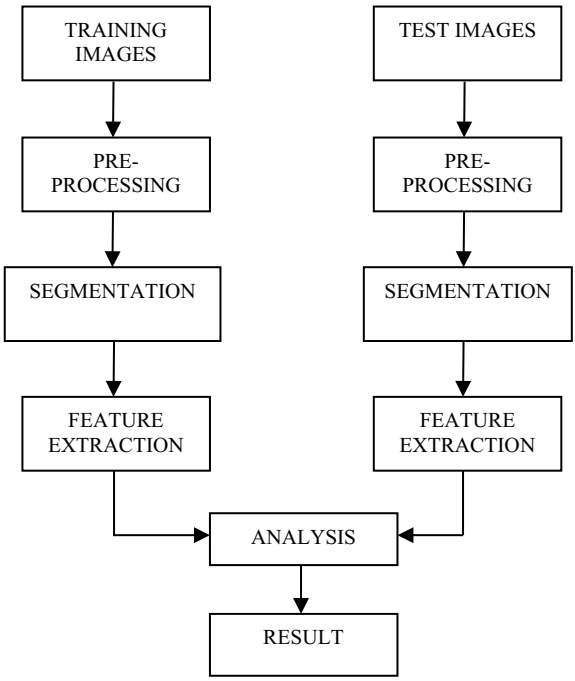

Fig. 3 System architecture

and the fully connected layer. In convolution layer after the computer reads an image in the form of pixels, then with the help of convolution layers we take a small patch of the images. Fully connected layer: The layers have to be stacked up after passing it through the convolutional layer, ReLU layer, and the polling layer. These layers need to be repeated if needed unless you get a 2×2 matrix. Based on this list we classify the input images [15] (Fig. 4).

3 Experimental Results and Discussions

The dataset consists of seven categories of Skin Cancer. Melanocytic nevi, Melanoma, Benign keratosis-like lesions, Basal cell carcinoma, Actinickeratoses, Vascular lesions, and Dermatofibroma are the seven types of skin cancer. This model uses the HAM10000 dataset. This is processed on a CPU, Importing Libraries. It is a collection of functions or methods which allows you to perform the actions required.

This proposed work includes Matplotlib, Numpy, Pandas, Torch, Seaborn, Glob, Sklearn, and Keras.

- Numpy: It is a tool used to work with arrays and different operations.
- Matplotlib: It is used to plot a graph, used in histogram or barplots.

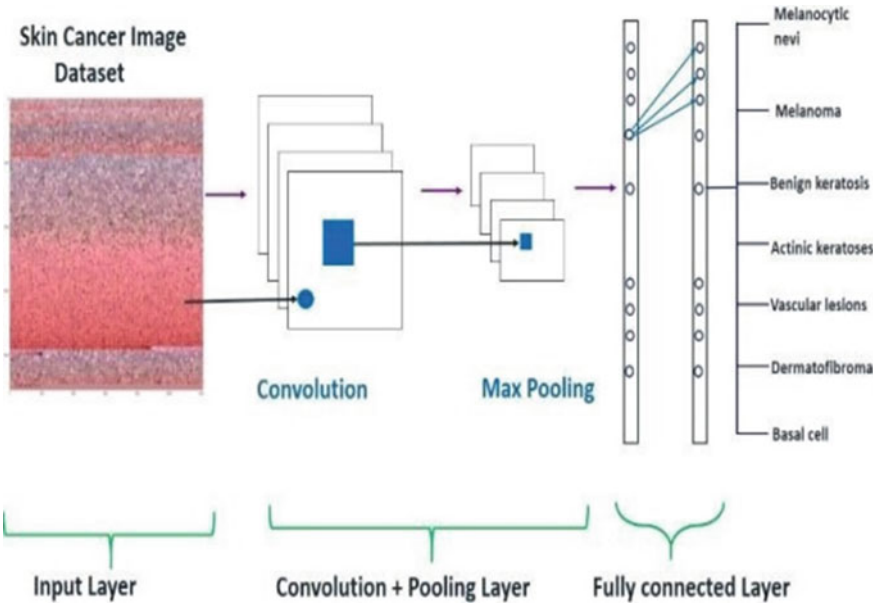

Fig. 4 CNN applied on a skin image

- Pandas: It is used for machine learning in the form of data frames. It is also used to import various files like csv and Excel.
- Sklearn: Used in machine learning for classification, regression, etc.
- Keras: It is used for deep learning. It makes deep learning models as fast and easy as possible.
- Seaborn: To plot graphs.
- Glob: Used for pattern matching library.
- Torch: Responsible for training the model.

One more function is used to plot validation loss/accuracy. Making dictionary of images and also labels. There are two folders in the dataset. Merging images from both folders into one dictionary and labeling seven types of Skin Cancers is required. This dictionary is used for displaying labels later on. It is very human friendly. We are creating a path for each image in the dataset.

3.1 Reading the Data and Processing

To merge the image folder and the csv folder a path is created. Also creating new columns for organization of data and better readability. Loading and adjusting pretrained models in PyTorch. Here the features are extracted using torch vision model. Due to PyTorch, well-established models are obtained. The proposed model

is Resnet50. The proposed model is derived from the standard Resnet50 model architecture, which is already proved to perform well on classification tasks. Here all the model parameters are updated to perform new task. Loading the pretrained Resnet50 and adjusting the last layer is for feature extraction.

3.2 Split the Data

The dataset consists of 10,015 images. This is the step where the dataset will be split into training data, testing data, and validation data. A validation dataset is a sample of data used to provide an unbiased evaluation of a model fit on the training dataset while tuning model hyperparameters. The evaluation becomes more biased as a skill on the validation dataset is incorporated into the model configuration. Here, the test set will be split into the validation set and test set, i.e., 5% each.

3.3 Train the Model

In the proposed work, the number of iterations has to be set, i.e., epochs as 5. We calculate the training error and testing error after training the model per epoch. Initially, it will be zero and soon. So basically, after 100 images are passed, the error will be appended to training error. It will be stored temporarily. The mean is computed, an average of 100 images are stored in training error. Then the model is trained where the model will learn from the images, i.e., pixels and value of the image. The model will be stored in the CPU. The predicted as well as the actual output is obtained. Criterion is used to calculate the difference between the predicted and the actual output. Backpropagation optimizer technique is applied to make the model better over time. The same steps are performed for validating the error. Plot the graph based on the error generated. The proposed model is tested on the testing data set for accuracy. The model is evaluated again. Test generator will be created with two models, one model will generate predicted output and the other one will provide the actual output. The probability of seven values associated with each class, anyone will have a high probability. This will be stored in the result. Check both the predicted as well the actual value and assign if true if matching else false. Creating a confusion matrix for the above. The proposed model obtained 89% accuracy rate.

3.4 Design a User Interface

User Interface for this project is designed using Django which is a Python based tool for web application design. With the help of this UI, user can select any input skin images, it will be processed at the backend and the final result will be displayed back to the user.

Table 1 Testing of the data samples

TC #	Description	Expected result	Actual result	Status
TC-1	When submitted without any image	Key error	Key error	Pass
TC-2	When the image of the skin cancer patient is entered	Skin cancer detected	Skin cancer detected	Pass
TC-3	When the image of a normal patient is entered	Skin cancer not detected	Skin cancer not detected	Pass

3.5 System Testing and Unit Testing

Testing is the process to detect any errors in implementation. This allows us to verify that the product has been made as per requirement. Programming testing is the way toward checking a framework with the motivation behind recognizing any errors, gaps, or missing prerequisites versus the genuine necessity.

Unit testing tests a single unit or module of the software without considering other units or modules this allows for all units of the software to be verified. While unit testing verifies each module of the software whether they work to get the intended output must also be checked, this is done using integration testing which tests multiple units or modules combined. The testing phase is depicted in Table 1.

The results obtained are shown in the following figures.

Figure 5 displays the Home page of the proposed work. In the home page an image can be selected by clicking on browse button. Image can be uploaded by clicking on submit button and the result will be displayed which are depicted in Figs. 6 and 7, respectively.

Figures 8, 9, and 10 display the output obtained when the input images with various lesions are selected.

4 Limitations and Future Scopes

It is noticed that the performance of the proposed system is less than it was actually expected cause of the test and results are based on those internet images. Basically, the data is obtained from internet site for truth images of skin cancer types, i.e., namely KAGGLE. The testability of the project is improved by processing images obtained by medical colleges. The limitation, i.e., henceforth depends on the clarity of the image, by maintaining the images saturation, contrast, and brightness.

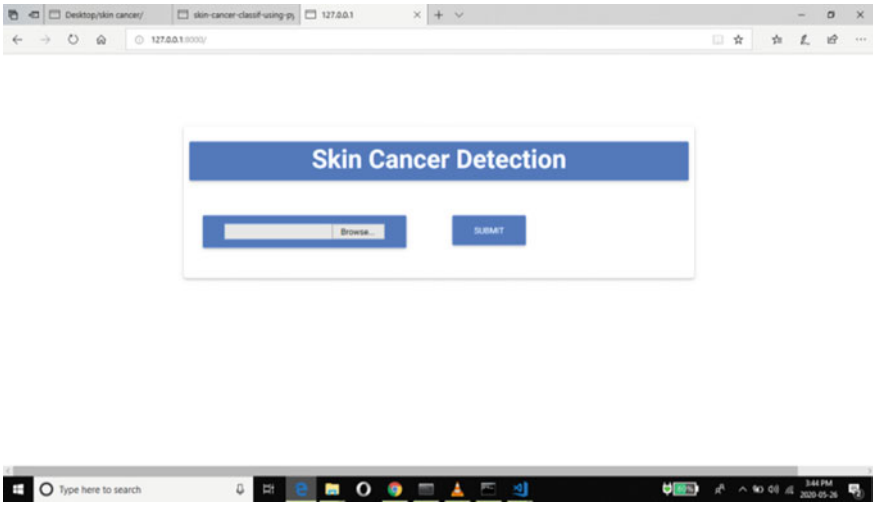

Fig. 5 Home page

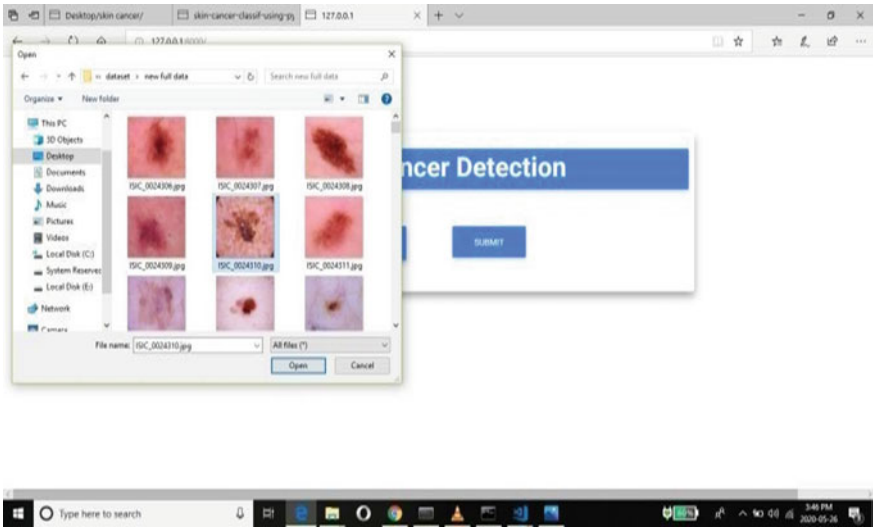

Fig. 6 Selecting input image 1

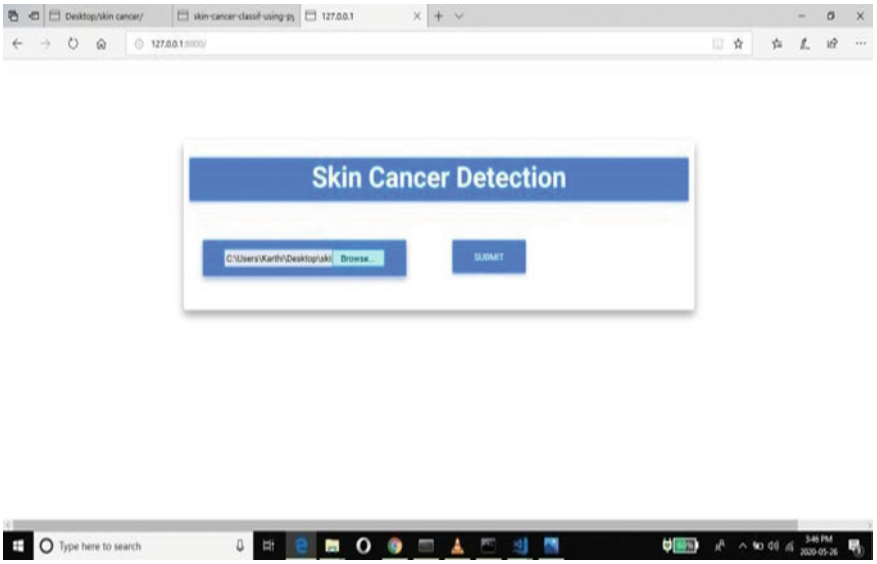

Fig. 7 Submit the input image 1

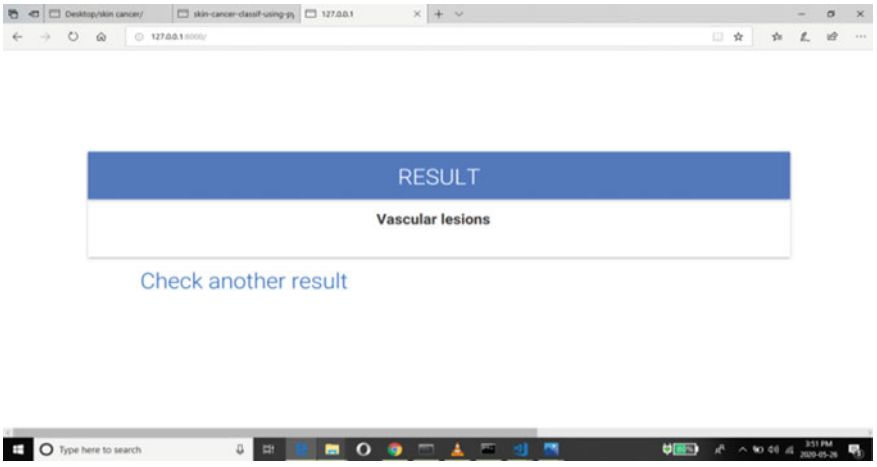

Fig. 8 Vascular lesion output

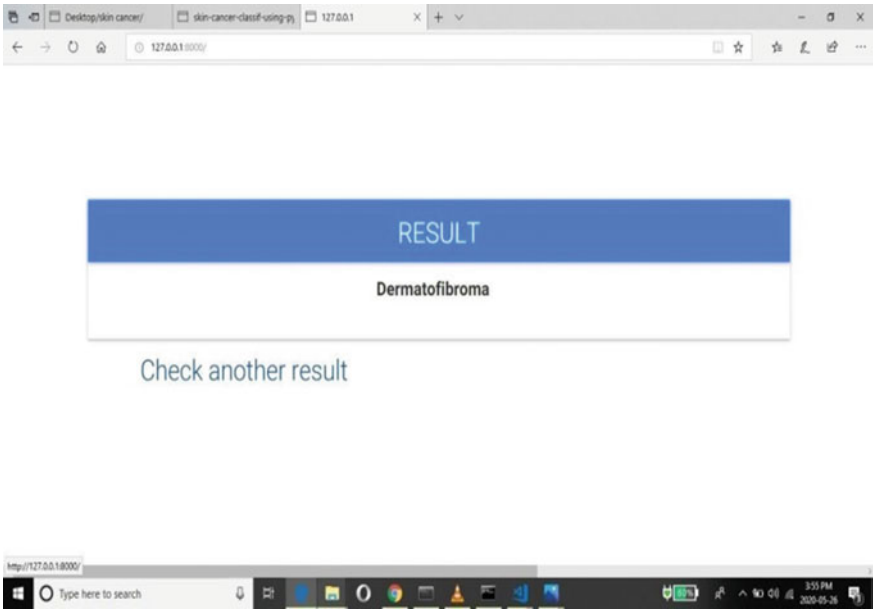

Fig. 9 Dermatofibroma output

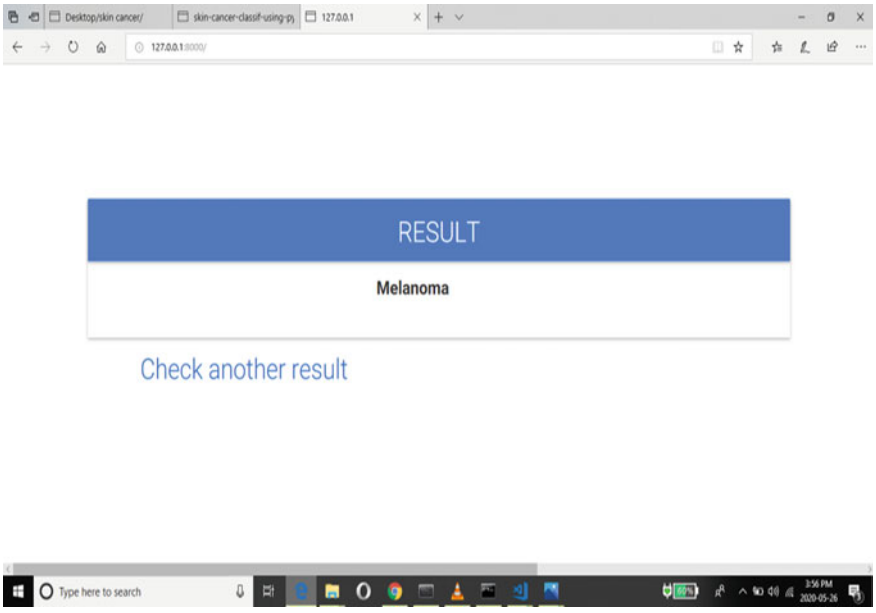

Fig. 10 Melanoma output

5 Conclusion

The system of detecting skin cancer at its earliest using techniques which are computer based including image processing are found far better than the traditional method. This proposed methodology is advantageous because it consumes less time and cost. The proposed model showed an accuracy of 89%. This method requires no expertise since it is an efficient and simple method. This method is an alternative and efficient way to detect Skin Cancer types, its simplest way of diagnosing helps the user.

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Design and Development of a BCI Framework to Control a UTM Using EEG Headset

E. S. Manish, Pratheesh, Pruthviraj Umesh, and K. V. Gangadharan

Abstract We live in a period where machines have become a fundamental piece of our day-to-day existence. These machines that surround us largely depend on human assistance. To operate them, a human would nearly have to be functional. We only lose the capacity to engage with machines when these capabilities are hindered, possibly by a bodily condition or injury. This study picks the Universal Testing Machine as the machine to be operated to help physically challenged people run machinery. Additionally, it uses an Internet of Things architecture to monitor specific brain activities in the person's brain, while controlling the machine.

Index Terms Electroencephalogram · Brain Computer Interface · IoT · MQTT · ESP32 · Node-RED · Emotiv EPOC+ · UTM

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1 Introduction

One of the most complicated systems in the body is the human brain, which serves as the decision-making command center. The brain is made of billions of neurons linked together to create a group of neurons known as a mesh. These neurons produce nerve impulses whenever we think or act. When these nerve impulses reach a particular threshold, it stimulates the action potential, further propagating the impulses along the axon. Every action we do results in a specific pattern of neurons firing. Typically, these neurons stimulate the neuron in the spinal column enabling the movement of hands and legs. For instance, any injury to the spinal cord would result in paralysis since it would restrict the passage from the brain to the muscles. It is intriguing to think that this ailment can be rectified if it were possible to artificially stimulate the pattern of neuron spikes to match the appropriate muscle activity. This notion opens up a wide range of applications in the brain-computer interfaces, where the brain's sole function is to fire a particular sequence of neurons. These neuron spike signals would then be subjected to processing, and then the signals would be converted into appropriate instructions. This would enable us to trigger muscular movement without using the body's standard Neuromuscular system [1]. The first step in this direction is to monitor the action potential. It could be pulled off by harnessing the capability of the electrode to sense subtle changes in electrical voltages. Essentially there are two significant ways of encapsulating brain signals: the invasive and the non-invasive approach. This study uses the Electroencephalogram (EEG), which involves placing several electrodes on a subject's scalp to track minute variations in brain signal activity that require no surgical intervention. The brain encrypts all the information required to carry out the desired process in the form of electrical signals, which are later decrypted by the body [2]. An excellent foundation for achieving the interface between the brain and any hardware component is shown in Fig. 1 [3].

One of the significant sources of Neuromuscular information is the Raw electrical brain waves that are obtained by using the electrode's capabilities to detect minute variations in electrical impulses. EEG caps are the best way to accomplish this is because they do not require any medical intervention and allow one to gather brain data from multiple channels. The individuals would benefit from exposure to various stimuli, including olfactory, gustatory, tactile, visual, and auditory stimulations. These stimulations activate the neurons in the respective brain areas, acting as the primary information source for processing brain signals. A pre-processing and feature extraction phase primarily tries to reduce noise and any other unnecessary patterns obstructing the segregation process and change the data into a conducive format appropriate for classification. This stage ideally includes varieties of filtering techniques such as low-pass, high-pass, band-pass, and notch filtering to reduce

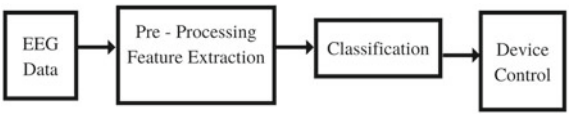

Fig. 1 General BCI framework

noise, interpolation to negate wrong channels, fill in missing data for pre-processing, and a variety of data transformation methodologies such as time–frequency distribution, fast Fourier transform, eigenvector method, and auto-regressive method [4]. The classifier's job would be to divide them into classes of different kinds that may then be used to operate various devices.

2 Related Work

The outline by Thomas Setiono, Informatics Department-Faculty of Industrial Technology, Petra Christian University, Andreas Handojo, Informatics Department Faculty of Infor-mation Technology, Institut Informatika Indonesia, Rolly In-tan, Electrical Engineering Department Faculty of Industrial Technology, Petra Christian University, Raymond Sutjiadi and Resmana Lim Mobile Computing Research Group, Petra Christian University [5] takes into account the Steady State Visual Evoked Potential (SSVEP) as a stimulus to trigger brain impulses. This signal is a typical outcome of frequency-dependent visual stimulation. The brain typically generates electrical activity at a frequency that is the same as the specified visual stimulus frequency when the retina is stimulated by visual stimuli between 3.5 and 75 Hz. When a large number of stimuli with different frequencies are present, the brain uses this strategy to identify which signal the person sees. Moreover, they use SSVEP methods in conjunction with SVM as a classifier to divide the produced brain signals into three related instructions, left, right, and forward, respectively, to operate an RC car. However, this study attempted to expand on these ideas using mental instructions instead of SSVEP as a stimulus source.

The study considers a subject's mental instructions, which would be pre-trained on a platform designed to train for different mental activity states. Several procedures are applied to develop a personal training profile. Following a succession of data churning processes, the data gathered will be used to aid the model's practical learning. The training data will be saved in a model that can be utilized to operate any device in the various architecture systems of interest after the training phase is completed.

This experiment leverages the 14-Channel EEG (Electroencephalogram) headset, developed by Emotiv EPOC+ that enables the capturing of brain signals. These signals are elicited by sensors of the Emotiv Epoc+ headset [6]. The user's or subject's brain waves serve as input data for a system that has already been pre-trained on specific brain wave patterns utilizing a training platform. These learned patterns will then be transmitted to a Node-RED architectural framework, which will gather the data during a testing phase and then transmit it to a Broker-Client network architecture that has already been prepared and is based on MQTT protocols. An Micro Controller Unit (MCU) in this study is an ESP32 controller, a powerful SoC Microcontroller [7], which will also act as one of the clients in this Broker-Client architecture, subscribing to particular topics for further processing. The specified network architecture is used to push data whenever it is published from the input EEG side. The MCU and its peripherals (discussed below) will then follow a set of

procedures to control a Universal testing machine (A Mechanical Instrument utilized to conduct Compression and Tensile tests on sample objects), which acts as an end device concerning the changing input.

3 Materials and Methods

This section describes the proposed BCI-based UTM control system in detail. Figure 2 shows a general description of the proposed system.

A. *Signal Acquisition and Processing Unit*

This BCI study intends to operate a Universal Testing Machine utilizing learned mental commands of specific individual for various machine states. The Signal acquisition is achieved using an Emotiv BCI Epoc+ headset, capable of recording raw brain signals using a non-invasive EEG technology. Emotiv BCI is a BCI software designed with an Epoc+ headset to set up, simulate, and train mental commands. The subject first wears the 14-channel EEG headset (Epoc+) to create essential contact with the scalp of the head. The headset is connected to a computer that runs the BCI software through a proprietary 2.4 GHz wireless BLE, which aids in setting up and configuring subsequent stages. The Further processing of the training phase begins after fulfilling the criteria of extracting high-quality signals from all 14 electrodes [8]. In order to control the functionalities of the UTM (Universal Testing Machine), this study extends its three distinct control states, Tensile Test, Compression Test, and STOP, to three finite mental commands [9]. The study creates mental commands in

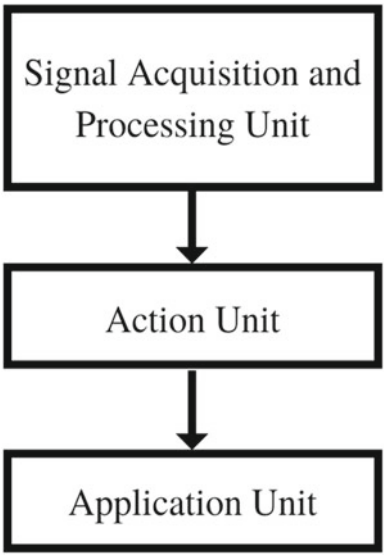

Fig. 2 Proposed system architecture

Correspondence to the three distinct machine control states throughout the training phase. Furthermore, this study utilizes the Emotiv BCI EEG training platform, where the training of mental commands is very flexible.

This study utilizes a dedicated Emotiv BCI EEG training platform or a BCI Software Tool customized for each subject. Each training profile comprises a training area where recordings of each subject's thought patterns are achieved. These profiles are capable of storing a maximum of 15 learned mental activities. This study directs subjects to visualize three different specific scenarios, for instance, directing a snooker ball to three different corners of a triangular snooker table for 10 s as a stimulus for these mental commands. The three envisioned scenarios correspond to three distinct courses of action, Up, Down, and STOP, each representing one of the three UTM machine states facilitating distinct neural spike patterns. Simultaneously the EEG headset would extract patterns from these envisioned scenarios. These instructions could then be tested or performed in real time once the brain-command patterns are elicited. In addition, the subjects must undergo repeated training for each of the three commands. The more practice the subject receives, the better the system will recognize the pattern of brain activity linked to the orders. The more adept the subject becomes at mentally recreating those thoughts.

The BCI Software Tool also offers in-depth information on the learning accuracy of the corresponding commands to each profile in numerical form. This crucial bit of knowledge will serve as a feedback mechanism to assist in self-tune the orders, improving the UTM control's effectiveness and accuracy.

B. *Action Unit*

The Action Unit is set up using an MQTT architecture which connects every other unit. The MQTT Architecture setup established in this study is shown in Fig. 3.

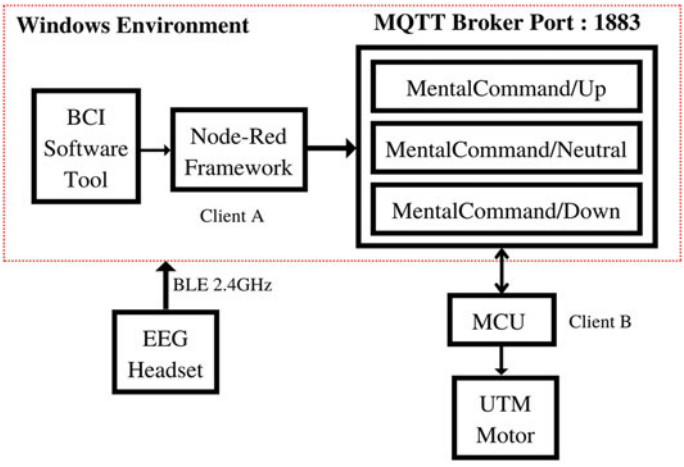

Fig. 3 MQTT architecture setup

The Action unit comprises two main sub-modules, the MQTT Broker, also known as Eclipse Mosquitto and Node-RED framework. Eclipse Mosquitto is an open-source (EPL/EDL licensed) message Broker that implements the MQTT protocol. It is a Publish/Subscribe, a lightweight messaging protocol that makes a direct connection between the devices obsolete by relaying the data from the central server called the MQTT Broker.

The highlight of this protocol is that it allows for adding new IoT devices to the network on the fly since it does not require alteration of the existing infrastructure [10]. In this study, the MQTT Broker manages three different topics named MentalCommand/Up, MentalCommand/Neutral, and MentalCommand/Down to route incoming values from Client A, which comprises values from the trained mental commands to Client B, which controls the UTM, which will be the end device here.

The Node-RED module, a flow-based programming tool that facilitates connecting physical devices with APIs and other web services, is another vital module [11]. With the help of all the palette tools offered by the Node-RED framework tool, it is a browser-based editing interface that makes it simple to wire up all the flows and nodes. Additionally, this may be deployed with a single click throughout its runtime. Flow-based programming is the method used by the whole Node-RED framework tool. As stated in "Node-RED," it is only a method of modeling an application's behavior as a network of nodes. This node network's ability to be readily reconfigured makes it redundant and modular on its own. By just rigging up some of the nodes provided from the very own tool itself, one may save writing lines of code in this situation. The Node-RED framework designed for this study is shown in Fig. 4.

The framework begins with the Emotiv node, a Node-RED add-on that makes communicating easier for the Emotiv BCI Software tool and Node-RED framework. Any architecture that contains an Emotiv headset as one of its components must

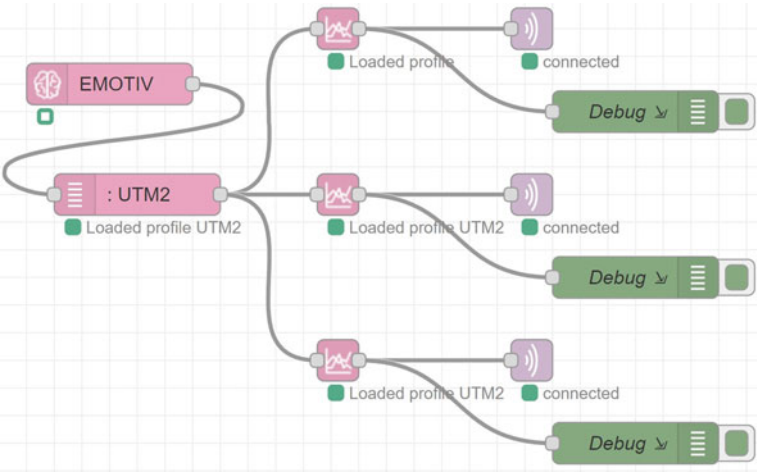

Fig. 4 Node-RED linking Emotiv BCI and MQTT broker

employ the Emotiv and profile name nodes as the two necessary nodes. The trained mental commands Neutral, Up, and Down would be imported and loaded into the Node-RED interface by this profile node. These three mental command nodes are linked to an MQTT publisher node, which will subsequently send the values of the mental command to an MQTT Broker. The data from the Node-RED tool would subsequently be managed by this MQTT broker, as seen in Fig. 3. It depicts two clients connected to a broker that controls data flow across ports, in this case, port 1883. Client A is a Node-RED framework that publishes mental command magnitudes to the Broker over the MQTT protocol. The Broker created and used the MentalCommand/Up, Neutral, MentalCommand/Up, and MentalCommand/Down topics to rocess the three incoming mental instructions. Client B refers to an MCU in this study, ESP32, that would serve as the UTM's state controller and is subscribed to these topics. Every time Client A publishes data on one of the three topics; Client B receives those values via the same topics, which may be processed further in the Application unit for UTM navigation. The study then combines the strengths of both MQTT and Node-RED modules [12] with the primary objective of controlling the three UTM machine states using processed brain signals produced by the first block, as shown in Fig. 2.

BCI-based UTM controlling framework employed in the study is based on the MQTT Architecture setup as depicted in Fig. 4.

The architecture intertwines the UTM device and the EEG headset via a Windows OS-based PC, acting as the backbone of the network framework architecture. The Emotiv BCI software processes the brain waves being recorded from the EEG headset and continues through the training step described in the preceding subsection (Signal Acquisition and processing unit). These Trained Brain waves would be connected to the Node-RED framework, which would act as one of the clients in the network framework architecture.

C *Application Unit*

The Application unit comprises a UTM Motor and a Microcontroller Unit (MCU). The UTM, as shown in Fig. 5, mainly comprises of a Motor Hub, a Load cell that gives appropriate values for Compression and Tensile tests, jaws that hold the test sample, and a Moveable crosshead that has Upward and Downward motion for Tensile and Compression tests.

A 3-phase AC Motor is connected to this moveable crosshead so that the clockwise and anti-clockwise direction of the Motor would result in an upward and downward motion of the crosshead, thereby allowing anyone to perform Tensile and Compression tests for a sample, respectively.

The Motor allows the MCU to control the direction and stopping of the Motor by using electrical relays. The electrical relays will switch 2 of the 3-phase lines connected to the Motor. This switching would allow the MCU to control the direction of the Motor. The wiring of the MCU, relays, and Motor is depicted in Fig. 6.

The Motor circuitry consists of two electrical relays, R1 and R2. R2 is used to switch the direction of the Motor, and R1 is used to stop the Motor by breaking the circuit between R1 and R2. Both these relays are controlled using an MCU which

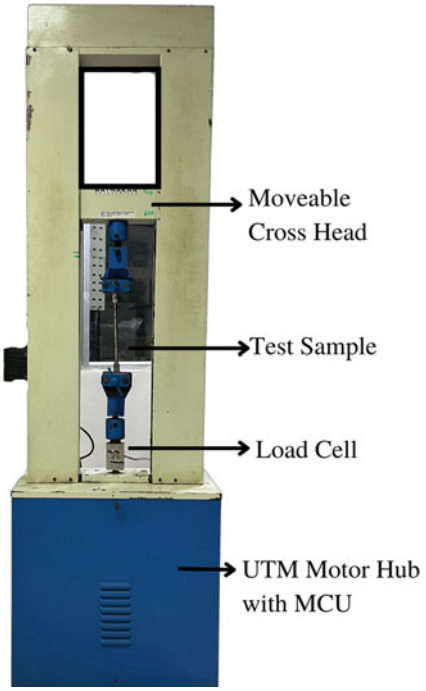

Fig. 5 Labeled UTM

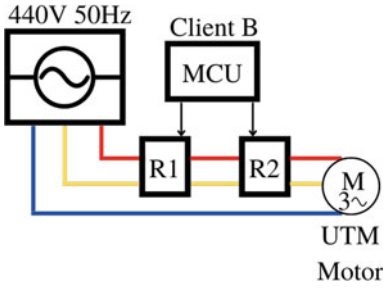

Fig. 6 Client B to UTM motor circuitry

acts as Client B in this study. The states of relays affecting Motor's and UTM's state are depicted in Fig. 7.

After the circuitry, the study moves on to configure the MCU to accept and process mental command values, thereby controlling the states of the relays.

The WiFi chip of the MCU enables it to connect to a network architecture wirelessly, in which the broker and Client A (Node-RED) reside. The MCU starts by connecting to the broker using a specific IP address. Once the connection to the broker is established, the MCU subscribes to the three topics, which is managed by the Mosquitto Broker. After subscribing to those topics, the MCU would be ready to receive mental command values from Client A.

Fig. 7 Relay state affecting Motor and UTM states

R1	R2	UTM Motor State	UTM State
0	0	OFF	-
0	1	OFF	-
1	0	Clockwise	Tensile Test
1	1	Anti - Clockwise	Compression Test

Fig. 8 Client B logic diagram

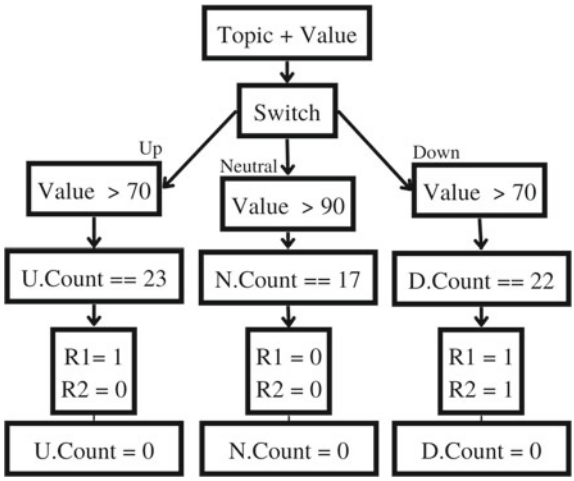

Figure 8 displays the logic programmed into the MCU for the same.

In this study, the MCU would initially begin by connecting to a WiFi router. This WiFi router is to locate the Mosquitto broker on the same network and receive data from the broker. The MCU then connects to the Mosquitto broker using the Broker's IP address and a Port number after connecting to the local network. The MCU would subscribe to those three topics after connecting to the Mosquitto broker, as seen in Fig. 3. Once the MCU controller subscribes to the topics, it will receive Mental command values anytime Client A (Node-RED) publishes them. The type of data published by Client A would have values ranging from 0 to 100 for every topic.

The logic diagram explained here begins with the Topic name and the associated value, which takes into a switch case where it divides into three cases based on the topics from which the values get published. If the MCU starts getting values from the "Up mental command," which the study shows as the Upward motion of the Moveable crosshead in the UTM, the switch case will direct the logic flow into checking for the value limit being more than 70. The limit 70 is chosen based on several iterations of these tests corresponding to the reaction time of Signal transmission. If the value exceeds 70, a global counter (U.Count) will start incrementing every time the value

magnitude exceeds 70. Once the counter reaches 23, the logical flow would proceed with triggering the relay via a Digital Pin from the MCU. The value 23 has been arrived upon after several iterations for stable conditions.

Once all these logical conditions meet, the relay, in this case, R1, would be triggered, which directs the current flow to R2, where the default state of R2 will make the AC Motor rotate in a clockwise direction resulting in the Tensile test of UTM. The counter resets and the logical flow diagram would continue in this loop for the other two possible cases, as mentioned in the logic diagram in Fig. 8.

4 Results and Discussion

A. *Experiment Setup*

The study designs an experiment setup comprising a subject with an EEG Headset whose mental commands were pre-trained, a Universal Testing Machine with the MCU, and a Windows System with Node-RED and MQTT Broker running in it.

The experimentation involved setup and observation of multiple parameters. The specifications of the computer used are shown below.

- Processor: 11th Gen Intel(R) i7 @ 2.30 GHz.
- System Type: × 64-based processor.
- RAM: 32.0 GB (31.7 GB usable).
- OS: Windows 10 Home 64-bit.

The experimentation involves conducting Tensile and Compression testing on samples harnessing the UTM, using the designed BCI Interface as shown in this study. The overall experiment setup with the subject is displayed in Fig. 9.

B. *Evaluation*

Mental command accuracy was measured with respect to change in contact quality of the EEG Headset electrodes. These variations in contact sensor quality also resulted in change in EEG signal quality which is discussed in Table 1.

As shown in Table 1, the contact quality of the 14-channel electrodes varied due to difficulty in contact with the scalp of the subject with factors like hair and poor hydration. The contact quality is a measurement of the impedance of channels (electrodes) which is calculated by the EEG headset and can be monitored using the Emotiv BCI Software where each electrode placement and its quality is shown. This aids in an accurate adjustment of the EEG Headset to attain maximum contact quality.

Furthermore, as shown in Table 1, this study tested multiple EEG Quality values in relation to their mental commands. EEG Quality is a reference parameter in the Emotiv BCI program that rates the quality of the signal from the EEG headset. To accomplish this, the BCI Emotiv software harnesses a machine learning algorithm trained on high-quality two-second EEG recording dataset.

Fig. 9 Experiment setup

Table 1 Mental command values with change in contact and signal quality of the EEG headset

Contact quality (%)	EEG quality (%)	Mental command values		
		Up	Neutral	Down
100	**100**	**92**	**95**	**88**
100	**92**	**90**	**96**	**85**
90	**83**	**80**	**82**	**78**
82	**75**	**72**	**78**	**70**
76	67	64	68	60
70	58	55	58	50
65	50	44	47	40
54	42	39	42	35
54	25	35	40	30

The Mental commands: Up, Neutral, and Down having magnitude values between 0 and 100 are captured from the Node-Red output console screen. Furthermore, these values are compared with each of Contact and EEG Signal quality to understand the limits and range of possible UTM control outcomes.

Once both the desired contact and EEG quality are achieved, the study tested out the mental command values for all three commands as shown in the table. Table 1 discusses the role of contact quality in determining the mental command magnitudes where there is a statistical linear relation between the contact quality and the average values of the mental commands.

Since the logic used in this study as shown in Fig. 8 considers the value only above 70 for both Up and Down commands, and above 90 for Neutral commands, the minimum contact and EEG signal quality needed to perform the experiment was 82 and 75% as shown in Table 1. The cells being highlighted green in Table 1 explains the same. Any quality value below this resulted in inaccurate Mental Command values for the driving logic. Overall, Neutral command stability performed better than the other two Mental Commands.

Once the necessary EEG headset requirements are achieved, the study moves toward carrying out the experimentation, namely, Tensile and Compression test.

The Tensile test experiment includes a subject wearing the EEG Headset who proceeds to recollect the mental commands used during the Training phase, where the subject had envisioned about moving a snooker ball to the left, as an example shown in chapter II of this study. By recollecting the same thought (Mental commands), the UTM's Motor rotates in a clockwise direction, making the movable crosshead part of the UTM move Up, resulting in the process of the Tensile Test of the sample. The T7 and T8 Electrodes of the EEG Headset, placed on left and right side of the subject's head, respectively, capture the brain activity from the Temporal lobe of The Brain [13]. Since the mental activity for this phase is mainly about the imagination of pushing something (like a snooker ball) to the left, whenever Tensile Test is performed, the recorded brain waves show a signal dip in the T7 part of the Temporal Lobe. The Brain activity metrics for this phase with the signal dip which is marked in red color from the T7 electrode is shown in Fig. 10. The y-axis in the graph represents the minimum and maximum Amplitude (uV) from −100 to 100 uV. The x-axis shows the channel spacing (uV) from 0 to 10 which is recorded from the BCI Software.

For the Compression test, the subject proceeds to recollect the mental commands used in the Training phase, where the subject had envisioned moving a snooker ball to the right. By recollecting the same thought (Mental commands), the UTM's Motor rotates in an Anti-clockwise direction, making the movable crosshead part of the UTM move Down, resulting in the process of the Compression Test of the sample.

For this phase, the Brain activity metrics of the T8 electrode placed to the right of the brain with signal dip marked in red color is shown in Fig. 11.

During Tensile and Compression tests, the subject would also use the Neutral command, which was also trained during the training phase along with the other two commands, to stop the movable crosshead wherever required.

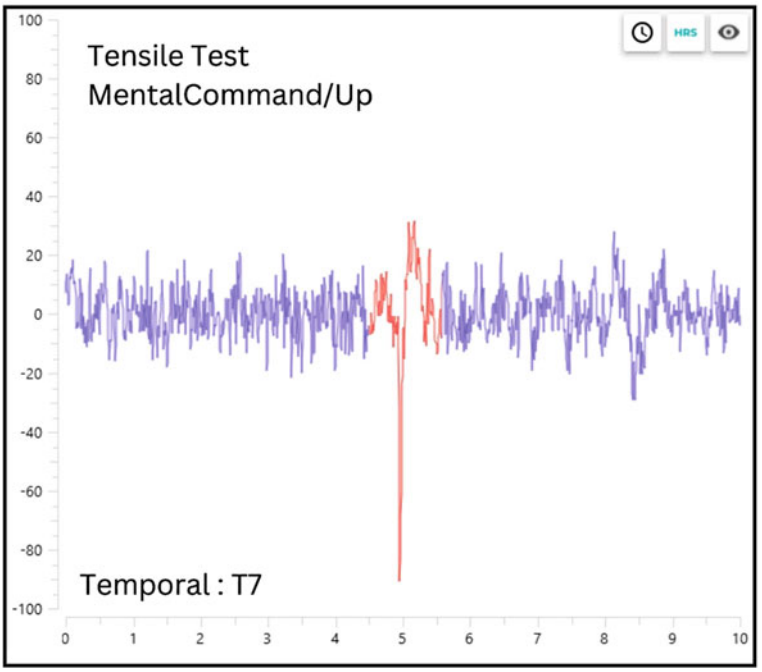

Fig. 10 Activity metrics of temporal Lobe: T7

It is observed from the study that the response time to stop the movable crosshead is quicker compared to the other two states (Upward and Downward motion of the crosshead).

This observation results in tuning the "N.Count" and "Value" limits to 17 and a value >90, respectively, as shown in Fig. 7.

For all 3 Mental commands, the detection of the Neutral phase is much quicker and stable than mental commands used for Compression and Tensile tests.

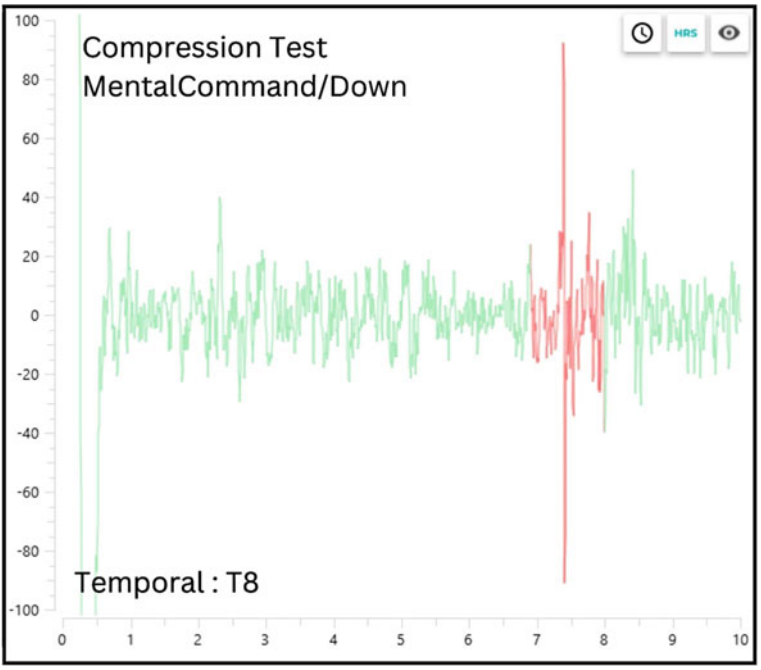

Fig. 11 Activity metrics of temporal lobe: T8

5 Conclusion

This paper addressed a method for creating a BCI frame-work that involves recording and training specific brain signals from a human, feeding those signals into a network architecture, and then using the network architecture to control the states of a machine.

Due to the flexibility of the IoT framework, this machine may be replaced with any machine that can be easily controlled and activated using an MCU.

The method described here can be extended to multiple experiment control by a person whose brain signals can be pre-trained for all potential states of the machines in the experiment using the discussed BCI framework. It can also be utilized for remotely triggered experiments across a network mesh. This BCI framework can be used for remotely triggered experiments by any physically challenged person willing to participate.

The study's final use is not just limited to remotely triggered labs; it can also be applied to routine machine-related tasks.

The BCI framework employed here can also be connected with Virtual and Augmented Reality platforms, Cyber-Physical Systems, Biometric authentication, and more.

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Approximate Compressors-Based Multiplier for Image Processing and Neuromorphic Modeling

D. K. Nisarga, Deeksha Sudarshan, Rashmi Seethur, and H. K. Shreedhar

Abstract Approximate computing in the era of high-speed multimedia applications increase in the demand of high-speed error-tolerant circuits. In this method, accuracy is compromised to achieve high performance. The main criterion is to reduce hardware complexity, power dissipation, and timing delay at the cost of accuracy. The main aim of this paper is to design and analyze two approximate compressors with minimum hardware complexity, delay, and power with reasonable accuracy, when compared with the existing compressors in literature. The proposed designs are implemented and verified using 90 nm Cadence NC-Verilog standard library cells. The parameters of interest in the approximate computing are Error Rate (ER), Error Distance (ED), and Accurate Output Count (AOC). The proposed compressors are used to implement 8×8, 16×16 unsigned multipliers, and signed 8×8 approximate multipliers. The application of the proposed design in image smoothing, multiplication, and LIF neuron modeling is discussed.

Keywords Approximate 4:2 compressors · In-exact multipliers · Error control coding applications · Image analysis · LIF neuron model

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1 Introduction

The elevated hardware complexity, power, and delay in high performance computation units of a processor can be reduced by introducing conjecture. Today's High speed multimedia communication applications demand immense concurrent operations which results in immense power dissipation [1, 2]. With the agreeable precision the complexity and power efficient systems could be realized. Accurate computing is a promising solution that provides equilibrium between complexity of the design and precision. It is possible to create high-speed systems with less sophisticated hardware and less power usage by approximating arithmetic operations [3, 4]. The tradeoff between reduced accuracy and complexity does not necessarily affect the intended result in the applications like machine learning, multimedia communication, Digital signal processing, artificial intelligence and hence, with added benefit of the human eye's incapacity to detect these minute variations, it opens up areas for exploration. To improve the efficiency of approximate arithmetic circuits, substantial research has been conducted [5–11]. The addition of a partial product is the primary cause of a peak in power dissipation and delay in multiplication operations [12]. Several researchers showed that compressors can decrease parameters such as area, power, and delay while summing partial products. Internally implemented compressors employ a series of half adders and/or full adders to determine the count of logic 1 in the input. The most common compressor topologies are 7:3, 5:2, 4:2, and 3:2 [14–16].

The regularity in the design of 4:2 compressor makes it more attractive over another existing topology. 4:2 compressor is the very important module to design Dadda multipliers and Wallace tree multipliers [2, 4, 13]. The 4:2 compressor design based on transistor-level XOR-XNOR is proposed as it is best suited for tree structured high-speed multipliers. Chang et al. [12] have proposed low supply voltage that operates at 0.6 V 4:2 and 5:2 compressor. Momeni et al. [17] designed approximation-based 4:2 compressor which optimized parameters such as power consumption, area, and delay. Akbari et al. [18] have proposed a re-configurable 4:2 approximate compressor for dynamic computation. Based on the application the compressor is able to switch between accurate and approximate compressor design. Ha and Lee [19] designed a novel 4:2 approximate compressor by inculcating an error recovery design. Based on the partial product count, the authors Guo et al. [20] presented a top-down structure for an approximate multiplier that is dynamically configured between different approximate compressors.

In literature, design optimization by using transmission gates [TG] is explored. The use of TG in compressor considerably reduces the area and delay but, the major issue with this approach has irregular rise and fall times. In this paper, two novel 4:2 compressor designs are proposed, evaluated, and further extensions are done based on the observations. Approximate 8×8 and 16×16 multipliers are designed using these compressor architectures. Later, evaluation on metrics such as error rate, error distance, Mean Error Distance (MED), and Mean Relative Error Distance (MRED) [26] is done. The multipliers designed are then compared with state-of-art multipliers.

A selection-based 8 × 8 approximate multiplier is designed which can perform both unsigned and signed operations. Performance evaluation of the existing compressor-based multiplier is done by implementing it in image multiplication, smoothing, and LIF neuron modeling.

2 Approximate Multipliers

Multiplication is one of the most important modules which determines performance in artificial intelligence and digital signal processing applications, and these require a swift multiplier design to perform parallel operations with acceptable accuracy in precision. The compromise in accuracy of a multiplier makes the possibility for faster computations with less hardware complexity, power, and delay, while maintaining acceptable levels of precision.

The summation of the partial product is the speed limiting factor in any multiplication circuit due to the propagation delay in adder networks. Sum and carry are computed concurrently at each level to reduce propagation delays in Compressors. The resultant carry and higher significant sum bit are combined in the following stage, and this operation is iterated until the final product is obtained.

A. 4:2 Exact Compressor

Figure 1 illustrates the general block diagram of an exact 4:2 compressor, which comprises five inputs, viz., A1, A2, A3, A4, and CIN, three outputs viz. CARRY, COUT, and SUM and two cascaded full adders.

$$\mathrm{COUT} = \mathrm{A3}(\mathrm{A1} \oplus \mathrm{A2}) + \mathrm{A1}(\mathrm{A1} \oplus \mathrm{A2}) \tag{1}$$

$$\mathrm{CARRY} = \mathrm{CIN}\ (\mathrm{A1} \oplus \mathrm{A2} \oplus \mathrm{A3} \oplus \mathrm{A4}) + \overline{\mathrm{A4}(\mathrm{A1} \oplus \mathrm{A2} \oplus \mathrm{A3} \oplus \mathrm{A4})} \tag{2}$$

$$\mathrm{SUM} = \mathrm{CIN} \oplus \mathrm{A1} \oplus \mathrm{A2} \oplus \mathrm{A3} \oplus \mathrm{A4} \tag{3}$$

Figure 2 depicts a compressor chain. The input carry from the previous 4:2 compressor is CIN, and the outputs: CARRY and COUT have a higher significance than the input CIN.

B. Area efficient 4:2 compressor

The number of primary outputs is reduced to 2, by approximating the 4:2 compressor. Since COUT is removed the design generates an in-accurate result. Only when the input combination is "1111" does this result in an error. The CARRY and SUM are raised to "11" and an error of "−1" is introduced when the input bits are "1111". Figure 3 depicts the proposed high-speed area-efficient 4:2 approximate compressor.

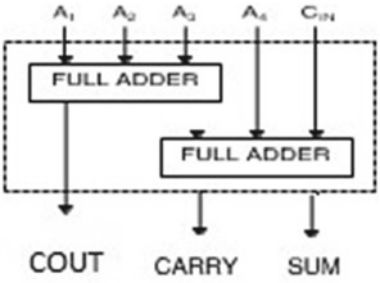


Fig. 1 Accurate 4:2 compressor

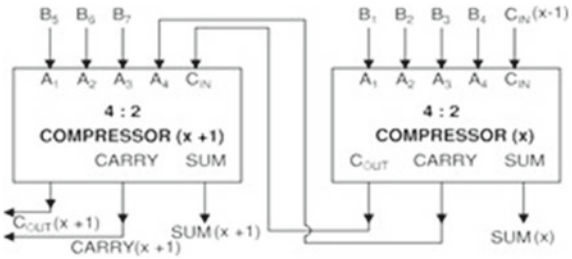


Fig. 2 Compressor chain

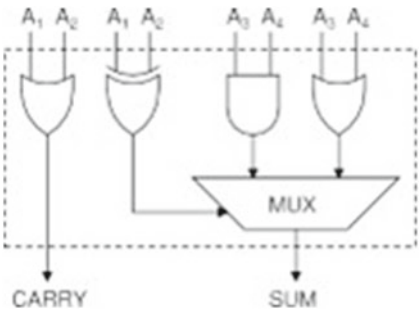


Fig. 3 Proposed area-efficient 4:2 compressor

A1, A2, A3, and A4 are the compressor's inputs, while the outputs are SUM and CARRY. Below are the logical expressions for realizing SUM and CARRY.

$$\text{SUM} = (\text{A1} \oplus \text{A2})(\text{A3A4}) + (\text{A1} \oplus \text{A2})(\text{A3} + \text{A4}) \tag{4}$$

$$\text{CARRY} = \text{A1} + \text{A2} \tag{5}$$

C. Modified dual stage 4:2 compressor

An alternative multiplier architecture [21–25] with multistage cascaded compressors is also suggested as a way to improve the proposed design's hardware efficiency. One XOR, one AND, and two OR gates are also necessary in addition to the MUX. Six

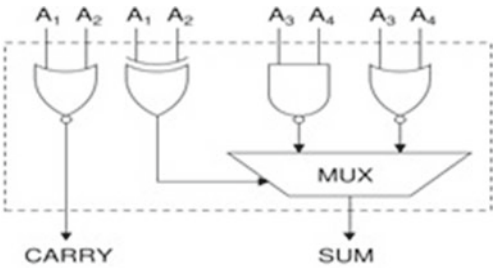


Fig. 4 Proposed modified dual-stage 4:2 compressor

transistors are required for each OR and AND gate in CMOS logic implementation. Figure 4 depicts a potential architecture using NAND and NOR gates to lower the transistor count. The stage 1outputs are different for both architectures, but the improved dual-stage 4:2 compressor generates the same outputs at stage 2 because negation in both stages occur in an integral multiple of two.

D. Parametric analysis

The level of precision attained by the multipliers created using suggested compressors and existing approximation compressors is measured using accuracy measures.

1. Error distance (ED)

Error Distance (ED) defines the absolute difference between the outputs of the exact 4:2 compressor and the approximate 4:2 compressor.

$$\text{ED} = \text{Exact output} - \text{Approx output} \tag{6}$$

2. Mean error distance (MED)

MED defines the mean of the ED for all possible input combinations. The formula to calculate mean error distance is given by,

$$MED = \frac{1}{2^{2n} \sum_{k=1} 2^{2n} ED_k} \tag{7}$$

where n is the no. of bits of input given to multiplication ED refers to the difference between the exact multiplier output and the approximate multiplier output.

3. Accurate output count (AOC)

AOC indicates the number of exact outputs for all input combinations. Table 1 represents the count of the half adders, full adders, approximate and exact compressors used for the Dadda, and approximate 8 × 8 multiplier design. We can observe that there is a 29.97% improvement in area, a 36.39% improvement in power, and a 16.56% improvement in delay in comparison with the conventional 8-bit Dadda multiplier (Table 2).

Table 1 8-bit multiplier result comparison

Types of multipliers	Area (μ m^2)	Power (μ W)	Delay (ps)	Half adders	Full adders	Exact compressors	Area efficient compressors	Dual stage compressors	Accurate output count	Mean error distance
8-bit Dadda multiplier	833.916	71.3045	2179	8	48	NA	NA	NA	65,536	NA
8-bit area-efficient compressor-based multiplier	584.485	45.457	1813	10	18	6	8	NA	7724	612.9

Table 2 16-bit multiplier result comparison

Types of multipliers	Area (μm^2)	Power (μW)	Delay (ps)	No of half adders	No of full adders	No of exact compressors	No of area-efficient compressors	No of dual-stage compressor
16-bit Dadda multiplier	3622.503	371.893	4387	16	224	NA	NA	NA
16-bit proposed compressor-based multiplier	2309.309	186.033	2310	61	15	32	32	26

3 Application of 4:2 Inexact Compressor in Image Processing

A. Image smoothing

Image smoothing [27] is used to remove noise, sharpness and clutter in the image to produce smoother and blended effect. It works by convolving the image with a suitable kernel. For a given image select a particular coordinate and align the center of the kernel matrix over that coordinate. Then multiply each kernel value with the corresponding value of the image matrix and sum all the results of multiplication. Ideally, it is the sum of the element-wise multiplication of a matrix. The Gaussian image kernel used in our image smoothing application is indicated in Fig. 5.

Both 8×8 exact multiplier and the approximate compressors-based multipliers are employed in the image smoothing and output images obtained for each case. The quality metrics of both the images has been checked through MSSIM (Mean Structural Similarity Index Matrix) metrics. Original Leena image is one of the 6 standard images considered for image processing applications represented by Fig. 6. Figures 7 and 8 represent the output images by image smoothing with Gaussian filter kernel using our exact Dadda multiplier and approximate multiplier design. Once output images are obtained, image from approximate multiplier is checked for MSSSIM with reference to the output obtained through exact multiplier. This approximate multiplier provides a satisfactory result of 0.987 which is an acceptable value. Thus, it may be concluded that instead of state-of-the-art exact multipliers, power, delay, and area-efficient multiplier design can also provide meaningful results for the image processing applications.

B. Image multiplication

Image multiplication is extensively used in image and video processing. Multiplication of two images is performed in a single pass using the formula:

$$Q(i, j) = I1(i, j) * I2(i, j) \tag{8}$$

Fig. 5 Gaussian image kernel

$$\frac{1}{273}\begin{bmatrix} 1 & 4 & 7 & 4 & 1 \\ 4 & 16 & 26 & 16 & 4 \\ 7 & 26 & 41 & 26 & 7 \\ 4 & 16 & 26 & 16 & 4 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix}$$

Fig. 6 Original Leena image

Fig. 7 Image smoothing output with exact multiplier

Each pixel value from image1 is multiplied by the corresponding pixel value of the image2 and the corresponding pixel of the output image is obtained. Figure 9 represents input images used for multiplication. The image outputs in Figs. 10 and 11 through the exact multiplier and approximate multiplier are compared to analyze the image quality between the two. Figure 12 represents the case where the approximate multiplier is constructed only using the proposed approximate compressors. In this case, it may be observed that the image obtained after multiplication is not good and the quality metrics are not maintained. This justifies the need for both exact and approximate compressors in the proposed approximate multiplier design, to achieve meaningful full accurate results along with performance efficiency of metric, viz.,

Fig. 8 Image smoothing output with approximate multiplier

Fig. 9 Input images for multiplication

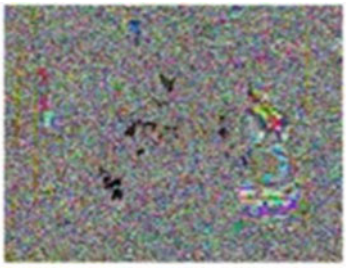
Figs. 10 and 11 Output images from exact and approximate multiplier reconstructed using MSB bits

power, area, and delay. Figures 13 and 14 represent the output images reconstructed using 8 LSB bits of image multiplication. This justifies that the consideration of the MSB bit is more suitable for image reconstruction rather than considering the LSB bits.

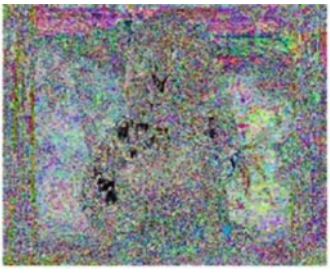
Figs. 10 and 11 (continued)

Fig. 12 Image formed only using approximate compressors based multiplier

Figs. 13 and 14 Output images from exact and approximate multiplier reconstructed using LSB bits



Figs. 13 and 14 (continued)



4 Selection Based Multiplier

In this section, an 8×8 approximate multiplier that works based on a selection line is discussed. Depending on the value selected on the selection line, same design can be used for both signed and unsigned multiplication. The proposed design has a selection bit when set to 0, the multiplier performs 8×8 unsigned multiplier operation, when the selection bit is 1, it performs 8×8 signed multiplication. When compared with exact compressor-based multiplier, the proposed multiplier was able to achieve lesser area, delay, and power.

5 Methodology of Increasing Performance of Existing Designs

It may be observed from the simple multiplication example that if multiplier bit is 1, all the multiplicand bits become the particular row's partial product. If the multiplier bit is zero the corresponding partial product row becomes zero. This would reduce the computation complexity involved in the generation of partial products. Secondly, since the overall delay of the multiplier circuit is measured by the critical path, here we can introduce pipelining which reduces the overall path delay. After all of the computations, it is clear that there is a considerable reduction in the average number of transitions occurring when compared to the prior approximation multiplier without code modification. The number of average transitions have reduced from 140.077 million transitions/second to 119.266 million transitions/second. The overall power consumption is lowered to 77.66 mW from 89.75 mW when the number of transitions per second is reduced. The critical delay path has also been reduced from 7.304 ns to 5.231 ns. That means that there is an average 29% reduction in total delay.

6 Application in Leaky-Integrate and Fire Model (LIF)

The leaky integrate-and-fire model (LIF-model), introduced by Louis Lapicque in 1907, is one of the most well-known neuron models. Selection-based multiplier is used to perform the computation of the LIF equation. This does not need accurate output, since neuron will be fired if the threshold value is reached. This method has the significant advantages area, power, and delay in comparison with state-of-the-art multipliers. The neuron output waveform is compared between both exact signed multiplier indicated in Fig. 15 and approximate multiplier indicated in Fig. 16.

From the simulation waveforms indicated in Figs. 15 and 16, it may be observed that LIF model behaves the similar way for both models. However, there is slight reduction in accuracy with respect to the approximate multiplier output.

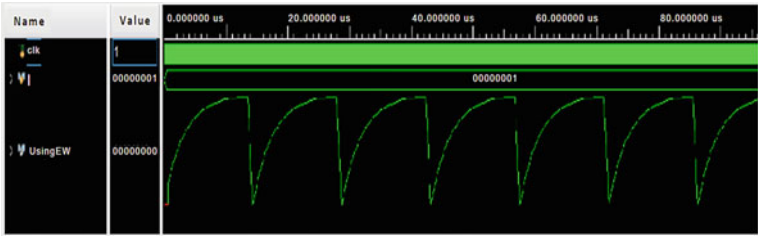


Fig. 15 LIF neuron waveform designed using state-of-the-art multiplier

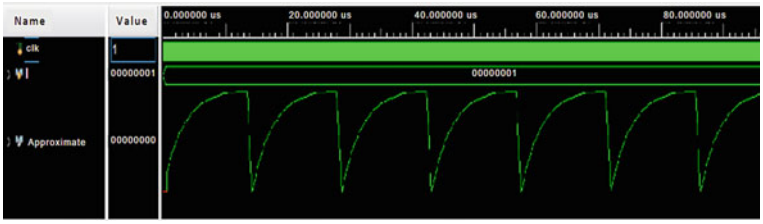


Fig. 16 LIF neuron waveform designed using approximate multiplier

It may also be observed that there is variation in the firing interval between the two waveforms. On an average approximate multiplier-based LIF neuron-based models work exactly like the exact multiplier cases 96.876% of times. Thus it is evident that approximate multipliers may be used instead of the exact multipliers which are more power, area, and delay efficiently.

7 Conclusion

In this study, the performance of two modern approximate 4:2 compressor topologies is evaluated. First, a high-speed area-efficient compressor architecture that, in contrast to other existing compressor designs, provides a significant decrease in multiplier characteristics including size, delay, and power The design has a 25% error rate, which is quite accurate. In addition, updated dual-stage compressor design is evaluated in the article, which further improves multiplier settings using the same accuracy measures. Utilizing transistor-level design and implementation, the architecture was created using 45-nm technology and a 1 V supply voltage. Using the 8×8 multiplier in various image processing applications served to validate the architecture. A selection-based 8×8 approximation multiplier that can handle both unsigned and signed operations is also developed.

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Integration of Particle Swarm Optimization and Sliding Mode Control: A Comprehensive Review

Sathisha Shetty, Abdul Kareem, and Ganesh Aithal

Abstract Particle swarm optimization (PSO) is among the prominent computing approaches that rely on population-based optimization. It is coupled to a swarm intelligence cluster and is used in global optimization challenges. Sliding Mode Control (SMC) is a first-order control approach which has a broad range of mechanical device applications. But due to its disadvantages such as chattering effect, a higher order control mechanism is necessary. Super-Twisting SMC (ST-SMC) is a second order control mechanism, has advantages like reduced chattering effect, and achieves convergence in time. In this review article, first a comprehensive review on PSO and its applications is performed. Later, ST-SMC is reviewed in detail and then optimization of SMC parameters using PSO for autonomous vehicle is discussed.

Keywords Swarm intelligence · Particle swarm optimization · Optimization problems · Tuning SMC parameters · Chattering effect

1 Introduction

An external disturbances and model inaccuracies cause instability in the system, it poses a paramount challenge to bring stability in spite of uncertainties. As recorded in various applications and research articles, Sliding Mode Control (SMC) is an effectual methodology in achieving this goal. Accomplishment of SMC is simple, straight forward and needs only few parameters to be considered. But it is tedious with respect to fine tuning of controller parameters, also dependent on sophisticated

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methods. Due to worst case assumptions in SMC leads to higher gain, but tends to produce unwanted effects such as chattering. The Super-Twisting Sliding Mode Control (ST-SMC) may eliminate chattering while also maintaining stability across a large parameter range. In the Conventional SMC, the equilibrium point is generally asymptotic and not finite time; the ST-SMC not only reduces the chattering effect, but also brings the equilibrium state in the finite time thus takes a vital role in design of the SMC. ST-SMC can explicitly adjust and track the system by conquering the uncertainties and outside disturbances. It is comparably simple and has a wide range of applications due to the fact that it just requires a sliding variable to apply the control law. The Super-Twisting Algorithm (STA) is a Second Order Sliding Mode (SOSM) approach that allows finite period of time convergence of not only sliding variables but also their derivatives. STA implies, in specifically, zeroing the sliding variable and first derivative within a certain time frame.

The ST-SMC is perhaps the most contemporary type of sliding mode controller, providing the distinctive characteristics of sliding mode control techniques while creating a smoother control signal than the ordinary sliding mode controller. As a result, ST-SMC has far less chattering than conventional sliding mode control.

Additionally, unlike second order sliding mode controllers, the ST-SMC technique has a simple method for ease of implementation since it does not require the derivatives of the sliding surface function. The dynamic performance of ST-SMC, on the other hand, is determined by the controller settings. Nevertheless, determining the ideal parameter values is a time-consuming operation.

Swarm Intelligence (SI) is a novel distributed intelligent model for addressing optimization problems that was inspired by the biological examples of swarms, flock, and grazing in vertebrates. The idea for Particle Swarm Optimization (PSO) came from a group of birds flying, swarms of bees, and human decorum at social gatherings. PSO is a population-based opti-mization method that is simple to design and deploy to address optimization issues. PSO has a significant advantage over other optimization methods, including Genetic Algorithms (GA), Simulated Annealing (SA), and many others, in terms of speed of convergence. As population-based optimization is tends to be expensive since, its dependency on function values is on the higher side, susceptible to untimely convergence; that is the instance when many decision variables are optimised. As a result, the PSO method is a feasible choice for determining the best combinations of super-twisting sliding mode controller settings.

2 Literature Review

A thorough literature review is conducted in order to comprehend the most recent research work on Particle Swarm Optimization and ST-SMC.

A. Particle Swarm Optimization (PSO)

The Adaptive Inertia Weight Particle Swarm Optimization Algorithm (AIWPSO) was created to address the challenges of global exploration and local exploitation of the

population in the particle swarm optimization algorithm. This strategy compensates for the inaccuracy of random mutation and in- creases the diversity of inertia weights [1]. For optimising the controller settings of a Fuzzy PID controller, a novel technique called hybridization of improved particle swarm optimization Algorithm and Cuckoo Search Algorithm (HIPSO-Cs) is proposed [2]. The basic PSO is enhanced in this approach by linearly lowering the number of particles and the inertia weight, and then a Cuckoo Search Algorithm's local random walk procedure is utilised to boost particle homogeneity. This has resulted in enhanced convergence correctness and iteration speed.

Robert et al. introduced a Culled Fuzzy Adaptive Particle Swarm Optimization (CFAPSO) technique for Collaborative Beamforming to increase the transmission range of Wireless Sensor Networks (CBF). CBF is frequently made up of highly multimodal functions, whereas traditional PSO is susceptible to premature convergence. To deal with it, a novel fuzzy-logic-based confidence and inertia weight parameter adaptation technique has been developed [3].

The author [4] proposed a prototype to reduce the snag of the formal PSO algorithm. The suggested concept was based on Bayesian optimization and stochastic surrogate, in which the model uses a Gaussian process to past estimations of the objective functions to predict the particle shape and thereby modify the movement of the particle. The experimental results of the suggested concept surpass the experimental results of SPSO2011.

The complexity on the number of views on a given set of data in multi-view learning was addressed by the author in his work [5]. To address the complexity, the author exhibited an optimization technique based on Multi-Objective Particle Swarm Optimization (MEL-MOPSO), which was developed with two key goals in mind: the number of data views and the classification accuracy of multi-view supervised methods. The study showed that the optimization process outperformed the existing model and obtained an efficient and effective result.

It is proposed to use an ensemble filter feature selection with PSO and SVM harmonised classification (Ensemble-PSO- SVM) [6]. The author describes the difficulties in prediction of the treatment for a patient depending on the volume of datasets available for the process. The author also pointed the importance of data dimensionality and classifier parameters on the accuracy of the system which are dependent on each other, performing them independently may reduce the system accuracy or efficiency. Tengku Mazlin Tengku Ab Hamid et al. designed an algorithm to remove the unnecessary features based on ranking and to erase the dependency problem between the data sets and accuracy of the system. A unique approach based on multi filters was proposed using the information gain (IG), Gain ratio, Chi-squared, and Relief–F. The system kernel was used to optimise the search results using Particle Swarm Optimization and Support Vector Machine in order to increase accuracy of classification.

The author points at the negative effects of unessential, turbulent and immaterial features used for classification in Machine learning and Data mining process. The effect of these unnecessary data or the attributes can be reduced by filtering the

features during the pre-processing stage. To mitigate the negative impact of negative datasets, an unique hybrid binary version of improved chaotic crow search and Particle swarm optimization approach is created [7]. The proposed system combines enhanced version of CSA algorithm and particle swarm optimization.

The researchers proposed a method for regulating differ-ential settling in an autonomous vehicle utilising higher order SMC and the super-twisting algorithm. The PSO technique was used to optimise the control parameters of higher order sliding modes. The findings of the proposed systems indicated that higher order sliding mode control with parameters optimised by Particle Swarm Optimization yielded better outcomes over random ones [8].

El-Shorbag and Aboul Ella Hassanien [9] evaluated the implications of particle Swarm Optimization in Swarm Intelligence. The authors have presented different issues that may be handled using PSO, such as restricted optimization, unconstrained optimization, nonlinear programming, multi-objective optimization, stochastic optimization, and combina-torial optimization. The discussion started with an overview to PSO behaviour, basic concepts and principles, and PSO innovation.

B. Super-Twisting Controller

To overcome the problem of trajectory tracking and quadro-tor stabilisation, the authors [3, 10, 11] suggested a super-twisting approach with better proportional integral derivative sliding mode control. To validate the overall stability of the rotational and translational controls, the Lyapunov Theorem is applied. The authors proposed an Adaptive Super-Twisting Sliding Mode Control for micro gyroscope application to achieve the enhanced convergence rate of reaching the sliding surface and trajectory tracking. To obtain, assess, and compute the unknown parameters and angular velocity, a Lyapunov stability theory is applied [12].

In this Lyapunov function is used for the STA, adaptiveness of the proposed controller design is exploited with certainty-equivalence principle [13]. The simulation result has shown the advantages such as structured and unstructured uncertainties are considered.

Ramesh Kumar and Bijnan Bandyopadhyay [14] presented a 6-degree-of-freedom paralleled robot that predicts leg lengths using inverse kinematics and a dynamic gain super-twisting technique that outperforms serialised robots. The su-per twisting observer was used to determine the appropriate leg velocity. The suggested model employs global finite amount of time convergence to provide the appropriate sliding surface for Stewart platform position stabilisation, which has been accomplished in the presence of uncertainties.

A robust tracking method is explained the author [15] for controlling the nonholonomic wheeled mobile robot. In the internal loop, the suggested model employs an inverse dynamic control, while the exterior loop employs a strong kinematic control using sliding modes control. The authors also depicted the deteriorated performance in the system due to the presence of chattering phenomena caused by the unmoulded dynamics.

Jayakrishnan [16] developed a quadrotor remotely piloted aircraft by cascading with an inner outer loop con- struction and using a ST-SMC. The introduction of the

super-twisting algorithm reduced the chattering impact, while the SMC eliminated model instability and disruptions. The per- formance of the solutions that have been verified against wind turbulence. The experimental setup's results were compared to those of a linear LQR-PD controller and a nonlinear feedback linearization-based controller. The experimental findings of the first-order sliding mode controller also were compared to the suggested system in terms of robustness.

The scholars [17] established the second order SMC tech- nique that is effective in dealing with uncertainties and external disturbances. The design is for a hovering wind turbine that uses collective blade pitch control. The results of the system were compared with traditional gain PI controller.

A block-controllable model was proposed for the evaluation of Sliding mode control for a rendezvous mission by the authors using a back stepping setup for a Super-Twisting SMC. By taking into account the relationship between translational and attitudinal movements, the suggested method was utilised to launch a timely restorative mission between the chaser spacecraft and an inactive target into a circular orbit around Earth [18].

von Ellenrieder and Henninger [19] proposed a resurrected third order sliding mode disturbance observer architecture for a super-twisting controller that was used for trajectory tracking in fully-actuated maritime where there's unidentified and scalar disturbances with respect to the time. The observer controller creates a generic vector form that may be employed in maritime vehicles, as well as configuration spaces with three, four, and six degrees of freedom. The suggested technology's value is demonstrated via simulations.

The author took advantage of the system's superiority, which was constructed using the particle Swarm Optimization method, to develop the Sliding Mode Control solution for quadrotors with unpredictable disruptions. To demonstrate the process initially author built a dynamic model of the controlled quadrotors with external interferences. An improved Radial basis function neural network was used to develop a sliding mode control system for quadrotors with unpredictable disruptions in order to reduce the interferences. The efficacy of the investigated model is defined by the author's demonstration of the system using a rapid and smooth trajectory tracking system [20].

The authors presented [21] a novel technique for ST-SMC that removes the tedious attempt process in determining the design criterion to obtain optimum performance of the controller. The main aim of the proposed system was to remove the chattering problem of a traditional SMC and also to inscribe the finite-time convergence of system trajectories to their analogous equilibrium states in a single axis propeller driven aircraft.

Humaidi and Hasan developed [22] a revolutionary approach for a super-twisting sliding mode controller for two axis helicopter that requires less time to gain homeostasis and eliminates chattering. The suggested model was developed utilising the Lyapunov principle to forecast the unknown characteristics of a helicopter with two degrees of freedom.

The author of this research [23] suggested a unique strategy for overcoming the control issues associated with nonlinear and undermined systems using set-point

weighting for super- twisting sliding mode control employing full order state observers. The author considered Quadcopter UAV to show the conclusion of the procedure, which is an excellent example of under actuated systems, for the implementation of the pro- posed work. The process findings indicated that the proposed system performed better than SISTASMC in dealing with uncertainty.

3 Integration of PSO and SMC

A new control strategy with combining PSO and SMC is proposed [8], for the autonomous vehicle. Here PSO is used to optimise forces operating on the vehicle's embedded force sensors. ST-SMC is utilised to provide lateral control at greater vehicle speeds. PSO is used to improve the settings of SMC for tracking reference trajectory, enhancing accuracy of the system, and velocity. A bicycle model is used to demonstrate the vehicle's lateral behaviour (see Fig. 1).

The Chattering effect is a severe drawback of SMC; to lessen it, the following strategies can be used: use of smooth functions, observer-based approach, and higher order sliding mode. ST-SMC is a second order system that may be applied to a system of subjective degree one, the derivatives of which is expressed in Eq. 1:

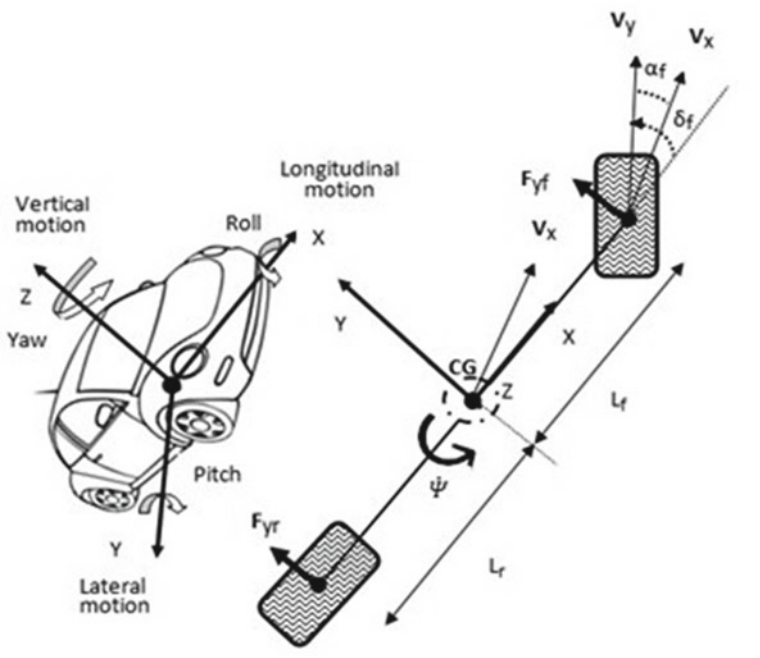

Fig. 1 Bicycle modelling vehicle and vehicle structure movements [8]

$$\dot{s}(t,x) = \Phi(t,x) + \phi(t,x)u(t) \tag{1}$$

The goal of this design procedure is to ensure that $s = 0$ ensures convergence to the sliding surface; to do this, s must be measured in real time. Researchers Kennedy and Elberhart invented the PSO, it is swarm theorem based simplified model, the velocity vectors of every particle are utilised to update the location of each and every particle inside a swarm. PSO start off with a random particle made up of "m" particles and the location is then updated by taking into account the fact that its memory, reasoning, and social behaviour aid in the finding of each new particle, as shown in Eq. 2.

$$\begin{aligned} v_i(j+1) =& w v_i(j) + c_1 r_1 (p_i(j) - x_i(j)) \\ &+ c_2 r_2 \big(p_g((j) - x_i(j))\big) \end{aligned} \tag{2}$$

$$x_i(j+1) = x_i(j) + v_i(j+1) \tag{3}$$

where j and w indicate the number of iteration and inertial weight, and c1 and c2 are random values distributed evenly between [0,1]. The ith possible solution of the issue is rep- resented by xi, and the flying velocity is represented by vi. The personal and global bests are represented by pi and pg. PSO is used in this experiment to assess the sliding control parameters. Strategy followed to optimise the SMC by PSO is:

Retain the all-other parameters of SMC and optimise only λ.
Retain the all-other parameters of SMC and optimise only β and α.

The improvement of SMC parameters using PSO resulted in much greater angular velocity than the regular SMC settings.

4 Conclusion

A detailed review on theory and applications of PSO and ST-SMC is carried out in this article, and the optimization of ST- SMC parameters using PSO is also considered. It has been discovered that the Adaptive Inertia Weight Particle Swarm Optimization Algorithm (AIWPSO) is the most coherent solution to overcome the hurdles of population-based optimizer's global exploration and local exploitation concerns. To overcome the limitations of the formal PSO technique, a Bayesian optimization and stochastic surrogate model that predicts particle shape and updates particle movement was proposed. ST-SMC is effective to suppress the chattering effect as it is higher order control method, integration of PSO and SMC is discussed for autonomous vehicle. The parameters optimization using PSO has shown significantly effective results as compared to the original parameters of the SMC.

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Design and Testing of a Solar Powered Automated Fruit and Vegetable Sorter

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Abstract The Middle East and Dubai are specifically well known for their large number of Hypermarkets, Supermarkets, and Groceries, generating a huge demand for high quality consumables such as vegetables and fruits. Modern Retailing will benefit much from offering fruit and vegetables sorted by quality (based on physical characteristics such as weight, size, color, shape, smell, etc.)—an essential step in post-harvest management for offering quality agricultural produce to the consumer. The proposed work focuses on sorting fruits and vegetables based on Color and Shape. It uses a Convolutional Neural Network Architecture (Deep Learning) for Fruit/Vegetable Sorting (Inception V3). High torque geared DC motors are used to operate the Conveyor belts. Graphical User Interface (GUI) is to be created and incorporated to make the system user friendly. Raspberry Pi 3B has been used to interface the entire system. System is programmed using Python 3 with Open CV and TensorFlow modules. System has been designed to use Solar Energy to make it sustainable. System is designed to sort 30 fruits/vegetables in a minute.

Keywords Vegetable sorter · Convolutional neural network · Deep learning · Computer vision

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1 Introduction

Automated systems are taking the world by storm due to their ability to ease and reduce user effort. In the olden times, people had to plow, sort, tend, and harvest crops, which is not the case anymore; and this was possible through systems that the users operate. Today, one conceives systems intelligent enough, that can make decisions that not only manage, but also boost harvest. This paper shall initially enlist the research done in current systems and further explain about a proposed system that has the capacity to sort multiple fruits and vegetables using artificial intelligence techniques and associated hardware. The aim of the system is explained along with appropriate methodology and system details. The retail industry shall highly benefit from such a system due to increase in the quality of products being delivered. While produce is grown, it experiences the harshness of climate, and one must discern defective yield before it is put up for sale. This paper tackles the need of such a system and proposes how it can be implemented. The system has been constructed in a manner in which it is able to harness renewable solar energy, through the utilization of 12 V, 100 W Solar Panel. Further on, details of the components that utilize this power are listed and a power calculation for the sorter is done.

2 Current Systems

Automation has seeded its roots into almost every sector. The attention of this paper is centered on the sector of agriculture and shall initially focus on the several methods currently being employed for enhancing the intelligibility of systems to be able to make human-like decisions. Further, this literature review shall attempt to enlist different existing agricultural automatized systems and food retail automatized systems pertaining to sorting using cutting-edge technology.

2.1 Agricultural Automation

Machine Learning Algorithms are using Convoluted Neural Networks (CNNs) from Deep Learning Techniques to achieve higher accuracy in crop disease detection, weed identification, fruit counting, classifying land cover, and recognizing and classifying several crops. These algorithms are executed using robots that are suited to agricultural terrain. Agricultural operation is dependent directly on the performance of the robot, which in turn depends on the ML/DL Algorithm which is trained on a collected dataset (furthering the importance of accurate collection for the precision of the end-result) which are executed on robotic platforms to manually control several components that make up a robot [1]. To enhance soil fertility, automation is done through technology such as aerial imagery using thermal and RGB cameras.

Things plants need, along with matching of objectives such as Yield, NKP utilization, Risk factors are done in a Decision Layer [2]. Usage of Terahertz waves within the frequency of 0.1–10 THz is used to classify the sound quality of food, making it a non-invasive method of determination. These waves consider, through spectroscopy and image analysis, water monitoring, soil sensing, detection of adulteration in multiple forms, monitoring, and analysis of the degradation of physicochemical processes [3]. Digitization of agriculture is not just limited to image processing; artificial intelligence has made the ill-effects of the impossibility of expansion of land into minor inconveniences through the inclusion of smart farm machinery which includes bed preparation, sowing, harvesting, and weeding. Sensors are used for continuous monitoring of what initially used to be a tedious handled by farm workers; real-time data is accurately sent and stored without the need for human intervention. Although management of the resources and methods relies on the usage of CNNs [4]. Wireless Sensor Networks are currently being used to promulgate enhanced precision farming, to be able to predict and manage crop output projections, and accordingly optimize proceeds [5].

2.2 Quality Control

For quality control, recent technology has adopted ultrasound—it is being used in the drying field to direct temperature variations and enhance methodologically/reduce physical pre-treatment procedures [6]. Application of external substances such as electrolyzed water [7] and aloe vera [8] have showed promising results as well in not only increasing the shelf-life of produce, but also reducing the hazard of losing nutrients in food, thereby degrading its quality. Further ozone technology has displayed promising results in maintaining the life of foods without emission of toxic substances into the environment [9].

2.3 Sorting

Depth Camera is being used for optimal sorting of dragon fruits considering plant disease using CNNs, while maintaining a Threshold through Deep Learning. Basic Features of the food were detected, using feature extraction for training and testing. This was physically accomplished using the Raspberry Pi device to count the number of dragon fruits and display the total number of fruits. The sorted selection could differentiate between High, Medium, and Low Quality, as well as Infected fruit [10]. The SORT algorithm-based tracker could track historical information and detect any infection; guided robot arms picked out defective ones, to prevent manual sorting [11]. YOLOv3 trained to detect holes in lotus seeds through an online sorting mechanism which was supplemented an auxiliary algorithm to put in appropriate bounding boxes and increase the accuracy [12]. Sorting Algorithms have also moved on to focus

of the ripeness of fruit using the stochastic decision fusion (SDF) methodology and CNNs by initially using the ConvNet to employ a Deep Learning Model to analyze imagery and using the SDF to classify and label. The model was trained on 2712 tomato sample images (stem end and flower end) collected using a CCD Camera using Ground Truth Annotation software. At least 500 samples were collected for every defined ripeness stage to finally move through the pipeline to generate a predicted confidence score and ground truth [13]. Grading and Sorting done for onions, included categories—size, quality, and shape. Two labels were the end result, Defected (Unhealthy) and Healthy (Good Quality). Hyperparameters such as Input image shape, kernel size, pool size, dropout rate, activation function, and batch normalization are tuned to minimize validation loss [14]. Apart from full fruits, similar techniques have been used in detection of ginger and chickpeas powder having samples with 0, 10, 20, 30, 40, and 50% of counterfeit product [15]. Image Recognition Software is used to obtain a 'time-effective solution' using similar techniques as enlisted above [16]. 'Alternating Circumrotating mechanisms' consisting of an electromagnet, blocking piece, and motion track to understand if the bean is normal, cracked, bitten by insects, diseased, and mildewed, have also been used to detect full-surface defects [17].

Therefore, one can understand that Deep Learning and Computer Vision have made the issue of detection of defects and easy sorting of produce simpler and automated. The system proposed in this paper aims to fulfill similar goals, but it is not limited to a single fruit species. A unique conveyor system has been employed to sort fruits at the rate of at least 30 fruits or vegetables per minute. This paper shall now delve into explaining the proposed system, demonstrating its features, and explaining its construction. The major aim of creating this system is not just limited to automation, but the vast utility it can share into the retail system. One can ensure that only quality produce reaches the customer, which shall not only lead to increase in brand loyalty and revenue, but also have a robust system that has the capacity to deliver quality product faster.

3 Methodology

To begin the groundwork for the proposed system, a survey was conducted to understand the different types of commercial sorters currently available in the market. The top relevant technologies have been listed below. Based on the benchmarks set by large commercial sorters, small scale system is formulated for the project. A preliminary design was worked up to provide a graphical idea of the mechanism. Based on the preliminary design, a 3D model with dimensions and constraints was formulated using the CATIA V5 tool (Table 1).

Based on sorting time and speed constraints, actuators were selected to perform the different mechanical operations in the design—servomotors to perform the actual sorting process, speed-controlled DC motors to drive the conveyor belt, and solenoid valves to release fruits or vegetables from the hopper. High frame rate cameras are

Table 1 Survey of current industrial technology for sorting

#	Current systems and their specifications		
	Name of the system	System details	Merits
1	Taiho fruit and vegetable grading system [18]	The system mainly comprises a feeding machine, a conveyor belt, a hoist, a fruit arranging machine, a visual inspection line, and a weighing line. The fruit and vegetable grading system in the FG series can provide a corresponding system solution scheme tailored individually to each customer according to his/her needs dynamically, which reduces cost, improves work efficiency, and maximizes the profitability	Taiho owns an independent core technology of the fruit and vegetable grading system in FG series. Using the computer vision and nondestructive detecting technology, the system classifies fruits and vegetables by shape, color, defect, internal quality, and weight comprehensively and accurately, and is very competitive in the marketplace
2	Optical sorter using a three-way separation [19]	This machine is capable of sorting tomatoes according to desired color. Depending on the application, it can reject either product of incorrect color or any foreign bodies from the product stream	The range of application is very wide; from tomatoes in general to peeled tomato, and to red peppers
3	Multi-functional single layer belt-type AI sorter [20]	Color sorter/color sorting is used for sorting granular materials according to their difference of optical properties, widely used in rice, wheat, grain, food, tea, plastic, chemical, and recycling	There is support for multi-vision technology for sorting without blind spot

mounted on a beam to provide real-time images for sorting as the produce moves along the belt. The actual sorting process is carried out by a CNN model, developed based on the algorithms provided by Google's Inception V3. Further, the proposed work has used Python 3.6 IDE and TensorFlow 1.10 deep learning framework. 12 V, 250 W Polycrystalline solar panel is used for powering the entire system. 12 V, 40 AH Solar gel battery is used for the storage, and charge controller is used to control the battery charging current.

3.1 Block Diagram

The major components of the Functional block diagram of the sorting system as shown above, along with their features, are listed as follows (Fig. 1):

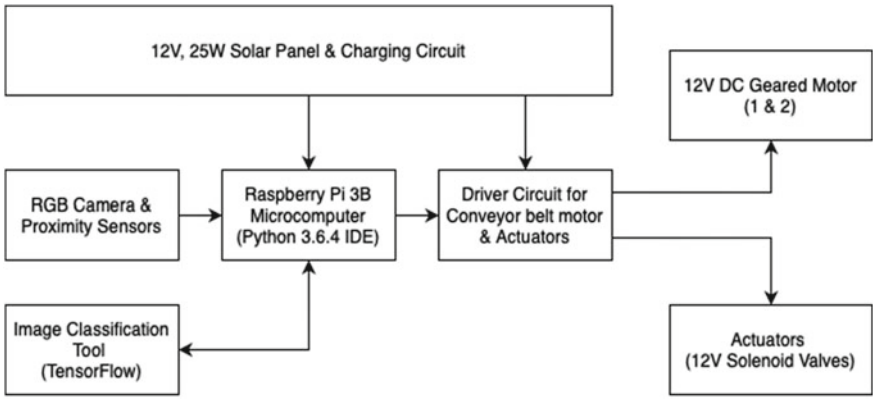


Fig. 1 Block diagram of the proposed framework

- Conveyer belt: Objects to be sorted are placed on the conveyer belt. It is operated using stepper motor with 5 V, 1 A specification. MOSFET-based driver circuit drives stepper motor.
- USB camera: Colors of the objects placed on the conveyer belt are sensed and OpenCV library is the software which included in Python IDE responsible for the detection of the color.
- Actuators: Solenoid actuators are used to push the objects to the appropriate bins.
- Raspberry Pi 3B: has been used for interfacing. The coding has been done in Python 3 with OpenCV and TensorFlow module.
- Convolutional Neural Networks: Sorting is accomplished through CNNs—the Inception Algorithm with TensorFlow is implemented in this project.
- Graphical User Interface: User and System Friendly Environment is generated through the GUI for easy interaction.

3.2 Workflow

The initialization process includes the following steps which need to be taken before the system can begin sorting:

- Check component availability
- Start up the conveyor belt
- Start cameras
- Check the Proximity sensor for Bin 1 and Bin 2 (Fig. 2)

The procedures described in the flowchart above are described as follows.

Step 1. Starting of the whole process with an inbuilt button from a GUI.

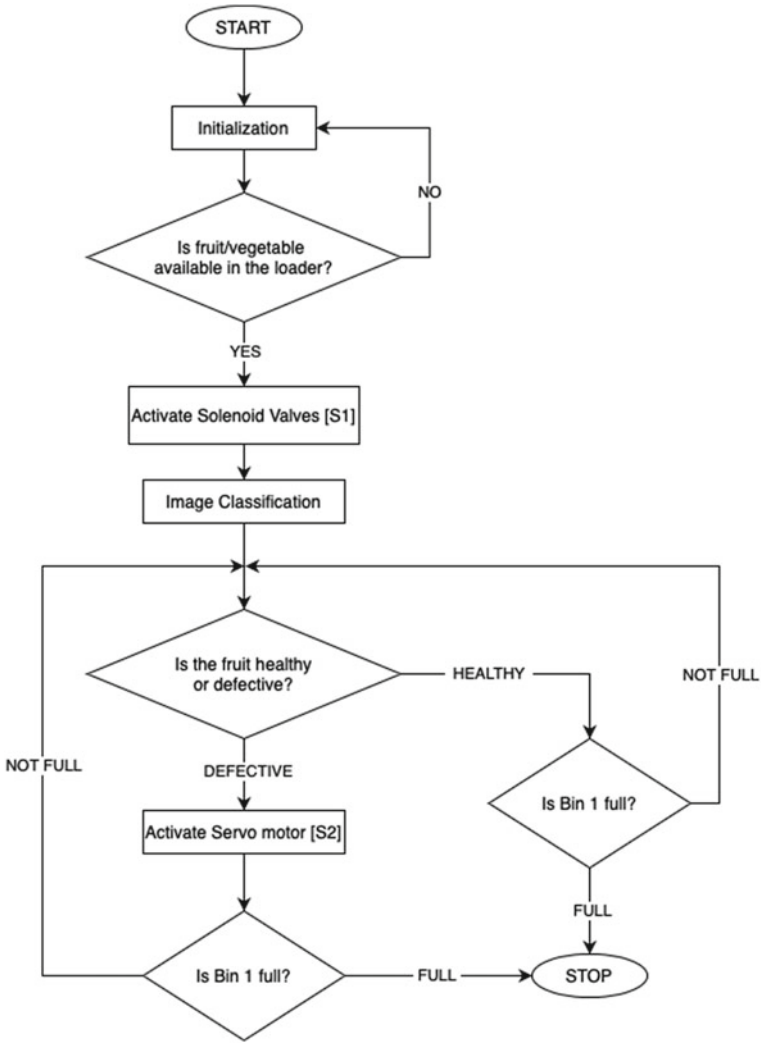


Fig. 2 Flowchart of the proposed system

Step 2. This involves the initialization of program functions and code from the Raspberry Pi. The process may include:

- Executions of Python codes
- Start up the conveyor belt
- Enable solenoid valves (S1 and S2)
- Enable cameras (C1 and C2)
- Enable proximity sensor (P1, P2, and P3)

- Enable servo motors (SV1 and SV2)

Step 3. Object classification using deep learning tenser flow software installed on the raspberry using python code. This is used to detect if the fruit is good or bad depending on the shapes and color by using the high-resolution camera.

Step 4. Object status is done in other to differentiate the good fruit from the bad ones in which the servo motor is activated.

Step 5. The servo motor pushes the good fruit to Bin 1 and allows the bad fruit into Bin 2 through the conveyor belt.

Step 6. When any of the Bins are full (or both) we get a buzzer alarm, or the system stops working for some time.

3.3 Design of the Proposed System

For the creation of selection of the motor for the conveyor belt, the following considerations were systemized:

- 30 fruits/minute or 1 fruit in 2 s
- Length of the conveyor: 90 cm (3′)
- Load on the conveyor: 2 kg
- Diameter of the motor: 2 cm
- Linear distance = 2 × 3.14 = 6.28 cm
- One revolution = Approx. 6 cm
- For 90 cm = 90/6 = 15 revolutions

Based on the above, the subsequent dimensions are set (Fig. 3).

The three-dimensional computer model of the proposed design of the automated fruit and vegetable sorter was designed using CATIA version 5 by Dassault Systems (Fig. 4).

3.4 Construction of Vegetable Sorter

After creation of the 3D model, a prototype was generated, which was ultimately transformed into a working system. Both can be viewed as follows (Fig. 5).

Specifications of the Sorter are conscripted below:

- 30 Dimension of Sorter: 90 cm
- Conveyor width: 5 in.
- Spacing between two conveyors: 5 in.
- Total dimension of the sorter: 150 cm × 15 in.

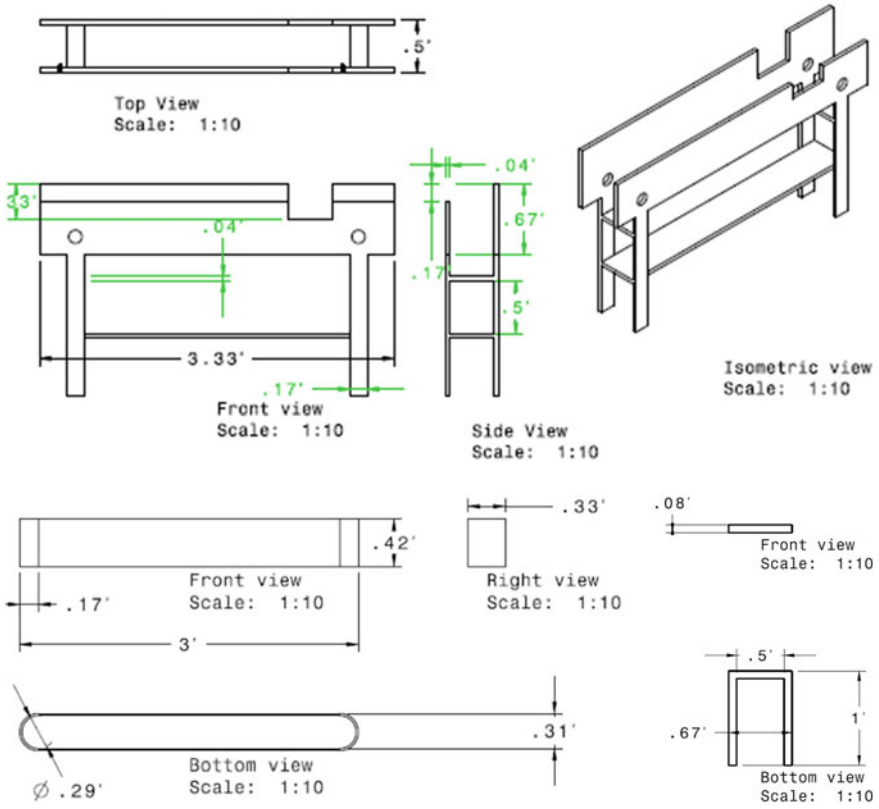


Fig. 3 System dimensions

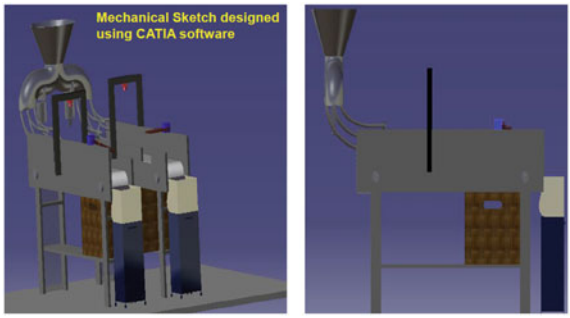


Fig. 4 Views of proposed system

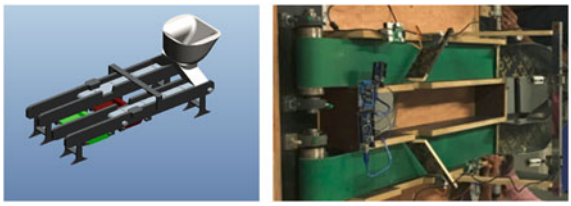


Fig. 5 Prototype and constructed model

4 Methodology

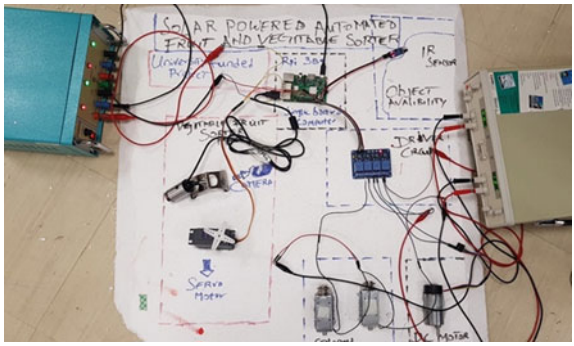
This section has been divided into three parts to discuss the development of the GUI for operating the sorter, Testing of the sorter using the Testbench, and Power Calculation.

4.1 Development of GUI

The graphical user interface is used to control the operations of the vegetable sorter and also give information on the status of the Bin if it's full or not. We can also control the speed of the conveyor belt and we can know the count of the vegetable/ fruits sorted from the GUI. The GUI is created using Python codes and makes use of an important module such Tkinter. Screenshot of GUI is shown in Fig. 6.

Fig. 6 Graphical user interface

Fig. 7 Testbench



4.2 Project Testbench

The test bench shown consists of various components listed under the literature review arranged in such a way that the vegetable sorter should work according to the flow chart given in Fig. 2. The test bench operates step by step based on the code written using Python, the code can be seen below (Fig. 7).

4.3 Power Calculation

The components that are needed for Solar Power Source are listed below:

- Polycrystalline Solar Panel—12 V, 150 W
- Lead Acid Battery—12 V, 20AH-1
- Solar Charge Controller (Table 2)

Table 2 Power calculation

#	Current systems and their specifications		
	Components	System details	Merits
1	DC motor 1 and 2	12 V DC geared motor-157 RPM-stalling current-5 A (full load) × 2	120
2	Servo motor 1 and 2	4.4–6.6 V—20 kg cm—2 A × 2	10
3	Solenoid actuator 1 and 2	4 W × 2	8
4	Raspberry Pi 3 B		1.2
5	IR sensor IR-08H	Max current: 40 μA at 3.3 V	Less than 1 mW
6	PAPALOOK 720P Webcam PA150 1 and 2	Current rating <220 mA × 2 (5 V × 0.22 A × 2)	Approx. 2 W
Total power consumed			Approx. 140 W

5 Conclusion

This proposed work has combined clean energy and artificial intelligence to help sort vegetables and fruits easily. The object sorting system is capable of sorting objects based on color and shape. Python utilizing OpenCV with Tensor flow software for image acquisition has been systemized along with the operation of conveyor belts and actuators for real-time dynamic sorting to support the massive retail systems. One can see that while this system is a step forward in the direction of automation for agriculture, as future scope, efforts shall be made to increase the efficiency and accuracy of the color and shape detection of the system using robust algorithms. Further steps shall be taken to increase the system usability.

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Characterization of Dust Particles and Their Impact on the Performance of Photovoltaic Panels: A Laboratory Investigation

M. K. Bhushith, Ashok Rao, A. D. Srinivasan, and Suvi

Abstract The effective operation of photovoltaic (PV) systems is substantially deterred by various factors like irradiation, temperature, soiling (dust accumulation), icing, and air mass. This paper considers the effect of soiling on the performance and operational life of a PV panel. Initially, the physical and chemical properties of the five most commonly encountered dust particles are examined using the images and data obtained through scanning electron microscope (SEM) and electron dispersive spectrometer (EDS). The impact of these soiling agents on the electrical performance and operational life of a PV panel is investigated in laboratory conditions using a test setup. I-V curves for each of the dust samples are obtained and the reduction in power output is also documented. Furthermore, the paper highlights the invalidity of generalized cleaning techniques for PV panels by taking into account the heterogeneity of the dust particles encountered in PV installations across the globe.

Keywords Photovoltaic · Soiling · Scanning electron microscope · Electron dispersive spectrometer · Heterogeneity

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1 Introduction

The unprecedented decline of emphasis on fossil fuels and the dramatic changes in global climate since the past few decades are propelling the growth of solar and other renewable energy technologies across the globe as it is a sustainable alternative to fossil fuel-based power plants. The eco-friendly nature along with the scaling and decentralization advantages of PV technology solidifies its place as an effective source of electrical energy for the present and the future.

The functional unit of a PV system is a PV cell, which converts sunlight into electricity without any intermediate electro-mechanical conversions. Ongoing materials research is still a long way from demonstrating exceptional conversion efficiencies in commercially available silicon-based photovoltaic panels. The installation and functioning of PV systems for optimum yield are mandated by the geographical location and design motifs like seasons, orientation, altitude, local insolation, and tilt of the PV panels. Even after these parameters are tackled appropriately, there are other trifling (overlooked) factors that hamper the performance of PV panels such as operating temperature and dust accumulation. These two factors dominate in an urban setting where large-scale PV applications are being deployed (rooftop systems and lately, proliferation of EVs).

Dust is the lesser acknowledged factor that quite significantly affects the performance and operational life of PV panels. Predominantly, researchers concentrate on the improvement of efficiency at the cell—level. But, in reality, due to the modular nature of PV technology, they are deployed mostly in dusty working environments and remote locations. Here, PV panel maintenance (keeping the panels devoid of dust/shading) is of paramount importance in the optimal generation of solar photovoltaic power. The impact of dust on the PV power production seems to become pronounced at the Mega Watt-scale installations. Thus, the economical production and export of solar power are also at stake.

Wide range of research studies across the globe have been undertaken that are centered around the impact of soiling on photovoltaic modules with a variety of operating conditions and time frames. Few of these studies have been reviewed in this article.

A study in the USA was carried out by Hoffman et al. on PV modules which was focused on surface soiling and delaminating of encapsulation [1]. Hoffman et al. also investigated the environmental variables that increase the dust deposition on PV module glass [2].

Mikhilef et al. from Malaysia examined the effect of dust on a photovoltaic module as a function of tilt angle. Pollens, fungi bacteria, volcanic particles, and vehicle exhaust were considered in this study [3]. Sulaiman et al. from Malaysia demonstrated a reduction of up to 18% in power where they considered mud and talcum for the experiments [4].

Jiang et al. from China conducted tests on PV modules where they obtained a reduction in efficiency by 26% for dust accumulation ranging from 0 to 22 g/m^2 [5].

In Kuwait, Wakim recorded a deterioration of 17% in PV power production due to the accumulation of sand on PV modules [6]. Salim et al. conducted experiments over a span of 32 weeks in Saudi Arabia where they witnessed a drop of 32% in photovoltaic performance [7].

Bing Guo et al. conducted research that focused on the effect of soiling agents and weather conditions on PV panels in Qatar [8]. F. Meja et al. showcased how soiling lowers the efficiency of solar PV plants and they found that soiling was vehemently dependent on the dry exposure time of the PV module. It was also observed that soiling losses were the highest during dry summers [9].

Monto Mani and Pillai R. from India have given general recommendations for mitigating the effects of dust on PV modules by taking into account the various climatic zones [10]. Ravi and Chetan S. Solanki reported that in India, a lot of the PV modules are working in dusty environments and power production is reduced significantly if left unclean. They eventually fabricated an automatic cleaning system with 180 sun tracking [11].

One of the world's technological leaders, Google, documented the effect of dust on a PV installation that generated 1.6 MW of power at their Mountain View headquarters in California. Two sets of PV arrays were considered for this study—flat ones (horizontally placed) on carports and tilted ones on the roofs of other buildings. Although the rain washed away quite a bit of dust on the panels, it was found that the impact of dust on the photovoltaic modules placed on carports was significantly higher as compared to the ones placed on roofs [12].

The review of the literatures presented in this paper is indicative of the research potential in this domain. This provides enough motivation to initiate and conduct research focused on the maintenance aspects of PV installations.

As can been seen from numerous works across the globe, pollution-related performance degradation is a matter of serious concern. What is not clear from these so far is quantifying clearly the nature of soiling and its relative performance. All of the above cases have looked at soiling by the heterogenous nature of impurities (soil, sand, vehicle exhaust, etc.). Thus, it is of extreme importance that the specific nature of soiling (dust) and its impact be looked at. This is the primary motivation for this research experiment that we undertook and are detailed below.

2 Experimental Setup

To examine and analyze the impact of various soiling agents on the electrical performance of a photovoltaic panel, a test setup is put together which consists of a wooden table on which a PV panel is placed. An artificial light source is mounted above the table which provides irradiation. Measuring instruments like a pyranometer and I-V curve tracer are used to obtain various operating data. This setup can be seen in Fig. 1.

A scanning electron microscope and an electron dispersive spectrometer are utilized to characterize the dust samples. The scanning electron microscope employed

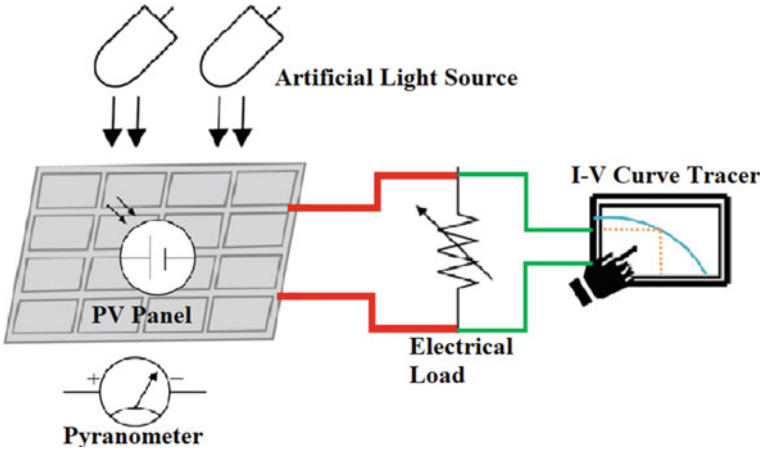

Fig. 1 Experimental setup

Table 1 Specifications of PV module

Parameters	Ratings
Rated power—Pm	20 W
Open circuit voltage—VOC	21.60 V
Short circuit current—ISC	1.20 A
Max. power voltage—Vmp	17.71 V
Max. power current—Imp	1.13 A
Module efficiency	12.01%
Electrical data @ 1000 W/m^2, 25 °C and a.m. 1.5 (STC)	

here is manufactured by Hitachi and the instrument model is S3400. Specifications of the PV panel considered for this investigation are furnished in Table 1.

Two light sources are considered because the intensity of the light incident on the PV panel will be evenly spread across it. The light sources are optimally placed at a height of 0.4 m from the upper surface of the PV panel. Black cardboards are placed around the PV panel which minimizes the effect of reflection and interference from the surroundings. DC fans are used to keep the temperature of the PV module at check. Irradiance is measured at several spots on the PV panel and the average of these values is considered for the study.

3 Characterization of Dust Samples

In order to better understand the complexities associated with the dust accumulation over PV panels, a meticulous analysis of the physical and chemical properties of dust particles is carried out. In this context, five most commonly encountered dust particles are considered—red soil, common soil, cement, vehicle exhaust, and sand which are dubbed as sample-1, sample-2, sample-3, sample-4, and sample-5, respectively. These five dust samples are specifically considered because they are quite commonly encountered at almost all the PV installations across the globe. The samples are shown in Fig. 2.

Micro-scale images of these samples are obtained through a scanning electron microscope. The SEM images and the associated data obtained reveal vital details about the physical properties of the dust samples. The SEM images of these 5 dust samples are shown in Fig. 3.

It is observed that samples-1, 2, and 5 are crystalline by nature; whereas samples-3 and 4 are amorphous by nature.

The images also reveal the mean particle size of these dust particles and the same is tabulated in Table 2.

Electron dispersive spectrometer is employed to study the chemical composition of each of these dust samples which is eventually used to obtain their respective pH value.

The dispersion profile obtained from electron dispersive spectrometer reveals the chemical composition of the samples and the same is presented from Figs. 4, 5, 6, 7 and 8. Their pH values are also tabulated in Table 3.

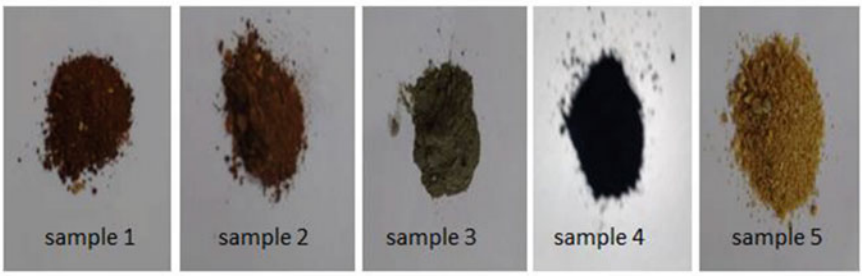

Fig. 2 Dust samples

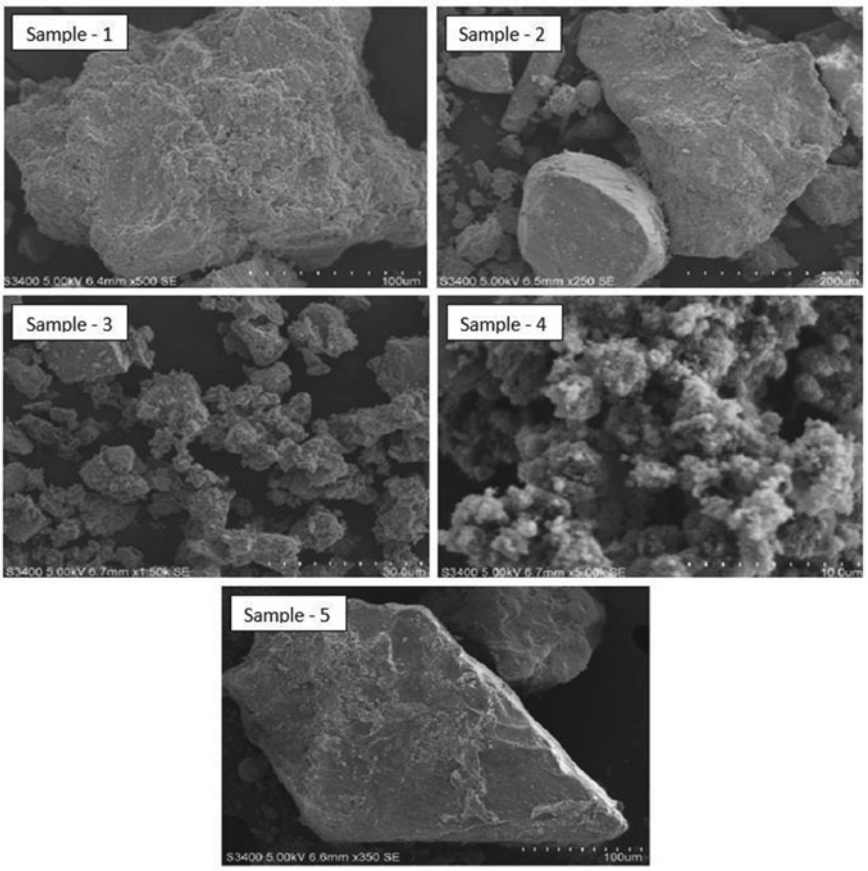

Fig. 3 SEM images of dust samples

Table 2 Data obtained from SEM

Sample	Type of dust	Magnification	Electron high tension (EHT) (kV)	Working distance (WD) (mm)	Mean particle size (μm)
Sample-1	Red soil	500x	5	6.4	100
Sample-2	Common soil	250x	5	6.5	200
Sample-3	Cement	1500x	5	6.7	30
Sample-4	Vehicle exhaust	5000x	5	6.7	10
Sample-5	Sand	350x	5	6.6	100

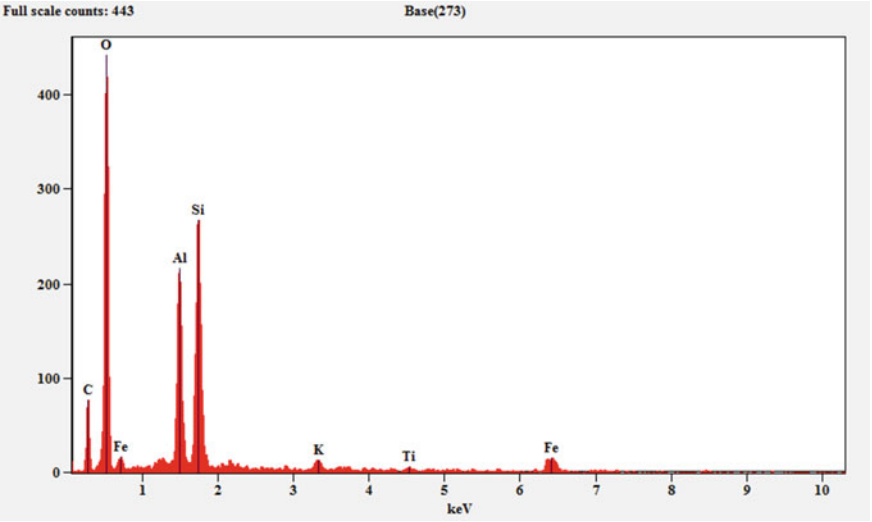

Fig. 4 Dispersion profile of red soil obtained from EDS

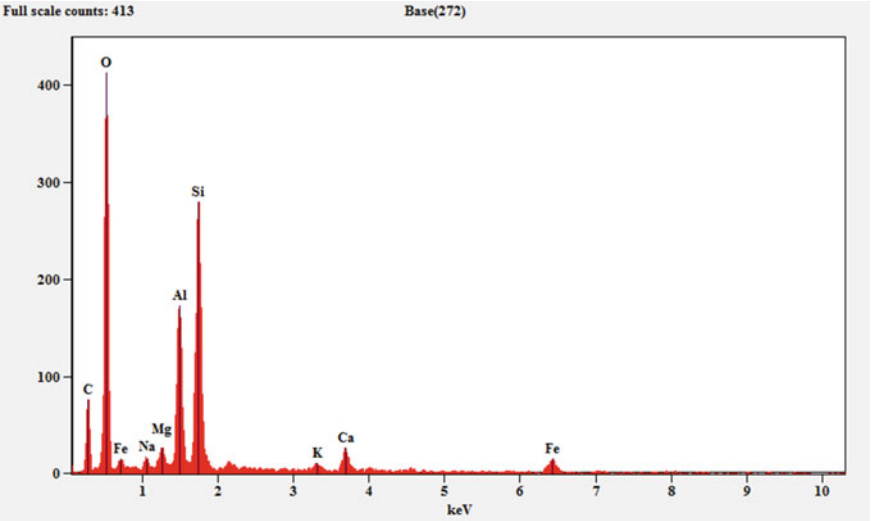

Fig. 5 Dispersion profile of common soil obtained from EDS

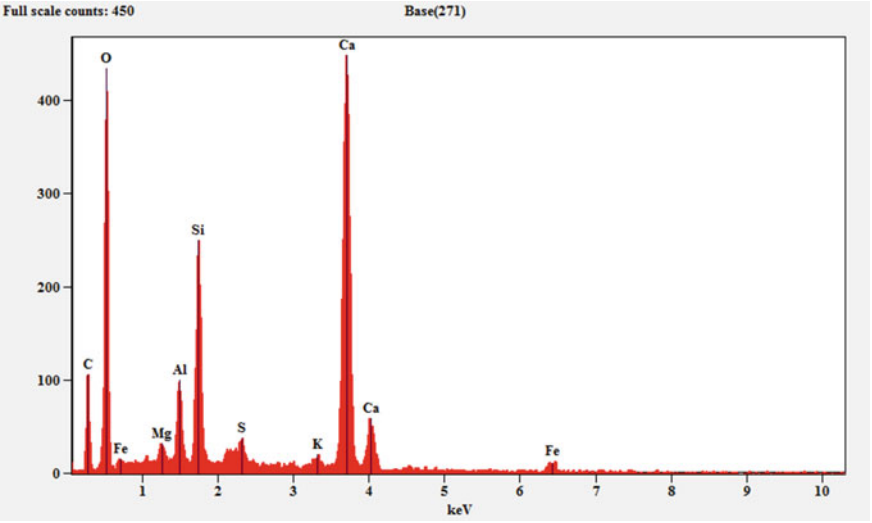

Fig. 6 Dispersion profile of cement obtained from EDS

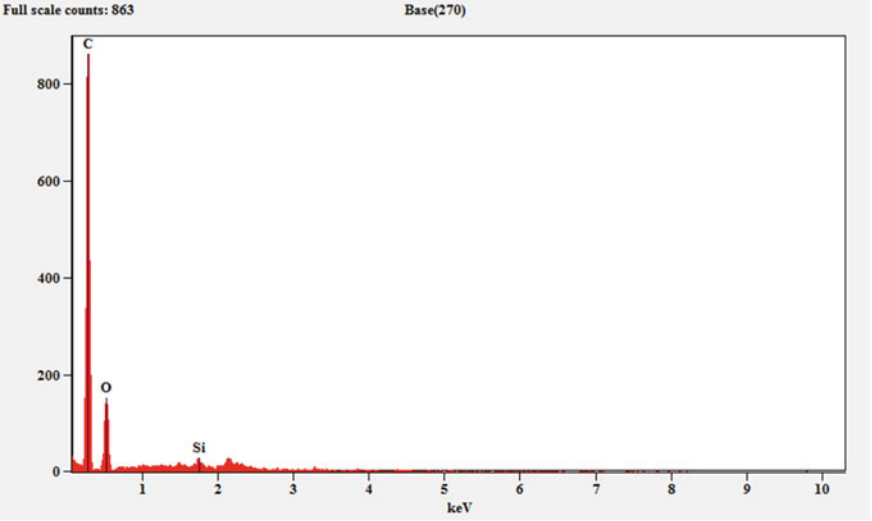

Fig. 7 Dispersion profile of vehicle exhaust obtained from EDS

4 Results and Discussion

Six test cases are formed to probe the performance of the PV panel under the influence of each of the five dust samples with similar levels of dust concentration and irradiation. Table 4 provides the details of the test cases considered. The I-V characteristics of the PV panel for each of the six test cases is presented from Figs. 9, 10, 11, 12, 13 and 14.

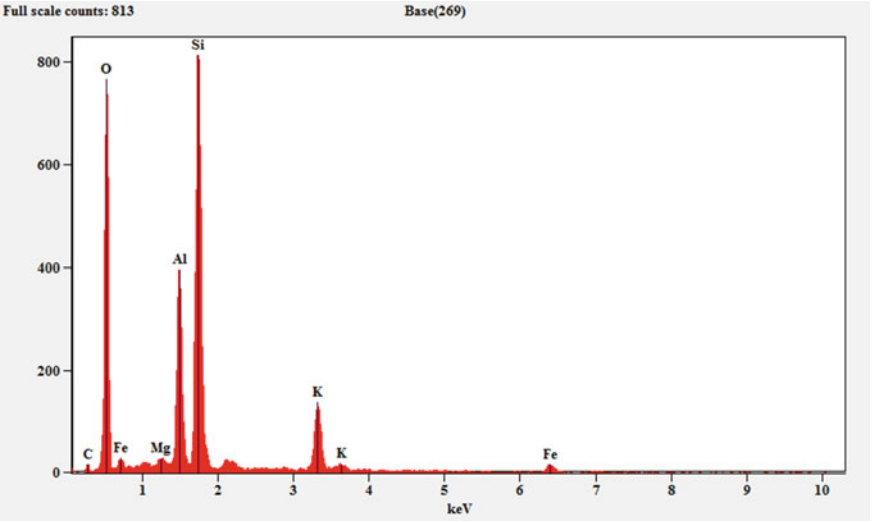

Fig. 8 Dispersion profile of sand obtained from EDS

Table 3 pH value of dust samples

Sample	pH
Sample-1	5.6
Sample-2	6.2
Sample-3	9.8
Sample-4	5.83
Sample-5	7

Table 4 Details of test cases

Test case	Type of dust	Dust concentration (g/m^2)	Mean irradiation (W/m^2)
1	Common soil	49	997
2	Red soil	49	997
3	Cement	49	997
4	Vehicle exhaust	49	997
5	Sand	48	997
6	Clean	–	997

The values of V_{oc}, I_{sc} and P_{max} for all the test cases are extracted from the respective I-V characteristics and are indicated in Table 5.

As per the performance data obtained in the laboratory for various test cases, it can be visualized that as a consequence of dust accumulation, the short circuit current

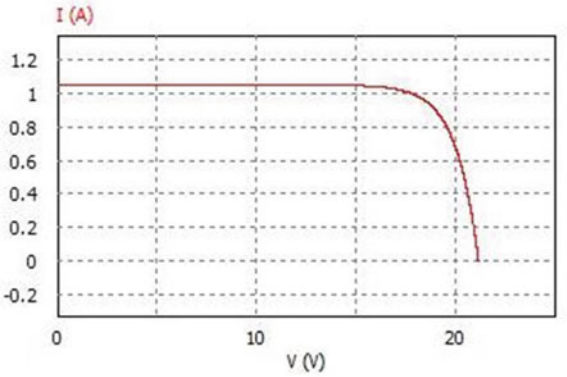

Fig. 9 I-V curve for test case-1

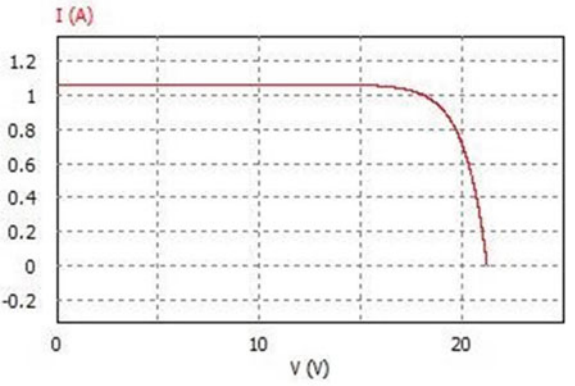

Fig. 10 I-V curve for test case-2

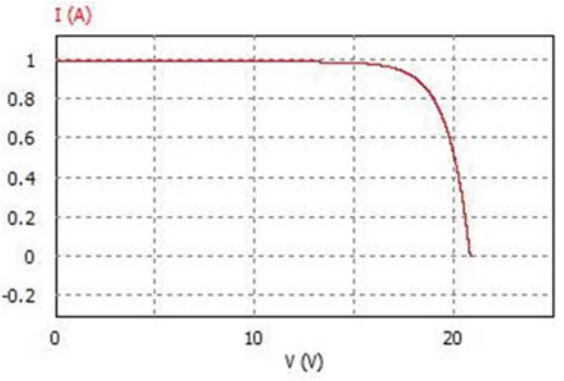

Fig. 11 I-V curve for test case-3

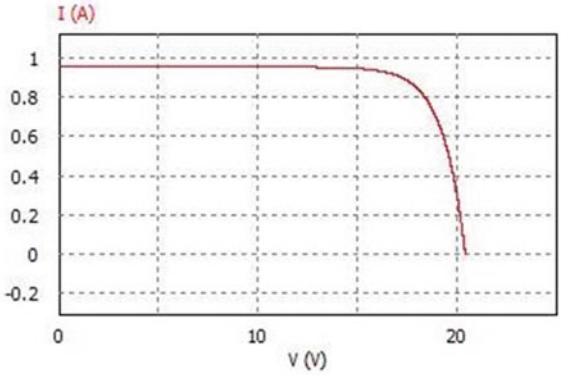

Fig. 12 I-V curve for test case-4

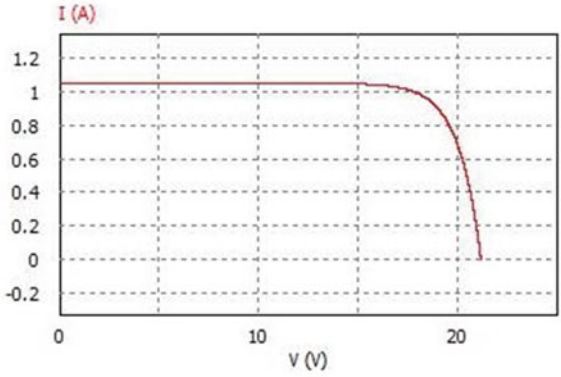

Fig. 13 I-V curve for test case-5

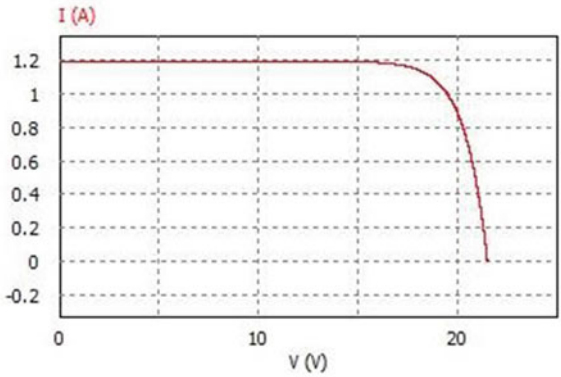

Fig. 14 I-V curve for test case-6

Table 5 Performance parameters of PV panel for different test cases

Test case	V_{oc} (in Volt)	I_{sc} (in Ampere)	Pmax (in Watt)
1	21.2544	1.0558	17.85
2	21.3408	1.0683	18.41
3	20.9304	0.9939	16.50
4	20.52	0.9591	15.55
5	21.276	1.0556	17.87
6	21.60	1.196	20.01

(I_{SC}) of the PV panel was significantly affected whereas the impact on the open circuit voltage (V_{OC}) is comparatively less. This in turn deteriorates the maximum power (P_{max}) that could be generated by the PV panel.

Percentage reduction (ΔP) is obtained for all the test cases by comparing the maximum power generated by the clean PV panel (as in test case-6) as in Eq. (1) and the same is plotted in Fig. 15.

$$\Delta \boldsymbol{P} = \frac{\boldsymbol{P}clean - \boldsymbol{P}sample\,(1\,to\,5)}{\boldsymbol{P}clean} \times 100 \tag{1}$$

As can be inferred from Fig. 15, the reduction in power generated by the PV panel is maximum under the influence of vehicle exhaust (22.28%) and least for common soil (7.99%) for a dust concentration of approximately 49 g/m^2, mean irradiation and mean temperature of 997 W/m^2 and 26 °C, respectively. The PV panel (encapsulant and outer covering) was also exposed to each of the five dust samples over a period of five months resulting in no deterioration whatsoever. The pH values presented in Table 3 also confirm that the dust samples do not pose a threat to the operational life of the PV panel.

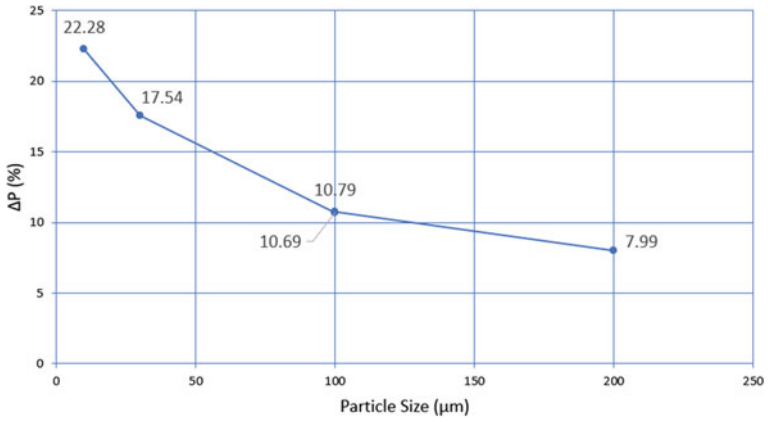

Fig. 15 Graph indicating percentage power reduction as a function of particle size

Table 6 Particle size and corresponding reduction in PV panel power

Particle size (μm)	ΔP (%)
10	22.28
30	17.54
100	10.79
100	10.69
200	7.99

By analyzing the data presented in Tables 2 and 5, it is evident that the deterioration in short circuit current and maximum power of the PV panel is dependent on the particle size of the dust samples. The particle having the least particle size, i.e., vehicle exhaust (sample-4) has the highest influence on the short circuit current (I_{SC}) and eventually on maximum power (P_{max}); whereas the dust sample having the highest particle size, i.e., common soil (sample-2) has the least impact on the short circuit current and maximum power of the PV panel. Table 6 relates the particle size and the corresponding percentage reduction in power. This is due to the fact that effective density of dust coverage increases with decrease in particle size. Or in other words, electrical mobility decreases with increase in effective density of the particles.

5 Conclusion

This laboratory investigation was conducted to study the impacts of the most commonly encountered dust particles when PV panels are deployed for operation. A test-bed was set up to analyze the change in solar PV power due to dust accumulation over the PV panel. Initially, the characterization of five dust samples, i.e., red soil, common soil, cement, vehicle exhaust, and sand, was undertaken to extract the mean particle size and chemical composition through scanning electron microscopy and electron dispersive spectroscopy, respectively. The data obtained from spectroscopy indicated that the pH levels of dust samples do not pose any threat to the operational life of PV panel. Later, the dust samples were uniformly spread across individually with a dust concentration of 49 g/m^2 (approx.) over the PV panel and corresponding I-V curves were plotted for six different test cases as indicated in Tables 4 and 5.

The extracted parameters revealed that power generated by the PV panel is a function of the particle size of the dust samples; the short circuit current, I_{SC} deviated a fair bit from the standard value. Power loss ΔP (%) due to all the dust samples (individually) was calculated which ranged from a drop of 7.99–22.28%. The dust sample with the least particle size (vehicle exhaust, 10 μm) had the most impact on I_{SC} which eventually led to the drop in PV output power. This is attributed to the fact that effective density increases with decrease in particle size. The study also suggests that different cleaning mechanisms are necessary for different dust samples to facilitate effective cleaning of PV panels. For instance, water should not be used

as a cleaning agent where cement particles are accumulated over PV panel because it results in formation of lumps which aggravates the loss in electrical power.

Further research points to standardization of dust types and particle sizes apart from other normalized or standard test conditions. These will help in better and more objective characterization of effect of dust deposition on PV panels. Further, the impact of dust on other types of PV modules (monocrystalline, amorphous, multijunction) needs to be considered.

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Design and Analysis of DC-DC Boost Converter

Bharat A. Gunhalkar, Sujata Kotabagi, Sandeep Ponkshe, Kotresh Basarikatti, and Govind Madhva

Abstract In this study, a DC/DC Boost (step-up) converter operating in Continuous Conduction Mode is designed and analyzed (CCM). The state space averaging technique is used to analyze both the open-loop and closed-loop analysis of the boost converters in order to calculate the transfer function. The step-up converter boosts the output voltage to 4.6 V from an input voltage range of *2.9–4.5 V*, and a maximum output current of *300 mA*. The Pulse Width Modulation (PWM) technique generates the closed-loop control signal for a fixed frequency of *1.7 MHz*. The complete system is modeled using *MATLAB & Simulink* and simulated in UMC 180 nm technology on *Cadence Virtuoso* platform.

Keywords DC/DC converter · PWM · CCM

1 Introduction

Modern electronic devices that mainly run on batteries, such as mobile phones, smartwatches, and laptops, make extensive use of DC-DC converters. Typical electronic devices contain several sub-circuits, each of which requires a different voltage level than the battery or an external source (higher or lower than the supply voltage). In addition, the voltage decreases when the stored energy of the batteries is exhausted. Rather than requiring a large number of batteries to do the job, boost converters boost voltage from a partially reduced battery voltage, saving space and cost.

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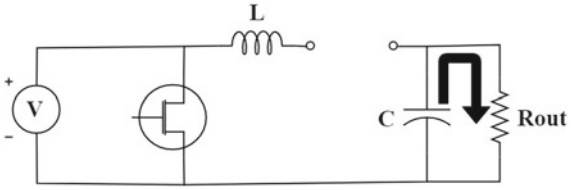


Fig. 1 Mode 1: switch is ON

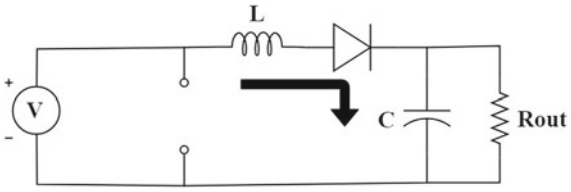


Fig. 2 Mode 2: switch is OFF

Boost converters are switched converters and are inherently non-linear systems. Classic linear control designs are often used to provide a consistent output voltage. Typically, PWM is used at a given frequency to achieve regulation [1]. There are two methods of realizing the boost converter: synchronous and non-synchronous. Synchronous rectification [3, 5, 9, 12] means that a transistor (usually a MOSFET) is used to control the current flow for minimal losses. Asynchronous rectification [4, 10] refers to using one or more passive diodes to control the flow of current. Figures 1 and 2 describe how the asynchronous boost converter works in Continuous Conduction Mode (CCM).

In mode 1, the diode is reverse biased (OFF) and the MOSFET is conducting (ON). As a result, the inductor begins to charge and the current flowing through it begins to linearly increase. At the start of the first cycle, the output voltage (voltage measured across the output capacitor) is *zero*.

In mode 2, the MOSFET is non-conductive (OFF) and the diode is now forward biased (ON). As a result, the output capacitor and load resistance start discharging the inductor current. The output voltage starts to increase until the following cycle starts. When the MOSFET starts conducting, the energy stored in the capacitor is converted into the load resistance, keeping the voltage almost constant.

Mathematical modeling of a circuit is essential to discuss its stability. The transfer function defines the whole system and the state space averaging technique [6–8] is used to derive the transfer function. The Right Half-Plane (RHP) zero of boost converters makes it difficult for the normally used Proportional-Integral (PI) controllers to perform well under load and line variations. For this reason, *Type Controllers* [11] are best suited. The primary goal of this work is to design a type-III boost converter controller and evaluate the closed-loop stability of the converter.

2 Design of Boost Converter

2.1 Relation Between Input and Output Voltage

Deriving the relationship between input and output voltage is the first step in designing the boost converter.

$$i_L = \frac{V_{\text{inp}} * T_{\text{ON}}}{L} + i_{\text{out}}$$

where i_L-Inductor current, V_{inp}-Input voltage, T_{ON}-Duration when MOSFET is ON, i_{out}-Output current and L-Inductance

$$V_D = V_{\text{out}} - V_{\text{inp}}$$

$$i_L = \frac{(V_{\text{out}} + V_D - V_{\text{in}}) * T_{\text{OFF}}}{L} + i_{\text{out}}$$

$$i_L - i_{\text{out}} = \Delta i = \frac{(V_{\text{out}} + V_D - V_{\text{in}}) * T_{\text{OFF}}}{L}$$

After equating (2) and (5), and solving:

$$V_{\text{out}} = \frac{V_{\text{inp}}}{1 - D} - V_D$$

where V_{out}-Output voltage and D-Duty cycle.

Writing (6) in terms of *duty cycle*:

$$D = 1 - \frac{V_{\text{inp}}}{V_{\text{out}} + V_D}$$

2.2 Inductor Design

Writing (2) in terms of *inductance (L)*, *duty cycle (D),* and *switching frequency (F)*:

$$L = \frac{V_{\text{inp}} * T_{\text{on}}}{\Delta i} * \frac{T}{T}$$

$$L = \frac{V_{\text{inp}} * D * T}{\Delta i}$$

$$L = \frac{V_{\text{inp}} * D}{F * \Delta i}$$

2.3 Capacitor Design

Consider the equation which describes the *charge* across the capacitor:

$$Q = C * V_{\text{out}}$$

$$\frac{\partial Q}{\partial t} = C * \frac{\partial V_{\text{out}}}{\partial t}$$

$$i_{\text{out}} = C * \Delta V_{\text{out}}$$

where ΔV_{out}-Output voltage ripple.

Now, writing (13) in terms of *capacitance (C)*, *duty cycle (D),* and *switching frequency (F)*:

$$C = \frac{i_{\text{out}} * D}{\Delta V_{\text{out}} * F}$$

2.4 Switch Design

The switch in the boost converter is implemented with a MOSFET. The standard *current* equation for an *N-channel* MOSFET in the *triode or linear* region (*ignoring the lambda effects*) is given below:

$$I_D = \mu_n * C_{OX} * \frac{W}{L} * \left[(V_{GS} - V_{TH}) V_{DS} - \frac{{V_{DS}}^2}{2} \right]$$

Differentiating Eq. (15) with respect to V_{GS}:

$$\frac{\partial I_D}{\partial V_{GS}} = \mu_n * C_{OX} * \frac{W}{L} * V_{DS}$$

$$\frac{\partial I_D}{\partial V_{GS}} = gm = \frac{1}{r_{DS(\mathrm{ON})}}$$

$$r_{DS(\mathrm{ON})} = \frac{1}{\mu_n * C_{OX} * \frac{W}{L} * V_{DS}}$$

Now, this can be written as

$$\frac{W}{L} = \frac{1}{\mu_n * C_{OX} * r_{DS(\mathrm{ON})} * V_{DS}}$$

2.5 Component Design

The design specifications are as shown in Table 1.

Components such as *Duty Cycle (D)*, *Inductance (L)*, *Capacitance (C),* and *Switch aspect ratio (W/L)* are calculated using Eqs. (7), (10), (14), and (19) and are shown in Table 2.

Table 1 Design specification

Design variable	Description	Value	Unit
V_{inp}	Input voltage	2.9–4.5	V
V_{typ}	Typical input voltage	3.7	V
V_{out}	Output voltage	4.6	V
$i_{\mathrm{out}}(MAX)$	Maximum output current	300	mA
F	Switching frequency	1.7	MHz
$r_{DS(\mathrm{ON})}$	Switch on-resistance	200	mΩ

Table 2 Designed component values

Component	Description	Value	Unit
D	Duty cycle	0.3018	–
L	Inductance	5.099	μH
C	Capacitance	2.315	μF
$\frac{W}{L}$	Switch aspect ratio	3200	–

3 Analysis in Open Loop

The frequency analysis of any circuit starts with the derivation of its *transfer function.* The state space averaging model is used to determine the transfer function of the open-loop boost converter. With the *state space averaging* approach [2] one obtains a comprehensive converter model with stationary and dynamic variables.

From Fig. 3, the *states* and *variables* are defined as

$$x = [\, i_L \; v_C \,]$$

$$u = [V_{\text{inp}}]$$

The *state equations* can be written for Fig. 1 as

$$i_L = \frac{1}{L}\int v_L \mathrm{d}t = \frac{1}{L}\int vg \mathrm{d}t$$

$$i_L = \frac{1}{L}\int v_L \mathrm{d}t = \frac{1}{L}\int vg \mathrm{d}t$$

$$v_C = \frac{1}{C}\int \frac{v_C}{R_L} \mathrm{d}t$$

$$\frac{\partial v_C}{\partial t} = \frac{-v_C}{R_L * C}$$

Now applying the standard *state space model* equations, we get

$$\dot{x} = Ax + Bu$$

$$y = Cx + Du$$

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_L * C} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} i_L \\ 0 \end{bmatrix} [vg] + \begin{bmatrix} 0 \\ \frac{-1}{C} \end{bmatrix} [iz]$$

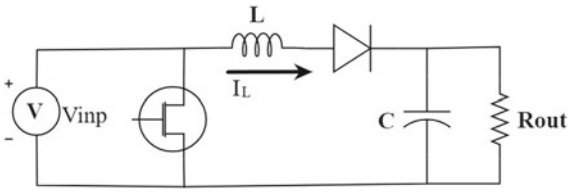


Fig. 3 Asynchronous boost converter

$$\begin{bmatrix} V_{\text{out}} \\ ig \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix}$$

$$A_1 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{R_L * C} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{i_L} & 0 \\ 0 & \frac{-1}{C} \end{bmatrix}, C_1 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

Similarly, for Fig. 2, the equations are

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_C} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{R_L * C} \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix} + \begin{bmatrix} i_L \\ 0 \end{bmatrix} [vg] + \begin{bmatrix} 0 \\ \frac{-1}{C} \end{bmatrix} [iz]$$

$$\begin{bmatrix} V_{\text{out}} \\ ig \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_C \end{bmatrix}$$

$$A_2 = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{R_L * C} \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{i_L} & 0 \\ 0 & \frac{-1}{C} \end{bmatrix}, C_2 = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

Employing the averaging technique

$$A = A_1 d + A_2 (1 - d)$$

$$B = B_1 d + B_2 (1 - d)$$

$$C = C_1 d + C_2 (1 - d)$$

$$D = D_1 d + D_2 (1 - d)$$

$$A = \begin{bmatrix} 0 & \frac{-1}{L} * (1 - d) \\ \frac{1}{C} * (1 - d) & \frac{-1}{R_L * C} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{1}{i_L} & 0 & V_C \\ 0 & \frac{-1}{C} & \frac{-i_L}{C} \end{bmatrix}, C = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, D = [0]$$

Taking *small-signal* equation from:

$$\dot{\hat{x}} = A\hat{x} + B\hat{u}$$

$$\begin{bmatrix} \dot{\widehat{i_L}} \\ \dot{\widehat{v_C}} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} * (1 - d) \\ \frac{1}{C} * (1 - d) & \frac{-1}{R_L * C} \end{bmatrix} \begin{bmatrix} \widehat{i_L} \\ \widehat{v_C} \end{bmatrix} + \begin{bmatrix} \frac{1}{i_L} & 0 & v_C \\ 0 & \frac{-1}{C} & \frac{-i_L}{C} \end{bmatrix} \begin{bmatrix} \widehat{vg} \\ \widehat{iz} \\ \widehat{d} \end{bmatrix}$$

Thus, the *transfer function* can be calculated using

$$\frac{Y(s)}{U(s)} = \left[C(sI - A)^{-1} * B\right]^{-1}$$

So, the *transfer function* $\begin{bmatrix} \widehat{V_{\text{out}}} \\ \hat{d} \end{bmatrix}$ is

$$\begin{bmatrix} \frac{\hat{}}{V_{\text{out}}} \\ \frac{\hat{}}{d} \end{bmatrix} = \frac{-I_L\left(s - \frac{V_C(1-D)}{I_L L}\right)}{C\left(s^2 + s\left(\frac{1}{R_L C}\right) + \frac{(1-D)^2}{LC}\right)}$$

Stability analysis in *MATLAB* shows the following Bode Plots (Figs. 4 and 5).

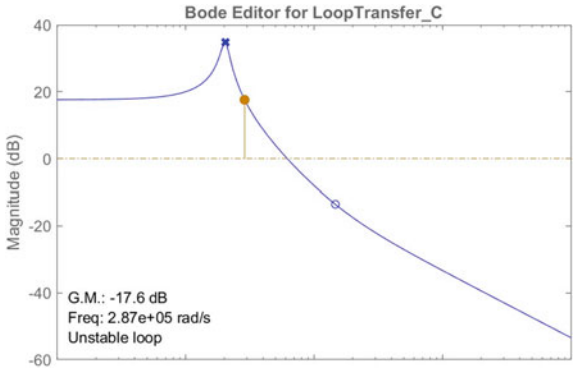


Fig. 4 Magnitude spectrum

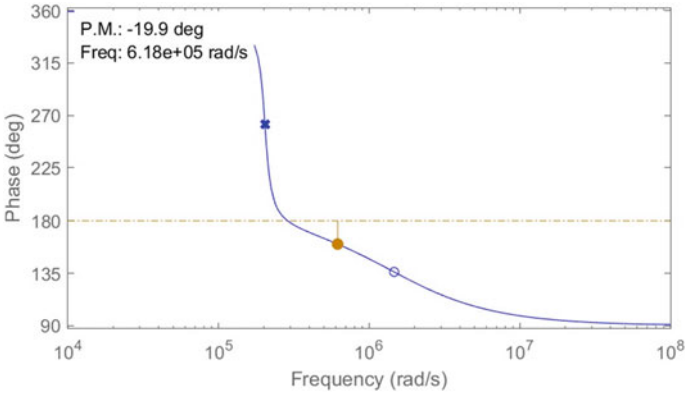


Fig. 5 Phase spectrum

4 Design and Analysis of Controllers

4.1 Need for Compensation

The controller design is critical in regulating and maintaining the performance of a power supply. The controller, which consists of a combination of poles and zeros, produces the traditional loop form and guarantees the stability of the converter by modifying the gain and phase properties of the open-loop frequency response.

4.2 Type-III Compensator

When more than 90° of phase boost is required, the Type-III compensator is used. The Type-III compensator can potentially increase the phase up to 180° by adding another pole/zero pair to the Type-II compensator. With this compensation method, the type-II compensator receives an additional RC branch. At low frequencies, there is an integrator followed by a pair of zeros. After that, the compensator enters a zone where the gain increases with frequency and the phase is positive. The compensator serves as a differentiator (Fig. 6).

Type-II compensators are often used in power converter control loops. While the maximum phase of a type-II compensator at any frequency is at most zero degrees, the phase lag of a power converter can approach 180° in some situations. As a result, in some cases, a type-III compensator is required because a type-II compensator is incapable of providing enough phase buffer to keep the loop stable. A type-III compensator must have a phase plot that rises above zero degrees at specific frequencies in order to maintain a respectable phase margin. Due to the *double pole and RHP zero* in the boost converter, a *Type-III* compensator is needed to make the circuit stable.

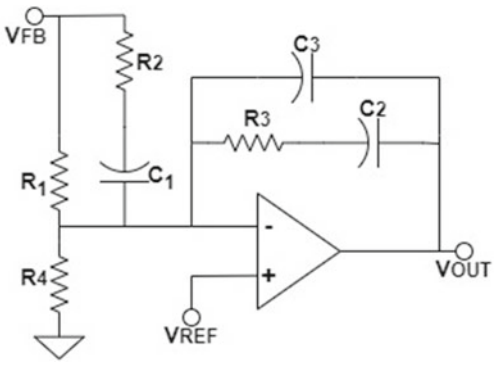


Fig. 6 Type-III compensator

Table 3 Components values

Component	Value	Unit
R_1	340	kΩ
R_2	40	kΩ
R_3	50	kΩ
R_4	120	kΩ
C_1	12	pF
C_2	150	pF
C_3	2	pF

4.3 Type-III Compensator Design

The transfer function for the *Type-III compensator* from Fig. 8 is

$$\frac{V_{\text{OUT}}}{V_{FB}} = \frac{-1 * (R_3C_2s + 1)(C_1(R_2 + R_1)s + 1)}{R_1(C_2 + C_3)s(R_2C_1s + 1)\left(\frac{C_2C_3}{C_2+C_3}R_3s + 1\right)}$$

The component values can be determined from zero/pole values p_1, p_2, and z_1, z_2 (in rad/s) by comparing the coefficients of (45) and the standard pole-zero transfer function as follows:

$$R_1 = r_1,\ R_2 = \frac{R_1z_2}{z_2 - p_1},\ R_3 = \frac{R_1p_2K}{z_1(z_1 - p_2)}$$

$$C1 = \frac{z_2 - p_1}{R_1z_2p_1},\ C2 = \frac{z_1 - p_2}{R_1p_2K},\ C3 = \frac{z_1}{R_1p_2K}$$

Thus, the component values are as follows.
The Bode Plot for the transfer function in (45) is (Table 3; Fig. 7).

5 Simulation

The designed boost converter and the Type-III compensator are integrated and modeled in *Simulink* in Fig. 8.

The designed circuit is also simulated in UMC 180 nm technology on *Cadence Virtuoso* platform. Figure 9 shows the schematic of the boost converter.

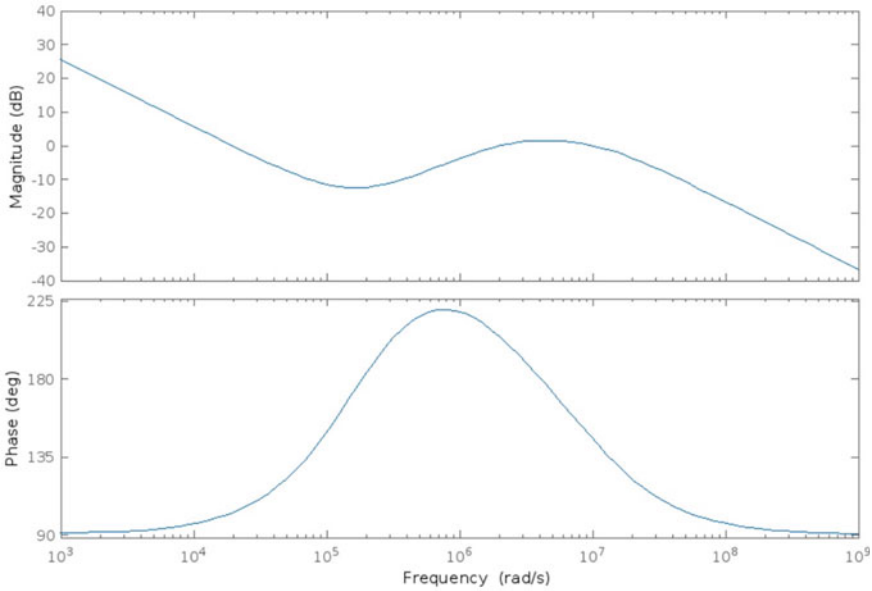


Fig. 7 Magnitude and phase spectrum

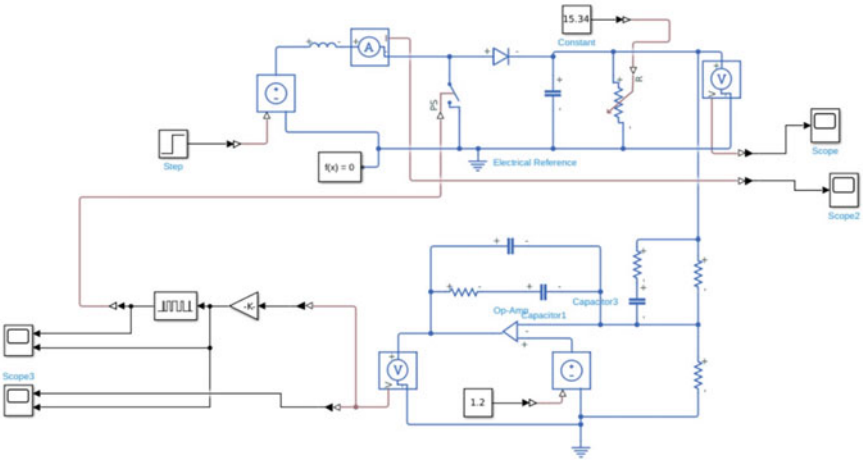


Fig. 8 Simulink model of the system

6 Result

The circuit is simulated in both the time domain and the frequency domain. The Bode Plot describing the stability of the whole system is (Figs. 10 and 11).

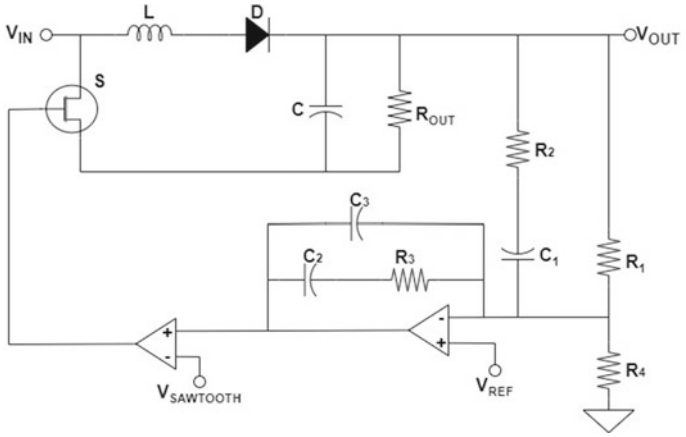
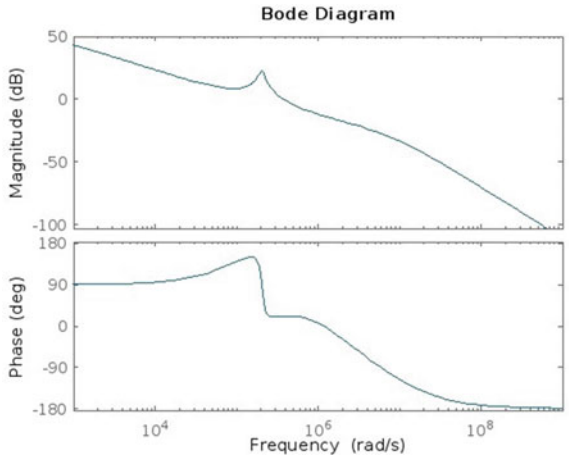


Fig. 9 Complete system implementation

Fig. 10 Magnitude and phase spectrum



The result is confirmed by the results of *ADEL (Advance Design and Simulation Environment)* after running the schematic with a transient analysis with a stop time of *1 ms* (Fig. 12).

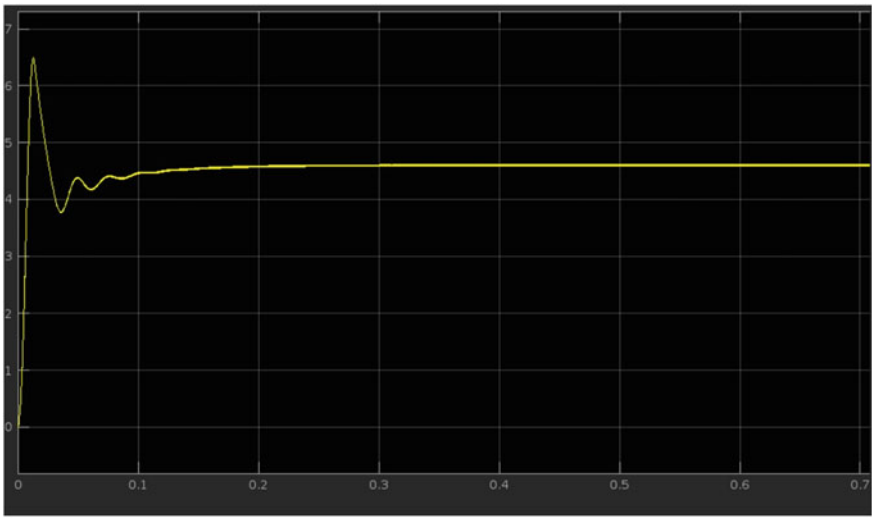


Fig. 11 MATLAB: V_{OUT} (*in V*) versus time (*in s*)

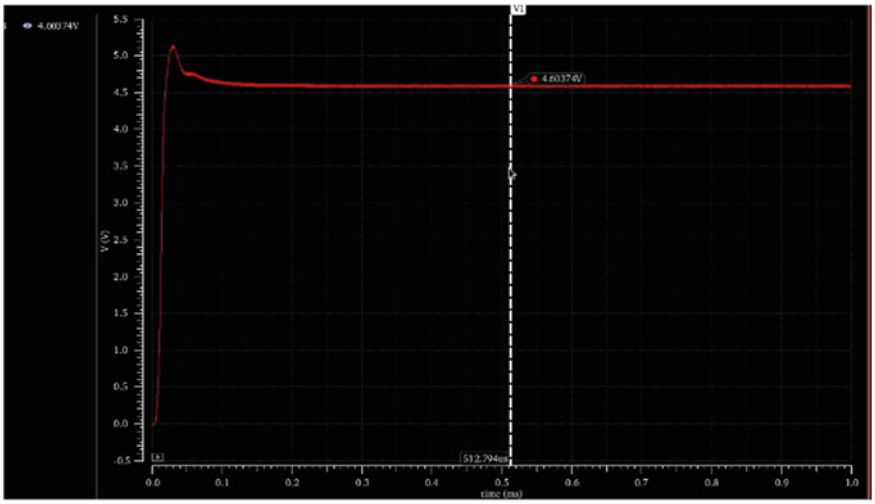


Fig. 12 Cadence: V_{OUT} (*in V*) versus time (*in s*)

7 Conclusion

The boost converter is designed for the given specifications. Type III compensator compensates the convertor to achieve the regulated output of 4.57 V for the maximum load current of 300 mA. The entire system is simulated both in MATLAB and Simulink and Cadence Virtuoso. Cadence results validate the results from MATLAB.

Table 4 Comparison between *expected* and *actual* values

Parameter	Expected value	Actual value
Output voltage (V)	4.6	4.57
Load current (mA)	300	296.66
Switching frequency (MHz)	1.7	1.7001

An overview of the specification and the designed converter results are shown in Table 4.

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Energy Management Analysis on Smart Street Lighting for Smart Cities

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Abstract The Smart cities with Information and Communication Technology (ICT) have made our lives simple, efficient, effective, and reliable. With the support of different technologies, the development of Smart Cities reached to the highest level by enabling cloud applications. In the case of smart street lighting, the primary objective of energy management in Smart Cities is to reduce power consumption, maintenance costs, and self-designed inbuilt energy meter for analysis. In this paper, the features of a Centralized Control Monitoring Systems (CCMS) system for LED street lighting, maintenance, and forecasting analysis of power consumption using a power saving strategy with real-time data are proposed for the development of Smart Cities.

Keywords Smart cities · Energy management · Street lighting · Information and communication technology

1 Introduction

Most of the smart cities are associated with a huge number of software applications and network devices that interlinks to the physical and social space, these applications are ranging in many activity fields like Health care, Agriculture, Home, Infrastructure, city services, Mobility etc. The interoperability of various entities or devices work together to solve the problems collaboratively and through policy-based agreements. There are numerous challenges involved in the smart cities like growth, safety, and sustainability. These challenges are to be achieved with the distributed systems through knowledge institutions with authenticated communication networks [1, 2].

The building blocks of ICT with emerging technologies are very much essential for the growth of smart cities in reference to the energy management. Street lighting is a basic essential to ensure safety in urban areas and enhance the quality

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of life. In a country like India, installation of street lighting in rural and remote villages has always played a key role in the development and improvisation of the country, decreasing the crime rates and increasing the mobility. Street lighting plays a crucial role in improving the safety of pedestrians, drivers, and riders. However, the brightness required at different times of night is different and employing a system to manage the same can result in energy savings and provide cost benefits to municipalities and corporations. For instance, the brightness required during midnight is less compared to that required during the evening. The duration of the day and night varies with season, due to which although the time of switching on remains the same, the intensity has to increase gradually and not drastically. In metropolitan cities, with an increase in pollution, visibility during the early dawn may decrease on the roads and highways, which requires more intensity of lights for better vision and decreased accidents. There are other numerous factors which require modulation of the brightness depending upon the time. The LED automated street light management system controls brightness or intensity of the light at different times of the night without any manual intervention. Statistics show that street lighting, including maintenance represents about 40% of the total expenditure of a community.

The economical growth and opportunities are found in the development of smart cities through the ICT tools and Industry 4.0 technologies [3, 4]. However, there are huge opportunities and challenges are found in the growth of sustainable development and urbanization, shown in Fig. 1. Some of the challenges on the components of Smart cities are:

(1) Connectivity and configuration of various devices and its applications.
(2) Data analytics, prediction strategies, forecasting, development, and deployment of AI-based algorithms.

Fig. 1 Components of smart city

Smart Homes: Huge number of applications is found in smart homes like security, care for elderly people, fire protection, water supply, energy saving, communication networks in case of emergency, waste management, and ease of access for societal needs.

Smart Industry: Industrial automation found in a new shape with the revolutionary developments of Industry 4.0 technologies, such as applications based on Artificial Intelligence algorithms, cloud computing, Machine-2-Machine, Industrial IoTs, cyber security, etc. These technologies are much required for the growth of the Smart industry in terms of energy saving methods, ease of transportation system for dispatching the goods, fire safety, health care system in emergencies, and administration systems.

Smart Infrastructure: The challenges of smart infrastructure involves strong monitoring and maintenance system for roads, bridges, traffic systems, drainage and garbage systems, smart energy with EV charging stations.

Smart Transportation: Smart transportation with smart vehicles has many challenges in parking management, parking slots, traffic signaling systems for smooth flow of vehicles to avoid congestion, navigational and GPS technologies on roads like closed-circuit television systems (CCTVS). This can lead to improvements in safety, network management, traffic congestion, environmental performance, accessibility, convenience, and public perception.

Smart Health Systems: The IoT-based health systems are suitable in collection of data over time, enabling preventive care of the patients and also, understand the type of therapy on the patient [5–7]. The wireless IoT has several advantages:

(1) It gives better understanding of the patient health status rather than attending patients to health care.
(2) The sensed data can be analyzed with smart algorithms, thus reduces the latency and costs.
(3) The sensed data can be shared to health professionals for better recommendations to the patients.

There are certain challenges are found in health care system

(1) Continuous monitoring the data from routers or gateways.
(2) Storing the data in cloud service providers.
(3) Development of smart algorithms for various patients.

2 Centralized Control Monitoring Systems (CCMS)

The CCMS is an advanced smart lighting control solutions for LED street lighting in the smart cities than in co-operates the ICT technologies. The main objective of CCMS to make the LED lighting system more reliable, efficient and flexible configuration, also, each CCMS access the data from 15 to 18 street lamps. The system access the data with Radio Frequency-based technology which is transmitted the clod through GPS/GPRS. The data is analyzed with web enabled system for

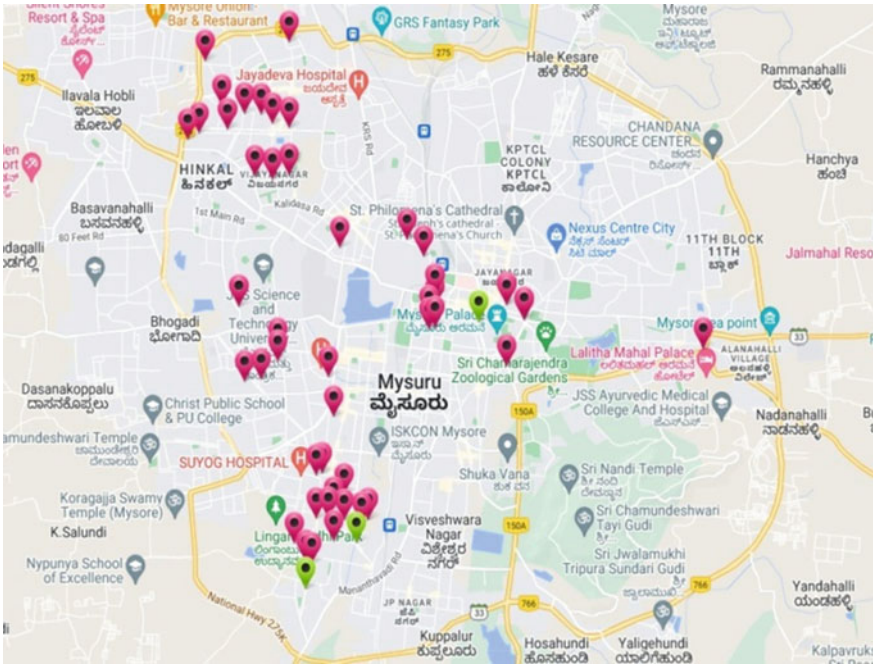

Fig. 2 Geographical location of CCMS in smart city

remote monitoring and controls the street lighting with auto ON/OFF based on the geographic location shown in Fig. 2 and almost 70% of energy is used over the conventional street lighting systems. The scheduling of the street lights at different times, controlling the intensity of street lights based on sunrise/sunset, and monitoring the faults are achieved through this CCMS.

The data can be fetched from the CCMS wireless system and can be accessed in the data centers through a cloud server for forecasting and scheduling the lights based on sun set/rise. CCMS features and technical specifications:

Specification single/three phase	12 A/24 A/32 A
Rated input voltage	240 V and 415 AC, 50 Hz
KVA rating	3 KVA/9 KVA
Current rating	12 A/24 A/32 A (single and three Ph)
Connection	Single phase 2 wire/4 wire
Remote connection	GSM/GPRS web enable
Energy saving mode	3 Modes
Mounting	Pole/foot mounted
Ingress protection	IP55
Operating temperature	−10 to +55 C

(continued)

(continued)

Dimension L × W × H	345 × 410 × 880 mm
Protection	MCB for short circuit and overload

2.1 *Network Architectures and Communication Protocol for the CCMS*

The network structures are used for transmitting the information to a sensor node before sharing to the cloud which are connected through the Internet Home Area Network/Wide Area Network/Field Area Network or Neighborhood Area Network (HAN/WAN/FAN (or) NAN) are three types of network services used for smart cities [8, 9]. The HANs are Service oriented Architecture (SoA), not associated with any software language and useful for short-range network.

HAN architectures	FAN/NAN	WAN
Not associated with system software language	Not associated with system software language	Not associated with system software language
Used for short range network	Used for medium ranges	Used for larger ranges
Smart homes and LED street lighting	Cellular services and on wired connection using fibre optics	Smart grid application

There several network protocols are available for various smart city applications and enable remote control of devices and systems. Some of the network protocols used for smart city application is RFID, NFC, Bluetooth, Zigbee, Z-wave, Wi-Fi, LoraWAN, and 6LOWPAN. The CCMS uses low cost Z-wave protocol for serving the data access from LED street lighting and makes simple implementation [10, 11].

The data collected from each CCMS is further shared to the cloud for monitoring, forecasting, and power saving analysis. The parameters listed below are obtained from each street light and saved into a.csv file. The data collected from CCMS is further shared with the cloud for maintaining, forecasting, and power saving analysis. Each CCMS provides device ID, voltage, current, power factor, THD (V, I), over voltage, under voltage, fault information, and time stamp for every 15 min. The time stamp can be varied as per our convenience from 5 min to 1 h. This CCMS is networked with a cloud server to store the above-mentioned parameters for data analytics. The information collected is represented in the dashboard by the data center which is shown in figure.

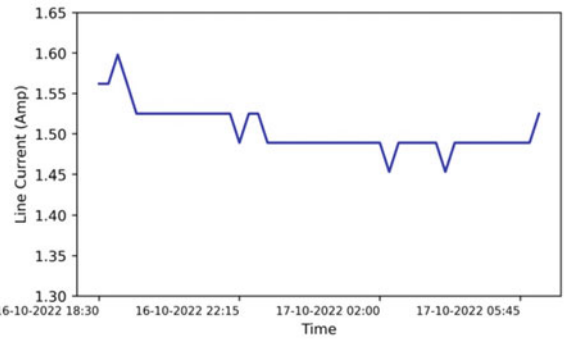

Fig. 3 Line current of street lighting (amp)

2.2 Power Saving Strategy

Introducing CCMS-based smart panel with smart group controller. Wired connection between street lights and smart panels is given in three different phases, namely, R, Y, and B. As per our calculation there are 18 Streetlights that are connected to one CCMS unit. This can be divided into 3 groups as 6 Streetlights in a group. Either of one out of 3 phases is connected to 2 Streetlights, i.e., there are 2-R phase, 2-Y phase, and 2-B phase Streetlights from each group are turned on alternatively with one common neutral. Whenever the fault occurs fault signal is generated automatically and will notify the concerned person on the system. On this way problem is getting auto-identified. In the night after the fixed time any one phase out of three will be turned off to save the energy. Day wise rotation of these staggering phases also can be done.

The survey report is conducted for Zone-2, Ward-63 of Mysuru region with a longitude 76.63461. In this area it is found that 1,197 street lights are connected and consume 1, 74,290 Watts, the line current waveform as shown in Fig. 3. For better illumination, visibility and power saving various types of street lights like LED and SVL. Are connected to 65 switching points for monitoring and controlling. However, each CCMS access data from 18 streets light and networked with data center via cloud. A CCMS device that can upload this data to the Internet, and operate the lights at the same time, will help the supervisors immensely. A connection backbone of wireless technologies like Wi-Fi, GSM (2G/3G) are the most cost-effective solution for data sharing between the devices and control center for controlling and monitoring as shown in Fig. 4.

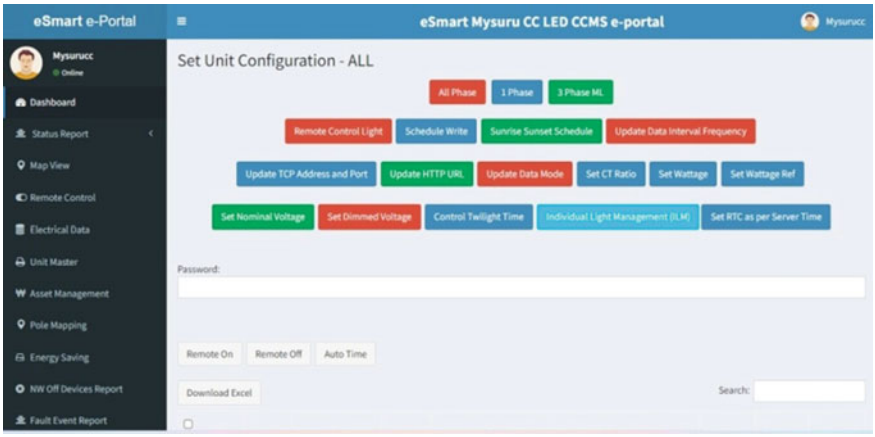

Fig. 4 Dashboard parameters

3 Conclusion

Energy solutions on street lighting enhance the energy management and forecasting analysis, thus reducing the cost of energy and increase the life span of the equipment. Around 30% of the energy is saved through power saving strategies either with On/Off or dimming the lights based on the traffic flow. The energy management forecasting analysis is presented using real-time data of the street lighting of Mysuru city, Karnataka, India.

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Design and Development of Efficient Feeding Network Structure for Patch Antenna Array Modules in UAV Communication Applications

Chandravijay Bharati, R. Prasanna, and E. Balasubramanian

Abstract This article focused on the development of microstrip patch antenna with linear and planar array distribution structures. Ansoft HFSS electromagnetic simulation software was used to analyze the radiation and reflection parameter of the designed element. Initially, single element antenna was realized and further 1 × 2, 2 × 2, and 1 × 4 array structures were analyzed with a due consideration of two different substrate materials such as Duroid-5880 and FR-4. 1 × 4 array antenna with Duroid-5880 offers highest gain of 14.12 dB. To validate the design concept, 1 × 2 array antenna was fabricated. S_{11} parameter was measured using a vector network analyzer and it has downward frequency shift by 54.5 MHz as compared to simulated results. The radiation characteristic of the antenna was measured on anechoic chamber, and the *E*/*H* plot reveals that antenna is unidirectional. Measured gain is enhanced by 7.82 dB as compared to simulated results.

Keywords Microstrip · Array antennas · High gain · Duroid substrate · UAV

1 Introduction

Microstrip antennas are the commonly used conventional antennas for fixed and flexible structures. They are widely used for body mounted applications over the rigid and flexible structures depending on the substrates [1]. Even though there are

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several disadvantages such as lower band width and frequency deviation and several other material-based disturbances still they play a major role in space and terrestrial applications [2]. It was achieved by deviating the thickness of the radiating structures and also by the thickness of the substrate materials. Due to these changes, they play major change in the resonance values and gain parameters [3]. The effect of ground plane is a major part in the antenna design where the full and defected ground planes are important in fixing the frequency resonance [4]. Including the defected ground plane or slots in the radiating structures and also the ground plane will improve the antenna parameters [5]. However, the ground plane and the radiating structures have to be in proper ratio because of which the antenna pattern will be effective. The truncation of the antenna patch sides will help in improving the antenna bandwidth [6]. The material and the pattern used in the design are responsible for directivity [7]. The edge cutting of the antenna material along the axis will help in improving the directivity and also the axial ratio of the antenna [8]. The edge truncation of the antenna will make the change of the impedance or stub matching value of the antenna [9]. Recent printed antenna structures are more convenient such as material occupancy and multi-layer printing of materials [10]. It can improve the antenna gain and return loss. Axial ratio of the antenna is also related to the multi-layer printing [11] gain of the antenna. It can be altered by changing the dimensions of the antenna. The fixed airgap [12] in the printed layers of the antenna increases the bandwidth of the antenna [13, 14] and it can be done both in patch as well as in substrates. Many literatures are available based on the stacking of patch antenna and some of them are discussed here. The antenna with array structure with four layers of 0.77 mm each and patch based on copper material presented in [15] achieves high peak gain. The circular polarization was achieved due to the truncation of corners of the patch. The dual frequency patch with the copper material and substrate thickness 3 mm and permittivity of 2.2 in [16] provided a broad bandwidth in the lower and upper band. The square patch with air gap of 12 mm and substrate thickness of 1.5 mm provides gain improvement with parasitic patch [17]. A double layer stack with a total thickness of 4.8 mm with inset feeding for gain improvement is presented in [18].

The polarization in the successive layers can be changed using multiple feeding [19] and a higher dielectric constant substrate can be used for controlling the radiating structure [11]. A second frequency resonance due to the parasitic stacked patches was introduced in [20] which are helpful to design dual band antennas with low profile. The air-filled stacks were suitable for increasing the bandwidth [21]. With stacking, the gain was improved from 9.42 to 10.30 dB gain and directivity was increased from 9.56 to 10.48 dBi [22]. In [23], the novelty of frequency reconfigurable stacked antenna with well controlled unidirectional polarization was proved. Enhancement in the bandwidth due to the parasitic patches over the antenna element and increase in the S_{11} Parameter were shown in [24]. Stacking of linearly polarized antennas produce circular polarization when alternate stack patches were rotated in a particular fashion with respect to the aperture [25]. The stacking of antenna with the ferrite-based material is given in [26]. Enhancement in the impedance and axial ratio bandwidth with a single feed was achieved by parasitic stacked patches parallel to the main

radiating patch [27]. Multi-layer stack array over Duroid substrate was proposed in [28] where the lower patch was matched directly to the feeding and the upper patch was proximity coupled with the lower feeding network. This structural arrangement of patches improves the gain by approximately 5 dB than the structure without stacking.

Kuar et al. identified that, the gain and bandwidth was improved by altering the thickness of the radiating structure and ground plane. This is also possible by including slots [29]. Ndujiuba et al. inferred that the ground plane in the patch antenna structures provided polarization. Decrease in the ground plane will reduce the polarization and directivity [30]. Nguyen et al. suggested that, the ground plane optimization leads to the impedance matching frequency resonance [31]. Salleh et al. observed that the reduction of the ground plane reduces the material occupancy and also reduces the antenna gain [32]. Kurniawan et al. inferred that, the ground plane truncation and optimization of the ground plane will change the antenna parameters [33]. Sacharias et al. suggested that the truncation leads to improve the antenna parameters such as gain and bandwidth [34]. Kurniawan et al. identified that polarization changes with the truncation of the antenna edges and also by changing the antenna dimensions [35]. Sekra et al. suggested that the stub matching can be controlled by edge truncation [36]. Torrisi et al. discussed that an alternate material can give good electrical and antenna properties than the copper material [37]. Pan et al. suggested that using the spray method, the conventional copper can be replaced and the desired antenna value can be achieved [38]. Shaik et al. explained the relation between the multi-layer and antenna parameters [39]. Chae et al. discussed that gain can be controlled by changing the dimension and aperture value of the antenna [40]. Kortright et al. proposed that stacking and airgap of the antenna are related to each other and they can be modified [41].

2 Design and Analysis of Microstrip Array Antenna

The antenna single patch was designed by using the conventional design approach. The desired antenna frequency and the bandwidth were achieved by altering the dimensions and the height of the antenna. The array design was obtained by building the combination structure of the desired array number and by altering the dimensions.

2.1 Single Element Antenna Design on Duroid-5880 and FR4

In the undertaken investigations, the single element antenna operating in S-band was considered. The microstrip antenna has a three layered structure, namely, a radiant piece, a dielectric substrate, and a ground plane from top to bottom. Excitation method

that has been employed to feed the radiating element was the microstrip feed line with inset feeding method.

The length of the fundamental patch was calculated using the following relation

$$fr = \frac{c}{2L\sqrt{\in_r}} \tag{1}$$

where

c speed of light
fr resonance frequency
L length of the radiating patch
ε_R dielectric constant

In order to get the optimized radiation, there should be proper impedance matching between the feed line and radiating element. In general, the inset feed technique provides low loss. Initially, the feed line and inset width were evaluated for impedance matching. The return loss of the antenna is the ratio of the power sent to the tx line and the amount of power it radiates out. With the minimum return loss maximum match was achieved. With S_{11} <−10 dB criteria, bandwidth range of the antenna was calculated. In general, the VSWR of the antenna has to be 1–2. The simulation analysis obtained VSWR as 1.02, which is much closer to the ideal value. In addition, the Duroid-5880 based antenna provided 6.96 dB of gain, while FR4 based antenna achieved 2 dB as it is having a high dielectric constant. However, wireless communication requires high directivity and gain for overcoming attenuation and increasing communication distance. The efficiency of the antenna is the multiplication of the directivity and antenna gain. When the gain is fixed and the directivity increases, the efficiency will be increasing. It should be between 70 and 90% in practical parameters. The performance of the Duroid and FR4 based antenna is given in Table 1 which shows that the Duroid material is providing comparatively good results in terms of the antenna parameters. The bandwidth is comparatively good in FR4 than the Duroid substrate performance.

Table 1 Performance comparison between Duroid and FR-4 based patch antenna

Parameters	Duroid-5880	FR-4
RL (dB)	−54.00	−52.16
VSWR	1.02	1.01
Gain (dB)	6.96	2.00
RE (%)	98.00	43.00
BW (MHz)	29.00	55.00

2.2 Design of 1 × 2 Square Patch Linear Array Antenna with Duroid-5880 and FR4

In order to extend the design to an array configuration, two single elements structure were added with the united ground plane, which forms a 1 × 2 linear array antenna as shown in Fig. 1. In the array, both the patches were added through the microstrip line. The separation distance between radiants has been evaluated that improved the radiation characteristics.

The feeding structure will divide the power and the phase into number of branches. The antenna patches which are connected to the feeding structure will radiate the power out as the polarization structure. The power dissipating from the antenna feeding structure should be uniform and then it will form the proper polarization with maximum gain.

After many iterations, an optimal dimension of ground, patch, substrate, and feed network were obtained which is given in Table 1 for both Duroid and FR4. Also, the antenna characteristics are presented in Table 2.

All the antenna structures of this Sect. 2 have obtained the return loss of less than −40 dB and VSWR between 1 and 2. However, the radiation efficiency was less than 70% for both FR4 based antennas, because loss tangent of the FR-4 substrate is 0.02 which is much higher than the loss tangent of Duroid-5880 as 0.0009. The 1 × 2

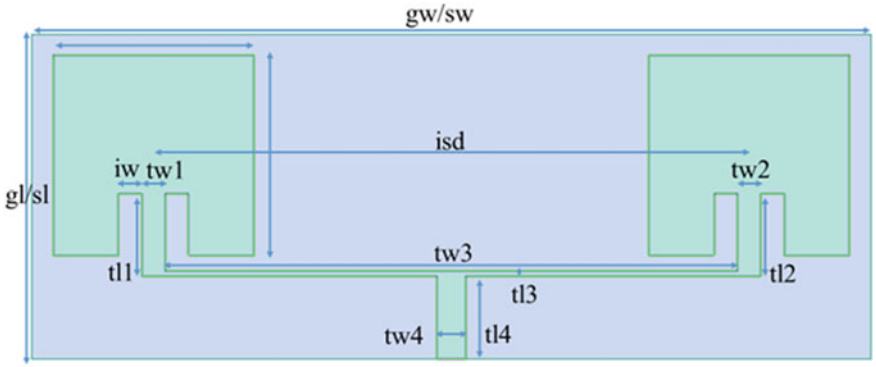

Fig. 1 Square patch array antenna: dual radiant

Table 2 Performance comparison between Duroid and FR-4 based 1 × 2 array antenna

Parameters	Duroid-5880	FR-4
RL (dB)	−46.99	−50.00
VSWR	1.02	1.01
Gain (dB)	10.63	5.85
RE (%)	98.00	47.00
BW (MHz)	33.00	67.00

Table 3 Performance comparison between Duroid and FR-4 based 2 × 2 array antenna

Parameters	Duroid-5880	FR-4
RL (dB)	−48.40	−51.17
VSWR	1.03	1.02
Gain (dB)	12.92	6.19
RE (%)	98.00	29.42
BW (MHz)	24.00	48.00

array antenna (Duroid-5880) has obtained a maximum gain of 10.63 dB among the all four antenna structures that means it has got more range of about 33.22 km for the receiver sensitivity of 94 dBm, as compared to other three antenna structures.

The antenna parameters of the array antenna of 1 × 2 structure is given in Table 2 which shows that the return loss is almost the same level, gain is double in the duroid material, efficiency is almost double in the duroid material but the bandwidth is only half of the performance of the FR4 material-based array.

2.3 Design of 2 × 2 Square Patch Linear Array Antenna with Duroid-5880 and FR4

The performance of the 2 × 2 antenna structure is given in Table 3. Here gain is double in the duroid material, and radiation efficiency is triple times that of the FR4 material and the bandwidth is only half of the performance of the FR4 material.

2.4 Design of 1 × 4 Square Patch Linear Array Antenna with Duroid-5880 and FR4

The performance of the array is given in Table 4. Here the return loss of the FR4 is improved, gain is double in the duroid material, radiation efficiency is double but the bandwidth is one third that of the FR4 based material.

Table 4 Performance comparison between Duroid and FR-4 based 1 × 4 array antenna

Parameters	Duroid-5880	FR-4
RL (dB)	−48.67	−59.00
VSWR	1.02	1.01
Gain (dB)	14.12	7.97
RE (%)	98.00	36.62
BW (MHz)	28.00	77.00

2.5 Fabrication of 1 × 2 Array Antenna on Duroid-5880

The practical evaluation of the Duroid and the FR4 based 1 × 2 antenna structure is given in Table 4. Here the gain of the duroid antenna is double that of the FR4 design, efficiency of the antenna is double in the duroid based antenna structure but the bandwidth is only half of the performance given by the FR4 material (Table 5).

This section presents fabrication of the 1 × 2 patch antenna using the PCB milling method. The PCB milling mechanism is the conventional method of fabricating the patch antennas. The copper cladded sample was used as the base material. The computer aided design (CAD) model was generated using the Ansys tool module for 1 × 2 array antenna as discussed in section B that was utilized. Based on the CAD model, PCB milling is performed on the copper cladded samples. The mechanical etching process was carried out to remove the unwanted copper material resulting in the printed geometry. The fabricated 1 × 2 patch antenna structure based on PCB milling is shown in Fig. 2.

Table 5 Optimal geometry of 1 × 2 patch array antenna with two different dielectric material

Parameters	Description	Duroid-5880 (mm)	FR4 (mm)
gl	Ground length	67.18	52.61
gw	Ground width	173.52	122.16
sl	Substrate length	67.18	52.61
sw	Substrate width	173.52	122.16
st	Substrate thickness	1.57	1.57
pl	Patch length	41.51	29.77
pw	Patch width	41.51	29.77
tl1/2	Feed line-1/2 length	17.18	13.61
tw1/2	Feed line-1/2 width	4.79	2.92
tl3	Feed line-3 length	1.07	0.84
tw3	Feed line-3 width	118.40	79.88
tl4	Feed line-4 length	17.18	13.61
tw4	Feed line-4 width	5.89	4.50
isd	Interspacing distance	123.20	82.80
iw	Inset width near feed line	4.85	2.83
	Dielectric constant	2.2	4.4
	Loss tangent	0.0009	0.02

Fig. 2 S_{11} Measurement of developed antenna on vector network analyzer

In order to determine the return loss of the 1 × 2 array antenna, vector network analyzer which can measure the frequency of any active or passive device up to 110 GHz was used as depicted in Fig. 2. Later the prototype was tested in the Anechoic chamber as shown in Fig. 3. The measured reflection coefficient using VNA and simulated was compared as in Fig. 4, and it was observed that there was a frequency shift. It was evident that 54.5 MHz downshifting in the measured result for 2.4 GHz resonance was compared to simulation due to fabrication tolerance and unpredictable losses such as cable and soldering loss. The Bandwidth of 33 MHz was observed for both the simulated and measured results.

Near field testing of the antenna was performed in the anechoic chamber as shown in Fig. 3 which has the horn antenna as the transmitting antenna. The distance between the transmitting and receiving antenna (prototype) was kept as 1.5 m. Figure 5 shows the measured *E* and *H* plane, which indicates the unidirectional radiation pattern of the antenna. In addition, the gain measured in the anechoic chamber is about 18.45 dB and it is quite high as compared to simulated gain of 10.63 dB. The difference may be due to the calibration error of the antenna. Based on the simulated and measured

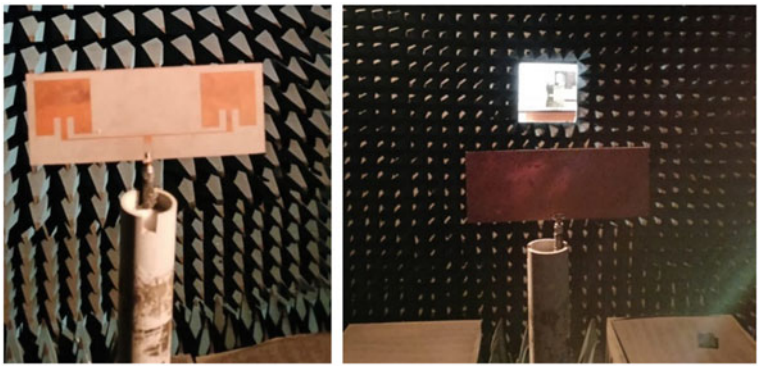

Fig. 3 Anechoic chamber testing of 1 × 2 microstrip patch array antenna

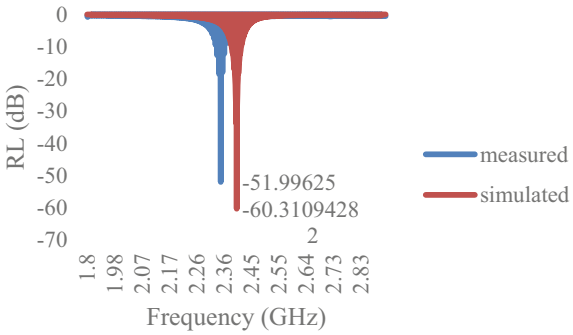

Fig. 4 Return loss of 1 × 2 array antenna

gain, antenna range prediction is given in Table 8. The gain of the compared antenna with 1 × 2 structures are shown in Fig. 6.

The correlation study of the simulated and the actual measured values are given in Table 6. Here it is understood that when the frequency increases, the gain of the antenna increases with both the material-based substrates that is by using the duroid and the FR4 based antenna structures. The gain of the antenna using the duroid material is 10.63 dB with the duroid material. But in the case of the FR4 material

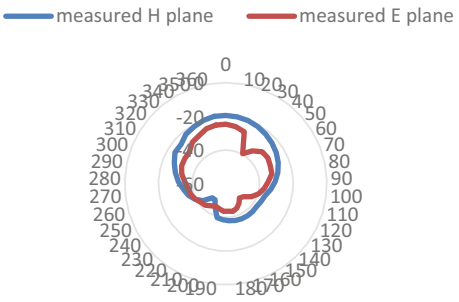

Fig. 5 Measured *E* and *H* plane of 1 × 2 antenna

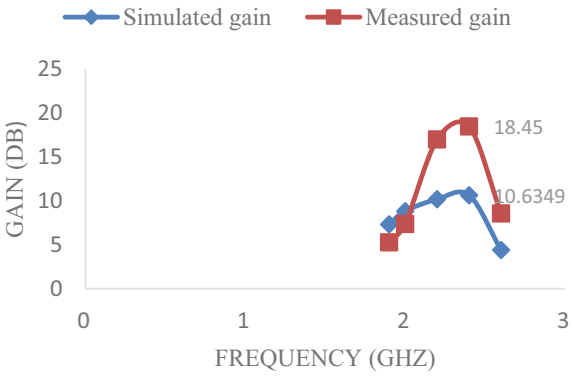

Fig. 6 Gain of 1 × 2 antenna

Table 6 Simulated versus measured gain

Frequency (GHz)	Simulated gain (dB)	Measured gain (dB)
1.9	7.332002	5.27
2	8.827532	7.37
2.2	10.18222	16.98
2.4	10.6349	18.45
2.6	4.415928	8.57

it was observed as 18.45 dB and this shows that the material property of the FR4 based antenna structure gives more gain than that of the duroid based structure. Several factors such as thickness and the dielectric constant also responsible for this deviation.

The performance of the different types of antenna available in the literature with the duroid based material is given in Table 7. Here the parameters are compared to understand the effect of the substrate in the antenna parameters. This correlation study shows that our proposed design works better comparatively in terms of gain and return loss.

Antenna coverage distance was calculated by using Eq. 2 given in Table 3.

$$\begin{aligned} \text{EIRP (dB)} &= P_t \text{ (dBm)} - \text{cable loss (dB/meter)} + G_t \text{ (dB)} \\ \text{FSL (dB)} &= \text{EIRP (dB)} - P_r \text{ (dBm)} \\ \text{Distance (m)} &= \text{FSL (dB)} + 20(\log_{10} \lambda) - 21.98 \\ \text{Range (m)} &= 10^{\text{Dist.}/20} \end{aligned} \tag{2}$$

where

EIRP Effective isotropic radiated power
FSL Free space path loss
P_t transmit power

Table 7 Comparison among the antenna with same substrate (Duroid-5880) in terms of gain, frequency, return loss, and dimensions

Design	Frequency (GHz)	Return loss (dB)	Gain (dB)	Dimension (mm)
This paper	2.346	−51.99	18.45	1.35 × λ
[42]	28	−14	11.7	12 × λ
[43]	6.7–17	Not reported	6	10 × λ
[44]	6.5–10	Not reported	15.6	8 × λ
[45]	8.5	Not reported	10	4 × λ
[46]	3	−18.4	5.8	1.5 × λ
[47]	5.78–5.82	Not reported	18.2	7.8 × λ
[48]	26–30	Not reported	10.6	6 × λ

Table 8 Antenna coverage prediction based on simulated and measured gain (maximum transmitter power = 30 dBm, simulated gain = 10.63 dB, measured gain = 18.45 dB, cable loss = 4.16 dB/m)

8 MHz channel bandwidth				
Modulation	Multicast IP ref throughput (Mbps)	Receiver sensitivity (dBm)	Range (Duroid-5880) (km)	Prototype antenna range (km)
QPSK_1/2	6	−94	33.22	81.73
QPSK_3/4	9	−91	23.52	57.86

G_t transmit gain
P_r Receiver sensitivity
λ Wavelength (m)

From the antenna range calculation, it is concluded that for enhanced antenna coverage, the transmission gain and power have to be maximized. In view of this, the antenna array method is used to improve the antenna gain (Table 8).

3 Conclusion

The first phase of this project focused on designing a microstrip patch array antenna of 2.4 GHz. By means of various iterations for a single radiant 1 × 2 array antenna dimensions were optimized. The simulation results for two different materials such as Duroid-5880 and FR-4 were compared with respect to their performance characteristics of the antenna. It was evident that Duroid based antenna structures outperformed with respect to gain and radiation efficiency. The simulation results suggested that the 1 × 2 array antenna obtained the maximum range of 33.22 km which is 1.73 times as compared to the 1 × 2 FR-4 patch structures. However, to perform preliminary fabrication studies and validate the theoretical results, the 1 × 2 patch array antenna was fabricated using PCB milling. The fabricated antenna was tested in the anechoic chamber and there was a deviation in the gain due to improper calibration, fabrication error, improper soldering and radiation loss. Expected and actual gain of the antenna are 10.63 dB and 18.45 dB respectively. The S_{11} parameter was also characterized using VNA and there was a downward frequency shift of 54.50 MHz as compared to 2.4005 GHz of simulated frequency.

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E—RiCoBiT—II: A High Performing RiCoBiT (Ring Connected Binary Tree) Topology with Fully Adaptive Routing Algorithm

V. Sanju, Sunil Kumar Manvi, Jude Abishek Shah, Hussam Taqhi, Harsh Mishra, and P. Chetana Reddy

Abstract Network on Chip (NoC) is very useful in connecting the different components of a chip. Many NoC topologies like 2D mesh, torus etc. are already in use. RiCoBiT (Ring Connected Binary Tree) is a new topology which was recently proposed and studied. RiCoBiT is a topology where performance parameters like maximum hop and average hop are better than the other topologies. Area parameters like wirelength and number of wire segments are approximately the same as compared to other topologies, but one of the biggest problems with this topology was the lack of an adaptive routing algorithm. Thus, we propose a new routing algorithm which is adaptive in nature. The algorithm is tested for all cases: destination and source in the same ring, destination is above the source ring, and the destination is below the source ring. The testing of the algorithm was performed by using a simulation setup for E-RiCoBiT- II (Enhanced RiCoBiT). It is observed that the topology is 100. The average hop, maximum hop, and total time are studied for the proposed architecture and algorithm.

Keywords Network on chip · Mesh · Torus · RiCoBiT · Adaptive routing algorithm

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1 Introduction

Network on chip [1, 2] is becoming one of the most crucial ways to implement any processing chip. Network on Chip (NoC) topologies makes use of packet transfer technique for communications on a chip. Earlier a common bus topology was used to connect the different modules of a processor. Bus topology has been eventually modified in different ways to meet the requirements of efficient communication. Later it was proved to be inefficient. Thus the concept of network on the chip evolved which was efficient in terms of speed, parallel processing, etc.

Topologies discovered earlier like mesh and torus as shown in Figs. 1 and 2, respectively were used in NoC based applications, but they had some drawbacks: when the topology increased in size and the size of the logic increased, these topologies could not provide the desired output. Thus, RiCo- BiT (Ring Connected Binary Tree) [3] was proposed which is faster in terms of speed and showed a positive edge in performance.

In all of the topologies, routing algorithms [4] play a very important role in the movement of the information and processing of the data. In case of mesh and torus, existence of a routing algorithm both adaptive and non-adaptive was there from the beginning of its inception. But in case of RiCoBiT, its inception was topology with a non-adaptive routing algorithm.

A. *Problem Statement*

The major problem is that RiCoBiT does not have an adaptive routing algorithm. If any node in the path fails, then the whole transmission in the RiCoBiT topology along the broken node will fail. Thus, there is a need to design adaptive routing algorithm for RiCoBiT topology which is free from deadlocks and has improved response time, better throughput, lower convergence time and lower energy consumption. In this paper, we propose a routing algorithm that is adaptive in nature which is deadlock

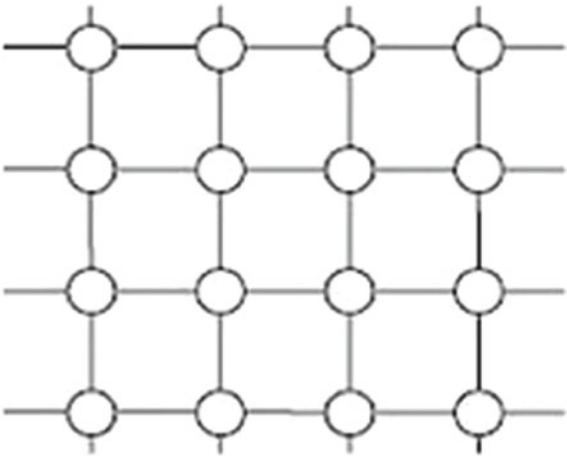

Fig. 1 Mesh topology

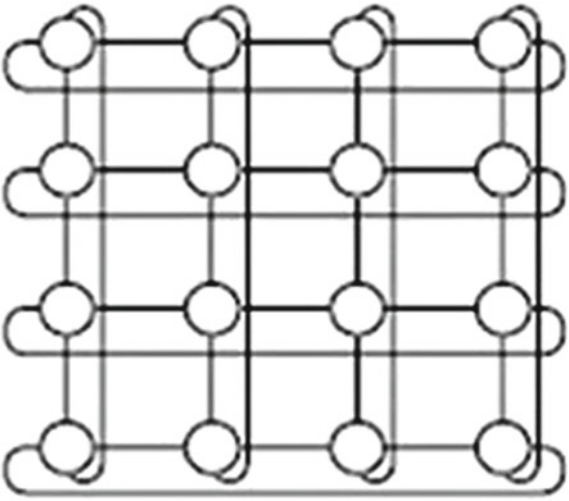

Fig. 2 Torus topology

free and will be able to route all the packets from source to the destination. If a route exists in various configurations such as 1:1, 1:N, N:1 and N:M. RiCoBiT with adaptive routing then it is called E-RiCoBiT -II (Enhanced RiCoBiT).

B. *Our Contribution*

- We propose a new routing algorithm which is adaptive in nature for our proposed E-RiCoBiT topology.
- The topology and algorithm were studied through simu- lation to test operation effectiveness of the routing algorithm.
- Algorithm works in case of node and link failures and offers better packet delivery and throughput.

C. *Organisation of the Paper*

The paper is organized as follows. In Sect. 2, the concepts of Ring Connected Binary Tree (RiCoBiT) is explained. It also describes the performance comparison of mesh, torus and RiCoBiT by considering the parameters maximum hop, average hop, number of wire segments and wire length. It proves that RiCoBiT is better than mesh and torus topology. This section also brings out E-RiCoBiT (Enhanced Ring Connected Binary Tee). Section 3 describes the proposed adaptive routing in E-RiCoBiT (Enhanced RiCoBiT). Section 4 presents the simulation, results and discussion. Finally we conclude in Sect. 5.

2 Ricobit Topology

Figure 3 Shows the RiCoBiT (Ring Connected Binary Tree) [3] topology. From the figure, we can observe that RiCoBiT has n rings, where in each ring consists of many nodes and the number of nodes is 2^n, where n is the ring number. For ring $n = 2$, it will have $2^n = 2^2 = 4$ nodes. The nodes are connected in a way that node n in k ring is connected to 2n and 2n + 1 node in ring k + 1. Therefore *kth* ring will consist of 2^k nodes. Thus, the total number of nodes of a topology with n rings will be equal to $\sum_{k=1}^{n} = 2^k$..

A non-adaptive routing algorithm which is 100% optimal is already present in RiCoBiT. This algorithm finds the shortest path from the source to the destination. A method of mathe- matical induction was used to prove the algorithm [1]. When compared to other topologies like 2D mesh, torus, etc. in terms of performance, it was proved efficient.

Now let us compare the performance parameters like maxi- mum hop and average hop and the area parameters like number of wire segments and wire length with mesh and torus. The comparison with mesh, torus and RiCoBiT is done using the Figs. 4, 5, 6, 7. First let us consider the maximum hop of the three topologies as shown in

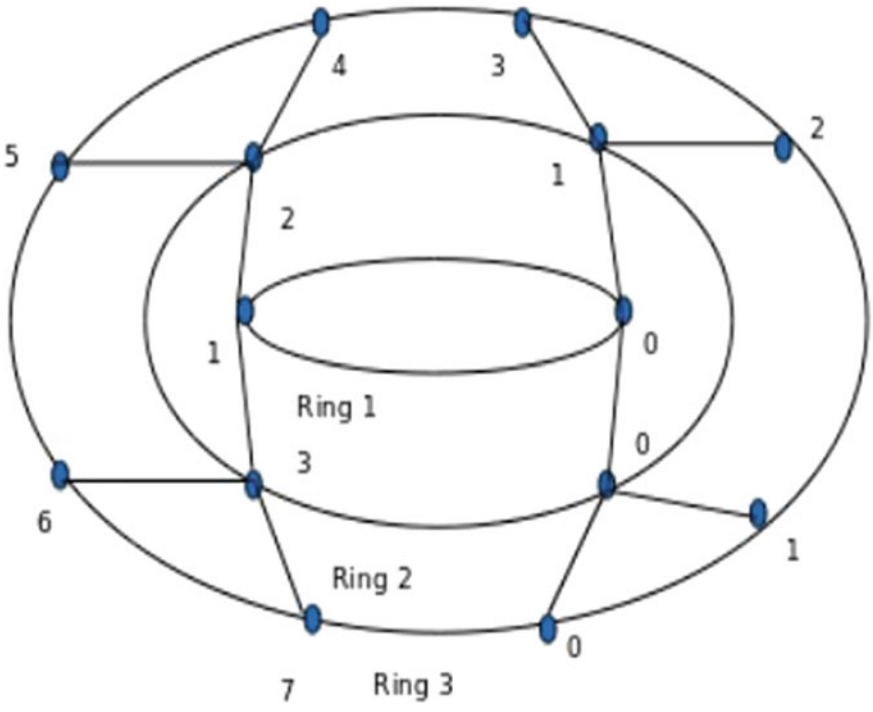

Fig. 3 RiCoBiT topology with three rings

Fig. 4. We observe that the RiCoBiT uses less maximum hops compared to other topologies.

From the graphs shown in Figs. 4, 5, we can conclude that the maximum hop and average hop count of RiCoBiT is very less when compared to the other topologies. Thus, we conclude that RiCoBiT is very efficient in terms of performance when compared to other topologies like mesh and torus.

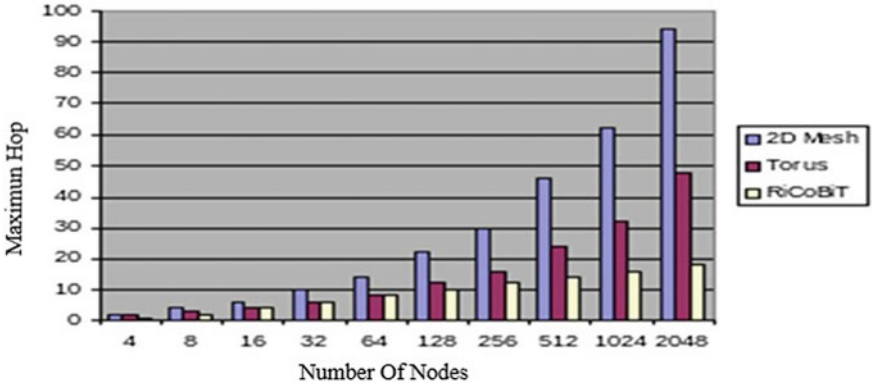

Fig. 4 Maximum hop versus number of nodes

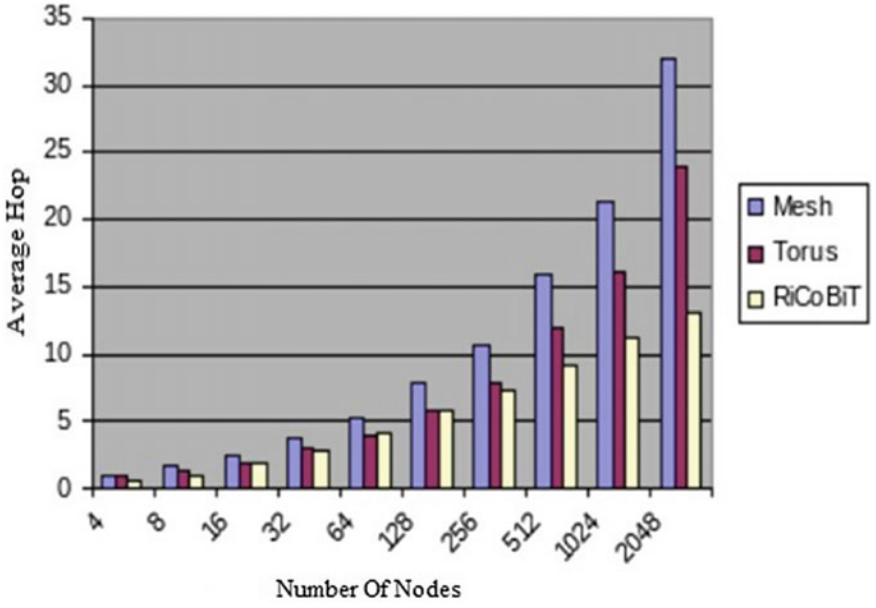

Fig. 5 Average hop versus number of nodes

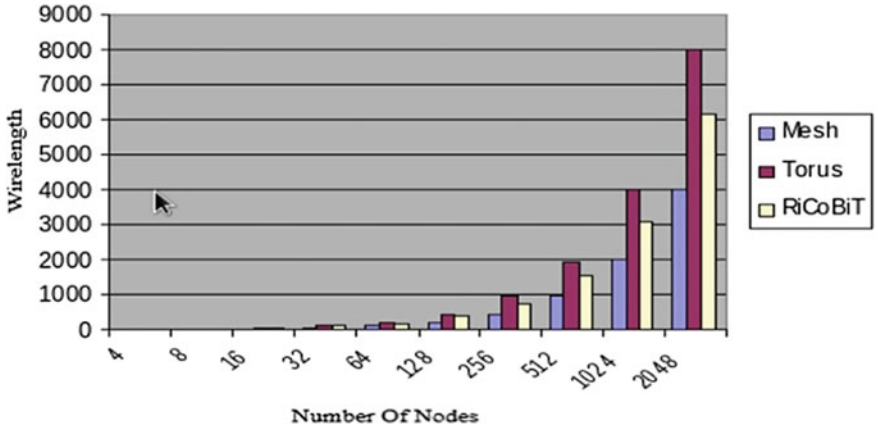

Fig. 6 Wirelength versus Number of Nodes

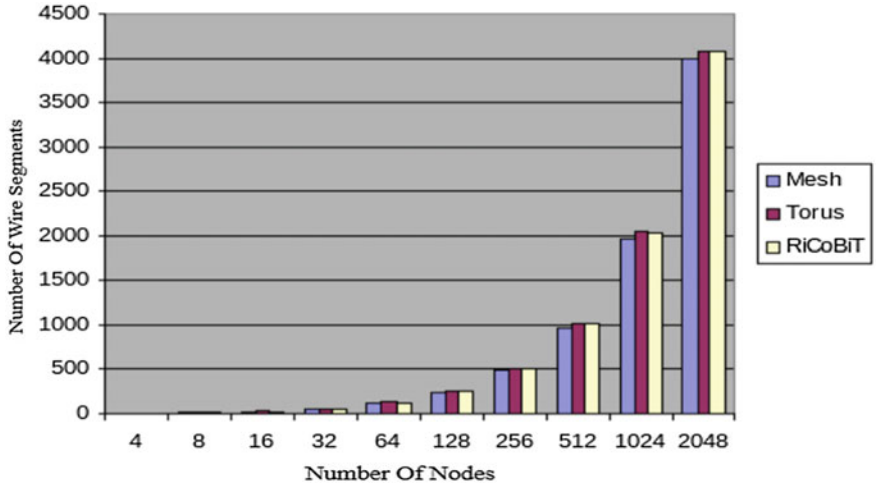

Fig. 7 Number of wire segments versus number of nodes

When we look at the area parameters for an integrated circuit, the number of wire segments and wire length are the main parameters. The Figs. 6 and 7 represent the wire length and number of wire segments.

From the Figs. 6 and 7, we can conclude that the number of wire segments and wirelength are almost equal compared to mesh and torus.

Thus, we can conclude that RiCoBiT topology is better in terms of performance for system building as well, when compared to mesh and torus. But the disadvantage with RiCoBiT is the absence of an adaptive routing algorithm. In this paper, we discuss a fully adaptive algorithm for RiCoBiT topology. Therefore, we term the RiCoBiT topology with a fully adaptive routing algorithm as E-RiCoBiT—II i.e., Enhanced Ring Connected Binary tree—II.

3 E—RICOBIT—2 (Enhanced Ring Connected Binary Tree—II)

E-RiCoBiT (Fig. 8) has the similar topology of RiCoBiT with the end nodes disconnected but it differs in the routing algorithm. E-RiCoBiT -II has an adaptive routing algorithm whereas RiCoBiT has a non-adaptive algorithm. In physical parameters like number of wire segments, wire length remains the same as that of RiCoBiT. In the case of E—RiCoBiT, if the node in between the transmission is not correct/ damaged, then the packet is routed.

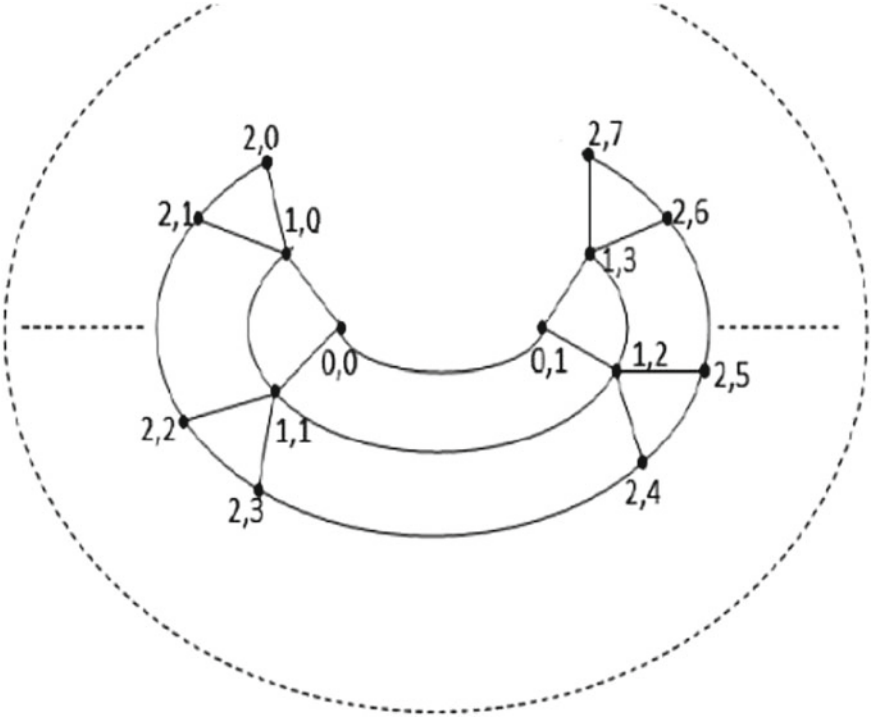

Fig. 8 ERiCoBiT topology

A. *Fully Adaptive Routing Algorithm*

In this section we present a fully adaptive routing for E- RiCoBiT. Here the routing algorithm routes all the packets from the source to the destination if there is a path between them. Let us explain the algorithm.

The routing algorithm is divided into four cases.

- Case 0 is when the node which is sending the packet is the sender and the receiver is also the same node. In this case the packet transmission stops here
- Case 1 is when the destination node address and the current node address are in the same ring.
- Case 2 is when the destination node address is below that of the current node address.
- Case 3 is when the destination node address is above that of the current node address

All the cases of routing are explained as follows.

Case 0—When Destination Node Address is the Same as the Current Node Address

Input: Current Node Address
Output: Next Node Location

Begin:
1.Absorb the packet
End

Case 1 is when the source and the destination are inthe same ring. First let us take up the case wherein all nodes are working. Here it will check whether the difference between the source and the destination node is greater than three. If it is greater than three then the node is moved to the bottom from the source and destination nodes until the difference between the nodes is less than three. If the position of the source node and the destination node becomes less than 3 then move towards the temporary destination and then move up to the original destination. If the node below is not working or if it is busy for a long time, then comes the solution of adaptive algorithm comes into picture. It will take the path which is to the right/left depending on the shortest path and then the packet is forwarded to the next node for possibly routing the packet from the source to the destination node.

Case 1—When the Destination Node Address and the Current Node Address Are in the Same Ring

Input: Current Node Address
Output: Next Node Location

Begin:
1. Calculate the node difference
2. If the node difference is greater than three
3. Send a request through the bottom interface to check if the node is available
4. If an acknowledgment is received within 'n' cycles
5. Then go through the bottom interface
6. If no acknowledgment is received from the bottom interface
7. If the destination is to the left
8. Send a request through the left interface.
9. If an acknowledgment is received within 'n' cycles
10. Then go through the left interface
11. Else if no acknowledgement is received from the left interface
12. Send a request to the top-left interface
13. If an acknowledgment is received within 'n' cycles
14. Then go through the top-left interface
15. Else if the destination is to the right
16. Send a request through the right interface.
17. If an acknowledgment is received within 'n' cycles
18. Then go through the right interface
19. Else if no acknowledgement is received from the right interface
20. Send a request to the top-right interface
21. If an acknowledgment is received within 'n' cycles
22. Then go through the top-right interface
23. If an acknowledgement is received from neither of the interface, the destination node cannot be reached.
24. Repeat the process till the node difference is less than three
25. If the node difference is less than half the number nodes in the ring
26. Then go through the left interface
27. Else go through the right interface.
End

There is no limit on the number of hops a packet can take.

Consider the case for example (Fig. 8) when the source node is (3,0) and the destination node is (3,2). These nodes are separated by a distance of 2 hops. Since the distance between the source and the destination is less than 3 it is routed straight from (3,0) to (3,1) and then to the destination (3,2).

Now consider the case wherein the source node is (3,0) and the destination node is (3,5). These nodes are separated by a distance of 5 hops. Since the distance between the source and the destination is more than 3, it is routed (2,0) to (2,1) then to (2,2) and then to (3,5).

Case 2 happens when the source node is at the higher ring compared to the destination node. First let us examine the normal when the nodes are all active and are capable of routing. It first transfers the packet from the source node to the node which is directly connected to the destination node along the same ring. It then routes the packet to the nodes in the higher level till the destination is reached. In case of the adaptive nature of the algorithm, it will take the path which is to the right / left depending on the shortest path and then forward the packet to the next node for possibly routing the packet from the source to the destination node.

Case 2—When the Destination Node Address is Below that of the Current Node Address

```
Input: Current Node Address
Output: Next Node Location

Begin
1. Calculate the node difference
2. Send a request through the bottom interface to check if the
node is available
3.      If an acknowledgment is received within 'n' cycles
4.           Then go through the bottom interface
5.      If no acknowledgment is received from the bottom
interface
6.              If the destination is to the left
7.                   Send a request through the left interface.
8.                   If an acknowledgment is received within 'n'
cycles
9.                        Then go through the left interface
10.                  Else if no acknowledgement is received
from the left interface
11.                       Send a request to the top-left interface
12.                       If an acknowledgment is received within
'n' cycles
```

```
13.                    Then go through the top-left interface
14.            Else if the destination is to the right
15.                Send a request through the right interface.
16.                If an acknowledgment is received within
'n' cycles
17.                    Then go through the right interface
18.                Else if no acknowledgement is received
from the right interface
19.                    Send a request to the top-right interface
20.                    If an acknowledgment is received within
'n' cycles
21.                        Then go through the top-right
interface
22. If an acknowledgement is received from neither of the
interface, the destination node cannot be reached.
23. Then repeat the process till destination node is reached.
End
```

There is no limit on the number of hops a packet can take.

Consider the example (Fig. 8), here we take the source is (1,0) and the destination node is (5,3). Here the node comes down from (1,0) to (2,0) and then to (3,0). Now the packet is traced to (4,1) and then to the destination node (5,3).

Case 3 is when the source packet is to be transmitted from a higher level to the destination which is in the lower level. Here again let us take when all the nodes are fine. The packet is routed to the same level that of the destination node and then as it is routed towards the destination node. In case of the adaptive nature of the algorithm, it would take the path which to the interface which is free depending on the shortest path and then forward the packet to next node for possibly routing the packet from the source to the destination node.

Case 3—When the Destination Node Address is Above Than that of the Current Node Address

```
Input: Current Node Address
Output: Next Node Location

Begin
1. Calculate the node difference
2. Calculate parent node
3.      Calculate node difference between current node and
parent node.
4.     If the node difference is greater than three
5. Send a request through the bottom interface to check if the
node is available
6. If an acknowledgment is received within 'n' cycles
7.          Then go through the bottom interface
8. If no acknowledgment is received from the bottom interface
9.          If the destination is to the left
10.             Send a request through the left interface.
11.             If an acknowledgment is received within 'n'
cycles
12.                 Then go through the left interface
```

```
13.          Else if no acknowledgement is received from
the left interface
14.              Send a request to the top-left interface
15.              If an acknowledgment is received within
'n' cycles
16.                  Then go through the top-left interface
17.      Else if the destination is to the right
18.          Send a request through the right interface.
19.          If an acknowledgment is received within 'n'
cycles
20.              Then go through the right interface
21.          Else if no acknowledgement is received from
the right interface
22.              Send a request to the top-right interface
23.              If an acknowledgment is received within
'n' cycles
24.                  Then go through the top-right interface
25. If an acknowledgement is received from neither of the
interface, the destination node cannot be reached.
26. Repeat the process till the node difference is less than
three
27. If the node difference is less than half the number of
nodes in the ring
28. Then go through the left interface
29. Else go through the right interface.
End
```

There is no limit on the number of hops a packet can take.

For this case take the example wherein the source node is (5,3) and the destination node is (1,0). In this case the packet is routed from (5,3) up to (4,1) and then (3,0). Now the packet is routed towards (2,0) and to the destination (1,0).

4 Results and Discussion

A simulator was made to check and verify the correctness of the algorithm. It was observed that the algorithm worked perfectly in all cases of simulation run. In this we could observe the working of the topology in all the cases such as 1:N, N:1, M:N when all the nodes were working, with some error nodes were nonfunctional etc. Here we have used Intel i7 multi core machine with 8 GB RAM, 1 TB HDD for the purpose of simulation. It was observed that the topology does not come to a deadlock situation in any of the simulation run. The following output screens display the different results of the simulator. First let us discuss if there are no nodes which are damaged. The Fig. 9. shows the path from the source to the destination. A node in the simulation is represented as a node of a tree which is interconnected as shown in Fig. 10. Here the source node is 1 (1,0) and the destination is 7 (3,0). All the pathways are perfect i.e. all the paths and nodes are working perfectly.

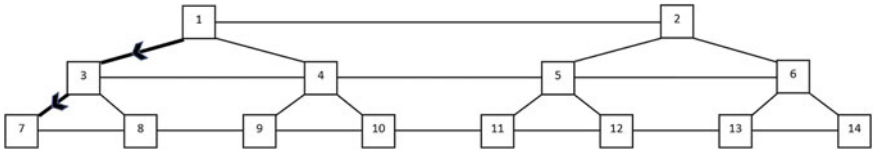

Fig. 9 Movement of packets from node 1(1,0) to node 7 (3,0) without any damaged node

```
Enter the number of rings 3
                                    1->(1,0) 2->(1,1)
                              3->(2,0) 4->(2,1) 5->(2,2) 6->(2,3)
        7->(3,0) 8->(3,1) 9->(3,2) 10->(3,3) 11->(3,4) 12->(3,5) 13->(3,6) 14->(3,7)

Maximum binary representation of source row number is : 2 bits
Maximum binary representation of source node number is : 3 bits
Maximum binary representation of destination row number is : 2 bits
Maximum binary representation of destination node number is : 3 bits
Size of data : 8 bits
Total number of bits : 18
Enter your choice:
1. One source node -> One destination node
2. One source -> All destinations
3. All sources -> All destinations
1
Enter the source row number 1
Enter the source node number 0
Enter the destination row number 3
Enter the destination node number 0
Source node is 1
Destination node is 7
Enter the number of broken nodes 0
Outer cycle : 1
Request sent from 1 to 3
Outer cycle : 2
Acknowledgment recieved from node 3
Outer cycle : 3
ACKNOWLEDGEMENT
Acknowledgment sent from 7 to 1
Hop from 7 to 1 is : 2
Path taken by the packet is : (3,0) (2,0) (1,0)
       OR
Path taken by the packet is : 7 3 1

Total time is : 38
Average time is : 36
Maximum time is : 38
```

Fig. 10 The simulator output screen about movement of packets from node 1(1,0) to node 7 (3,0) without any dam- aged node

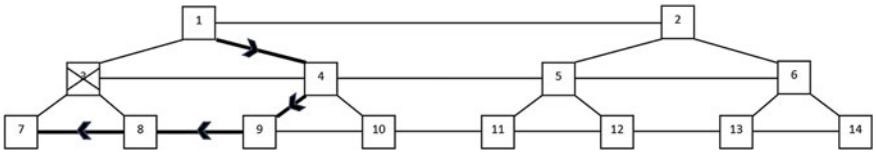

Fig. 11 Movement of Packets from Node 1 (1,0) to Node 7 (3,0) with one damaged node 3 (2,0)

Now let us see the working of the simulator when one node is broken. Here we take up the same settings as above, but we consider node 3 i.e. (1,0) is not working or is damaged. Here the adaptive algorithm works wherein the packet is routed from 1 to 4 to 9 to 8 to 7. Figs. 11 and 12 depict the same.

The topology is tested extensively to check for deadlock, livelock cases. We have tested for errors with zero node, one node, two nodes and higher cases. We simulated the case of one error nodes for 1:1, 1:N and M : N nodes to find the working of the topology and the algorithm, It was quite clear that the routing algorithm worked fine in all the cases without causing any deadlock, livelock situations.

First let us take the max hop quantity with the number of levels. We have simulated the situation with different configurations. Figure 13 depicts the performance analysis between the number of levels and maximum hop quantity with one error node in between. As the number of levels (number of nodes) increases the maximum hop also increases. This is due to the fact that when the numbers of nodes increase with the number of levels, the distance between them increases, hence the maximum hop.

Similarly performance analysis with one error node is done for average hop. The Fig. 14 depicts the same. As the number of levels (number of nodes) increases the average hop also increases. This is due to the fact that the numbers of nodes increase with the number of levels, the distance between them increases, hence the average hop.

Similarly performance analysis with one error node is done for the total time taken for the simulation to complete. Figure 15 depicts the same. The same explanation holds good even in this case.

```
Enter the number of rings 3
                                        1->(1,0) 2->(1,1)
                                3->(2,0) 4->(2,1) 5->(2,2) 6->(2,3)
        7->(3,0) 8->(3,1) 9->(3,2) 10->(3,3) 11->(3,4) 12->(3,5) 13->(3,6) 14->(3,7)

Maximum binary representation of source row number is : 2 bits
Maximum binary representation of source node number is : 3 bits
Maximum binary representation of destination row number is : 2 bits
Maximum binary representation of destination node number is : 3 bits
Size of data : 8 bits
Total number of bits : 18

Enter your choice:
1. One source node -> One destination node
2. One source -> All destinations
3. All sources -> All destinations
1
Enter the source row number 1
Enter the source node number 0
Enter the destination row number 3
Enter the destination node number 0
Source node is 1
Destination node is 7

Enter the number of broken nodes 1
Enter 1 broken node(s)
Enter the broken node 1 row number 2
Enter the broken node 1 node number 0
Broken node is 3

Enter the number of broken nodes 1
Enter 1 broken node(s)
Enter the broken node 1 row number 2
Enter the broken node 1 node number 0
Broken node is 3

 Outer cycle : 1
Request sent from 1 to 3
 Outer cycle : 2

ACKNOWLEDGEMENT
Acknowledgment sent from 7 to 1
Hop from 7 to 1 is : 4
Path taken by the packet is : (3,0) (3,1) (3,2) (2,1) (1,0)
       OR
Path taken by the packet is : 7 8 9 4 1

Total time is : 76
Average time is : 72
Maximum time is : 76
```

Fig. 12 The Movement simulator screen about movement of packets from node 1(1,0) to node 7 (3,0) with one node damaged (2,0)

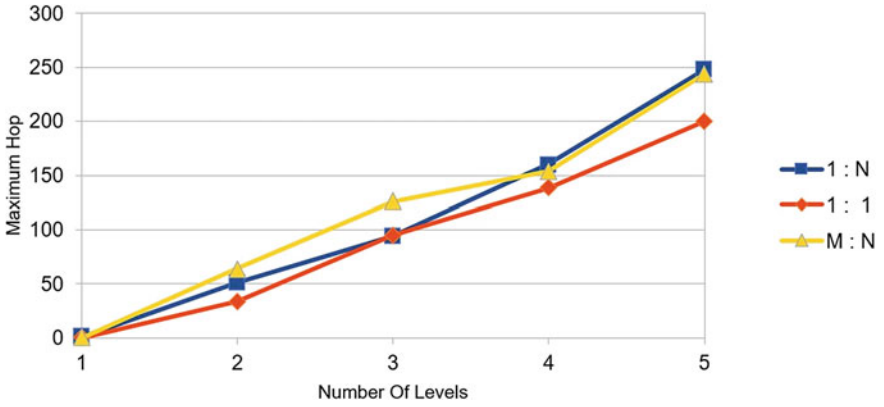

Fig. 13 Performance Analysis—Maximum hop versus number of levels

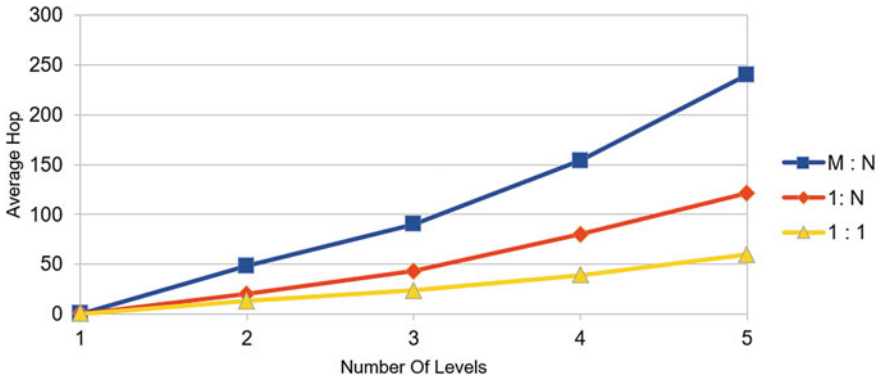

Fig. 14 Performance Analysis—Average hop versus number of levels

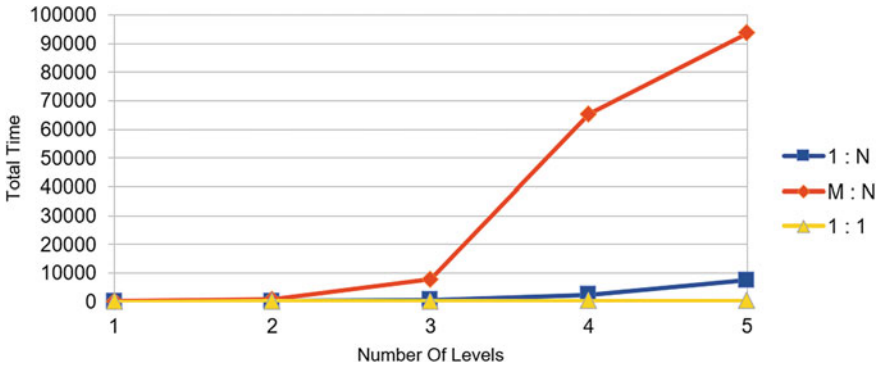

Fig. 15 Performance Analysis—Total time versus number of levels

5 Conclusion

The initial discussion made it evident that RiCoBiT is superior to mesh and torus. However the RiCoBiT topology has a drawback in that it lacks an adaptive routing mechanism. Here, we introduced a completely adaptable routing system for the RiCoBiT with a variety of functional outcomes. The results make it very plain and obvious that the method functions well in every situation. The testing procedure also shows that a deadlock condition is not brought about by the algorithm. Additionally, the aforementioned topology has been evaluated for deadlock scenarios and it has been found that there are none. We could advise developing applications like an FPGA using RiCoBiT and the adaptive algorithm as additional work. We also plan to develop a multi core processor based on RiCoBiT topology.

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Design and Development of Autonomous VTOL for Medicine Deliveries in Hilly Areas

K. Jeevan, V. Mukesh Kumar, S. Pranav, E. S. Manish, and Chandra Singh

Abstract This paper discusses the configuration of an autonomous hybrid VTOL (Vertical Take-Off and Landing) aircraft is systematic for the last mile delivery of medicines to rural and remote places. The developed aircraft has a payload capacity of 4 kg, a flying period of up to 45 min, and a high stability speed of 65 km per hour. This UAV is fitted with intelligent systems that enable it to operate autonomously even in places without a Global Positioning System and away from obstructions, which is essential in disaster-prone areas. This VTOL's folding wing structure reduces the Take-off and Landing area, making it more reliable.

Keywords VTOL · GPS · PX4 · ROS · Gazebo

1 Introduction

India has a massive health care system, yet there are still significant disparities in health care quality between urban and rural areas. Rural and remote locations continue to be under-treated by medical emergency services. The primary cause of death is a failure to provide medications or emergency supplies on time. During a pandemic or natural disaster, standard human-to-human interaction or door-to-door delivery will be disrupted, affecting the supply chain. The required commodities, including medicine, will expire or be delayed if they are not delivered on time. These issues generate a new branch of the problem and become exponentially larger until appropriate action is done. These are significant issues in nations like India, where the entire population is over 137 crores. Thus, employing drone technology to distribute food and medication during pandemics, natural disasters, and medical emergencies in rural and remote places has had a significant influence on the medical industry. However, the inefficiency of drones is another hindrance to the deployment

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Fig. 1 Prototype model

of the drone delivery system. The conventional method of drone delivery employs a quadcopter or a multirotor, which is ineffective owing to its inability to provide a sufficient flight duration, a low cruising speed, and so on. To address these obstacles, we devised a novel solution of developing a hybrid VTOL (Vertical Take-Off and Landing). This VTOL is fitted with a folding mechanism that allows the wings to be folded, reducing the needed surface area for takeoff and landing while also avoiding dynamic obstructions. The VTOL is capable of navigating in GPS-denied areas through Visual Inertial Odometry (VIO), making delivery possible in hilly locations (Fig. 1).

2 Literature Survey

Pain Multirotors or Unmanned Aerial Vehicles (UAVs), have become increasingly popular in recent decades. A wide variety of uses are possible, from emergency response [1] to agriculture [2, 3] to safety checks [4, 5]. They function in comfortable and clear surroundings. Pilot certification is sometimes required when deploying these multirotor in more challenging locations such as inside or on mountainous area. The traditional approach involves using the configurations like quadcopter, hexacopter [6]. The drawback of these configurations is increased current consumption, less cruise speed, decreased flight time. Our approach uses hybrid configuration of a quadcopter and fixed-wing aircraft known as VTOL. The advantages of using this as configurations are decrease in the overall current drawn, hence it leads to increase in flight time due to the transition from fixed-wing to multirotor [7]. During takeoff and landing multirotor mode is utilized, where all the four motors will be running

and providing the thrust for the vehicle to perform takeoff and landing with more stability. Once the vehicle has reached the target takeoff altitude, it transitions into fixed-wing mode thus utilizing only one motor for providing vertical thrust. ROS framework is used for building software stack and perform autonomous navigation [8]. The surrounding data is captured using depth camera [9] to generate point cloud data which is used for performing obstacle avoidance tasks. The vehicle is capable of avoiding obstacles by applying the VFH+ (Vector Field Histogram) algorithm [10]. The simulation of the navigation and obstacle avoidance along with transition in flight modes is necessary. Some use simulink to simulate the behavior of the vehicle [11]. Our approach involves Gazebo as a simulation platform to test bench all software and behavior of the vehicle.

2.1 System Characteristics

2.1.1 Increase in Flight Time

The orthodox method used in drone delivery systems obeys conventional quadcopter or hexacopter drones to accomplish the missions. The major drawback of this system is failing to attain minimum flight time. Due to the synchronized power consumption by multiple motors throughout the mission, the flight time provided by the batteries will be very low. To overcome this issue, we are designing a VTOL which is a combination of a plane and a multirotor. It adopts a multirotor configuration during the takeoff and landing, and a conventional plane configuration to complete the mission. Hence an increase in the flight time is achieved due to the usage of a single motor leading to a very less amount of power consumption from the battery.

2.1.2 Folding Mechanism of the Wing

The conventional plane configuration is not adopted in UAV delivery systems due to its inefficient ways of takeoff and landing. This is due to the high surface area of the wing and the requirement of a long takeoff run for takeoff and landing. Hence we are designing a VTOL with a wing folding mechanism which takes off and lands as a multirotor reducing the takeoff run. A unique wing folding mechanism is adopted in the aircraft during the takeoff and landings, hence making the UAV capable of working in compact places [12].

2.1.3 Increase in Cruise Speed

The orthodox method used in drone delivery systems obeys conventional quadcopter or hexacopter drones to accomplish the missions. One of the major drawbacks of the system is the low cruise speed. The maximum average speed of a multirotor can go

up to 55 kmph whereas a plane configuration has an average cruise speed of 80–110 kmph. Hence this is one of the main reasons for adopting a plane configuration over a multirotor during the cruise mission. The wing of the aircraft is optimized and iterated numerous times with multiple airfoils to obtain an ideal wing that provides high lift, stability, and cruise speed [13].

2.1.4 Landing

One of the main issues faced in the drone delivery system is landing, especially in rural and hilly areas. The conventional method adopted by the delivery companies is delivering by dropping from mid-air, due to the issues of landing. To overcome this unfit we have the solution of introducing arUco code landing pads in the landing zones. Once the aircraft reaches the desired GPS coordinate, it searches arUco landing pads with the help of its RGB camera and lands on it safely [14].

2.1.5 GPS Denied Integration

By using the Visual Inertial Odometry Technique, we can make drones navigate even in GPS denied areas. Visual Inertial odometry (VIO) is a technique for calculating a robot's state (position and velocity) primarily from the input of one or more cameras and one or more attached Inertial Measurement Units (IMUs). To accomplish precise state estimate, VIO has been the only suitable option to GPS and light detection and ranging odometry [15].

2.2 System Architecture

The above Fig. 2 shows the complete architecture of our system. The 8MMNavQ is used as a companion computer for the UAV to perform autonomous missions. Robot operating system (ROS) is implemented on the board.

2.2.1 Simulation Architecture

Testing the algorithm for our drone is crucial. Thus, testing it with real hardware is risky, because if there are any bugs or glitches in the code the drone might end up crashing thus damaging the components used. This can result in loss of time and money. Hence, we decided to test bench all our code in the simulation. The hardware component is shown in Fig. 3.

(1) Gazebo: The Gazebo was used as a 3D physics simulator for testbenching the VTOL behaviour. Gazebo enables the precise and efficient simulation of robot

Fig. 2 System architecture diagram

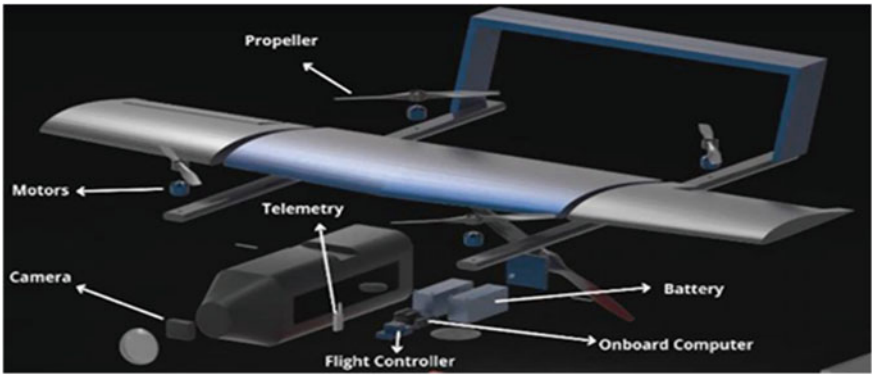

Fig. 3 Hardware component placement

populations in dynamic indoor and outdoor situations. Gazebo simulation is shown in Fig. 4 (Fig. 5)

(2) PX4 SITL: Inorder to simulate the behaviour of the drone precisely with the real world, we utilized the PX4's Software-In-The-Loop (SITL). With this we can interact with our drone just as you might with a real vehicle, using QGround-Control, an offboard API, or a radio controller. PX4 interacts with the simulator in order to receive sensor information from the simulated environment and to transmit actuator values. It interfaces with both the Ground Control Station Software and an Offboard API in order to transmit and receive telemetry from the virtual environment.

(3) The Safe Landing: This feature ensures that VTOL only lands on a flat terrain. Thus avoiding crash landing on trees and rocks. If the vehicle is instructed to land, it falls to a height from which it can analyze the surface. If the landing

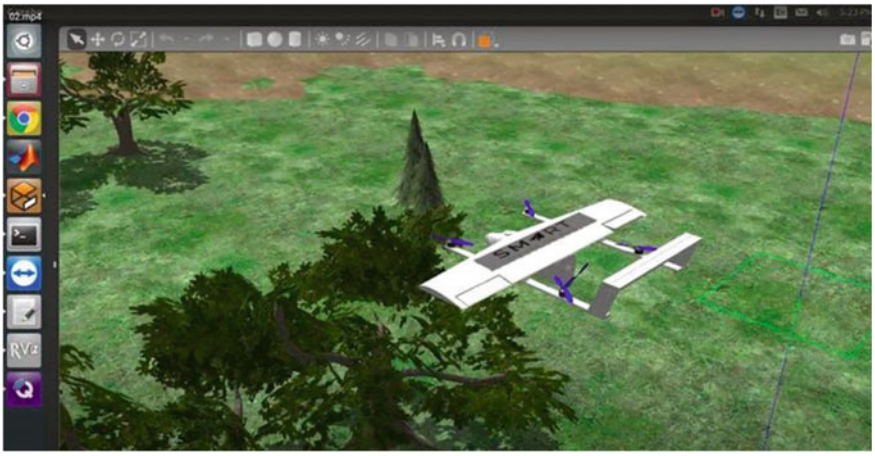

Fig. 4 Gazebo simulation of VTOL

Fig. 5 Software in the loop

location is not adequately flat, the vehicle proceeds outward in square-spiral pattern, frequently pausing to re-check the landscape for a suitable landing place. It uses point cloud data from depth cameras and takes standard deviation to detect irregularities between each point in point cloud and thus detects whether a terrain is flat or not. Landing Simulation is shown in Fig. 6.

Aerodynamics simulation: High stability, high lift, and minimum drag are the parameters prioritized during the design of the wing. Numerous airfoils were iterated for a set of Reynolds numbers, to attain the desired airfoils. An array of airfoils was imported from the UIUC Airfoil Data Site which includes coordinates for a vast amount of airfoils. The filtration criteria were mainly under cambered, thin airfoils. A high coefficient of lift and a low drag coefficient at a low Reynolds number were favored. The primary analysis of the airfoils is supervised using software such as XFLR, XFOIL, Flow5. According to the results of preliminary analysis, the airfoil is chosen and performed CFD (computational fluid dynamics) using software such as ANSYS and Solidworks. The results of the CFDs are compared and the efficient airfoil is accepted for the design of the wing as depicted in Fig. 7.

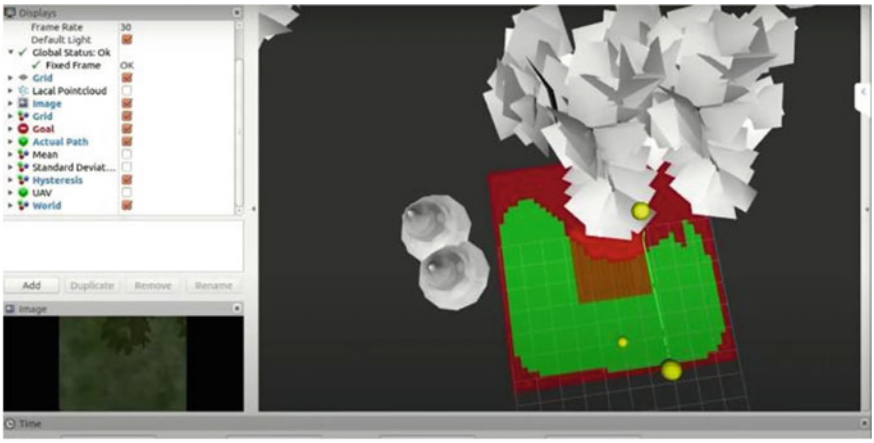

Fig. 6 Safe landing simulation

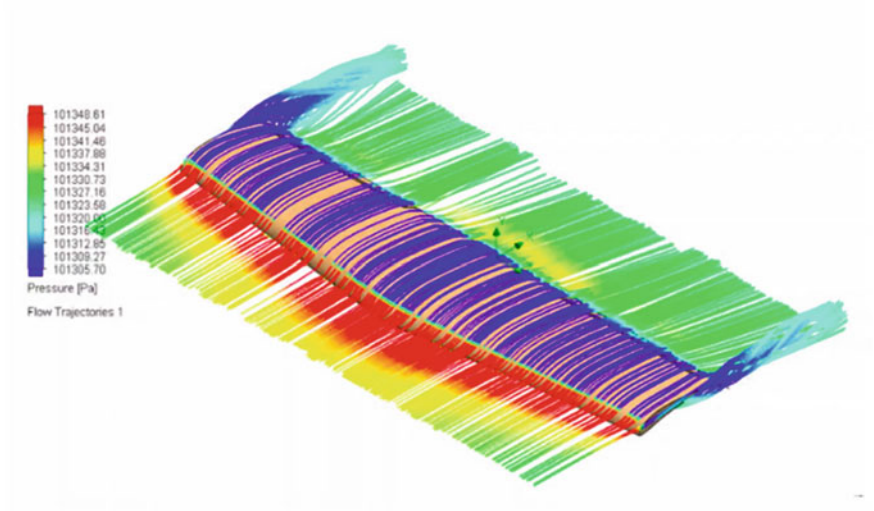

Fig. 7 Wing CFD fluent analysis

After Rigorous analysis of the airfoils, the Selig S1223 is finalized as it meets all aerodynamic and manufacturing requirements. A significant alteration that the airfoil went through was a 10% camber reduction and an additional 10-degree flap at the trailing edge. The S1223, a supercritical airfoil, has an implausible lift to drag ratio in addition to a provisional high coefficient of lift. The airfoil is unwavering even at higher angles of attack.

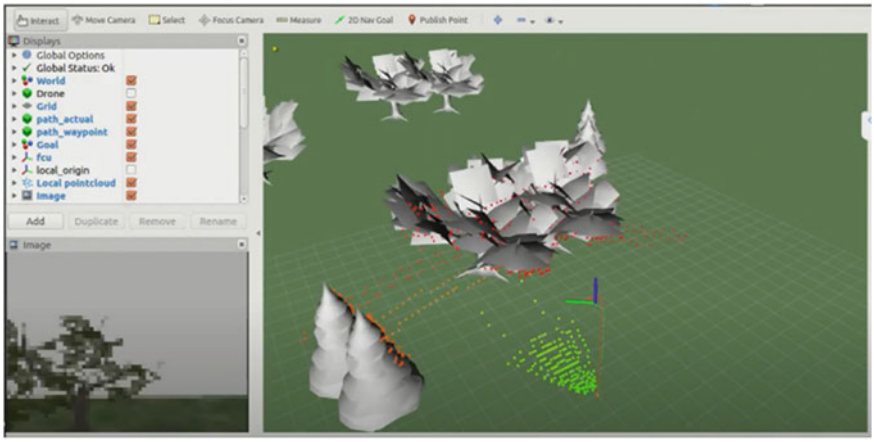

Fig. 8 Obstacle avoidance in RViz

2.2.2 Result

The VTOL was deployed in the Gazebo simulator, where the obstacle avoidance and safe landing algorithm were tested in custom environment containing various obstacles and uneven terrain. Figure 8 shows the VTOL avoiding the obstacles around it while traversing to the given goal location. We conducted test flights of our real-world model of VTOL where both quadcopter and plane configuration were examined. VTOL was tested in both simulation and real-world under various circumstances and the behaviors were found to be identical. The plots of Fig. 9 Shows the amount of current drawn during the takeoff and landing phase in quadcopter configuration. It has been observed from these plots that a max of 33.05A of current is drawn. While plots from Fig. 10 show the current drawn during cruising in plane configuration. Initially more current is drawn until the VTOL attains a certain velocity and gradually gains lift from wings. The current drawn is minimal while cruising at mean velocity. Overall the amount of current drawn is less when compared to quadcopter configuration, therefore more efficient. The cruising velocity of the VTOL is measured and plotted. Figure 11 Shows the airspeed graph with a max value of 26 m/s with a mean of 13 m/s.

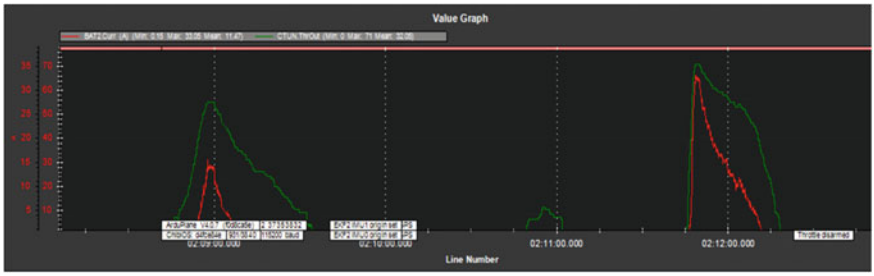

Fig. 9 Quad configuration current consumption

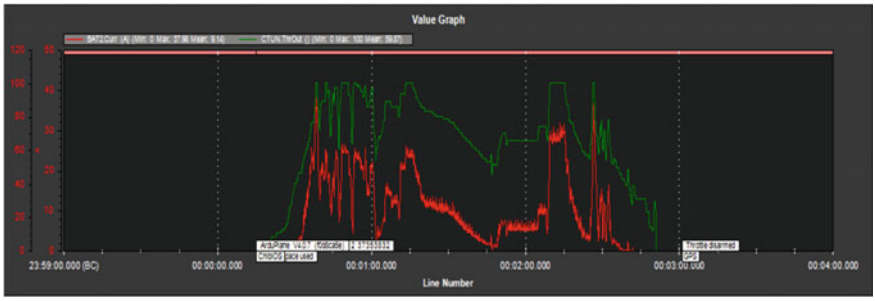

Fig. 10 Fixed wing configuration current consumption

Fig. 11 Air speed plot

3 Conclusion

In this paper we proposed and validated an autonomous VTOL which is capable of performing autonomous navigation from the initial point to the given goal location, and perform obstacle avoidance and localization using Robot Operating System wrappers. Also, we have proposed a novel approach to solve the safe landing problem of the UAV by evaluating the terrain using point cloud data obtained from depth camera. Initially these approaches were tested in a simulation environment before porting it into a real UAV prototype. The UAV prototype has been tested in the real-world environment. Results show that we were successful in applying our proposed approaches into UAV in simulation as well as in real world. Future scope of the work lies in optimizing the overall design of VTOL and developing anti- crash system to improve the redundancy of UAV while preforming real-time missions.

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Implementation and Design of Agile and Multipurpose Autonomous Robot Using ROS

K. Jeevan, Sohan M. Rai, V. Mukesh Kumar, E S Manish, Pranav Sathish, and Chandra Singh

Abstract This paper discusses an implementation of autonomous navigation functionality on a differential drive mobile platform called AMAR (Agile and Multipurpose Autonomous robot) based on the Robot Operating System (ROS). The paper's primary contribution is to describe an unmanned platform capable of mapping, localizing, and navigating in an enclosed environment that is well-suited for industrial operations. The approach used for mapping is through the ROS framework, a technology stack containing multiple software stacks for controlling, visualization, and debugging the robot, wrapped with the help of sensors such as RGBD camera and LiDAR (Light Detection and Ranging). For navigation, Adaptive Monte Carlo Localization is used for localizing the vehicle and thus leading to autonomous operation. The proposed solution is computationally efficient and capable of dynamic obstacle avoidance. The simulations were performed using the 3D physics simulator Gazebo and the results were visualized using RViz.

Keywords Agile and Multipurpose Autonomous robot *AMAR* · Robot Operating System (*ROS*) · *Gazebo* · Simultaneous Localization and Mapping (*SLAM*) · Light Detection and Ranging (*LiDAR*) · Dynamic-Window Approach (*DWA*)

1 Introduction

Unmanned Ground Vehicles are widely used for a variety of purposes nowadays. Collaboration between different types of robots from different manufacturers or even self-developed robots within the same ecosystem is becoming more popular. With the advancement of robotics and computer science, manufacturers and Industrial Robotics have reached a point where they are concentrating their efforts on developing systems that are more agile and adaptable to changes in the environment.

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Customer satisfaction is a primary objective in today's economy, and it necessitates production tailored to customer needs at lower costs, with greater reliability, and of higher quality, because customers drive business. Warehouse management involves large numbers of labor due to the high demand of online shopping, and laborers in warehouses need to follow strict social distancing. Of course, automation was well advanced in the warehouse world long before the pandemic. The trend dates all the way back to the late nineteenth century, when the conveyor belt was invented. However, today's distribution robots are entirely different, emulating human actions and thought processes. The pandemic swiftly changed consumer purchasing behaviors as much of the population transitioned to online shopping and services. As warehouses scramble to adopt technology that can help them adapt to these changes and become more efficient, there is a shortage of manpower that can help with these logistical challenges. Along with automated warehouse robots that move inventory from warehouse shelves to pack- out areas, many warehouses are implementing newer innovations such as human-like robotic arms and mobile applications to improve the efficiency of picking and storing inventory across warehouses. Unmanned mobile robots are used to perform challenging, unsafe, and/or highly unpleasant tasks that would be performed by humans but are prohibitively expensive in terms of ease of access, protection, and survival, or when lack of energy, time, or discomfort are increased. As a result, missions for unmanned ground, aerial, and underwater vehicles now include monitoring infrastructures such as roadways, canals, and offshore oil and gas installations (Fig. 1).

An unmanned Ground Vehicle is designed and developed for autonomous operations in industrial environments. It consists of an onboard computer and various sensors for achieving fully autonomous navigation. The autonomous robotic platform is based on a differential drive mobile base, which enables the robot to move

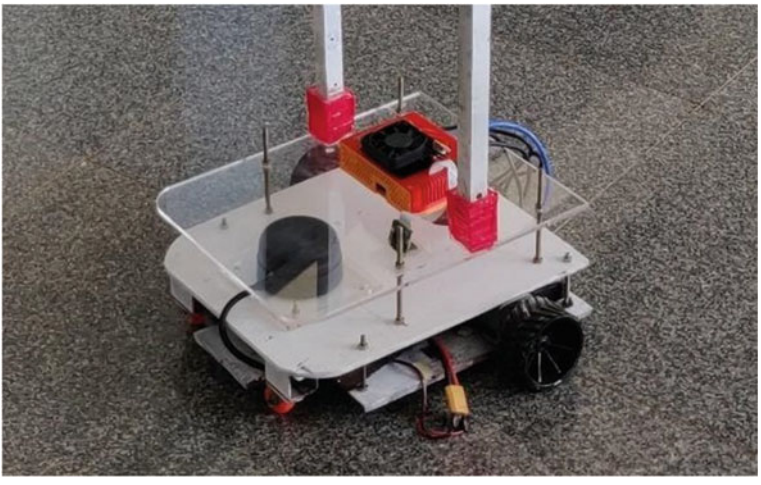

Fig. 1 Prototype model

forward, backward, and turn by controlling the angular velocity of the left and right wheels. The wheels are powered by encoder-equipped motors. The odometry system is implemented by interpreting data from the robot's wheel encoders to determine the robot's position and orientation for localization. The robot platform is equipped with intelligent sensors aiding in performing the operation. The system comprises sensors like a depth camera for perception tasks and LiDAR for indoor navigation and obstacle avoidance. Actuators and feedback sensors make sure the operations are going right. It uses the ROS framework for performing SLAM (Simultaneous Localization and Mapping) and other high-level tasks such as transporting packages from one location to another. SLAM is concerned with creating a map based on the robot's perceptions and then localizing the robot within that map. G-mapping algorithm is used for the ROS Navigation Stack's SLAM functionality. This creates no involvement of humans hence no risk of error. The solution is unique as it contains a single mobile base with multiple plug- in extensions on top of the mobile base, making it a simple and multipurpose system. It is also cost-effective due to the use of minimal sensors while maintaining the same accuracy.

The advancement of robotic platforms is time and cost- intensive and complex, simulation is increasingly being used to test and validate the ability of robotic platforms and their sensors to perform sensing and navigation. Because simulation enables low-cost and rapid robotics testing and validation, an initial emphasis on broad strategies is placed. The testing environment can be recreated in robotic simulations to match specific agricultural use cases and robotic sensor platforms, and algorithms can be evaluated for efficacy and efficiency. With simulated sensors completing a feedback loop, complete control strategies can be tested and developed. Numerous agricultural robot drive systems and navigation techniques have been developed and validated in simulation before being implemented successfully.

2 Related Work

With the rapid advancement of robotics, an increasing number of robots are appearing in the field of cleaning service, safety [1] and warehouse management. To accomplish this, intelligent robots require location and mapping capabilities. In [2], magnetic localization is used, a common technique is to first construct a magnetic representation of the area wherein the robot will be deployed. Their computational and memory costs, on the other hand, scale inadequately if large amounts of data are used for training, making them unsuitable for use in large-scale environments. Several other methods [3] like ceiling mounted [4] bar codes [5], range or camera-based wall-following [6], using floor markers [7] or magnets [8], and following magnetic tape are available for vehicle localization and planning. In reference [9], localization and mapping functions are based on the Cartographer algorithm [10]. Path planning and navigation functions are based on the optimal path algorithm. It makes use of a cartographer slam algorithm and sensory inputs from lidar and wheel encoders only. However, navigation accuracy is minimal when using only lidar and encoder data.

Additionally, numerous edge cases will occur as a result of the uncertain environment. To compensate this, [11] The authors describe a hybrid navigation strategy that makes use of both a LiDAR-based control algorithm and GPS waypoint navigation. Additionally, in reference [12] an inertial measurement unit and depth camera [13] can be integrated to improve robustness in navigation. ROS (Robot Operating System) framework along with Gmapping algorithm is been described for solving the navigation problem in an unknown environment [14]. Simulation of robots play a crucial role while testing and validating various algorithms for localization and navigation. In this work, we use Gazebo for simulating our robot behavior [15] and testing the model in various custom environment.

3 Methodology

In this context, we propose a solution of developing an autonomous robotic platform capable of doing multiple tasks thus avoiding unnecessary repetitive work, contact between humans and helps to increase productivity. Compared with traditional human work, robots and autonomous systems have advantages such as the ability to perform tasks with high accuracy, efficient path planning, increased flexibility and safety (Fig. 2).

$$x = R/2(Vr + Vl)\cos\theta \tag{1}$$

$$y = R/2(Vr + Vl)\sin\theta \tag{2}$$

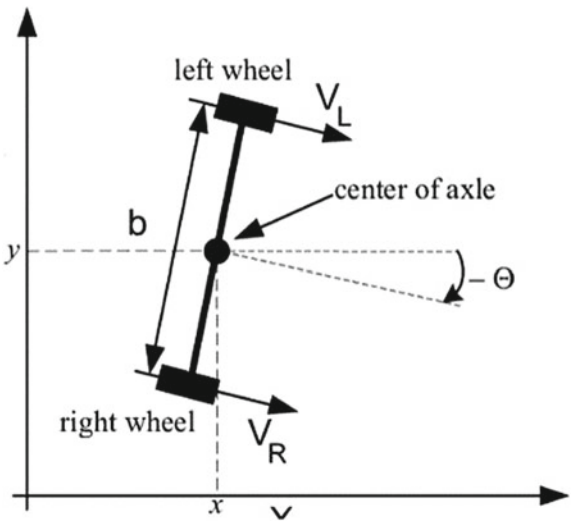

Fig. 2 Differential drive kinematics

$$\theta = R/b(Vr - Vl) \tag{3}$$

The designed robot uses the unicycle model with two wheels separated by distance b. Each left and right wheel velocities are represented by *Vl* and *Vr*. In the unicycle model, the state of the vehicle is defined as a three-element namely *x*, *y* and theta. Using (1–3), we calculate the x,y coordinate and theta given wheel velocities and vice versa. Our approach uses this method to calculate respective wheel velocities required to reach a destination point.

3.1 Software Architecture

The software architecture is heavily dependent on ROS. The most common robotics development environment is currently ROS. ROS includes libraries and tools to aid software developers in the creation of robot applications. The ROS framework's main advantage is that it treats all sensors as nodes. Hardware abstraction, device drivers, libraries, visualizers, message passing, and package management are all included, as well as a variety of other features. ROS provides us with a full set of robot communication channels, removing the tedium of programming from our lives. The navigation problem mainly deals with two things: localization and path planning. Our approach involves SLAM (Simultaneous Localization and Mapping) to get the initial map of the surrounding environment. SLAM is a computational problem that involves creating or updating a map of an unknown environment while also tracking the position of an agent within it. While this appears to be a chicken-and-egg problem at first glance, there are several algorithms known for solving it in tractable time in certain environments. The SLAM algorithm simultaneously maps the environment and localizes the robot by utilizing laser scan data from the LiDAR sensor and odometry data from the wheel encoders (Fig. 3).

The initial map is later used for path planning to move from the initial pose to the goal location. AMCL (Adaptive Monte Carlo Localization) algorithm is used to get the pose of a robot in a given map. AMCL works with the help of particle filtering. In particle filtering, particles are scattered randomly in the environment. During each periodic iteration, the particles obtain a higher amount of weight whenever it estimates the pose of the laser. The particle is reassembled according to the updated weights, while they are converging to a specific point, then that corresponding position is the maximum likelihood position of the robot. For path planning and static obstacle avoidance A star (A*) grid-based algorithm is implemented on the robot. A star search algorithm is one of the most effective and widely used techniques for path discovery and graph traversal. A* is an informed search algorithm, or a best-first search algorithm, in the context that it is described in terms of weighted graphs: it seeks the shortest path to a specified goal node starting from a specific starting node in the graph. This is accomplished by maintaining a tree of paths that begin at the beginning node and trying to extend them one edge at a time until the process has

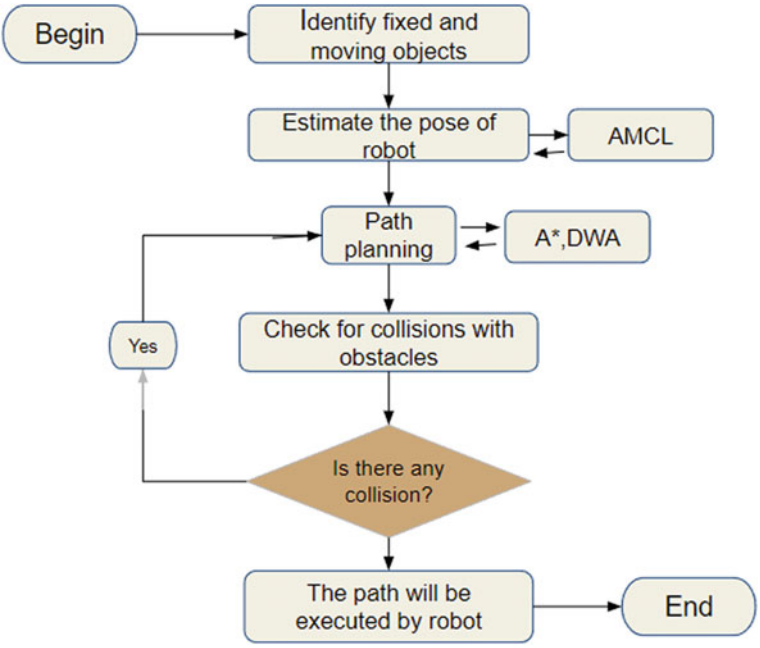

Fig. 3 Overall software architecture

finished. As a result, the shortest distance between start and objective is covered, as well as faster real-time execution (Fig. 4).

We employ DWA (Dynamic-Window Approach) running parallel to A star to avoid Dynamic Obstacles that occur suddenly, allowing the robot to avoid any type of dynamic obstacle. This increases the robustness of the system in real-world scenarios. If the robot encounters any barriers in its path while navigating in the unknown environment, it recalculates its course to its destination. If the computation is successful, the robot will be given a new course to take in order to attain the goal, which it will then follow. For tracking the actual path with the required path, we are using a PID controller to control the motor speed, thus reducing the error while following the required path. The robot's wheel encoders give odometry data, which is fused with LiDAR and Inertial Measurement Unit (IMU) data using the Extended Kalman Filter while the robot is moving (EKF). With great precision, the EKF produces the most definite pose, i.e., the robot's X and Y coordinates, as well as orientation (). The robot deems the specified path complete once it reaches the goal pose and waits for the following commands.

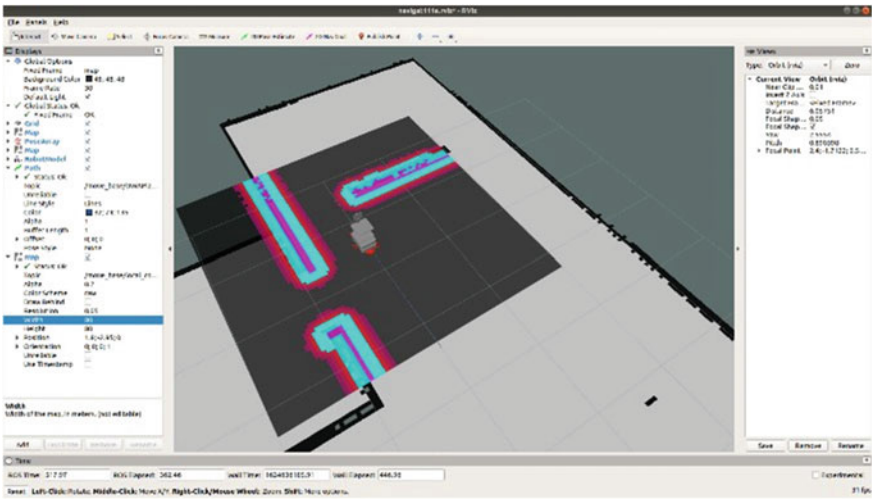

Fig. 4 Navigation simulation

3.2 Hardware Architecture

The implementation is carried out on a differential drive- wheeled robotic platform. NVIDIA Jetson Nano is used as a companion computer that indeed acts as the brain of the system to perform high-end computations such as SLAM, path planning, and obstacle avoidance. The onboard companion computer is connected to a controller through serial communication. The controller helps to steer the differential drive base on the bases of the commands received by the companion computer. Motor drivers are connected to the controller for driving the motor. An Atmel-based controller is used as the main controller. It calculates the odometry of the robot using the data from the IMU and the data from the encoders of the motor through the CAN bus. MPU6050, an IMU (Inertial Measurement Unit) is used to calculate the pose of the robot with the help of a Kalman filtering. The motor controlling methods adopted are by speed and current control loop. A PI control loop which is one of the preferred control systems for error reduction on the control system on an industrial scale is used to achieve high precision of the robot (Fig. 5).

The companion computer runs with the Ubuntu 18 as the operating system. Robot Operating System is implemented in ubuntu to perform autonomous navigation and control of the robot. The RPLIDAR A2 is a 360-degree omnidirectional laser range scanner that is used to scan the surrounding environment and generate an outline map of it. Due to the carefully designed internal mechanical system, the RPLIDAR A2 maintains its excellent performance while being only 4 cm thick. It is an excellent fit for all types of service robots. The sample rate of the LIDAR sensor has a direct effect on the robot's ability to map quickly and accurately. RPLIDAR enhances the sample's internal optical design and algorithm system.

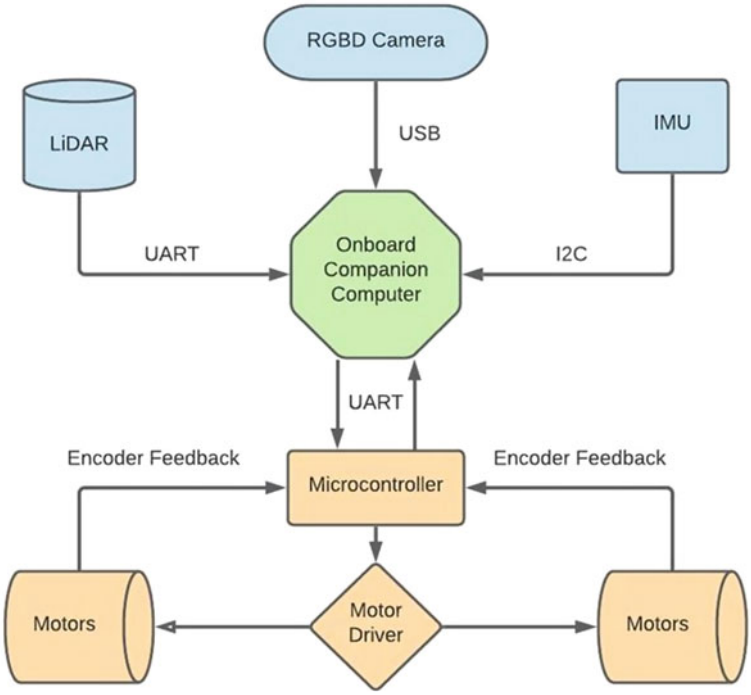

Fig. 5 Hardware architecture diagram

A depth camera is used to comprehend the environment, i.e. it provides depth perception capabilities to the robot. As a depth camera, we used the Intel® RealSense D435. The camera has the widest field of view of any of our cameras and a global shutter on the depth sensor, which makes it ideal for fast-moving applications. The camera is a stereo solution that provides superior depth for a wide range of applications. Its wide field of view is ideal for applications like robotics or augmented and virtual reality, where seeing the entire scene is critical. This small form factor camera with a range of up to ten meters integrates easily into any solution and includes our Intel RealSense SDK 2.0 and cross-platform support.

3.3 Experiment Setup

The proposed robot is benchmarked against different use cases using the 3D dynamic simulator Gazebo for faster iteration and accurate results. Figure 6 URDF workflow is shown below.

The navigation stack of our robot consists of two planners, global and local to increase the robustness while planning paths. Global planner uses A* algorithm to

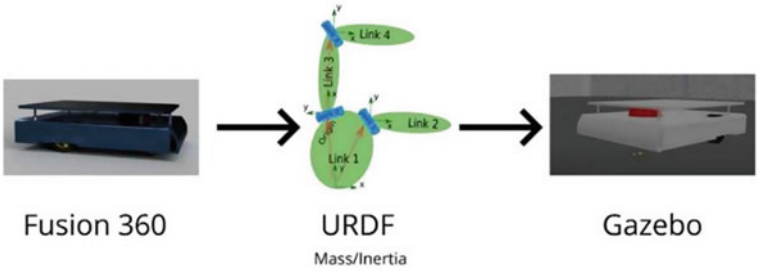

Fig. 6 URDF generation workflow

navigate from the initial pose to the final goal location while the local planner use Dynamic Window Approach (DWA) to plan short paths while avoiding obstacles and moving towards the goal location. It's more than a matter of finding workers to fill each position. To export the robot in gazebo a URDF description of the robot must be created. To export the robot in gazebo a URDF description of the robot must be created. URDF is an XML file format which is used in ROS to define all of a robot's elements. Firstly, the robot modelling is done with CAD software. While modelling all the real-world parameters like mass, the material is chosen. Later the CAD model is converted into URDF format. Suitable plugins like motors, castor wheels, cameras, etc are added to the URDF. Finally, the URDF model is imported into the Gazebo simulator where the required simulations are performed. We use fusion 360 as the cad software to create a 3D model of the robot and to generate URDF. Fusion 360 enables the exploration and iteration of product ideas, as well as collaboration among members of a distributed product team.

4 Results

The robot was designed and imported into custom gazebo simulation environment. Figure 7 shows the robot model spawned in gazebo world. We have successfully completed real time simulation of our robot in gazebo simulator. Figure 8 shows the mapping of surrounding using laser scanner.

The robot is capable of performing point to point navigation and can localize itself using Robot Operating System wrappers. Dynamic obstacle avoidance is tested in different simulation environments. In Fig. 9 shows the plot where the accuracy was validated by plotting odometry and estimated pose values. Real-world prototype of the robot was developed and tested for different scenarios with fixed and moving obstacles. Destination point was given as input in RViz and the robot computes shortest path from the initial point to the destination point. If the destination is unreachable, then the robot would traverse to the nearest free space.

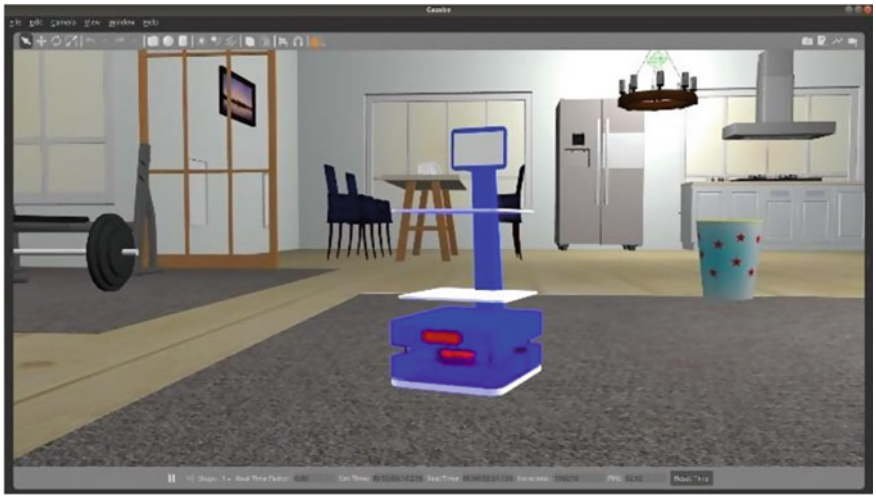

Fig. 7 Robot model in Gazebo

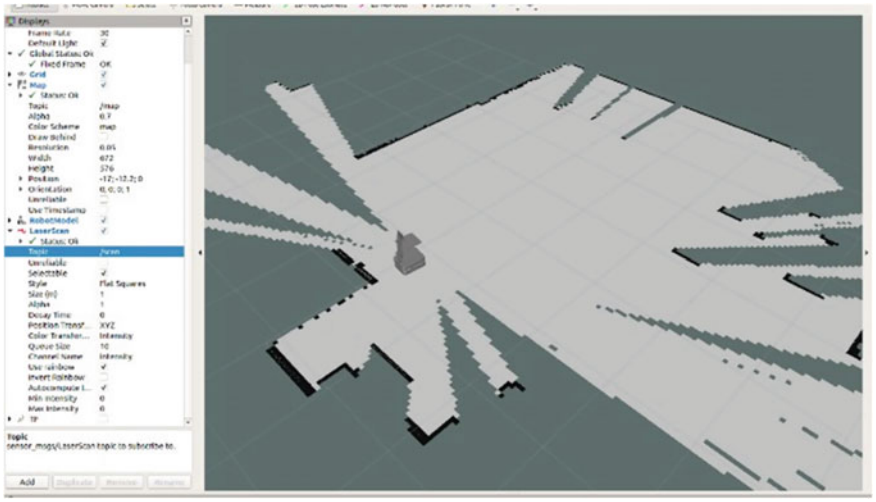

Fig. 8 Mapping using LiDAR

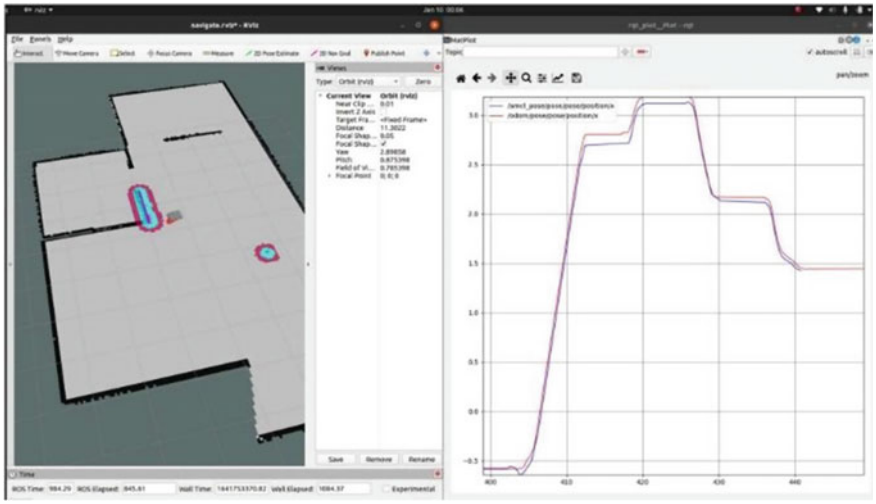

Fig. 9 Odometry, estimated pose plot

5 Conclusion

A novel method was used for solving the problem of navigation and obstacle avoidance for a ground robot in indoor environment where using GPS is unreliable. Data from various sensors like lidar, IMU, camera, wheel encoders are fused to estimate the pose of the robot accurately and with increased robustness. Results from both simulation and real-world prototype are obtained, validated and showed that the robot was successful to navigate in an unknown indoor space and avoid obstacles. Further scope of the work lies on using reinforcement learning techniques for solving the navigation problem and comparing it with this approach. Another challenge lies in implementing the navigation stack using only camera, which would cut down the need of several other sensors. This can be accomplished using visual-slam based approaches which are efficient and robust.

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Prediction of Chronic Pain Onset in Patients Experiencing Tonic Pain: A Survey

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Abstract Pain is caused by particular nerve fibers that transmit impulses to the brain, where they are interpreted. Pain has a multidimensional nature, making it hard to decipher, because of its subjectivity. Chronic or recurring pain is a common impairment among the elderly, significantly bringing down their quality of life. Assessment and treatment of pain are critical challenges in providing interventions for a variety of illnesses, especially because their origins are closely related to deep rooted issues. There is a rising interest in finding objective, nonverbal methods to quantify pain in people who are unable to self-report discomfort, such as those suffering from dementia or those in a minimally conscious state. Though, self and subjective reports are the common means of measuring the impact of pain and assessing its intensity, studies suggest that there are multiple sensory means through which a cumulative and concise data on occurrence of pain (tonic or phasic) can be retrieved, such as, through HRV (Heart Rate Variation), EEG/ECG/EMG readings and health performance metrics based on everyday activities. Our project aims to utilize the space of sensory technologies, with a focus on EEG data and IoT to conduct pain assessments with the help of machine learning techniques and explore IR therapy as well as electrical stimulation in subjects that experience chronic pain. Our intervention in pain assessment looks to combine subjective reporting and sensor based crucial data points on occurrence of pain to derive a reliable method of pain reporting.

Keywords Pain assessment · EEG · HRV · Body sensor networks · IoT · Objective assessment · Chronic pain · Tonic pain

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1 Introduction

Pain is a very multidimensional, subjective and fluctuating experience. Although self-reporting has become one of the most relied upon methods of quantifying pain, there's a large majority, about 5 million in India alone, that lack the capacity to communicate their perception of physical discomfort. This is mainly prevalent in older people and patients with certain communication roadblocks like disabilities or a language barrier. Along with being detrimental to a patient's physical well-being, varying levels of pain have also proven to be damaging to vital organs. The inability to properly convey this to a physician has become a roadblock to gaining access to good healthcare or in some cases, even the bare minimum [1, 2]. Even today, pain is very inadequately managed post procedures like surgery for instance. This leads to adverse consequences for them. This also leads to a failure of intervention during possibly life-threatening emergencies. To mitigate this, a lot of solutions have been proposed, some more effective than others. The aim of this project is to measure the effectiveness of these strategies and employ the ones with the most promising results [3, 4].

1.1 Problem Statement

To analyze a patient's response to pain (either nociceptive or tonic), the following factors are examined:

- Notable past, present or continuous pain and its impact on the patient.
- Pain sensitivity.
- Effective methods used by the patient to control pain
- Patient's history with medication.
- The typical way that the patient copes with pain.
- A patient's behavior when in pain.

Adding to this, various pain assessment tools have been successfully employed. Of these tools, the best features have been integrated onto our model to make it efficient [5, 6].

1.2 Physiological Indicators of Pain

Pain acts as a vital indicator of internal issues. It could range from mild pain to one that causes major distress, severely affecting the quality of life. Chronic pain is categorized as one that lasts for over 3–6 months and can be a consequence of a disease or a disease in itself, like in the case of Fibromyalgia (FM). Pain in circumstances like these can be a useful biomarker for disease [7, 8]. The space of accessible pain

assessment tools and resources represents a diverse array of alternatives that can be used to address the multifaceted nature of pain. Patients lack a comprehensive report on the frequency and intensities of the pain, hence putting the burden of data collection and analysis on the medical staff. Lack of a consistent dataset to back patients' claims result in inaccurate diagnosis leading to insufficient therapy.

1.3 Pain and Its Assessment

Pain can alternatively be classified as nociceptive (induced by the excitation of sensory nerve fibers), neuropathic (caused by a malfunctioning somatosensory nervous system), or psychogenic (induced by psychological factors). What you find excruciating may be merely irritating to someone else. Another factor that makes its assessment harder is the inaccuracy of patients' pain recall, as it is a possible impediment to reliable assessment of temporal characteristics of pain [9, 10]. For example, when asked to recall pain experienced in the last week, patients' recall is heavily influenced by the worst pain they had during that time and the most recent pain they encountered. Pain also happens to be one of the most prevalent reasons for medical visits according to W. H. Cordell. It is also a reliable factor to determine underlying issues and is also a reliable symptom of diagnosis. Given the importance of this subjectively reported condition, multiple researchers have for long studied and devised means to standardize its measurement. This ongoing study aims to identify reliable means of pain measurement by combining subjective reporting with EEG and HRV body sensors to determine a reliable benchmark of the pain experienced [11]. To effectively optimize treatments, a comprehensive understanding of residual nociceptive pain processing is important. Pain is a serious concern that might provoke severe internal intricacies. The Joint Commission on Accreditation of HealthCare Organizations proposes that as a vital symptom, pain should be considered accordingly, and it must be monitored at regular intervals for future exigencies. For instance, in one of the case studies done, if the patient is experiencing pain at a high frequency and this isn't resolved swiftly, it will take him longer than usual time to recover. Prolonged pain can easily induce feelings of fear and anxiety in patients, thereby increasing the prevalence of complications and might as well advance to incessant pain. A deliberate and detailed analysis calls for a credible and an intensive Pain Evaluation technique. Furthermore, pain assessment serves a variety of other purposes, including recording the intensity of chronic medical conditions, monitoring the pain's temporal course and generating the neurobiological data. Various categories of pain, such as the sensory and cognitive elements of pain, behavioral aspects of pain, as well as the position and corporeal distribution of pain must all be considered in a comprehensive pain evaluation. Tools for identifying the pathological conditions underlying the pain should be included in the pain assessment [12].

1.4 Parameters Used to Indicate Pain

Heart Rate Variation (HRV). To determine the explicit components of a HRV reading that contributes to the detection of this, a group in 2017 employed heat stimulation to instigate pain in their test subjects.

Electroencephalogram (EEG). The use of continuous EEG has been utilized to see which EEG patterns are associated with experimentally generated pain. Normal pain measurement techniques like the NRS or VAS are not accurate in measuring pain as they have two variables to it. The degree of Celsius of a heat stimulation is an instance of noxious stimulus intensity. Subjective pain sensation, on the other hand, is quantified utilizing rating scales to rate subjective pain feeling on a scale [6].

The drop in alpha activity commonly reported in experimental pain research was found to correlate with only noxious stimulus intensity when measured using EEG readings, whereas subjective pain intensity was associated with an increase in gamma oscillations. The EEG reading's susceptibility to even the smallest scale of change makes it pertinent to discerning pain.

1.5 Body Sensor Networks for Pain

Objective evaluation of pain can be carried out using vital physiological signs, If we consider HRV, we can witness its dependence on the autonomic nervous system as it regulates heart rate. Multiple studies using body sensor networks, such as Heart Rate Variation probes, EEG/EMG/ECG probes have helped us find relations between pain experienced by subjects and their medical history. In cases such as Fibromyalgia and Gastrointestinal Pain, HRV can be correlated closely to find frequency of occurrence and EMG can be used to identify muscular stress. Utilizing the potential that sensor networks bring, coupled with IR Therapy and electrical stimulation, pain measurement and management can be made more accessible to the general public without putting pressure on the medical institutions.

1.6 Proposition

Our solution proposes an integration of BSN (Body Sensor Networks) and Machine Learning techniques to generate reports on pain frequencies and promotes active engagement of the patient with their body conditions. In addition, it also proposes IR Therapy and electrical stimulation to ease patients with chronic pain integrated into a material that can be worn by the end user. This project aims to act as a mediator between chronic pain patients as well as physicians in a manner that it reduces clinical intervention for tests, such that citizens become more aware of their health status and take on a proactive attitude towards it (Fig. 1).

Fig. 1 Prototype headband with Neurosky TGAM1 (EEG sensor)

2 Methodology

2.1 General Overview of the System

One possible method to help patients with chronic pain history or phasic pain stimuli to take proactive measures is to monitor the intensity and effect of pain. This can be executed by integrating existing sensor technologies available and categorizing diagnosis on the basis of medical history. This tool can also act as an indicator of abnormality by studying patterns of pain reception. The system also alerts relatives, caregivers, or health-care personnel of any change in the subject's normal activity pattern is shown in Fig. 2.

Combining the pain assessment from the sensor nodes from both the wearables, a pain intensity questionnaire will be initially asked to the user, where standard tests such as the visual analog scale (VAS) and McGill pain questionnaire (MPQ) will be displayed. A model will be generated on each user type, which has information of the user's medical history, especially in association to the chronic pain experience or phasic stimuli pain. The data that is generated will be sent to the local server to create a basic log of pain that can be used as a pain frequency report for the medical staff. The fluctuation and change in pain intensities based on the response of the HF/LF components will be noted and sent to the server for computation.

The user will have access to visual representation of pain accessible through his/her mobile application. The local server will notify caretakers of the user in the case of strong pain pangs based on the HRV. The user will have access to reports which will include the intensity, frequency and impact of the pain on the body with respect to muscular activity (accelerometer), lifestyle and medical history. Prediction based on pain trends will also be employed as a part of the project through study of the

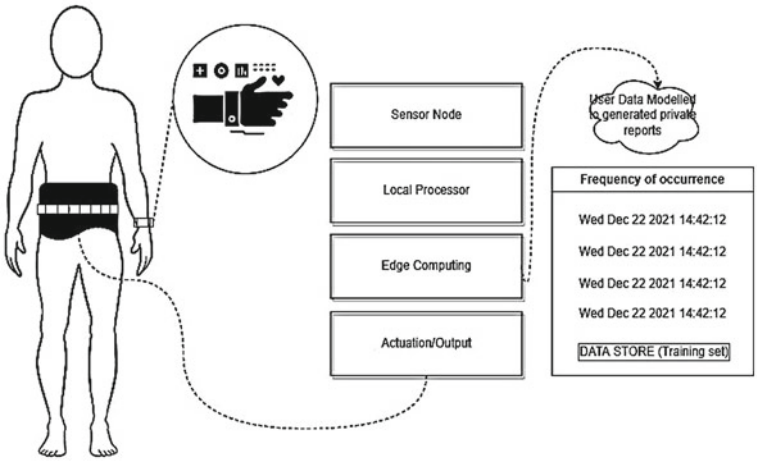

Fig. 2 General overview

user and comparing it with symptoms of other diseases that result in chronic pain. Differentiation between phasic and tonic pain will also be carried based on the data.

2.2 Components on the System

Local Processor—ESP32 WROOM DevKit: The ESP WROOM 32 is a potent, all-purpose WiFi-BT-BLE MCU module that can handle a wide range of functions. The ESP32S chip, which is made to be scalable and adaptive, lies at the heart of this module. The clock frequency of the two CPU cores, which can be adjusted from 80 to 240 MHz, can each be individually controlled or powered. The CPU can be turned off if the user prefers, and the low-power coprocessor can be used to continuously check the peripherals for changes or the crossing of thresholds.

Neurosky's Think Gear ASIC Module (TGAM1): It is a member of the Think Gear AM Product Family, where A stands for ASIC and M for Module. The chip has a model number of TGAM1, revision number 2.3. The device is protected at 4 kV for contact discharge and at 8 kV for air discharge. The system is capable of serial communication at baud rates of 9600, 1200, and 57,600 bps. There are pins for setup that allow us to alter the baud rate. Additionally, this TGAM1 chip can only handle one EEG input, and we only need to process one EEG channel, thus using this chip makes sense. This Sichiray development kit comes with the TGAM1, HC05 Bluetooth module, a battery holder and contact clips as well as the contact electrode.

ECG Pulse Sensor. A pulse sensor is a plug-and-play sensor which gathers heart rate data. By directly connecting to an ESP32 board, this sensor attaches onto the finger-tip.

2.3 Procedure

Using data mining techniques, the obtained data can be utilized to assess and predict chronic ailments or other diseases such as heart attacks in the basic stages, making the approach more advantageous for decision making. This module focuses on the procedures to take after a patient's health has been found abnormally, such as notifying his or her family as well as the hospital. In our application, we'll put up specific threshold values that, if exceeded, will send an alarm to the patient's family and doctor. The process is depicted in Fig. 3.

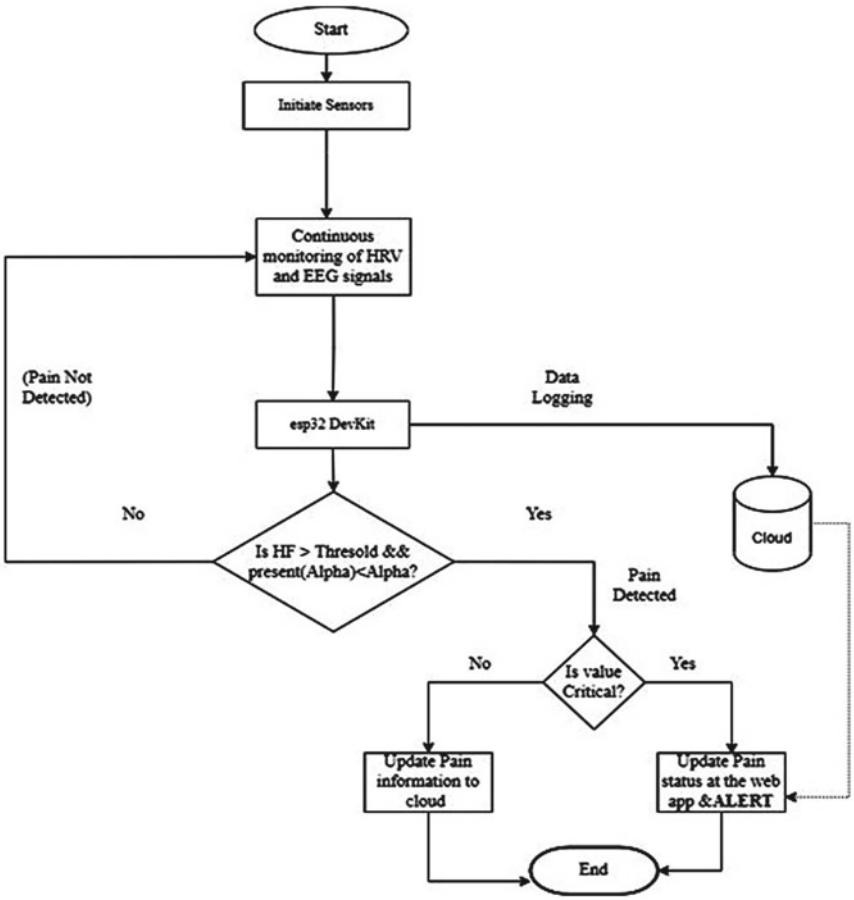

Fig. 3 Flow of processing pain instance

2.4 Edge Computing

The first part includes assignment of board pin values to the respective variables (*LED*, *BAUDRATE*, *DEBUGOUTPUT* and *powercontrol*) along with variables to cross verify the streamed data such as *payloadlength* etc. This is followed by the default setup () code, where the serial data stream is set to a baud of 57600. This is the default baud rate of the TGAM1 module, hence the same is set in the code. The next piece of code reads data streamed to the board through Bluetooth using the *ReadOne-Byte()* function and checks if the serial port is available (or receiving data).

In the next part, we are interested in 8 parameters that the raw data offers, delta, theta, low/high alpha, beta and gamma. That is why we assign the values as unsigned int. There are two function definitions in this code, one to extract the 3-byte data for each parameter and the second one to defining how the 3 bytes are extracted from the data stream. The *loop()* function repeats the entirety of the code within the function until termination. First, we have to check if the payload length is 170, this step is crucial as per documentation. The byte data is fed to an array called *payloadData.* The data is then read to memory using the *generatedChecksum* variable. We then declare 3 new variables*, poorQuality, Attention and Meditation. poorQuality* is set to 200 because that's the default disconnected value. The next steps include parsing of data which takes place using a switch case, where 5 cases are present each checking for a particular value in the payload data. In the 4 cases one includes checking for *poorQuality*, default attention and meditation values, followed by raw data and the six parameters of brain data. Specific to each character placement, the index variable is incremented in each case.

The last part of the code is used to print the values on the serial monitor. Recording of these serially streamed data from the COM port can take place using Tera Term as well, which is a useful software to log serial data.

3 Results

Using just HRV as a parameter was not effective enough to yield the results we were expecting. We were also unable to narrow down on a threshold as the HRV is extremely susceptible to any form of external stimulus, making it an unreliable indicator of pain albeit an important one in conjunction with other factors. The TGAM1 Module gave us raw data which the most promising results were obtained by a dip in the Delta values to a negative number. This has by far been the most important finding in both the research and implementation of the project. Currently data aggregation is underway in the form of datalog.txt files which are being streamed using bluetooth. Every instance of pain caused reduction in delta values and will be mapped to various case studies such as chronic joint disease, posture related pain and tonic pain. This setup will be improved further to relay data to our own application

Fig. 4 Proof of concept headband on team member

and include ECG readings to predict pain pangs is depicted in Fig. 4. The critical value threshold will be identified through further research.

4 Future Scope

The main motivation for this paper is to help alleviate patients of costly clinical support, overcome doctor shortages, and thus provide hassle-free care and services to patients, enabling data exchange between doctors and patients or between organizations, lowering costs and expanding the scope and reach of medical facilities especially for patients with chronic pain. Our project aims to identify major pain pangs and its frequency to at least an 80% accuracy and produce comprehensive reports that can be used by both the users and medical staff. With a focus on the modularization of the hardware and seamless time stamped reporting of pain on our app, we plan to further refine the project to be readily available in the market in the next two years. These two years will also see a boom in wearable technology with properties akin to the skin, further enabling our product to be even smaller and more compact, giving the end user a comfortable, non-disruptive wearable experience.

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Design and Analysis of Miniaturized Broadband Microstrip Patch Antenna for Aircraft Surveillance Applications

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Abstract In this work, a miniaturized, broadband, coaxially fed rectangular microstrip patch antenna (MPA) is designed for the traffic alert and collision avoidance system (TCAS) application. The TCAS is a legally mandated aircraft surveillance system that is installed in all aircraft to prevent accidents. A novel structure is proposed to minimize the overall size of the conventional TCAS antenna while increasing the bandwidth (BW). Many methods, such as multiple symmetrical slits, parasitic patches, and defects on the ground structure, have been incorporated into the conventional design to achieve miniaturized broadband antenna. The proposed antenna structures are designed and simulated using the High-Frequency Structure Simulator (HFSS) software. For the proposed design, antenna parameters such as impedance, VSWR, BW, reflection coefficient, gain, and radiation pattern are evaluated. The conventional antenna resonates at 1.06 GHz with 31.30 MHz BW (1.07–1.04 GHz), VSWR of 1.18, and a maximum gain of 4.68 dB, whereas, the proposed TCAS antenna operates at 1.07 GHz with 75.4 MHz BW (1.1–1.03 GHz), VSWR of 1.12, and a maximum gain of 3.31 dB. In the proposed design, the antenna gain is reduced by 1.38 dB, and it is mainly due to the reduced antenna size. The proposed antenna has improved the impedance BW from 31.3 to 75.4 MHz, which is more than double the BW of a conventional antenna. Furthermore, the overall antenna size

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has been reduced by 30.77%, making it an excellent choice for aircraft surveillance/TCAS applications.

Keywords Single band · Patch antenna · Miniaturization · Broad bandwidth · Defected ground structure · Symmetrical slits · Parasitic patch

1 Introduction

In the modernized wireless communication system (WCS), the microstrip patch antennas (MPAs) plays a very important role. The MPA has many attractive characteristics, including its low cost, lightweight, low profile, and ease of fabrication. As a result, MPAs are extensively used in various fields including radar technology, biomedical research, space science, military, aircraft safety, and so on.

In a MPA, both the radiating patch and the ground surface function as capacitors, hence the energy stored inside the antenna is proportional to the capacitor volume, which corresponds to the ground plane area. Thus, as the size of the ground surface increases, so does the stored energy, which raises the Q-factor, because the Q-factor represents the number of times the reserved system energy exceeds the dissipated energy. Since the bandwidth (BW) is inversely proportional to the Q-factor, increasing the ground plane size narrows the BW. As a result, the overall BW of an antenna designed for very low frequency (where the size of the ground surface increases with decreasing frequency) applications is extremely narrow, making BW enhancement a major consideration.

In addition to the aforementioned disadvantage, the size of MPAs is also a significant limitation when the antenna is designed for relatively low operating frequencies. For applications such as TCAS, where the operating frequency is 1.06 GHz, the maximum size of a single patch antenna element can theoretically be 141.5 mm ($\lambda/2$), which is significantly larger. Hence, the larger size and confined impedance BW are major drawbacks of the conventional patch antenna, especially for low operating frequency applications like TCAS. As a result, the design of a compact, broadband MPA is a critical component of TCAS applications. Wider BW is especially important in aircraft surveillance applications to improve airspace efficiency, channel capacity, and to increase surveillance over a larger area.

In the previous literature, different methods have been utilized to enhance the BW and to reduce the antenna size. In [1] a rhombus-shaped single complementary resonator (CR) is etched on the ground plane right beneath the microstrip feed line to enhance the BW of the MPA. The presence of CR as a defect will excite the new resonance by interacting with the feed line. By using this method, the overall BW of the antenna was increased by 200% with strong magnetic coupling. A simple way to augment the BW of the MPA is by increasing the thickness of the substrate [2]. However, increasing the substrate thickness introduces spurious feed radiation and surface wave. In [3], the above mentioned drawbacks were minimized by increasing the substrate thickness at the center of the patch antenna towards the vertical profile

using a circular pattern and gradually decreasing the thickness on either edges of the patch. Shorting pins are utilized in [4] to increase the BW of the MPA; in this work, the proper placement of shorting pins proximally allocated the TM10 and TM30 modes, which aided in increasing BW while maintaining a stable radiation pattern. Two folded shorting probes are diagonally placed on the patch to improve antenna BW while maintaining the same size in [5]. The addition of shorting pins divided the TM10 mode into two secondary modes, TM10+ and TM10−, which were then combined to improve BW in the aforementioned work. A merged U and T shape patch with stair shape defect is used in [6] to achieve 107.35% improvement in the antenna BW. In reference [7], a M-shaped radiating patch having U-shaped defect on the ground surface has been proposed for achieving broadband antenna. To improve antenna BW, several designs with modified patches and different shape defects, such as crescent shape [8], X-shape with asymmetric edges [9], tapered shape [10], square slot [11], rectangular slot [12], U slot [13], and so on, were proposed. Other techniques for increasing antenna BW include stacked patch [14–19], parasitic patch [20-22], slit and stub combination [23], differential feed [24], and low dielectric constant substrate materials [25].

In this work, a miniaturized, broadband MPA is proposed for the TCAS applications. To minimize the antenna size, the combination of asymmetric and symmetric slits are etched on the radiating patch. Later, methods such as parasitic patch and defects in the ground structure are used to improve the BW. The proposed design allows for an increase in impedance BW from 31.3 to 75.3 MHz, which is more than double the BW of a conventional TCAS antenna. Additionally, the proposed TCAS antenna (90 mm × 80 mm) is 30.77% smaller in size than the conventional antenna (130 mm × 111 mm).

2 Proposed Antenna Designs

In this Section, the design procedure and simulated structure of the conventional patch antenna followed by the proposed miniaturized broadband patch antenna designs are discussed.

2.1 Methodology

Before designing an antenna, many parameters must be thoroughly studied, including shape, size, cost, and application, among others. In our work, antennas are required for aircraft surveillance applications; thus, performance, rigidity, and low loss are more important than cost. Considering the aforementioned factors, the RT/Duroid 5880 substrate material was chosen for designing the TCAS antenna. The substrate material was compared to FR4, which is a common material for antenna design. In comparison to FR4, the RT/Duroid material has provided more than 45% higher

gain and approximately 40% better efficiency while maintaining the same reflection coefficient [26]. Furthermore, the RT/Duroid has the lowest electrical loss, the least moisture absorption, uniform electrical properties across the entire frequency band, excellent chemical resistance, and is very rigid. The rectangular patch antenna operating at 1.06 GHz central frequency is initially designed in our work using the standard formula. Later, the overall antenna size was reduced by employing symmetrical slits, a square parasitic patch, and asymmetrical defects on the ground surface.

2.2 Conventional Patch Antenna

Figure 1 depicts the top and ground plane of the conventional patch antenna operating at 1.06 GHz central frequency suitable for TCAS/Aircraft surveillance applications. The RT/Duroid 5880 with 2.2 relative permittivity ε_r, 0.0009 loss tangent (tan δ), and 3.175 mm thickness is used as the substrate material to design both conventional and proposed antennas. Rectangular patches are widely used for many fields since the configuration is easy to understand and fabricate, hence in our study a rectangular shape patch is designed. The following procedure is used to find the dimensions of the antenna.

To achieve excellent radiation efficiency from a rectangular radiator, the practical patch width should be approximately 'W_P' and it is calculated as follows [27].

$$W_p = \frac{c}{2f_0\sqrt{\frac{\varepsilon_r+1}{2}}} \tag{1}$$

Where, c is light wave velocity travelling in free space (3×10^8m/s), f_0 is the operating frequency (1.06GHz), and ε_r the substrate dielectric constant (2.2). By substituting the aforementioned values in Eq. (1), the patch width (W_P) of 111.87 mm is obtained. The effective patch length (L_{eff}) is determined by the effective dielectric constant (ε_{reff}) and is given by.

$$\varepsilon_{reff} = \left[\frac{(\varepsilon_r+1)}{2} + \frac{(\varepsilon_r-1)}{2}\left(1+12\frac{h}{W_p}\right)^{-1/2}\right] \tag{2}$$

Where h stands for substrate height (3.175 mm). The calculated ε_{reff} is 2.12, which is less than ε_r.

Equations (3–5) are utilized to evaluate the parameters 'L_{eff}', normalized extended length after accounting for the fringing effect (ΔL), and actual patch length (L_P), respectively. After assessing the expressions below, the values 97.20 mm, 1.58 mm, and 94.04 mm are recorded for 'L_{eff}', 'ΔL', and 'L_P', respectively.

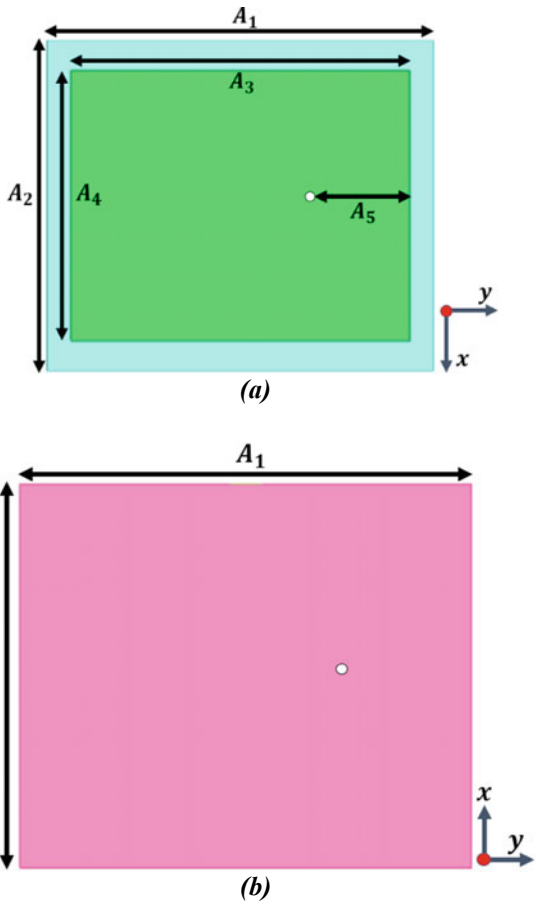


Fig. 1 The Conventional Patch Antenna (CPA) **a** Coaxial fed CPA (Top-view) **b** Ground surface (Bottom-view)

$$L_{eff} = \frac{c}{2f_0\sqrt{\varepsilon_{reff}}} \tag{3}$$

$$\Delta L = 0.412\,h\frac{\left(\varepsilon_{reff}+0.3\right)\left(\frac{W}{h}+0.264\right)}{\left(\varepsilon_{reff}-0.258\right)\left(\frac{W}{h}+0.8\right)} \tag{4}$$

$$L_p = L_{eff} - 2\Delta L \tag{5}$$

After defining the patch antenna dimensions, the overall dimensions of the substrate can be estimated using Eq. (6).

$$L_s = 6h + L_p \; and \; W_s = 6h + W_p \tag{6}$$

Table 1 Optimal physical dimensions of designed antenna structures

Parameter	Dimension (mm)	Parameter	Dimension (mm)
A_1	130	A_{11}	8
A_2	111	A_{12}	7.5
A_3	114	A_{13}	8
A_4	91	A_{14}	23
A_5	24	A_{15}	1
A_6	90	A_{16}	6
A_7	80	A_{17}	5
A_8	3	A_{18}	10
A_9	2	A_{19}	5
A_{10}	10		

The calculated values for length and width of the substrate are 112.04 and 129.87 mm, respectively.

Table 1 summarizes the optimal antenna dimensions for obtaining a resonating frequency of 1.06 GHz. The simulated results of the conventional antenna design is illustrated in Fig. 2. The impedance of 49.87 Ω, as shown in Fig. 2a, is very close to the ideal value (50 Ω), ensuring that the antenna operates efficiently over the intended frequency band. The conventional antenna, as shown in Fig. 2b, resonates at 1.06 GHz with −19.68 dB reflection coefficient, and an overall bandwidth of 31.30 MHz (1.07–1.04 GHz).

2.3 Evolution of the Proposed Antenna

In this section, the various techniques utilized to achieve the miniaturized, wideband antenna suitable for TCAS applications are thoroughly explained.

Initially, the size of the conventional TCAS antenna has reduced by 30.77% (from 130 mm × 111 mm to 90 mm × 80 mm) as depicted in Fig. 3 (STEP 1), and the miniaturization has really impacted the resonating frequency, BW, and gain of the MPA. In STEP 1, the reduced size has shifted the resonating frequency from 1.06 to 1.2 GHz, BW from 31.3 to 21.5 MHz, and overall gain from 4.68 to 3.3 dB. Increasing the patch length is the simplest way to lower the resonating frequency of the patch antenna. Hence, in STEP 2, three symmetrical slits are initially etched on the left edge of the radiating patch to increase the length and facilitate more current flow. The addition of these slits reduced the resonating frequency from 1.2 to 1.15 GHz without affecting other antenna parameters.

A parasitic element is basically a passive conducting element/radiator that is not connected directly to the active radiator/patch but is positioned in close vicinity to it. The placement of the passive radiator will disturb the symmetric radiation pattern of the patch, which in turn influences the polarization effect of the radiation field.

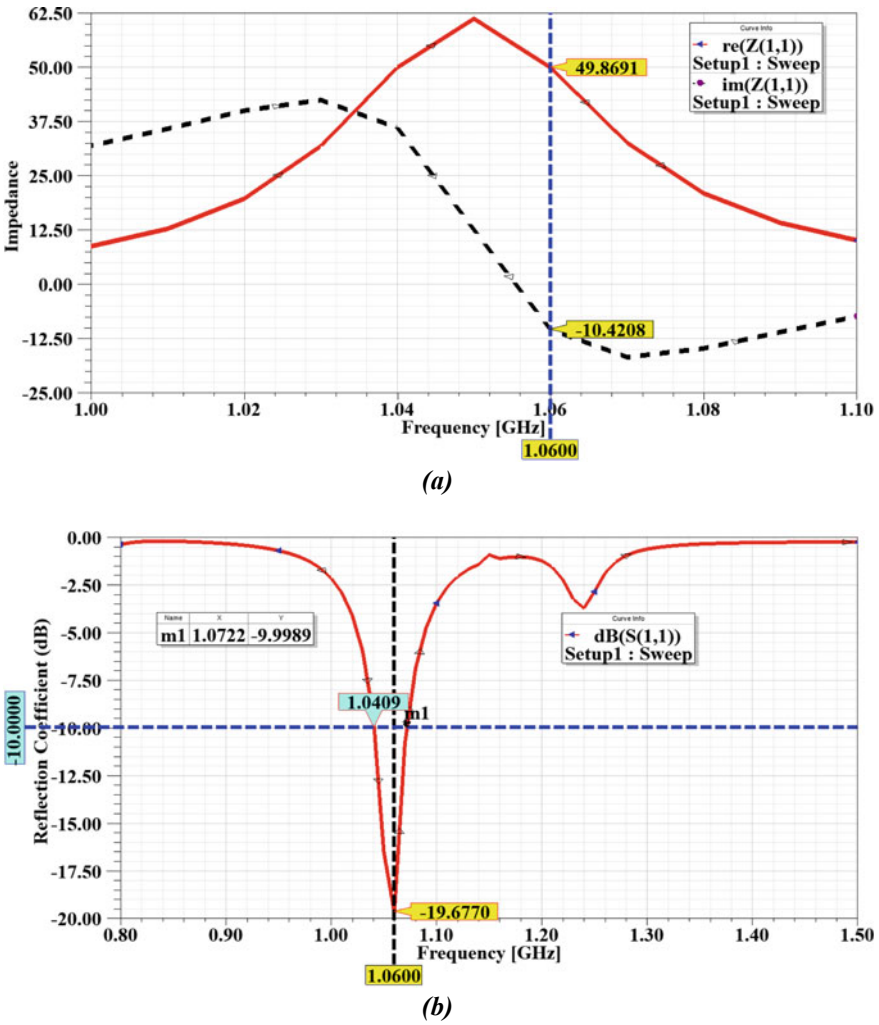


Fig. 2 The simulated results for the conventional antenna **a** Impedance plot (IP) **b** Reflection coefficient plot (RCP)

The effect on polarization causes excitation of a pair of degenerate modes (DM), which broadens the bandwidth and shifts the operating frequency. In STEP 3, a small square parasitic patch with asymmetric slits are added, and these substitutions have increased the BW by 20.2 MHz while lowering the resonating frequency to 1.08 GHz from 1.18 GHz. Furthermore, to reduce the resonating frequency, and to further improve the BW of the antenna, small asymmetric defects are etched from the ground surface in STEP 4. The excitation and propagation of electromagnetic (EM) waves through the substrate is controlled by defects in the ground plane. The shape and size of the defect have a significant impact on the uniform distribution of

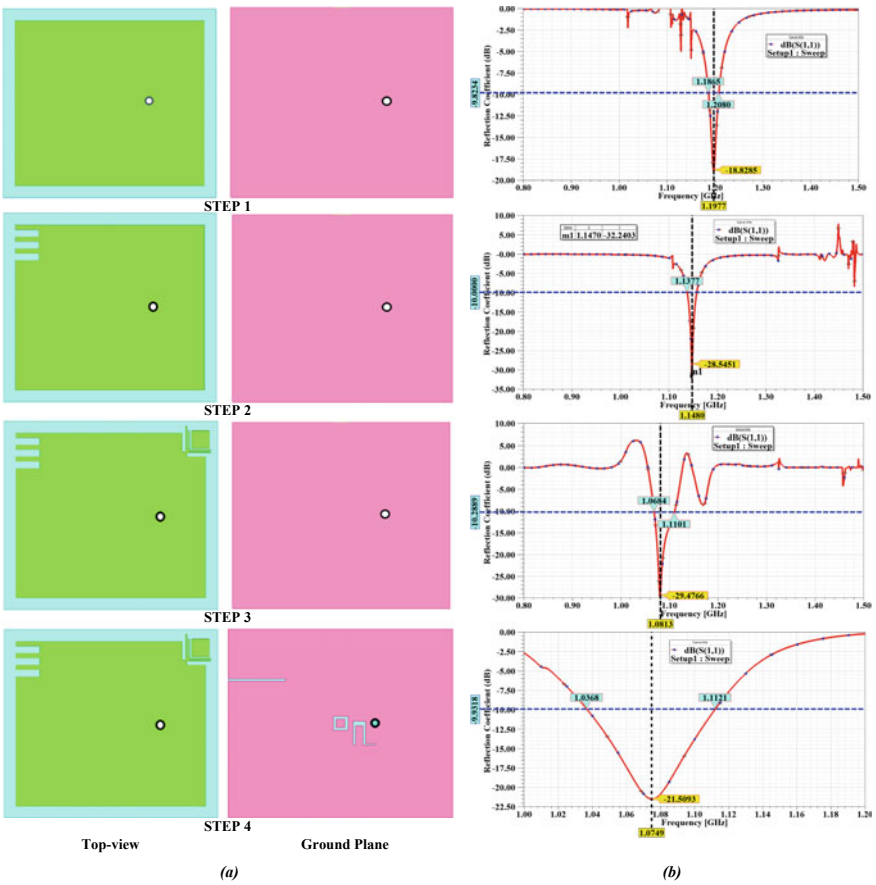


Fig. 3 **a** Evolution of the proposed antenna structure **b** Reflection coefficient plot of each stage

the shield current. The inclusion of the defect has improved the BW up to 53.8 MHz while shifting the resonating frequency to 1.07 GHz.

2.4 Proposed Miniaturized Broadband TCAS Antenna

This section describes the proposed antenna for TCAS applications. As depicted in Fig. 4, a combination of asymmetrical slits, slots, a small square parasitic patch, and defects on the ground layer are used to design the miniaturized, wideband antenna for the TCAS applications. In surveillance applications where effective scanning of the entire 360° azimuthal plane is required, a multi-feed antenna (either tri-feed or quad-feed) placed in a circular fashion is necessary. As a result, the size reduction of a single antenna element allows for the accommodation of multi-element antennas in a

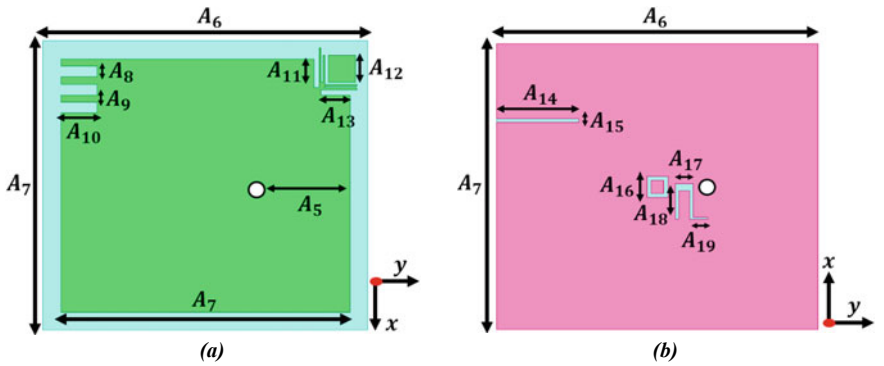


Fig. 4 The proposed TCAS Antenna **a** Coaxial fed RMPA (Top-view) **b** Ground surface (Bottom-view)

small substrate material. Since the proposed antenna has reduced its size by 30.77%, the overall size of the substrate material required has been reduced by nearly half, making the proposed antenna compact and cost effective.

Aside from miniaturization, achieving wider BW for low operating frequency is always a challenge, but it is required to improve channel capacity, broaden the surveillance region, and improve airspace efficiency. The proposed antenna increased the BW up to 75.4 MHz, a significant improvement for lower frequency applications.

The impedance plot for the proposed antenna is depicted in Fig. 5. At 1.07 GHz, an impedance of 58.44 Ω is noted, which is slightly deviated from the ideal value (50 Ω) due to mismatching. The proposed antenna resonates at 1.07 GHz, with −21.51 dB reflection coefficient, and an overall BW of 75.4 MHz (1.11–1.03 GHz) as shown in Fig. 6. The simulated gain value for the proposed antenna is 3.31 dB, as depicted in Fig. 7. In comparison to conventional antenna BW (31.3 MHz), the proposed design has increased the BW up to 75.4 MHz, which is a significant improvement for TCAS applications. Because antenna gain is directly proportional to total antenna dimension, miniaturizing the conventional antenna from (130 mm × 111 mm) to (90 mm × 80 mm), or 30.77% smaller in size, reduced antenna gain from 4.68 to 3.31 dB. There are numerous techniques for increasing antenna gain [28, 29], so in the future, the gain can be increased using the available methods.

The current distribution of the conventional TCAS antenna is depicted in Fig. 8. On the radiating patch, current flows outward from the coaxial feed and is uniformly distributed around the feed (Fig. 8a). The current density is extremely high on both sides of the patch antenna. The current distribution over the proposed TCAS antenna is depicted in Fig. 9, where the effect of symmetrical slits, slots, and parasitic patch can be thoroughly examined. The addition of these has completely changed the current flow direction, increasing current density, particularly on either side of the radiator. The addition of defects to the ground surface, as shown in Fig. 9b, has significantly increased the current flow density on both sides.

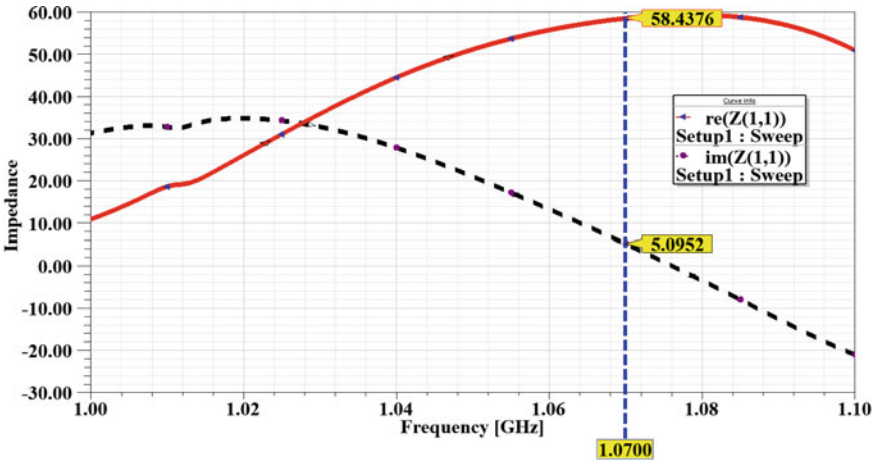


Fig. 5 Simulated impedance plot

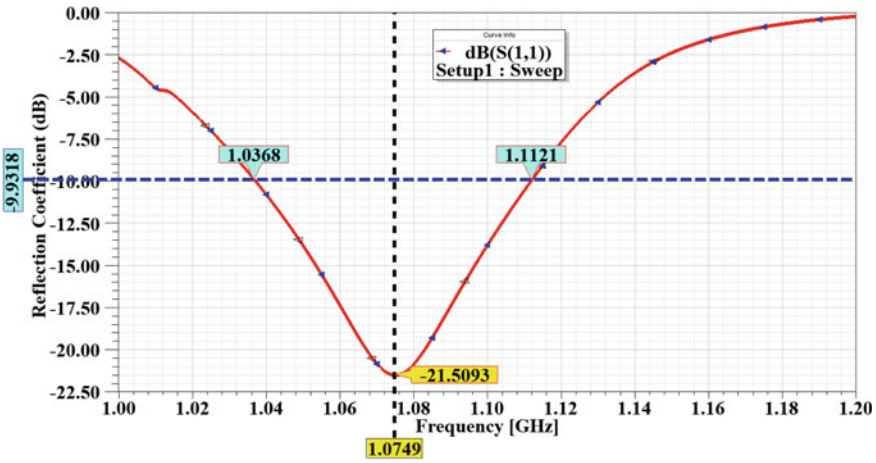


Fig. 6 Simulated reflection coefficient plot

The radiation plot of an antenna discusses the radiation properties/propagation characteristics in the far-field region with reference to azimuth angle (ϕ) and elevation angle (θ). The H-plane ($\phi = 90^0$) and E-plane ($\phi = 0^0$) radiation pattern of the proposed TCAS antenna is illustrated in Fig. 10. The 3D radiation pattern of the proposed TCAS antenna is depicted in Fig. 11. The 3D plot is placed on the proposed antenna structure to understand the radiation direction and distribution. The maximum radiation propagation can be observed along the positive z-axis, and the presence of small defects on the ground surface will slightly impede current flow, resulting in minor radiation propagation along the negative z-axis.

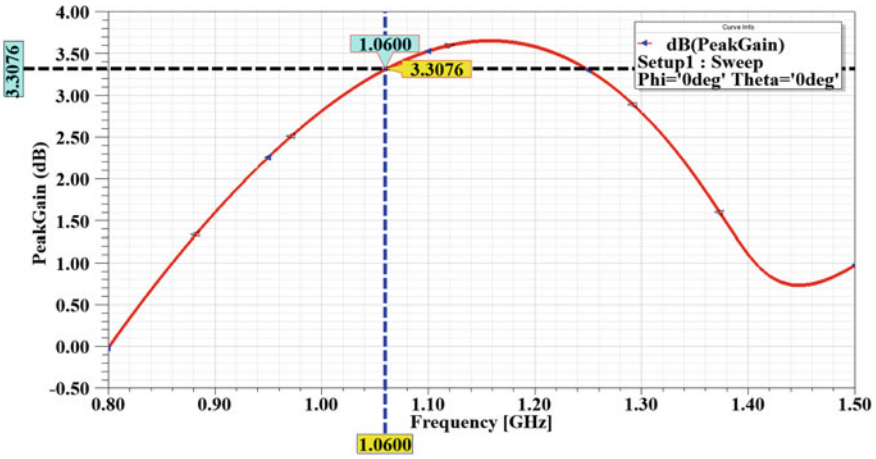
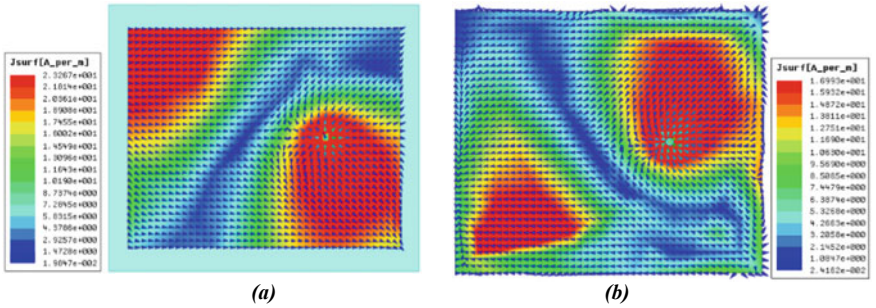
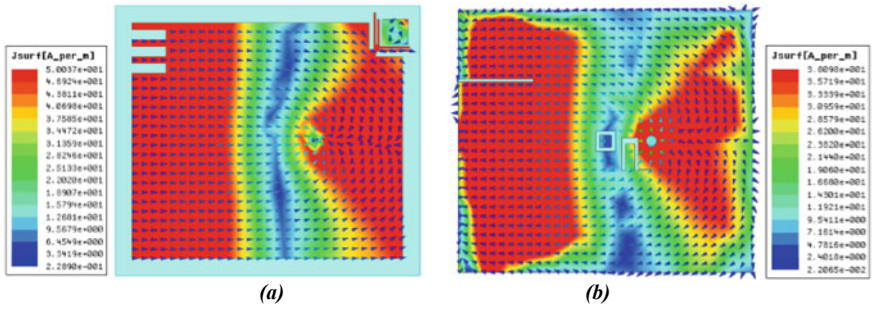


Fig. 7 Simulated gain plot



(a) *(b)*

Fig. 8 Current distribution inside conventional TCAS antenna



(a) *(b)*

Fig. 9 Current distribution inside proposed TCAS antenna

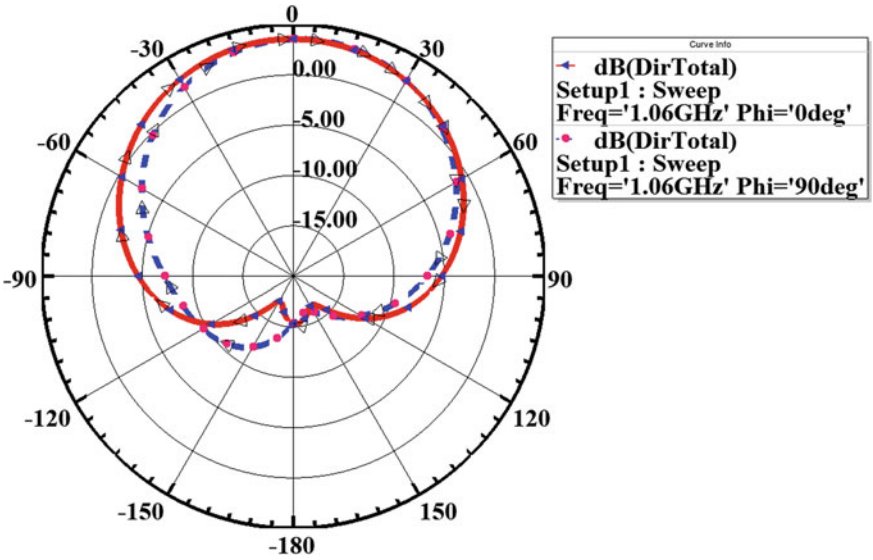


Fig. 10 Radiation pattern at 1.06 GHz (Proposed antenna)

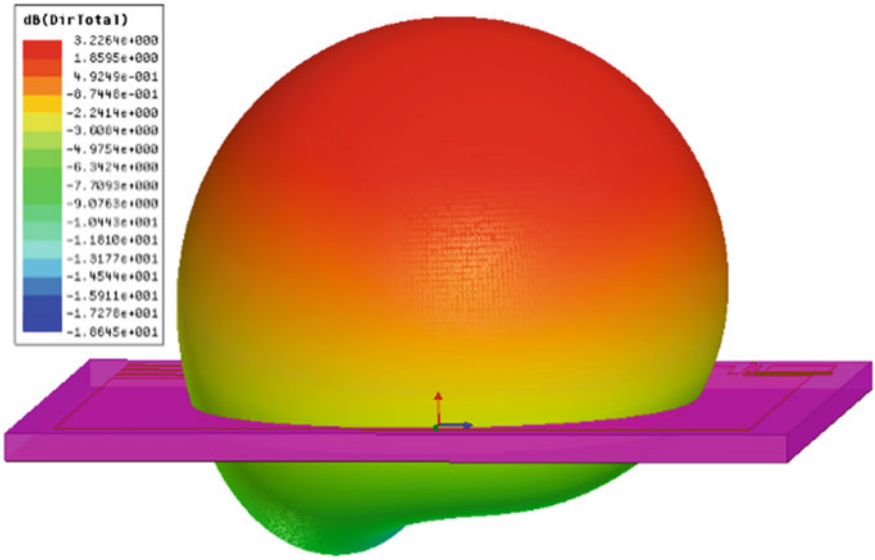


Fig. 11 3D Radiation pattern at 1.06 GHz (Proposed antenna)

3 Conclusion

For airborne surveillance or TCAS applications, a rectangular patch antenna with symmetrical and asymmetrical slits, a parasitic patch, and small defects on the ground surface is proposed. In comparison to the conventional TCAS antenna, the proposed antenna has reduced the overall size of an antenna by 30.77% while covering the frequency band from 1.03–1.1 GHz (BW of 75.4 MHz), which is 44.1 MHz (1.04–1.07 GHz) more.

In surveillance applications, a multi-feed antenna (tri-band or quad-band) is required in order to effectively scan the entire azimuthal plane. As a result, miniaturization of a single element antenna allows multi-feed antennas to be accommodated in a fixed substrate size. In addition to miniaturization, a larger BW is essential for increasing airspace efficiency, channel capacity, and to cover a relatively larger surveillance region. Hence, the proposed miniaturized, wideband antenna is best suited for TCAS applications.

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