



# Design and Implementation of FFT Based Fast Acquiring of High Dynamic GPS Signal Based on FPGA

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**Abstract.** For the high dynamic GPS receiver, the system key technology is to acquire the PN signal. The high dynamic characteristic of the system refers to that the radial distance and rate between the navigation satellite and the receiver result in the GPS signal phase delay and Doppler frequency shift, which makes signal acquiring more difficult. It needs a long acquiring time when using the general slippage correlation acquisition method. In order to improve the acquiring performance, a FFT based acquiring method is analyzed, the implementation based on FPGA is introduced. By using the high dynamic GPS signal generator to conduct experiments, the availability of the method is proved. Additionally, the improving measures are presented.

**Keywords:** Doppler Frequency Shift · Signal Acquiring · FFT

## 1 Introduction

Signal acquiring is to estimate the pseudo-code phase and Doppler frequency shift of the received signal, and to initialize the track loop with such estimations. For the PN signal acquiring, slippage correlation acquisition method and matched filter method are usually adopted [1, 2]. It needs a long time to acquire signal by the slippage correlation acquisition method due to pseudo-code cycle time, resulting from the method of time domain and frequency domain serial search that related to the phase of each frequency point. To some extent, a matched filter can achieve parallel computing, not affected by pseudo-code cycle time, but it takes up a lot of hardware resources. Therefore, this system adopts the domain FFT based parallel algorithm for signal acquiring.

## 2 Basic Algorithm

C/A code acquiring in the slippage correlation acquisition method refers to a code related process in time domain, this process can also be carried out within the frequency domain. That is, it can be faster to adopt FFT based acquiring algorithm.

Provided that sampling interval ( $\Delta t = t_{k+1} - t_k$ ) is a fixed constant, the GPS after inputting signal sample can be represented as [3],

$$z[n, \hat{\omega}] = I + jQ = \sum_{k=0}^{L-1} y_k CA_{k-n} \exp\{-j[(\omega_{IF} - \hat{\omega}D)t_k]\} \tag{1}$$

whereas, n refers to serial number of code starting time  $\hat{t}_{s(n)} = t_0 + n\Delta t$ , namely the code phase;  $CA_{k-n} = CA\{[1 + \eta(k - n)\Delta t]\}$  refers to signal sampling form of pseudo code.

When local carrier frequency is fixed, that is, one Doppler frame is selected [4, 5],  $z(n, \hat{\omega}D)$  can be calculated according to the code phase n, i.e.  $z(0, \hat{\omega}D), z(1, \hat{\omega}D), \dots, z(L - 1, \hat{\omega}D)$ . According to the convolution theorem, we can get the Formula (2):

$$Z = IFFT(Y * C) = IFFT \begin{bmatrix} C_0 Y_0 \\ C_1 Y_1 \\ M \\ C_{L-1} Y_{L-1} \end{bmatrix} \tag{2}$$

The above formula applies the cycle characteristic of the C/A code, namely  $CA_K = CA_{L+K}$  where L is the C/A code cycle [6]. The maximum value of k is the estimated value of  $t_s$ .

Therefore, frequency domain FFT based acquiring algorithm is to realize the parallel acquisition of PN code phase and Doppler frequency shift according to the property of inverse transform that the convolution in time domain is equal to the multiplication in frequency domain [7].

Figure 1 shows FFT based fast code acquiring circuit diagram in frequency domain.

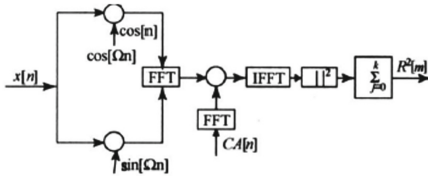


Fig. 1. FFT based fast code acquiring circuit diagram

### 3 Implementation

Based on the above algorithm analysis, this paper designs a more practical engineering application. See hardware function module for FFT based acquiring in Fig. 2.

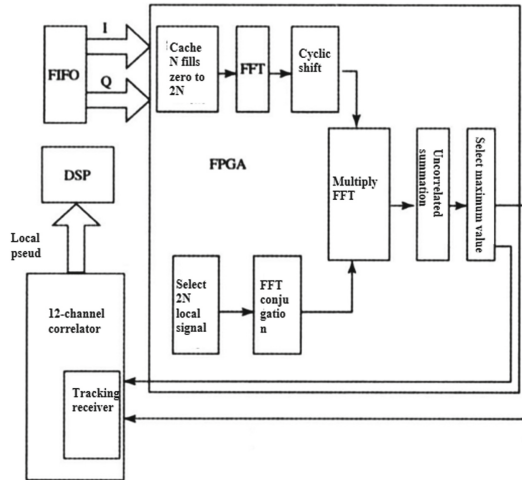


Fig. 2. Hardware function module for FFT based fast acquiring

### 3.1 Data Storage and FFT Arithmetic (FPGA)

Due to the larger scale of the system signal processing with high speed and high precision, system adopts FPGA chip (Vertex2XC2V3000), which can realize large-scale data parallel processing and meet the requirement. In addition, the FPGA has outstanding performance on flexibility and extensibility. FIFO chip is adopted for external storage, which avoids the short of the FPGA storage space and achieves the high-speed data transmission.

### 3.2 FFT Scheme Design

Based on the unit structure in Fig. 3, we can design a multi-point FFT or IFFT operation module. The Fig. 4. Shows the FFT module.

First of all, enter data ( $2N$  point) into the input data memory. These data can be divided into multiple sets of 1024 points, and each set carries out FFT arithmetic through a corresponding 1024-point FFT processing core. For the first time after the 1024-point combined FFT computation, the result is stored in the output data memory. However, only when adjust the data storage order in the memory can we get the correct result for the next 1024-point combined FFT arithmetic. Thus, the data in the output memory of FFT processing unit can be reorganized by means of the address generator and introduced to the input data memory for the next FFT arithmetic. At the last time the computing results directly stored in the output data memory for the final output.

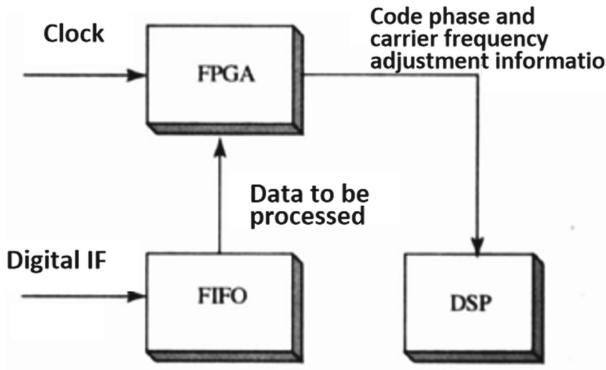


Fig. 3. Hardware structure for fast acquiring system.

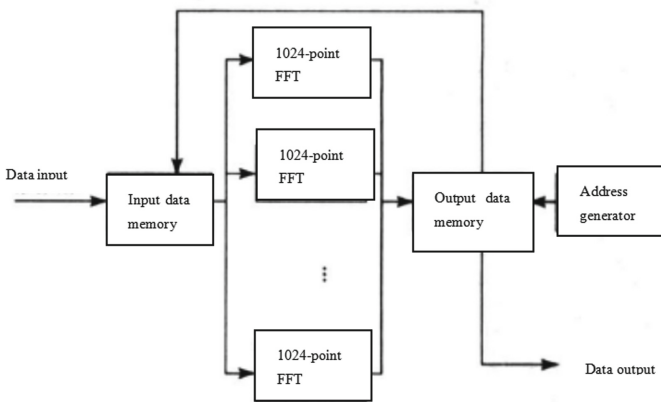


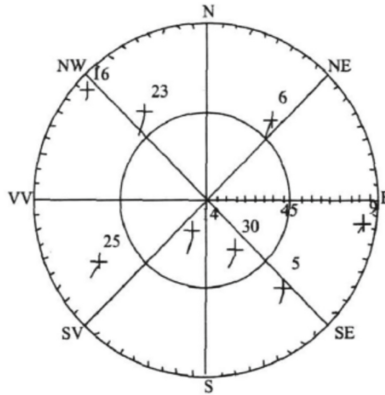
Fig. 4. FFT module internal structure in the fast acquiring system.

### 4 Algorithm Validation

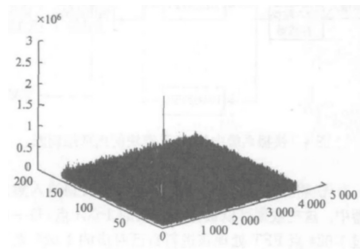
In order to verify the validity of the algorithm, high dynamic GPS test simulator is adopted. STR4760 GPS signal simulator, which can evaluate the high positioning precision of the dynamic user receiver, can be used for the test and validation of GPS receiver.

STR4760 technical indicators: relative speed between navigation satellite and users: 120000 m/s, accelerated speed: 360 g and 500 g/s acceleration; GPS signal source controlled by ALPHA workstation, reliable in performance. Visual satellite status diagram from the simulator is as shown in Fig. 5.

The algorithm hardware platform is used to search the entire range. See search correlation matrix for No. 5 GPS satellite (visual) in Fig. 6, a significant correlation peak can be observed.



**Fig. 5.** Visual satellite status diagram



**Fig. 6.** Search correlation matrix for No. 5 GPS satellite

## 5 Conclusion

In this paper, we discuss the hardware design of fast acquiring technology for GPS receiver and the detailed industry application of circuit for each part. Experiments show that if Doppler frequency shift is between  $\pm 50$  kHz and the shift length is 500 Hz, it takes 1.92 s ( $0.0096 \times 200 = 1.92$  s) to blind acquiring a satellite at most and takes up to 42 s to collect all the ephemeris. The new technology takes up to 1 min in positioning, which has greatly improved compared with the time consuming by original satellite-borne GPS receiver.

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