Research and Implementation of O-OFDM Transmission System Based on FPGA

Du Wu[1,2], Yupeng Li[1,2](✉), Qianqian Li[1,2], Xiaoming Ding[1,2], and Xiaocheng Wang[1,2]

[1] Tianjin Key Laboratory of Wireless Mobile Communications and Power Transmission, Tianjin Normal University, Tianjin 300387, China
fx_lyp@163.com

[2] College of Electronic and Communication Engineering, Tianjin Normal University, Tianjin 300387, China

Abstract. Orthogonal frequency division multiplexing (OFDM) can effectively eliminate the inter symbol interference (ISI) generated by the signal in the multi-path propagation. Using this feature, design an optical OFDM (O-OFDM) transmission system based on the field programmable gate array (FPGA), and give the system scheme and key technology implementation method. In the design, in order to effectively reduce the inter channel interference (ICI) and inter symbol interference, a cyclic prefix is introduced to avoid the influence of related interference through periodic convolution. At the same time, the training sequence (TS) is introduced in the design process for the relevant synchronous design and equalization processing, to reduce the complexity of the baseband system design.

Keywords: OFDM · FPGA · ICI · ISI · Cyclic prefix · TS

1 Introduction

OFDM is a modulation technique that can also be seen as a multiplexing technique. It is a special multi-carrier transmission scheme that is well able to combat frequency selective fading and narrowband interference. Its basic principle is to decompose a data stream transmitted in parallel into many low-rate sub-number streams and transmit them in parallel over multiple sub-channels. In 2005, N.E. Jolley and T.M. Tang et al. presented the first application of OFDM technology to fiber optic transmission systems at the OFC2005 conference and experimentally demonstrated that 10 Gb/s signals can be transmitted in multimode fiber transmission [1]. Since then, the research of optical orthogonal frequency division multiplexing technology has been started. O-OFDM has the advantages of high spectral efficiency, strong resistance to dispersion and outstanding effect of nonlinearity. Therefore, using the OFDM technology can effectively improve the anti-dispersion ability of optical fiber transmission system [2].

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O-OFDM systems can be divided into two categories according to the different detection methods at the receiver: direct detection optical OFDM systems (DDO-OFDM) and coherent detection optical OFDM systems (CO-OFDM) [3]. Among them, CO-OFDM has higher spectrum utilization and good receiver sensitivity, while DDO-OFDM system has simple structure, low power consumption and low cost. Considering the complexity of CO-OFDM structure, the structure used in this paper is DDO-OFDM system, and the design ideas of DDO-OFDM transmission system and FPGA implementation of baseband signal modulation and demodulation are elaborated.

2 The Design of DDO-OFDM Transmission System

A simple DDO-OFDM transmission system implementation is shown in Fig. 1. At the transmitter, the data to be transmitted is processed by FPGA to form OFDM data frames, however, the complex data output from IFFT to achieve optical modulation requires digital upconversion (DUC) processing to get the real number signal, and the digital high frequency signal is output without changing the information of the signal. Finally, the analog signal obtained after digital-to-analog conversion (DAC) is fed to a Mach-Zendel modulator (MZM) for modulation to obtain the optical signal transmitted in the fiber. At the receiver, the radio frequency signal is obtained after photoelectric detection (PD), and then the original binary bit stream is restored according to the inverse process at the transmitter.

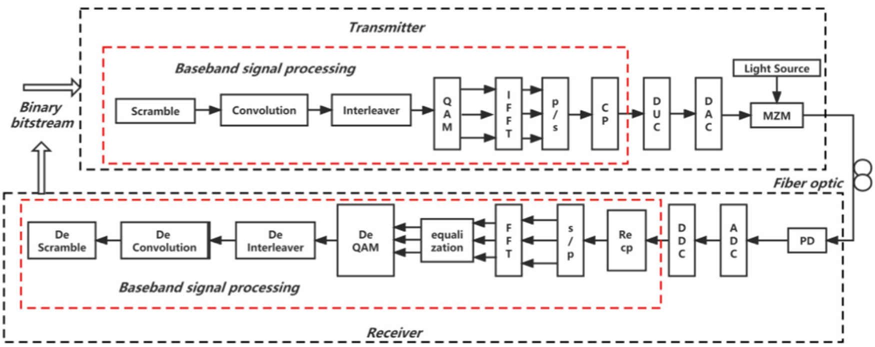

Fig. 1. DDO-OFDM transmission system block diagram

2.1 Processing of OFDM Baseband Signals

The modulation and demodulation of OFDM baseband signals is mainly implemented using FPGA (Fig. 1, red box). The data to be sent first passes through a scrambler to avoid long "0" or "1" that could affect the establishment and maintenance of synchronization at the receiver. Then the scrambled data is fed to the convolutional encoder with constraint length 7 for encoding to improve the reliability of information code element transmission. In this paper, 16QAM modulation is used, but the coded data need to be interleaved before QAM mapping to ensure that adjacent coded bits are mapped to non-adjacent subcarriers

[4, 5]. The symbol modulation is performed using the IFFT principle [6], and finally a cyclic prefix is added to form the OFDM data frame; The demodulation of baseband signal needs synchronization and equilibrium processing. First, the baseband signal after DDC is symbol synchronized and the cyclic prefix is removed. After FFI operation, the time domain or frequency domain response of the output channel should be estimated to ensure the accuracy of demodulation.

The OFDM data frame formed at the transmitter is preceded by two training sequences, which include a short training sequence (STS) of 10 cycles (16 samples per cycle) and a long training sequence (LST) of two cycles (64 samples per cycle), while the last 32 samples of the LST are copied to the front of the LST to form a cyclic prefix (Fig. 2). STS is mainly responsible for data detection, symbol timing synchronization, automatic gain control, etc. The LTS is mainly responsible for the frequency bias estimation and the channel estimation [7].

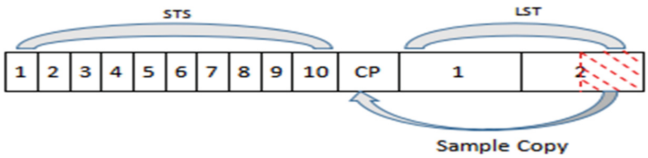

Fig. 2. Schematic diagram of training sequence

2.2 Symbol Synchronization

The intercorrelation operation of the data can be performed at the receiver using locally known short training symbols to determine the end point of the short training symbols or the start point of the long training symbols and to remove the cyclic prefixes. The module implementation can obtain the interrelation number C_k by multiplying the received data groupings with the conjugate complexes of locally known short training symbols and summing them [8].

$$C_k = \sum_{m=0}^{D-1} r_{k-m} \times S_m^* \tag{1}$$

In the above equation, the superscript * indicates the conjugate value. D is the length of the Correlation coefficient, whose size determines the performance of the symbolic synchronization algorithm. Larger values improve performance but also increase computational effort. For IEEE 802.11a systems, D = 16 is the cycle length of short training symbols. When C_k has a peak, this point serves as the end point of a short training sequence. Using this feature, you can find the end point of all short training symbols in an OFDM grouping.

2.3 Channel Estimation and Equalization

The purpose of channel estimation and equalization is to estimate the time or frequency domain response of the channel, correct and recover the received data, and obtain the performance gain of coherent detection (3 dB) [9]. The maximum multipath delay of the channel, the movement speed of the user, and the noise of the receiver are important factors that affect the performance of the channel estimation algorithm. The design can be done using two long training symbols for simple and efficient estimation of the frequency response of all subsequent subcarrier channels in that frame [10].

The frequency domain channel estimation and equalization method based on long training sequence symbols is as follows.

$$\mathrm{R}_{\mathrm{RLTS}} = (\mathrm{R}_{\mathrm{1LTs}} + \mathrm{R}_{\mathrm{2LTS}})/2 \tag{2}$$

$$\hat{\mathrm{H}} = \mathrm{R}_{\mathrm{RLTS}}/\mathrm{L}_{\mathrm{LTS}} \tag{3}$$

$$\hat{\mathrm{R}} = \mathrm{R}/\hat{\mathrm{H}} \tag{4}$$

where $\mathrm{R}_{\mathrm{1LTS}}$ and $\mathrm{R}_{\mathrm{2LTS}}$ are the first and second long training symbols received; $\mathrm{L}_{\mathrm{LTS}}$ is the standard long training symbol, $\mathrm{R}_{\mathrm{RLTS}}$ is the average of the two training symbols; $\hat{\mathrm{H}}$ is the estimated value of the channel frequency response; R is the OFDM symbol received; $\hat{\mathrm{R}}$ is the OFDM symbol after the channel equalization.

3 Simulation Results and Analysis

The modulation and demodulation of baseband signals are mainly implemented using IFFT/FFT algorithms [11]. The IFFT/FFT function can be implemented by using the IP core provided by Xilinx. The main parameters of the IP core are shown in Table 1, where the IP core performs IFFT operation when FWD_INV is 0 and FFT operation when FWD_INV is 1. From the joint simulation results of IFFT/FFT (Fig. 3), it can be seen that the input data of IFFT and the output data of FFT are basically the same, and a certain error is allowed here because the demodulation of the receiver dynamically selects the bit information according to the size of the judgment threshold.

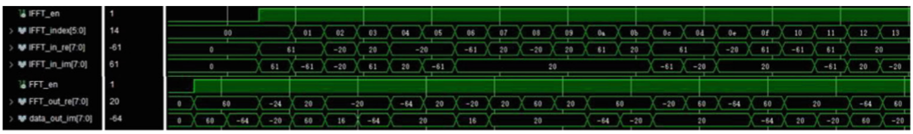

Fig. 3. The IFFT /FFT joint simulation diagram

In the baseband signal processing at the transmitter side, the training sequence is required to be transmitted before the modulated OFDM data frame and form a continuous sequence to be transmitted [12]. As shown in Fig. 4, four identical m-sequences (data_in) are input, and after coding, mapping and IFFT processing, a cyclic prefix is inserted to

Table 1. Main parameter settings for the FFT IP core

Parameter	Value/Option
Implementation	Pipelined, Streaming I/O
Input Data With	16
Phase Factor Width	16
Transform Length	64
Scaling Option	Scaled
SCALE_SCH	10110
FWD_INV	IFFT(0), FFT(1)

form the final OFDM data frame (cp_outr/cp_outi), and then the data to be transmitted (ofdm_re/ofdm_im) is formed after prepose the training sequence (TS_re/TS_im). In order to verify the correctness of the FPGA implementation of baseband signal modulation and demodulation, the baseband output data at the receiver side is compared with the baseband input number at the transmitter side (Fig. 5), and if the data agree, it shows that the design of OFDM baseband system based on FPGA is feasible.

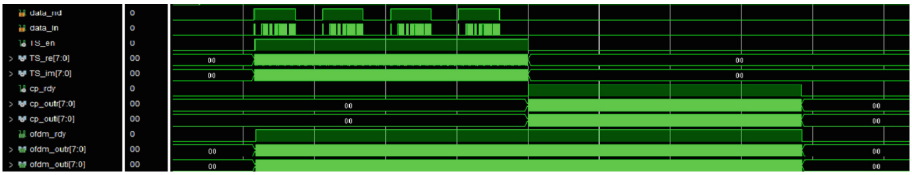

Fig. 4. Launch-end baseband simulation diagram

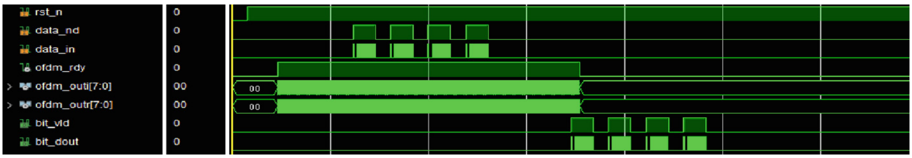

Fig. 5. Comprehensive simulation diagram of OFDM baseband system

Finally the paper gives the FPGA chip resource usage for the OFDM baseband (Table 2). Among them, the time-frequency conversion module takes up the most resources, mainly because the FFT ip core consumes a lot of DSP and RAM resources.

Table 2. Internal logical resource consumption of FPGA

Block	LUTs	FFs	Slicess	BRAMs	DSP48s
ADC interface & Storage	4343	4456	2172	116	0
IFFT & FFT	14017	31578	7086	100	192
Equalizer	4198	9213	2008	24	128
Mapper & Remapper	519	412	226	0	32
Add CP & Remove CP	2415	3823	1087	0	0
Total	34215 (11.3%)	55182 (9.1%)	16578 (21.8%)	391 (38%)	352 (13%)

4 Conclusion

The main work of this paper is to design and implement an O-OFDM communication system, and elaborate the design scheme of OFDM baseband system. The channel estimation and equalization algorithm in this paper can accurately estimate the frequency response of the channel, and can effectively correct and recover the received data. The IFFT/FFT operation is implemented using the IP cores provided by Xilinx, which is verified by simulation and can simulate the process of OFDM baseband modulation and demodulation to reduce the design complexity. Finally, the relevant data results are analyzed and the FPGA-based O-OFDM transmission system design is fully feasible.

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