



Space Vector Pulse Width Modulation Strategy for Cascaded Three-Phase Bridge Converters

Yunhe Wang¹, Cui Wang^{1,2}(✉), Qiangsheng Dai³, Zhanhao Zhao¹, Chenhang Wu¹, Zuojia Niu¹, and Haoran Li¹

¹ Nanchang Institute of Technology, Nanchang 330099, China
ouyang_wangcui@163.com

² Jiangxi Engineering Research Center of High Power Electronics and Grid Smart Metering, Nanchang 330099, China

³ State Grid Jiangsu Electric Power CO., LTD., Nanjing 210000, China

Abstract. Space vector pulse width modulation (SVPWM) strategy has obvious advantages in the output harmonic characteristics and dc voltage utilization of converters, and is widely used in converters below seven levels. However, with the increase of the number of levels, the space vectors and sector triangles increase dramatically, which complicates the reference vector's location and makes the calculation of the switching state corresponding to the space vector difficult. To solve this problem, an SVPWM for cascaded three-phase bridge converter (C3PBC) is proposed in this paper. The proposed SVPWM strategy simplifies the reference vector's location, and without calculating redundant switching states in the modulation process. The switching state's duty cycle is calculated quickly. The modulation strategy can easily be applied to C3PBC with more levels without increasing the computational burden. Finally, the proposed SVPWM strategy is verified by MATLAB/Simulink.

Keywords: Cascaded three-phase bridge converter · SVPWM · Coordinate transformation · Simulation

1 Introduction

The multilevel converter consists of a large number of low-voltage power switching devices. Compared with the two-level converter, the multilevel converter reduces the total harmonic distortion of the output voltage, and has the characteristics of high power factor, strong fault tolerance, etc. In recent years, the multilevel converter has been widely used in industry, such as flexible dc transmission [1], photovoltaic power generation systems [2], power electronic transformers [3, 4], etc. Multilevel converter topologies mainly include cascaded H-bridge multilevel converter (CHBMC), modular multilevel converter (MMC), and neutral point clamped multilevel converter (NPCMC) [5].

CHBMC and MMC are connected by star or delta, and are applied to three-phase systems. Under three-phase unbalanced conditions, the stability of the system will be greatly affected [6]. To solve this problem, a cascaded three-phase bridge converter

(C3PBC) topology is proposed in [7]. It uses the three-phase voltage source inverter (VSI) as sub-module. The line voltages in ac side of the converter are produced through cascaded way.

Modulation strategy directly affects the performance of the multilevel converters, such as harmonic characteristics, control stability [8]. Therefore, it is necessary to study the modulation strategy of the multilevel converter. The modulation strategies of the multilevel converters mainly include nearest level modulation (NLM), carrier phase-shifted pulse width modulation (CPS-PWM), and space vector pulse width modulation (SVPWM). CPS-PWM is simple and easy to be implemented. It is the main modulation method of C3PBC at present. However, when the level number is high, the phase shift angle decreases, the phase shift control accuracy and synchronization accuracy are improved, which increases the difficulty of CPS-PWM implementation. NLM is simple to calculate and easy to be implemented. However, when the level number is low, the harmonic characteristics of the output voltage of the converter are poor. So NLM is more suitable for the converter with high level number. SVPWM has the advantages of low THD, multiple control degrees of freedom, and high dc voltage utilization [9]. However, the traditional SVPWM strategy involves a large number of irrational calculations. Especially when the level number of converter increases, the space vectors and sector triangles increase dramatically, which makes it difficult to locate the reference vector and calculate the switching state. SVPWM strategy is difficult to be applied to converters above seven levels.

In order to extend SVPWM to higher level converters, many simplified SVPWM strategies have been proposed. The reference vector is expressed as a sum of a contender vector and an error vector in [10]. The error vector is mapped to a two-level hexagon centered at the origin. The two-level SVPWM algorithm is used to locate and synthesize the error vector. Finally, the multilevel SVPWM strategy is completed by inverse mapping. This method needs to complete two mapping at each reference vector sampling point. When the level number is high, the switching states corresponding to the competition vector increases, and it is difficult to select the appropriate switching state. Therefore, this method is not suitable for high level converters. Reference [11] proposes a simplified SVPWM strategy based on non-orthogonal coordinates $g-h$. In the $g-h$ coordinates, the coordinate components of the space vector are all integers, which simplifies the reference vector's location and speeds up the calculation of the switching state's duty cycle. However, due to the limitation of the C3PBC topology, its space vector distribution is different from that of the traditional converter, so this method is not suitable for the C3PBC topology.

This paper aims to explore an SVPWM strategy for the C3PBC. The space vector is located on the unit integer grid through coordinate rotation transformation, and it is convenient to locate the reference vector, simplifying the modulation process. The proposed SVPWM strategy is suitable for C3PBC of any level.

2 Cascaded Three-Phase Bridge Converters

The topology of C3PBC is shown in Fig. 1(a), and its sub-module is a three-phase inverter bridge with input dc voltage E . C3PBC cascades the line voltage of sub-modules

to achieve multilevel output. According to the definition of the cascaded cell number n of C3PBC in [6], it can be obtained

$$n = u_{max}/E \tag{1}$$

where u_{max} is the amplitude of the output line voltage at the ac side of C3PBC.

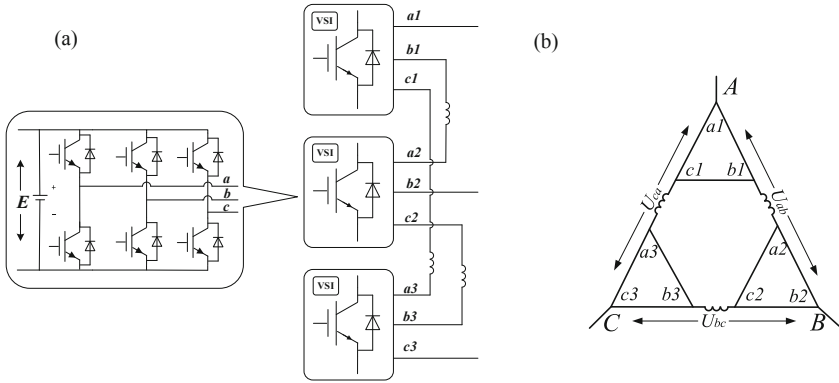


Fig. 1. C3PBC topology (a) 2-cell C3PB converter topology, (b) 2-cell C3PB converter simplified model

Figure 1 shows the topology and simplified topology of the 2-cell C3PBC. The 2-cell C3PBC consists of three sub-modules. Its three line voltages are u_{AB} , u_{BC} , and u_{CA} .

$$\begin{cases} u_{AB} = u_{a1b1} + u_{a2b2} \\ u_{BC} = u_{b2c2} + u_{b3c3} \\ u_{CA} = u_{c3a3} + u_{c1a1} \end{cases} \tag{2}$$

where u_{aibi} , u_{bici} , and u_{ciai} are the line voltages output by the i -th sub-module respectively. According to (2), the output line voltage of 2-cell C3PBC contains five voltages of $\pm 2E$, $\pm E$, and 0, corresponding to five levels of ± 2 , ± 1 , and 0, respectively. Similarly, n -cell C3PBC consists of $3(n-1)$ sub-modules, and its output line voltage includes $2n + 1$ levels of $\pm n$, $\pm (n-1)$, ..., 0. The output line voltage is

$$\begin{cases} u_{AB} = u_{a1b1} + u_{a2b2} + \dots + u_{anbn} \\ u_{BC} = u_{bncn} + u_{b(n+1)c(n+1)} + \dots + u_{b(2n-1)c(2n-1)} \\ u_{CA} = u_{c(2n-1)a(2n-1)} + u_{c(2n)a(2n)} + \dots + u_{c(3n-3)a(3n-3)} + u_{c1a1} \end{cases} \tag{3}$$

The line voltages u_{AB} , u_{BC} , and u_{CA} are normalized with the reference value E to obtain the line voltage levels a , b , and c as

$$\begin{cases} a = u_{AB}/E \\ b = u_{BC}/E \\ c = u_{CA}/E \end{cases} \tag{4}$$

According to the connection mode of C3PBC and the symmetry of the three-phase system,

$$a + b + c = 0 \quad (5)$$

3 Coordinate Transformation and Space Vector Distribution

Three line voltage reference signals of C3PBC are

$$\begin{cases} u_{rab} = mncos\omega t \\ u_{rbc} = mncos(\omega t - \frac{2\pi}{3}) \\ u_{rca} = mncos(\omega t + \frac{2\pi}{3}) \end{cases} \quad (6)$$

where m is the modulation index, $0 < m \leq 1$, and m reflects the dc voltage utilization rate of C3PBC, ω represents the angular frequency of the reference signals.

According to the principle of SVPWM and the definition of traditional coordinates $\alpha\beta$, transform the line voltage reference signals into the reference vector V_r in the $\alpha\beta$ coordinates. The coordinate components of V_r can be expressed as:

$$\begin{bmatrix} \alpha_r \\ \beta_r \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2u_{rab} - u_{rbc} - u_{rca} \\ \sqrt{3}(u_{rbc} - u_{rca}) \end{bmatrix} \quad (7)$$

The reference vector can also be expressed as $V_r(\alpha_r, \beta_r)$. The trajectory of $V_r(\alpha_r, \beta_r)$ is expressed as

$$\frac{\alpha_r^2 + \beta_r^2}{(mn)^2} = 1 \quad (8)$$

Equation (8) shows that the trajectory of the reference vector in the $\alpha\beta$ coordinates is a circle with a radius of mn . Same as (7), the space vector V in the $\alpha\beta$ coordinates can be expressed as

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2a - b - c \\ \sqrt{3}(b - c) \end{bmatrix} \quad (9)$$

where α and β are the coordinate components of the space vector V , the space vector can also be expressed as $V(\alpha, \beta)$. (a, b, c) satisfying (9) is called the switching state corresponding to the $V(\alpha, \beta)$, denoted as $S(a, b, c)$. The trajectory of the reference vector and space vector diagram of 2-cell C3PBC in $\alpha\beta$ coordinates are shown in Fig. 2(a).

Equation (7) indicates that the space vectors in the $\alpha\beta$ coordinates are located in non-integer grid, which makes it difficult to locate the reference vector. In the modulation process, there are a large number of irrational calculations, which makes the implementation of SVPWM strategy complicated. To solve this problem, the coordinates $\alpha\beta$ is transformed into a new coordinates $\alpha'\beta'$. The space vector $V(\alpha, \beta)$ in the $\alpha\beta$ coordinates is mapped to the space vector $V'(\alpha', \beta')$ in the $\alpha'\beta'$ coordinates.

$$\begin{bmatrix} \alpha' \\ \beta' \end{bmatrix} = C_r C_c \begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (10)$$

where C_c is the stretching matrix, which stretches the β -axis of the $\alpha\beta$ coordinates by a factor of $\sqrt{3}$, $C_c = \begin{bmatrix} 1 & 0 \\ 0 & \sqrt{3} \end{bmatrix}$, and C_r is the rotation matrix, which rotates the $\alpha\beta$ coordinates clockwise by 45° , $C_r = \begin{bmatrix} 1/2 & -1/2 \\ 1/2 & 1/2 \end{bmatrix}$, and The principle of the coordinate transformation is shown in Fig. 2(b). Substitute (5) into (10) to get

$$\begin{bmatrix} \alpha' \\ \beta' \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \begin{bmatrix} -b-c \\ b \\ c \end{bmatrix} = \begin{bmatrix} -b \\ -c \end{bmatrix} \quad (11)$$

Equation (11) shows that the space vector in the $\alpha'\beta'$ coordinates is located on the unit integer grid. Same as (11), the reference vector $V_r'(\alpha_r', \beta_r')$ in the $\alpha'\beta'$ coordinates is

$$\begin{bmatrix} \alpha_r' \\ \beta_r' \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & -2 & 1 \\ 1 & 1 & -2 \end{bmatrix} \begin{bmatrix} -u_{rbc} - u_{rca} \\ u_{rbc} \\ u_{rca} \end{bmatrix} = \begin{bmatrix} -u_{rbc} \\ -u_{rca} \end{bmatrix} \quad (12)$$

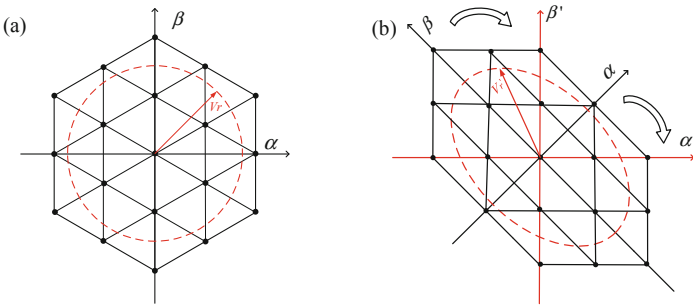


Fig. 2. Trajectory of the reference vector and space vector diagram (a) $\alpha\beta$ coordinates, (b) $\alpha'\beta'$ coordinates

$$\left(\frac{\alpha_r' + \beta_r'}{mn} \right)^2 + \left(\frac{\alpha_r' - \beta_r'}{\sqrt{3}mn} \right)^2 = 1 \quad (13)$$

In the $\alpha'\beta'$ coordinates, Eq. (13) shows the trajectory of the reference vector V_r' is an ellipse, as shown in Fig. 2(b). 2-cell C3PBC contains 19 space vectors that form two nested hexagons. n -cell CHBMC has $(1 + 6 \sum_{i=1}^n i)$ space vectors that form n nested hexagons.

4 Locating and Synthesizing Reference Vector

The reference vector $V_r'(\alpha_r', \beta_r')$ locates in a unit square formed by $V_0'(\alpha_0', \beta_0')$, $V_1'(\alpha_0' + 1, \beta_0')$, $V_2'(\alpha_0', \beta_0' + 1)$, and $V_3'(\alpha_0' + 1, \beta_0' + 1)$, as shown in Fig. 3.

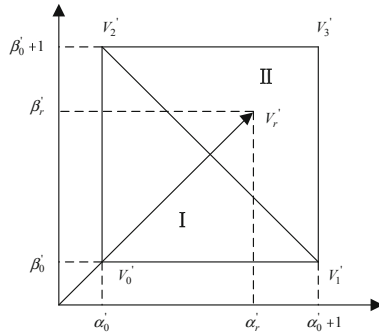


Fig. 3. Location of reference vector

$$\begin{cases} \alpha'_0 = \text{floor}(\alpha'_r) \\ \beta'_0 = \text{floor}(\beta'_r) \end{cases} \tag{14}$$

where $\text{floor}(*)$ represents the largest integer not greater than the number.

When $\left[(\alpha'_r - \alpha'_0) + (\beta'_r - \beta'_0) \right] \leq 1$, the reference vector is located in sector I composed of the space vectors V'_0, V'_1 , and V'_2 . V'_0, V'_1 , and V'_2 synthesize the reference vector. According to the volt-second balance principle, the duty cycles t_0, t_1 , and t_2 , of the space vectors V'_0, V'_1 , and V'_2 are calculated.

$$\begin{cases} t_0 = T_s \cdot \left[(\alpha'_0 + \beta'_0 + 1) - (\alpha'_r + \beta'_r) \right] \\ t_1 = T_s \cdot (\alpha'_r - \alpha'_0) \\ t_2 = T_s \cdot (\beta'_r - \beta'_0) \end{cases} \tag{15}$$

When $\left[(\alpha'_r - \alpha'_0) + (\beta'_r - \beta'_0) \right] > 1$, the reference vector is located in sector II composed of the space vectors V'_1, V'_2 , and V'_3 . V'_1, V'_2 , and V'_3 synthesize the reference vector. According to the volt-second balance principle, the duty cycles t_1, t_2 , and t_3 of the space vectors V'_1, V'_2 , and V'_3 are calculated.

$$\begin{cases} t_1 = (\alpha'_0 + 1 - \alpha'_r) \cdot T_s \\ t_2 = (\beta'_0 + 1 - \beta'_r) \cdot T_s \\ t_3 = T_s \cdot \left[(\alpha'_r + \beta'_r) - (\alpha'_0 + \beta'_0 + 1) \right] \end{cases} \tag{16}$$

According to (8), the switching state corresponding to the space vector $V'(\alpha', \beta')$ is $S(\alpha' + \beta', -\alpha', -\beta')$. So, $S_0(\alpha'_0 + \beta'_0, -\alpha'_0, -\beta'_0), S_1(\alpha'_0 + \beta'_0 + 1, -\alpha'_0 - 1, -\beta'_0), S_2(\alpha'_0 + \beta'_0 + 1, -\alpha'_0, -\beta'_0 - 1)$, and $S_3(\alpha'_0 + \beta'_0 + 2, -\alpha'_0 - 1, -\beta'_0 - 1)$ are the switching states corresponding to the space vectors V'_0, V'_1, V'_2 and V'_3 , respectively.

The five-segment switching method is used to synthesize the reference vector. Taking the reference vector $V'_r(\alpha'_r, \beta'_r)$ in sector I as an example, the

switching sequence composed of the switching states S_0 , S_1 and S_2 has six cases, namely, $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_1 \rightarrow S_0$, $S_0 \rightarrow S_2 \rightarrow S_1 \rightarrow S_2 \rightarrow S_0$, $S_1 \rightarrow S_2 \rightarrow S_0 \rightarrow S_2 \rightarrow S_1$, $S_1 \rightarrow S_0 \rightarrow S_2 \rightarrow S_0 \rightarrow S_1$, $S_2 \rightarrow S_1 \rightarrow S_0 \rightarrow S_1 \rightarrow S_2$, $S_2 \rightarrow S_0 \rightarrow S_1 \rightarrow S_0 \rightarrow S_2$. Taking the switching sequence $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_1 \rightarrow S_0$ as an example. Figure 4 shows the switching sequence and switching time distribution.

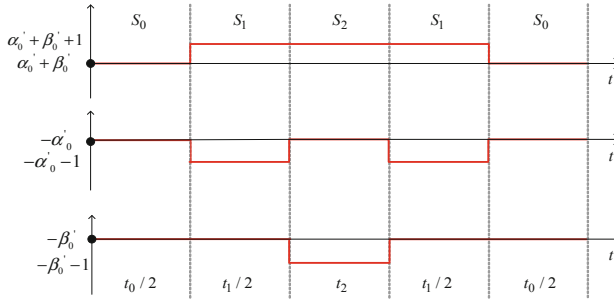


Fig. 4. Switching sequence and switching time distribution

5 Simulation Verification

In order to verify the proposed SVPWM strategy, the 4-cell C3PBC system is simulated in MATLAB/Simulink. The 100V voltage source is applied as the sub-module DC input, and the reference signal frequency f is 50 Hz, the sampling period is 0.1 ms, and the modulation index m is 0.96.

Figure 5 shows the line voltage waveforms and the spectra of the line voltage. The output line voltage has 9 levels, which verifies the previous analysis. The THD of the line voltage is 15.83%, the amplitude of its fundamental component is 382.2 V, and its rms value is 270.3 V. The rms value of the line voltage calculated with (6) is 271.5 V, with a small difference of 1.2 V from the simulation result, which is caused by the internal resistances of the switching devices in simulation. Figure 6 shows the output line voltage waveform and its corresponding input reference voltage waveform, which indicates that the line voltage tracks the reference voltage well.

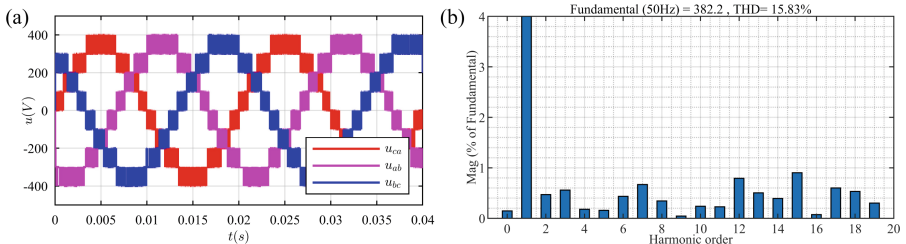


Fig. 5. Simulation results ($m = 0.96$) (a) Line voltage, (b) Spectra of the line voltage

Table 1. Comparison of Modulation Strategy

Modulation strategy	THD	Fundamental amplitude
SVPWM ($m = 0.96$)	15.83%	382.2 V
SVPWM ($m = 0.86$)	16.99%	343.6 V
CPS-PWM ($m = 0.96$)	25.31%	332.4 V
CPS-PWM ($m = 0.86$)	25.39%	297.8 V

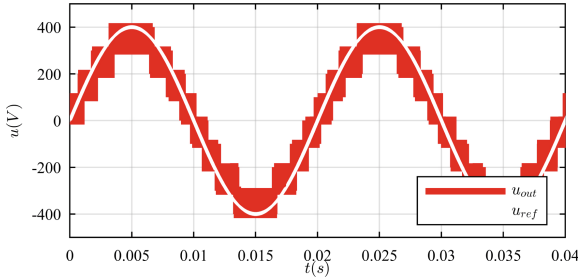


Fig. 6. Reference voltage u_{ref} (white) and output line voltage u_{out} (red)

Table 1 shows the comparison results between the proposed SVPWM strategy and the CPS-PWM strategy in [6]. As can be seen from the table, under the same modulation index, the THD of the proposed SVPWM strategy is significantly better than that of the CPS-PWM strategy.

6 Conclusion

An SVPWM strategy suitable for C3PBC is proposed in this paper. The traditional coordinates $\alpha\beta$ is transformed into a new coordinates $\alpha'\beta'$. The trajectory of reference vector and space vector distributions in the new coordinates $\alpha'\beta'$ are calculated. The space vector is located on unit integer grid in the $\alpha'\beta'$ coordinates, which simplifies the reference vector's location and speeds up the calculation of the switching state's duty cycle. The special relationship between the coordinate components of the space vector and the line voltage levels in the $\alpha'\beta'$ coordinates simplifies the calculation of the switching state, and the modulation process is simple without calculating many redundant switching states. The proposed SVPWM strategy can be easily extended to any level C3PBC without increasing the computational burden. Finally, the proposed strategy is verified by MATLAB/Simulink simulation.

Acknowledgment. This work is funded by the National Natural Science Foundation of China under Grant 51667015, the Natural Science Foundation of Jiangxi under Grant 20202BABL204050, and the Science and Technology Plan of Jiangxi Provincial Department of Education under Grant GJJ211918, GJJ211916.

References

1. Yang, X., Li, Z., Xue, Y., et al.: Analysis of Fault Blocking Characteristics of Enhanced Flexible Reverse Resistance Modular Multilevel Converter. *Trans. China Electrotech. Soc.* **34**(12), 2549–2557 (2019). (in Chinese)
2. Zhu, X., Wang, H., Zhang, W., et al.: A novel single-phase five-level transformer-less photovoltaic (PV) inverter. *China Electrotech. Soc. Trans. Electr. Mach. Syst.* **4**(4), 329–338 (2020)
3. Lu, S., Zhao, D., Li, K., Li, S.: A distributed feedforward control method for power electronic transformers. *China Electrotech. Soc. Trans. Electr. Mach. Syst.* **4**(4), 319–328 (2020)
4. Ma, D., Chen, W., Shu, L., et al.: A multiport power electronic transformer based on modular multilevel converter and mixed-frequency modulation. *IEEE Trans. Circuits Syst. II Express Briefs* **67**(7), 1284–1288 (2020)
5. Lin, L., Pei, Z., Cai, G., et al.: Hybrid isolated modular multilevel converter. *Trans. China Electrotech. Soc.* **36**(16), 3319–3330 (2021). (in Chinese)
6. Lu, Z., Zhao, L., Zhu, W., et al.: Analysis and simulation of 3P-bridge cascaded multilevel PWM converter. In: 7th International Power Electronics and Motion Control Conference. IEEE, pp. 1120–1124 (2012)
7. Lu, Z., Zhao, L., Zhu, W., et al.: 3P-bridge cascaded PWM rectifier suitable for HV side of PET. In: Asia-Pacific Power & Energy Engineering Conference. IEEE (2012)
8. Ronanki, D., Williamson, S.S.: Modular multilevel converters for transportation electrification: challenges and opportunities. *IEEE Trans. Transp. Electrification* **4**(2), 399–407 (2018)
9. Chen, X., Li, T.: A simplified multilevel space vector PWM control strategy based on the combination of control degrees of freedom. *Trans. China Electrotech. Soc.* **34**(22), 4781–4794 (2019). (in Chinese)
10. Zhang, Q., Wu, Y., Zhang, B., et al.: Space Vector Pulse Width Modulation Algorithm Based on Three-phase Current-Mode Five-Level Rectifier. *Transactions of China Electrotechnical Society* **35**(24), 5134–5141 (2020). (in Chinese)
11. Susheela, N., Kumar, P.S., Sharma, S.K.: Generalized algorithm of reverse mapping based SVPWM strategy for diode-clamped multilevel inverters. *IEEE Trans. Ind. Appl.* **54**(3), 2425–2437 (2018)