Chapter 8
Energy Efficient VgSOT-MTJ Based 1 Bit Subtractor

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Abstract To harness the potential of VgSOT MRAM in digital signal processing circuits, this study presents a 1-bit full subtraction circuit based on voltage gated Spin–Orbit Torque Magnetic Tunnel Junction (MTJ) technology. The circuit design adopts a dual-track structure that seamlessly integrates CMOS and MTJ components. By precisely controlling the timing of reading and writing operations, the circuit achieves the desired full subtraction functionality. This integrated structure enables the seamless integration of MTJ memory devices into the full subtractor circuit while significantly reducing overall power consumption by minimizing the frequency of MTJ writing operations. This paper has implemented VgSOT, SOT, and STT based subtractor and borrow circuit for performance evaluation. Performance parameters like average delay, energy consumption, and Average power consumption have been analyzed in this paper. With VgSOT MTJ based subtractor, performance improvement of 93% and 97% is seen in terms of energy/Average power consumption over SOT and STT based implementations. In terms of average delay. VgSOT MTJ based subtractor performs 47% and 69% better over SOT and STT based implementations.

8.1 Introduction

In the realm of advanced technologies, the continuous scaling down of CMOS (Complementary Mosfet) technology [1, 2] to lower nodes has led to an upsurge in leakage current, which contributes significantly to the overall dynamic power consumption, accounting for approximately 40% [3]. As a consequence, the demand for low-power devices becomes paramount for achieving high-performance in deep sub-micrometer technology. To overcome these challenges, researchers in academia and industry have shifted their focus towards nanoscaled technologies [4, 5], with magnetic tunnel junctions (MTJs) [6–8] emerging as a prominent contender. MTJs have garnered considerable attention due to their remarkable attributes,

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including non-volatility [9], high speed, minimal leakage [10]/power consumption, and compatibility with semiconductor devices [11, 12]. These spintronic devices [13–15] leverage both the charge and spin properties of electrons and are composed of two ferromagnetic layers separated by a dielectric layer. The pinned layer or reference layer remains firmly magnetized, while the free layer's magnetization direction can be altered. MTJs exhibit two distinct states: the parallel state (R_P) with low resistance and the anti-parallel state (R_{AP}) with high-resistance.

The unique characteristics of MTJs have positioned them as a promising candidate for various applications, particularly in the field of memory technology [16]. The ability to switch between low resistance parallel and high resistance anti-parallel states offers the foundation for reliable data storage and retrieval. Furthermore, the compatibility of MTJs with existing semiconductor technologies facilitates seamless integration into conventional CMOS circuits, enabling the development of hybrid systems that leverage the strengths of both spintronic and traditional electronic components. This opens up exciting possibilities for the design of advanced memory architectures, such as spin-transfer torque magnetic random-access memory (STT-MRAM) [17, 18] and spin–orbit torque magnetic random-access memory (SOT-MRAM) [19, 20], that offers enhanced performance, reduced power consumption, and improved scalability. With ongoing research and development efforts, the potential of MTJs in revolutionizing memory technologies is being realized, paving the way for future advancements in data storage and processing.

The emergence of voltage-controlled spin–orbit torque (VgSOT) MTJs (leveraging the voltage-controlled magnetic anisotropy effect [21]) [22] has revolutionized the field of memory design. VgSOT MTJs provide an additional degree of freedom in spintronic device design, enabling precise control over the magnetic states of the MTJ through the application of voltage pulses. This unique feature has led to significant advancements in data storage and processing capabilities. By utilizing VgSOT MTJs in memory architectures, it becomes possible to achieve lower-power, higher-speed, and trustworthy operations. The ability to dynamically control the magnetic states of the MTJs allows for efficient data storage, retrieval, and manipulation, thereby opening up new possibilities for memory applications in various domains. The continued exploration and utilization of VgSOT MTJs in memory designs will undoubtedly lead to exciting developments and transformative improvements in data storage and processing capabilities.

This research paper presents the design of a functional circuit for digital signal processing systems. The circuit focuses on implementing a full subtractor utilizing a VgSOT MTJ device. The circuit ensures efficient utilization of resources while maintaining the desired functionality of the full subtractor, showcasing its potential for low-power digital signal processing applications. Section 8.2 presents the subtractor and borrow circuits implemented using VgSOT, SOT, and STT MTJ respectively. Simulation results have been presented in Sect. 8.3 while performance analysis in terms of energy, delay has been done in Sect. 8.4. Section 8.5 concludes the research work on VgSOT performance compared to SOT and STT and Sect. 8.6 presents the future scope for VgSOT based devices.

8.2 VgSOT MTJ Based Full Subtractor

The hybrid functional circuit [23] designed for MTJ device applications is depicted in Fig. 8.1. This circuit comprises three essential components: the MOSFET circuit, the pre-charge Sense Amplifier (PCSA) [24], and the MTJ device. The PCSA component facilitates the reading of the memory content stored in the MTJ device, while the MOSFET circuit is specifically designed to execute the necessary logic functions required by the circuit. The MTJ device serves as the storage element, storing the necessary circuit information (logic "0" or "1" based on the states of the MTJs) to perform the desired circuit function. The circuit structure provides numerous advantages such as fast readout speed, high readout accuracy, and lower power consumption during the readout process.

Figures 8.2 and 8.3 present the VgSOT MTJ based subtractor and the borrow circuit. Within each part, two non-volatile MTJ devices are employed to create a Non-volatile circuit, where the VgSOT devices store complementing information. The circuit arrangement includes a set of output terminals that are complementary to each other, which generate the subtraction—Sub and $\overline{\text{Sub}}$ and borrow variables—borrow and $\overline{\text{borrow}}$.

The subtractor circuit works in the writing and the reading/calculating modes of operation. The transition between these modes is controlled by the clock signal. During the low phase of the clock, transistors MP1 and MP2 are activated, allowing Sub and $\overline{\text{Sub}}$ being set to a logic Vdd. During the reading operation, the stored information from the VgSOT MTJ is retrieved through the pre-charge sense amplifier (PCSA).

The logical functions of the full subtraction circuit depicted in Figs. 8.2 and 8.3 are expressed by Eqs. (8.1) and (8.2), representing the operations of subtraction and borrowing, respectively. The circuit corresponding to these equations is divided into two parts, each responsible for implementing the subtraction and borrow functions. Each part of the circuit in the figure consists of two tracks, with MTJs utilized in

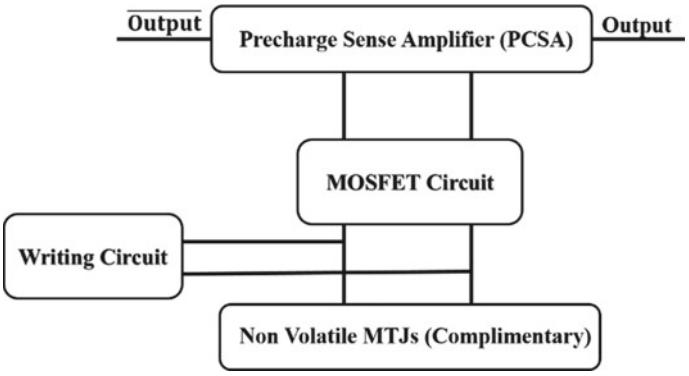

Fig. 8.1 Hybrid MTJ/CMOS circuit [23]

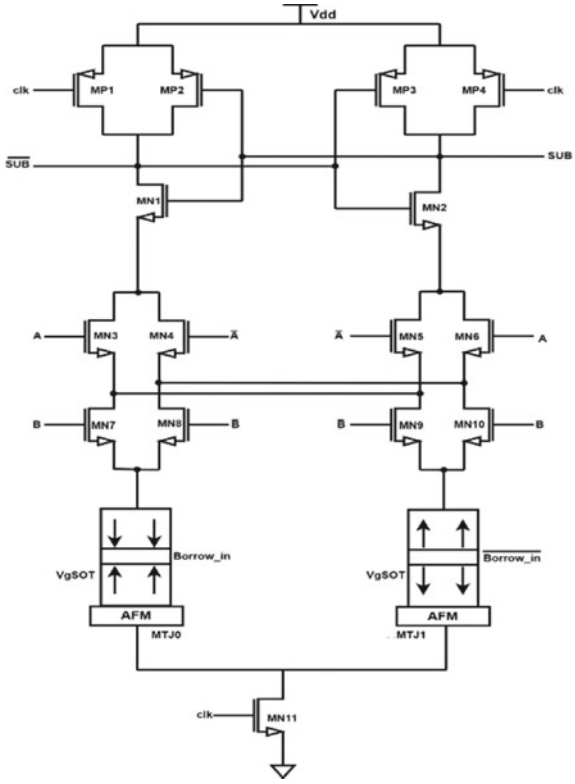

Fig. 8.2 VgSOT MTJ based subtractor circuit

both tracks.

$$Sub = A \oplus B \oplus Borrow\_in$$

$$= A.B.Borrow\_in + A.\overline{B}.\overline{Borrow\_in} + \overline{A}.B.\overline{Borrow\_in} + \overline{AB}Borrow\_in \tag{8.1}$$

$$Borrow = \overline{A}.\overline{B}.Borrow\_in + \overline{A}.B.\overline{Borrow\_in} + \overline{A}.B.Borrow\_in + A.B.Borrow\_in \tag{8.2}$$

The subtractor and borrow circuit, during the writing operation, MP1 and MP4 transistors get enabled, causing the potentials of Sub, $\overline{\text{Sub}}$, Borrow, and $\overline{\text{Borrow}}$ being pulled to a logic high level. Concurrently, MN5 and MN6 transistors are closed, allowing for the writing operation of the MTJ storage content.

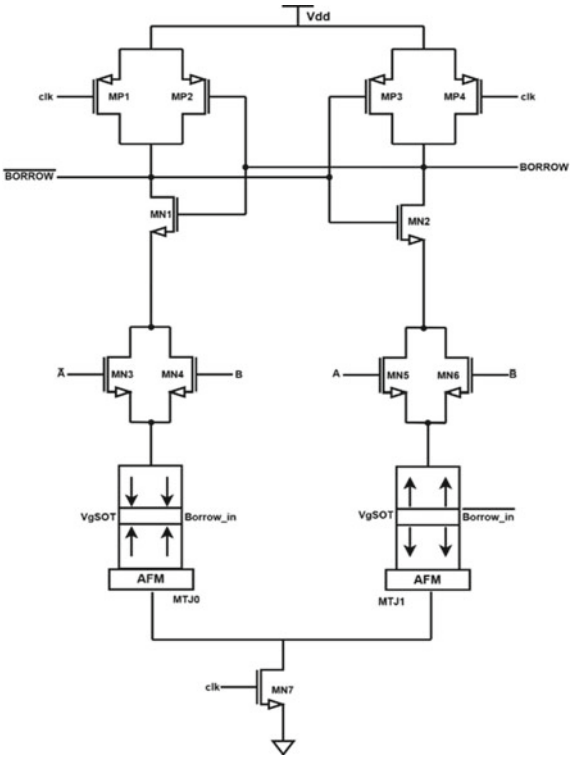

Fig. 8.3 VSOT MTJ based borrow circuit

During the calculating/reading mode, the transistors MP1 and MP4 are closed, while MN5 and MN6 are open. This configuration enables the reading of the MTJ storage content. Additionally, based on the input signals A, B, and Borrow_in, the outputs of Sub and Borrow can be obtained, thereby achieving the full subtraction function of the circuit.

Consider the scenario where the inputs B = 0 and A = 0, and the stored state of VgSOT MTJ0 in Figs. 8.2 and 8.3 is logical "0," representing Borrow_in = 0. Correspondingly, MTJ1 stores the content "1" indicating $\overline{\text{Borrow}} = 1$. In the writing mode, the signals Sub, $\overline{\text{Sub}}$, Borrow, and $\overline{\text{Borrow}}$ are set to logic 1 level. When CLK signal is also logic 1, MN5 is turned on, establishing conducive paths in: MN4-MN84-MTJ0-MN11 and MN6-MN10-MTJ1-MN11. However, since the stored state of MTJ1 is "1," it exhibits a lower resistance state, causing a large current to flow through path MN6-MN10-MTJ1-MN11. As a result, the output Sub transitions between lower and high state values, achieving the difference function when Sub = 0. Simultaneously, MN6 is activated, creating a conductive path in path 5: MN3-MTJ0-MN7 and path 8: MN6-MTJ1-MN7 in borrow circuit. As the stored state of MTJ1 is "1," it also presents a low resistance state, leading to a large current in path 8. Consequently, the Borrow terminal reaches a low level first, followed by

Table 8.1 Subtractor truth-table

Borrow_in	B	A	Sub	Borrow
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

the later transition of $\overline{\text{Borrow}}$ to a high level. This condition corresponds to Borrow = 0, accomplishing the borrowing function.

For various combinations of inputs B, A, and Borrow_in in the MTJ device, Sub and Borrow are determined following the same operating principle. These values align with the truth table of the VgSOT based subtractor circuit, as shown in Table 8.1. The truth table presents the correlation between the input variables and the corresponding output values of the full subtractor circuit.

Similarly, we have implemented the SOT and STT based subtractor and borrow circuits, as seen in Figs. 8.4, 8.5, 8.6, and 8.7, respectively. The functionality of subtractor remains the same for SOT and STT based implementations similar to VgSOT MTJ subtractor. VgSOT employs Antiferromagnetic layer (AFM) as compared to Heavy Metal (HM) layer in SOT.

8.3 Simulation Results and Modulation Parameters

The simulation of the Vg-SOT based Full subtractor has been conducted using CADENCE VIRTUOSO 16.6 software on a 45 nm technology node, with a supply voltage (VDD) of 1.2 V. Vg-SOT MRAM, SOT MRAM, and STT MRAM Verilog-models are employed in this paper. Table 8.2 shows the Vg-SOT, SOT, and STT device parameters used in circuit simulations.

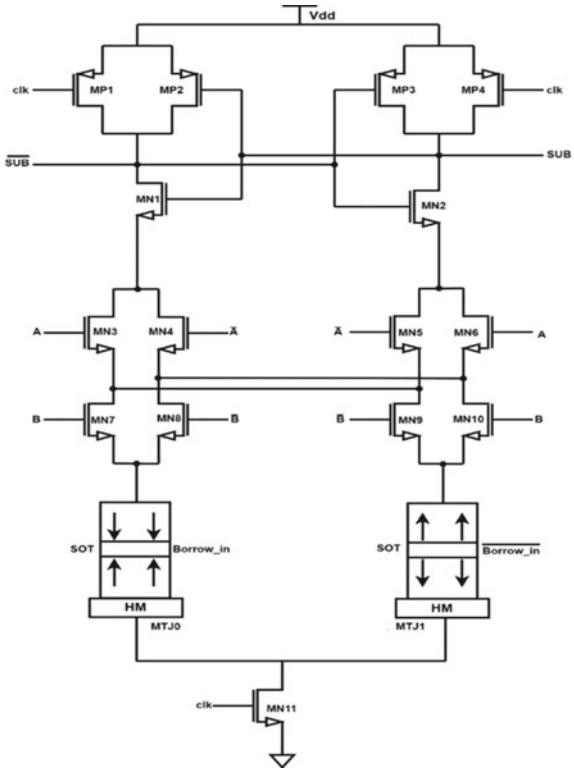

Fig. 8.4 SOT MTJ based subtractor circuit

As per subtractor truth table, inputs A, B, and Borrow_in are configured. The transient analysis of VgSOT MTJ based subtractor, depicted in Fig. 8.8, confirms the validity of the circuit. During the "writing" mode, when CLK is set to 0, the VgSOT MTJ undergoes a "writing" process. Specifically, the stored content in MTJ0 transitions from "0" to "1", while the content in MTJ1 transitions from "1" to "0". Conversely, when CLK is set to 0, the stored content in MTJ0 switches from "1" to "0", and the content in MTJ1 switches from "0" to "1".

By analyzing the simulation results in Fig. 8.8, it is evident that the circuit operates in accordance with subtractor functional truth table. For each combination of A, B, and Borrow_in, the corresponding values of Sub and Borrow align precisely with the expected outcomes. The simulated behavior of the circuit matches the predicted functionality, thereby validating the accurate operation of the full subtractor circuit.

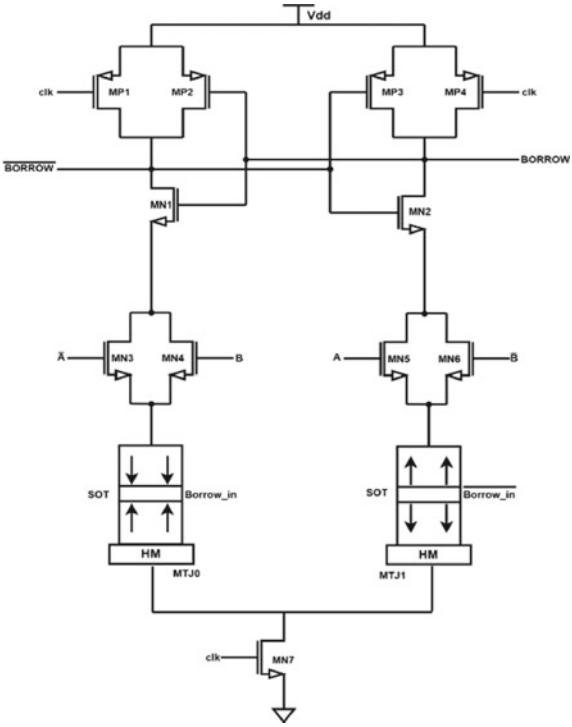

Fig. 8.5 SOT MTJ based borrow circuit

Similarly, Figs. 8.9 and 8.10 show the transient response of SOT and STT-MTJ based subtractor respectively.

8.4 Performance Evaluation

Table 8.3 presents the comparison between different performance parameters such as Energy consumption (fJ), Delay (ns), and Average power consumption (μW) among VgSOT, SOT, and STT MTJ based subtractor implementation respectively.

From Table 8.3, it is seen that in terms of Energy consumption, VgSOT MTJ based subtractor performs 93% and 97% better as compared to SOT and STT-based subtractor implementations. In terms of average delay, VgSOT MTJ based implementation perform 45% and 69% better as compared to SOT and STT-based implementations, respectively. In terms of Average power consumption, performance improvement of 93% and 97% is seen over SOT and STT based subtractor.

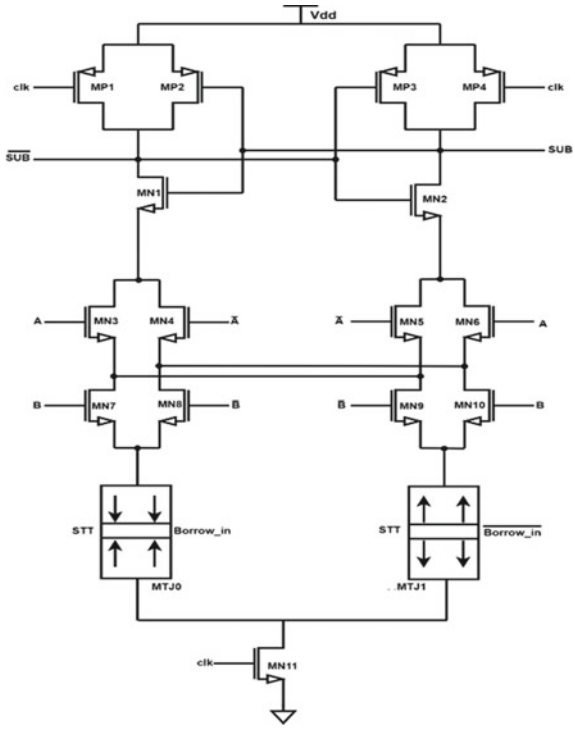

Fig. 8.6 STT MTJ based subtractor circuit

Figures 8.11, 8.12, and 8.13 show the graphical representation of performance parameters comparison between different design implementations of subtractor as shown in Table 8.3.

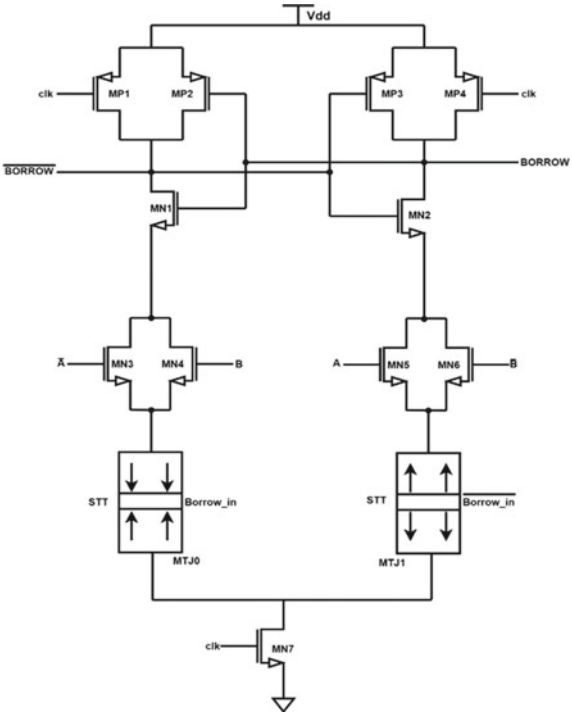

Fig. 8.7 STT MTJ based borrow circuit

Table 8.2 Device parameters

Parameters	Vg-SOT [25]	SOT [26]	STT [27]
Write voltage (V)	1.2	1.2	1.2
CMOS technology (nm)	45	45	45
Tunnel magnetoresistance ratio (TMR) (%)	100	120	200
MTJ surface area (nm * nm)	50 * 50	40 * 40	40 * 40
Oxide barrier thickness (nm)	1.4	0.85	0.85
Free layer thickness (nm)	1.1	0.7	1.3

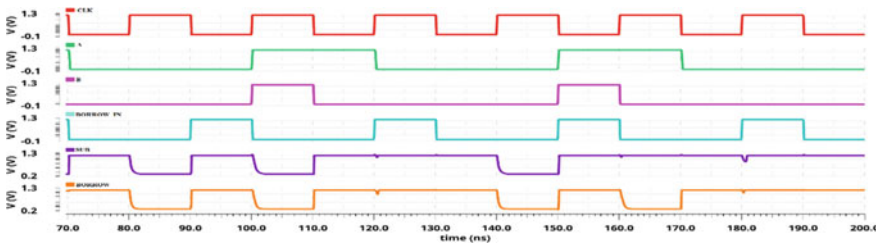

Fig. 8.8 Transient analysis of VgSOT MTJ based subtractor and borrow circuit

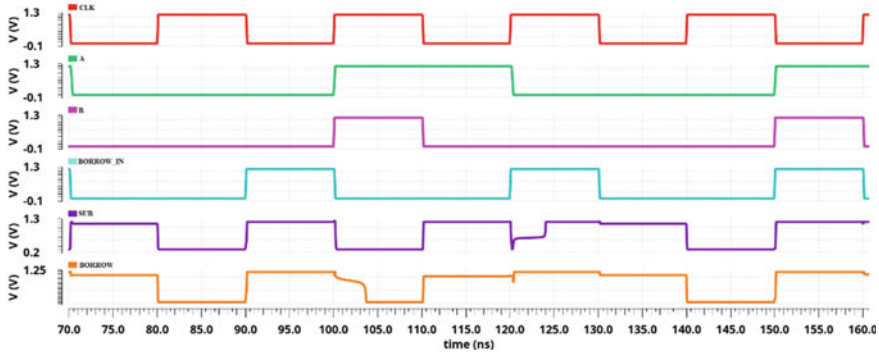

Fig. 8.9 Transient analysis of SOT MTJ based subtractor and borrow circuit

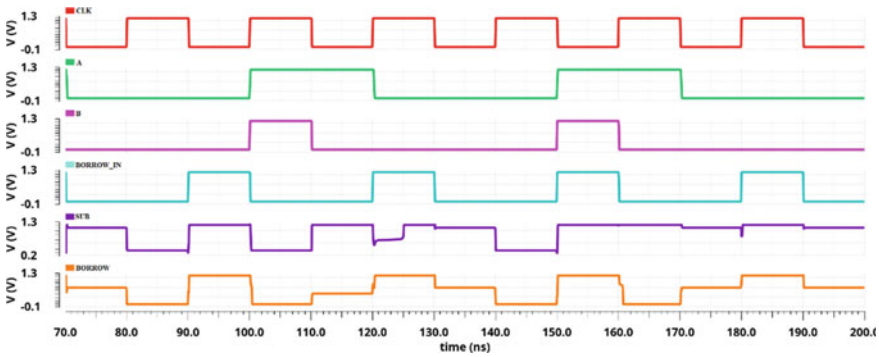

Fig. 8.10 Transient analysis of STT MTJ based subtractor and borrow circuit

Table 8.3 Performance parameters comparison between different designs

Design	Energy consumption (fJ)	Delay (ns)	Average power consumption (μW)
VgSOT MTJ subtractor	19.4	1.26	0.986
SOT MTJ subtractor	310	2.3	14.81
STT MTJ subtractor	691	4.11	35.22

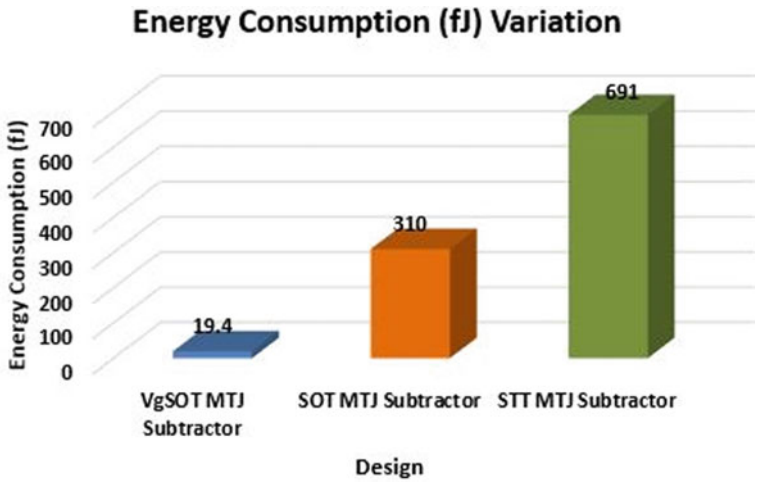

Fig. 8.11 Energy consumption variation for different design

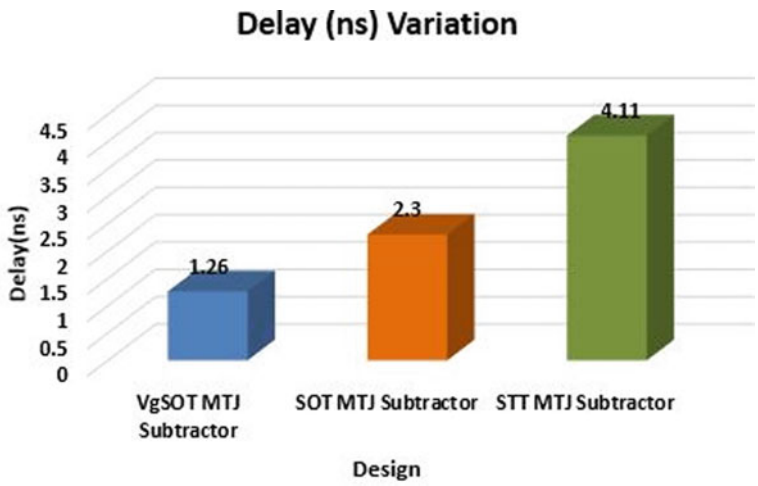

Fig. 8.12 Delay consumption variation for different design

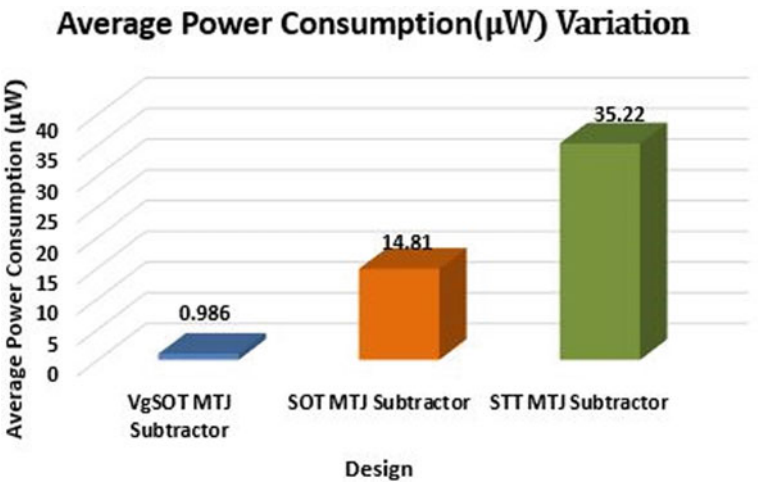

Fig. 8.13 Average power consumption variation for different design

8.5 Conclusion

In conclusion, the VgSOT-based 1-bit subtractor circuit presents a novel approach for digital signal processing. By utilizing the VgSOT effect in conjunction with vertical MTJs, this circuit offers an efficient solution for performing subtraction operations with reduced power consumption. Simulation results demonstrate the successful implementation of the subtraction circuit, validating the outputs sub and borrow as per truth table. From performance parameters comparison, With VgSOT MTJ based subtractor, performance improvement of 93 and 97% is achieved in terms of energy/Average power consumption as compared to SOT and STT based implementations. In terms of average delay. VgSOT MTJ based subtractor performs 47 and 69% better over SOT and STT based implementations. With its low-power characteristics and reliable functionality, the VgSOT-based 1-bit subtractor circuit holds significant promise for enhancing digital signal processing systems in the domain of performance and energy efficiency.

Furthermore, VgSOT MTJ 1-bit subtractor circuit opens up possibilities for broader applications in the field of digital signal processing. Its successful implementation serves as a foundation for the development of more complex arithmetic units and computational circuits. By leveraging the advantages of VgSOT and MTJ technology, it is feasible to explore the design of higher-order subtractor, multi-bit subtraction circuits, and even more advanced computational modules for low-power and high-speed processors.

Additionally, the integration of VgSOT-based circuits with existing digital systems holds potential for enhancing overall system performance and efficiency. The reduced power consumption and high-speed operation offered by the VgSOT-based 1-bit subtractor circuit make it an attractive choice for various applications, such as in

portable devices, Internet of Things (IoT) systems, and embedded systems. The compact size and compatibility with semiconductor devices further contribute to its versatility and integration capabilities.

8.6 Future Scope

The successful implementation of VgSOT-based circuits in the 1-bit subtractor has opened up exciting possibilities for their application in various fields. Moving forward, there are several potential areas of future research and development for VgSOT-based applications:

Advanced Computing Systems: VgSOT-based circuits can be further explored and optimized for advanced computing systems, such as high-performance processors and data centers. Their unique characteristics, including non-volatility, low-power consumption, and high speed, make them attractive candidates for improving overall system performance and energy efficiency.

Non-Volatile Storage Solutions: The integration of VgSOT with memory technologies holds great potential for the development of non-volatile storage solutions. By leveraging the advantages of VgSOT, such as low write energy and high endurance, researchers can explore the design of next-generation non-volatile memory devices, such as MRAM, that offer fast access times, high density, and reliable data retention.

Neuromorphic Computing: VgSOT-based circuits can play a significant role in the advancement of neuromorphic computing systems. With their ability to emulate the behavior of biological synapses, VgSOT-based circuits can enable the development of energy efficient and high-performance neuromorphic systems for applications in artificial intelligence, machine learning, and pattern recognition.

Integration with IoT Devices: As the Internet of Things (IoT) continues to expand, there is a need for low-power and compact devices. VgSOT-based circuits have the potential to meet these requirements by enabling the design of energy efficient IoT devices with enhanced computational capabilities and non-volatile memory storage, contributing to the growth of smart homes, wearable devices, and industrial IoT applications.

Emerging Technologies and Applications: VgSOT-based circuits can be explored in emerging technologies and applications. For example, their compatibility with semiconductor devices makes them suitable for integration in flexible electronics and sensor systems, where low-power and high-density circuitry is essential. Additionally, their ability to operate at cryogenic temperatures makes them attractive for quantum computing and quantum information processing.

System-level Integration: Future research can focus on the system-level integration of VgSOT-based circuits into complex electronic systems. This includes exploring their compatibility with existing semiconductor processes, optimizing their performance in mixed-signal environments, and designing efficient interconnects for seamless integration with other functional blocks.

In summary, the future of VgSOT-based applications holds tremendous potential for advancing computing systems, non-volatile storage solutions, neuromorphic computing, IoT devices, emerging technologies, and system-level integration. Continued research and development in these areas will drive innovation and unlock new opportunities for VgSOT-based technologies in various domains.

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