Simulation-Based Optimization for Automated Design of Analog/RF Circuits

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Abstract Automation tools for circuit optimization have proven their usefulness in solving design issues by considering the technological aspects of downscaling. Recent advances have proven that the optimization method based on simulation is a powerful and important solution for the optimal sizing of electronic circuits. In this paper, we propose a simulation-based methodology for automatic optimization of the multi-objective design of an analog/RF circuit. As applications, we use both analog and RF circuits, respectively the LC tank Voltage Controlled Oscillator (VCO) and the new Current-Feedback Operational Amplifier (CFOA). For the LC-VCO, we optimize the power consumption and the phase noise. For the CFOA, we optimize its important performances such as bandwidth and parasitic resistances, for low-voltage, low-power applications. All simulations are performed by HSPICE using 0.13 μm RF CMOS and 0.18 μm CMOS technologies for the LC-VCO and the CFOA, respectively.

Keywords Simulation-based method · Multi-objective optimization · Optimization algorithms · Analog circuit · IC design · Voltage controlled oscillator · CFOA · NSGA II · MOPSO-CD

1 Introduction

The progressive trend of CMOS technology towards smaller sizes has made the integration of integrated systems possible for wireless communication implementations [1]. Through the use of CMOS processes and technology development, the design

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of analogue/RF circuits is imposing more stringent requirements in terms of accuracy, speed and integration [2]. Thus, the design challenge today is to design circuits meeting the required specifications with low noise and low consumption [3], despite the presence of parasitic effects in the CMOS technology. To meet the demands of low-power, low-cost wireless telecommunication technology, wireless devices must be efficiently optimized.

For instance, the most common used oscillator architecture in transceivers is the VCO. This circuit controls the oscillation frequency using a control signal. These types of oscillators always need selective circuits, usually RC circuits, LC circuits, switched capacitor, etc., which form a feedback for generating a sinusoidal output. Due to its advantages in RF applications, the LC-VCO is the most frequently used [4]. The LC resonator is made up of a spiral inductor and a CMOS variable capacitance (Varactor) which is controlled by a control signal voltage to change the oscillation frequency. However, the use of integrated inductors causes many problems, such as increased energy consumption and phase noise degradation [1].

Moreover, CFOA are among the more important integrated active elements. Compared to the operational amplifier, the CFOA are preferred in signal processing systems due to their essential advantages, namely, low power consumption, lower sensitivity, ease of performing different functionalities with few passive components and a closed-loop bandwidth that is independent of dc gain, eliminating the gain-bandwidth product constraint [5]. In addition, they provide the best performance in applications such as filters, integrators and oscillators, etc. [6].

In our previous work [7–10], we have studied the optimization of analog circuits including CMOS current conveyors, a CFOA and a Butterworth active filter using the model-based method. In this paper, we propose an efficient method based on multi-objective simulation that uses both the circuit simulation to guarantee the accuracy of the approach and the advantage of optimization algorithms to search for the optimal solutions. We focus on optimizing the important performances of the LC-VCO and the CFOA. The LC-VCO performances are evaluated by the following specifications: phase noise (PN), oscillation frequency (f_{osc}) and power consumption (P_{diss}). Thus, the purpose is to perform a multi-objective optimization while minimizing the two functions PN and P_{diss} at a fixed oscillation frequency with a given control signal. For the CFOA, the goal is to perform simultaneous optimization of four objectives such as minimizing the two parasitic input resistances, as well as maximizing the current cut-off frequency and voltage cut-off frequency.

The rest of the paper is structured as follows. In Sect. 2 presents the proposed automated design approach. In Sect. 3 shows two application examples where the automated design approach is applied to CFOA and LC-VCO. The conclusion is drawn in Sect. 4.

2 Simulation-Based Method to Analog Circuits Design

The simulation-based approach uses electrical simulations in order to evaluate the performance of the circuit. It extracts the parameters of the circuits to be optimized/sized which correspond to the results of the performed simulation. This approach is seen as very flexible in comparison to other approaches (knowledge-based, equation-based) since it adapts to any circuit topology and offers higher accuracy (depending on the simulator models) [11–13]. As long as the objective functions are adapted, the circuit design can be optimized multiple times for various specifications. As a result, almost any kind of circuits can be designed with this method and with a short set-up time. The basic diagram of the simulation-based method is shown in Fig. 1. The main part of this approach is the optimization block which is built by a meta-heuristic approach with the aim of finding the component values (transistors, inductors, resistors, etc.) that will give the best performance of the circuit. The evaluation block of this method is built with a circuit simulator.

This method works as follows: Once the Netlist file of the circuit is created, the algorithm responsible for the optimization randomly generates the input parameter vector in this netlist file, then, it calls the circuit simulator (HSPICE in this case) to check the imposed constraints and evaluate the required performances. Once the constraints are checked, the found performances are stored in an output file. After this, the optimization process returns to the first step, in which it randomly generates new values for the circuit parameters. Then, the circuit simulator is run to check the imposed constraints and evaluate the performances. Once the constraints verified, the new found performances are compared to the ones already saved in the output file, if are better, they will be saved in the output file, if not they will be rejected and the process will return to the first step. At each iteration, the best chosen solutions from the output file are saved in an external archive using the dominance sorting technique [14]. The optimization and evaluation cycle will be stopped when the stop requirement is met, and the final external archive only contains the non-dominated solutions. The proposed tool flowchart is given in Fig. 2.

Fig. 1 The simulation-based approach

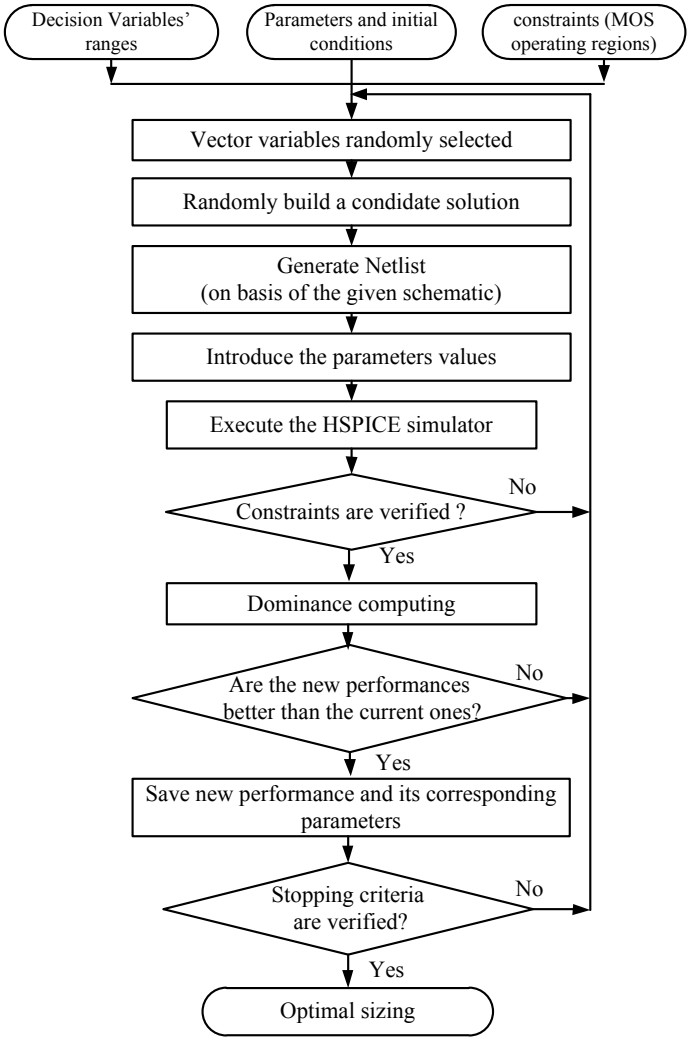

Fig. 2 The proposed tool flowchart

3 Simulation-Based Method Applications

3.1 CMOS LC-VCO

Figure 3 shows the LC-VCO circuit. The transistors M_{bias} are responsible for the polarization of the oscillator by I_{bias}. The inductor L and the capacitor C_{var} constitute the LC tank where, the variable capacitor C_{var} is designed by the transistor M_{var} as shown in Fig. 3, while the inductance L is designed by the 2 π-model shown in Fig. 4.

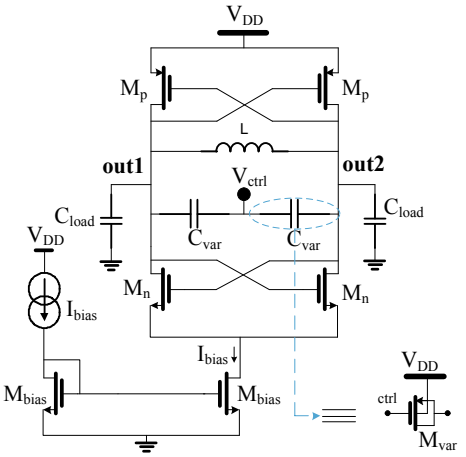

Fig. 3 CMOS LC-VCO topology

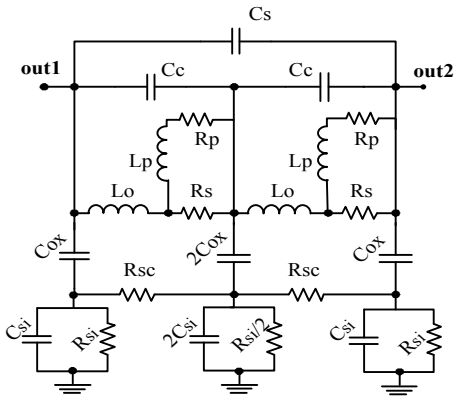

Fig. 4 Lamped inductor 2 π-model

The oscillation frequency is controlled by varying the capacitor C_{var} by the voltage C_{ctrl}.

In an integrated spiral, the parasitic interferences occur between the metal tracks of the spiral and the layers of oxide and substrate [12], these parasites are represented by the resistances R_i, the capacitances C_i and the inductances L_i, in the inductor equivalent model given in Fig. 4.

The LC-VCO has several important performances, such as: the oscillation frequency, the Phase Margin and the Power Consumption. Most oscillator designs aim to achieve both minimum power consumption and phase noise at a given oscillation frequency. For example, if we aim for low power consumption, the bias current of the circuit must be low. However, the parasitic effects caused by the low current will have a major effect in the behaviour of the circuit, leading to the phase noise degradation. But, if we aim for low phase noise, the bias current must be high, which will lead to high power consumption. Therefore, the most appropriate objective for

Table 1 LC-VCO encoding variables and decision space

Variable	Encoding	Decision space
x_1	f_{osc}	[1.5 GHz, 2.5 GHz]
x_2	Mn, Mp, Mbias	[0.4 µm, 1 µm]
x_3	Mvar	[0.4 µm, 10 µm]
x_4	Mn	[1 µm, 400 µm]
x_5	Mp	[1 µm, 400 µm]
x_6	Mbias	[1 µm, 400 µm]
x_7	Mvar	[1 µm, 400 µm]
x_8	C_c,C_S and C_{si}	[0.1 pF, 20 pF]
x_9	C_{ox}	[0.1 fF, 1 pF]
x_{10}	L_o, L_p	[0.01 nH, 10 nH]
x_{11}	R_s	[0.01 Ω, 30 Ω]
x_{12}	R_p	[1 Ω, 1 kΩ]
x_{13}	R_{sc}, R_{si}	[10 kΩ, 10 MΩ]

the oscillator design is to optimize simultaneously its phase noise and its power consumption. In other words, the objective is to find a set of solutions with the best trade-offs. There are thirteen design variables, their encoding and their decision space are given in Table 1.

The optimization was performed to generate a set of oscillator designs for a frequency band of 1.5–2.5 GHz using 0.13 µm RF CMOS technology with a power supply of 1 V. Two different experiments were investigated, firstly, the inductance L is considered to be ideal, secondly, the inductance is replaced by its equivalent 2π model. The objective is to find a set of optimal parameter values of the LC-VCO that correspond to the set of trade-offs between phase noise and power consumption for an ideal and real inductance. In both experiments, the optimization results are given in Fig. 5.

As can be seen, the optimization method offers the designer the best available designs for the specific trade-off. As expected, given ideal inductors, optimization results are quite better than those with real inductors. The values of the achieved performance corresponding to the obtained Pareto front edges are shown in Table 2.

3.2 LV LP CFOA

Figure 6 shows a CMOS implementation of the CFOA, it is a current mode device with 4-ports (X, Y, Z and W). The relationships between the CFOA ports can be, in the ideal case, expressed as [15].

$$i_y = 0, \quad i_x = i_z = v_x = v_y \quad \text{s} \; v_w \; = \; v_z \tag{1}$$

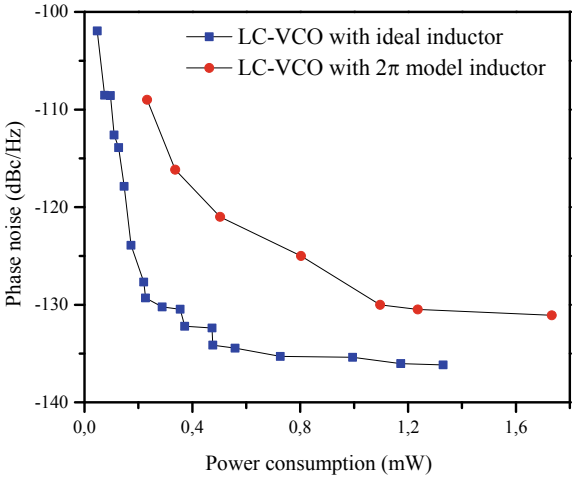

Fig. 5 The optimization results of LC-VCO

Table 2 The achieved performance values at Pareto front edges

	Phase noise (dBc/Hz)		Power (mW)		Oscillation frequency (GHz)	
Inductor type	Ideal	Real	Ideal	Real	Ideal	Real
Low Pareto front edge	−101.95	−109.23	0.0477	0.23	1.98	1.83
High Pareto front edge	−136.16	−131.08	1.33	1.73	1.57	1.52

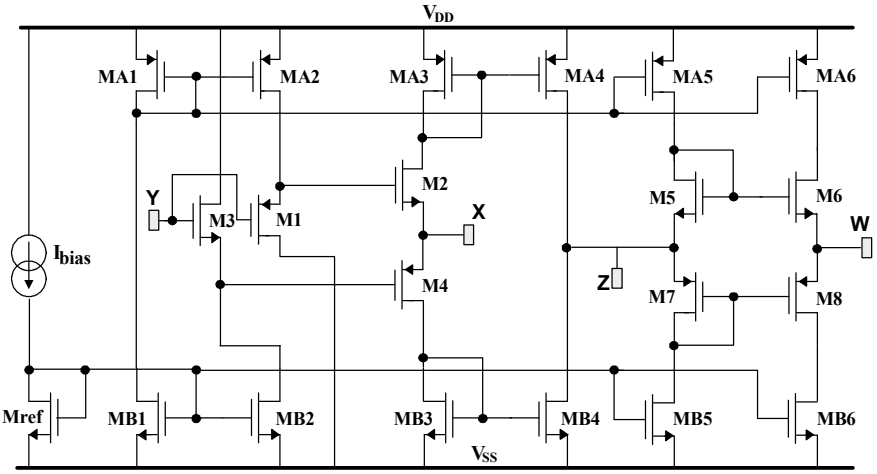

Fig. 6 CMOS CFOA circuit

Table 3 CFOA encoding variables and decision space

Variable	Encoding	Decision space
L_1	All NMOS transistors	[0.18 µm, 0.54 µm]
L_2	All PMOS transistors	[0.18 µm, 0.54 µm]
W_1	Mref,MB1-4	[1 µm, 100 µm]
W_2	M3	[1 µm, 100 µm]
W_3	M1	[1 µm, 100 µm]
W_4	M2	[1 µm, 100 µm]
W_5	M4	[1 µm, 100 µm]
W_6	MA1-4	[1 µm, 100 µm]
W_7	M5, M6, MB5, MB6	[1 µm, 100 µm]
W_8	M7, M8, MB7, MB8	[1 µm, 100 µm]
I_{bias}	Bias current	[0.1 µA, 20 µA]

where i_j and v_j are respectively the current and voltage at port j.

The CFOA is biased with ± 0.5 V and all simulations were done with the 0.18 µm CMOS process. All the CFOA transistors are encoded with W_i and L_i, i denotes a specific transistor or transistors sharing the same parameters. The variables encoding and their boundaries for this circuit are listed in Table 3.

For this circuit, we show the application of the proposed approach using two algorithms namely Multi-Objective Particle Swarm Optimization based on crowding distance (MOPSO-CD) [16] and multi-objective genetic algorithm (NSGA-II) [7, 17], to optimize the circuit performances. These algorithms have been programed in C++ and the circuit simulations are performed by HSPICE. For all algorithms, we use a population of 100 individuals and an iteration number of 200.

The objective is to find the optimal lengths and widths of the transistors that correspond to all the trade-offs between the chosen performances. For this, three different optimization experiments were performed using the proposed approach.

- First experiment: Minimizing the X-port resistance R_X and maximizing the Z-port frequency, f_{ciZ},
- Second experiment: Minimizing the W-port resistance R_W and maximizing the Z-port frequency, f_{ciZ},
- Third experiment: Minimizing the X-port resistance R_X and maximizing the W-port frequency, f_{ciW}.

In each experiment, we aim to generate the Pareto front of the two various objectives. The optimization results are given by Figs. 7, 8 and 9 for the first, second and third experiments, respectively.

By a simple observation, it is easy to see that for a specific cut-off frequency, the parasitic resistance obtained by MOPSO-CD is better than that generated by NSGA II, which means that the obtained results with the proposed method using MOPSO-CD are more improved (more optimistic).

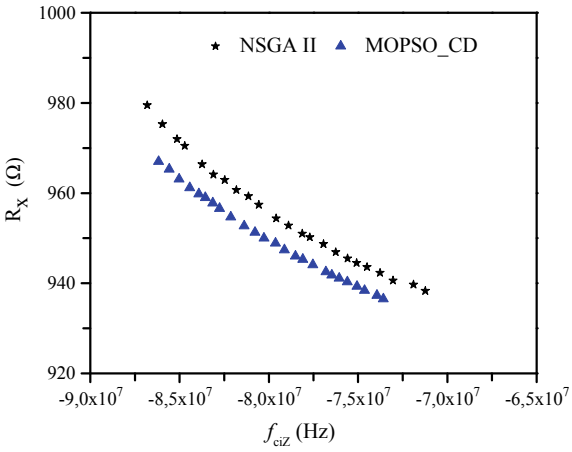

Fig. 7 Pareto front (R_X, $-f_{ciZ}$)

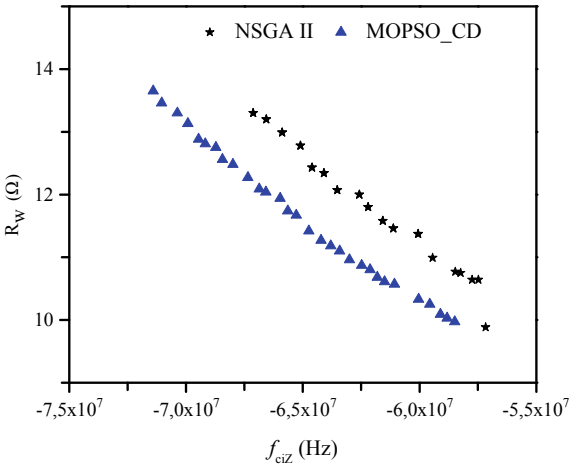

Fig. 8 Pareto front (R_W, $-f_{ciZ}$)

4 Conclusion

A simulation-based approach was used to optimize the performances of analog and RF circuits. This approach uses meta-heuristics to search for feasible solutions and HSPICE simulator to evaluate circuits performances. As a proof of concept, our work is focused on the design of LC-VCOs and a CFOA for low-voltage, low-power applications as multi-objective optimization problems. The multi-objective optimization choice allows us to deal with the various design trade-offs, i.e., phase noise and power consumption for the oscillator and parasitic resistances and cut-off frequencies for the CFOA. Based on the obtained results, the proposed approach provides very good results. Moreover, the obtained results are more improved when using the MOPSO-CD algorithm compared to the NSGA II. Our future work focuses on the integration

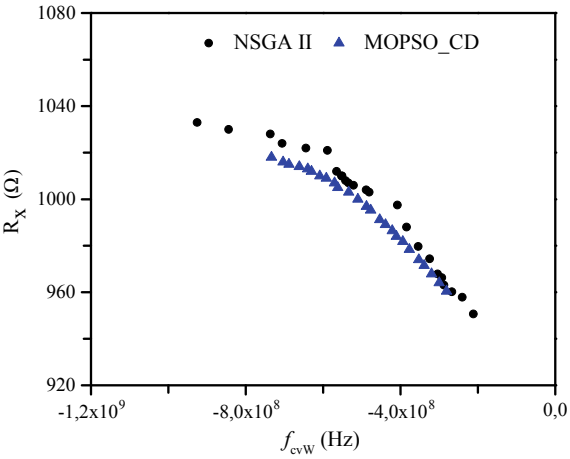

Fig. 9 Pareto front (R_X, $-f_{cvW}$)

of new optimization algorithms in the proposed approach, to combine their benefits in finding optimal solutions with the accuracy of the simulation-based method.

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