Analysis of MTCMOS Cache Memory Architecture for Processor

Reeya Agrawal and Vishal Goyal

Abstract In this paper, power reduction technique is applied over SRAM and sense amplifier and then calculate the power consumption through cadence tool. Over the conclusion of analysis, A Architecture of cache memory has been done with lowest leakage power. In this paper from different sense amplifiers, we conclude that Charge-Transfer SA have lowest power dissipation, i.e.,11.06 μW. SRAM has 220.078 μW power dissipation after applying leakage power reduction technique such as MTCMOS_technique, Footer Stack Technique, Sleepy Keeper Technique and Sleep-Stack Technique, and there is 98–99% reduction and 75–76% reduction in Charge-Transfer SA. So, after all conclusion, architecture has been made with MTCMOS SRAM memory and MTCMOS Charge-Transfer SA with 98% reduction in power dissipation. This paper describes that MTCMOS_technique applied over different circuits reduces leakage power reduction as well as SRAM and CTSA with MTCMOS_technique in architecture gives low power consumption for a cache memory.

Keywords MTCMOS CTSA (charge-transfer sense amplifier with MTCMOS_technique) · MTCMOS SRAM (Static Random Access memory with MTCMOS_technique) · SA (Sense Amplifier)

1 Introduction

In today's world, technology needs low power dissipation devices. Due to portable handle devices as they have low number of power plugs at their surrounding, i.e., they need a high battery backup devices [1] which consume less amount of energy during non-working process and as well as in working process.

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Table 1 Power dissipation of different techniques applied on SRAM

S. No.	SRAM with techniques	Power consumption (μW)
1	SRAM	220.078
2	MTCMOS SRAM	89.91
3	Sleep-stack SRAM	135.92
4	Sleepy keeper SRAM	133.39
5	Footer stacked SRAM	118.72

Table 2 Power dissipation of different sense amplifiers

S. No.	Sense amplifier	Power consumption (μW)
1	Voltage mode sense amplifier	86.66
2	Current-mode sense amplifier	54.21
3	Charge-transfer sense amplifier	11.06
4	Voltage latch sense amplifier	419.502
5	Current latch sense amplifier	152.89

In proposed work, a design is made under convince of day to day life as it consumes less amount of energy. In this architecture [2], we apply MTCMOS technique over SRAM cell because after applying leakage reduction techniques, we compare all SRAM cell as shown in Table 1 conclusion arises that SRAM with MTCMOS technique consumes lowest power. Similarly, from Table 2, conclusion arises that VMSA, CMSA and CTSA consume lowest power among all sense amplifiers. Due to this reason, leakage reduction techniques [3] are applied over VMSA, CMSA and CTSA. And from Tables 1 and 2, architecture is form of MTCMOS SRAM, WDC, PCH and VMSA, CMSA and CTSA, respectively.

After this analysis, A "MTCMOS CACHE MEMORY ARCHITECTURE" is formed which is made up [4] of MTCMOS SRAM, PCH, WDC and MTCMOS CTSA which shows 98–99% less power consumption [5].

2 MTCMOS Cache Memory Architecture

2.1 Write Driver Circuit

When discharging bl (bit lines) voltage, then WDC reduces the write margin of "SRAM" from highest PCH value [6] as shown in Fig. 1.

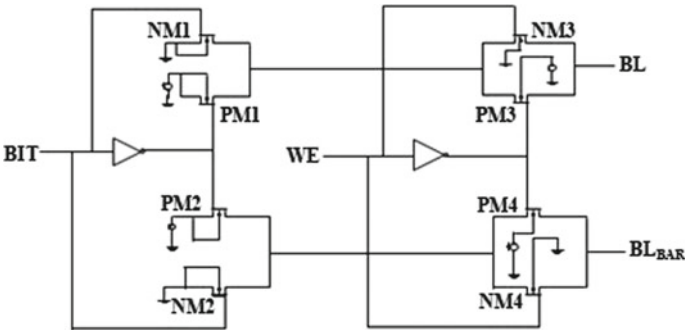

Fig. 1 Write driver circuit schematic

2.2 *Conventional SRAM*

"SRAM" is a 6T design. SRAM works as a cache memory in computers. It is used to store a data. It is made by connection of two invertors back to back with two complementary transistors [7]. The "read" and "write" operations can be done through bit lines in "SRAM" cell as shown in Fig. 2. It is popular due to its high stability property and lowest "static" power dissipation. "Access" transistors which are connected to the bl (bit_lines) are in working process when write line (wl) is enabled so "read" and "write" operation can be done [8]. Figure 3 shows the 8T design, i.e., 6T SRAM cell with 2T technique, i.e., MTCMOS technique [13].

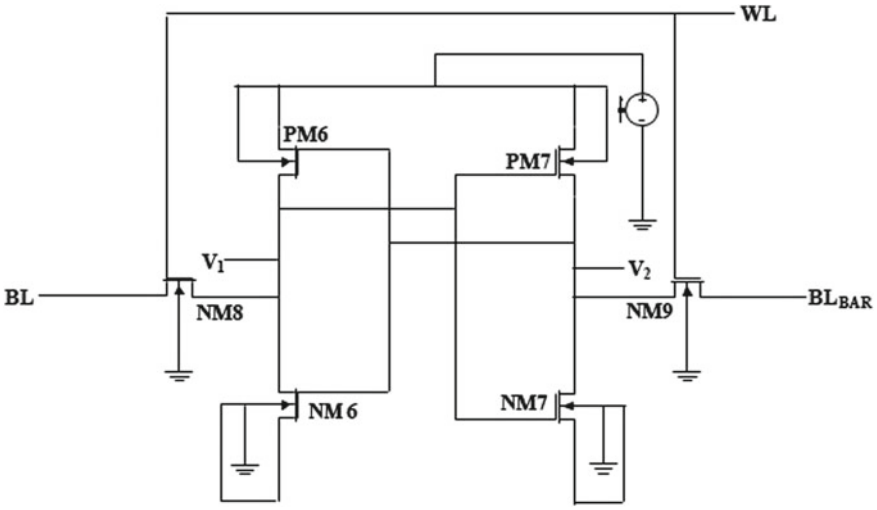

Fig. 2 Conventional SRAM circuit diagram

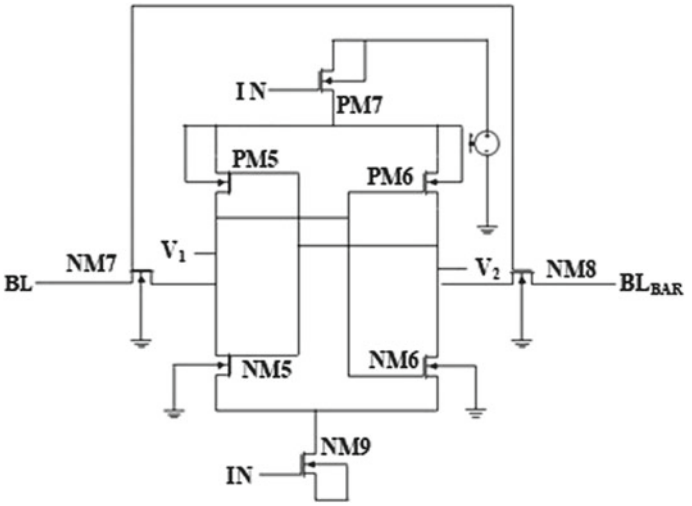

Fig. 3 MTCMOS SRAM cell

2.3 Sense Amplifier's

2.3.1 Voltage Mode Sense Amplifier

For sensing the potential difference at bit capacitance, VMSA requires differential discharging [9]. Some voltage differential is developing at bl when WL is enabling. Saen is enabled when sufficient voltage differential is developed in VMSA due to which interconnected inverters follow +ve feedback loop and convert the difference in o/p to full rail o/p [10]. Figure 4 presents the electrical picture of VMSA.

2.3.2 Current-Mode Sense Amplifier

The CMSA manage by sensing the bit_lines current. CMSA does not depend on variation in voltage value developing on bl (bit_lines). It is suitable in reducing the bit line (bl) voltage considering that low voltage at bit line can be clamped at high voltage. Figure 5 presents the electrical diagram of CMSA [11].

2.3.3 Charge-Transfer Sense Amplifier

CTSA works on a principle of charge rearrangement, i.e., from high capacitance bl to low capacitance SA o/p points. Due to this, CTSA consume low power [12]. Figure 6 presents the electrical diagram of CTSA. The circuit is divided into two parts. In first part, CG cascade made with P_1, P_3 and P_5 (and P_2, P_4 and P_6). The pmos

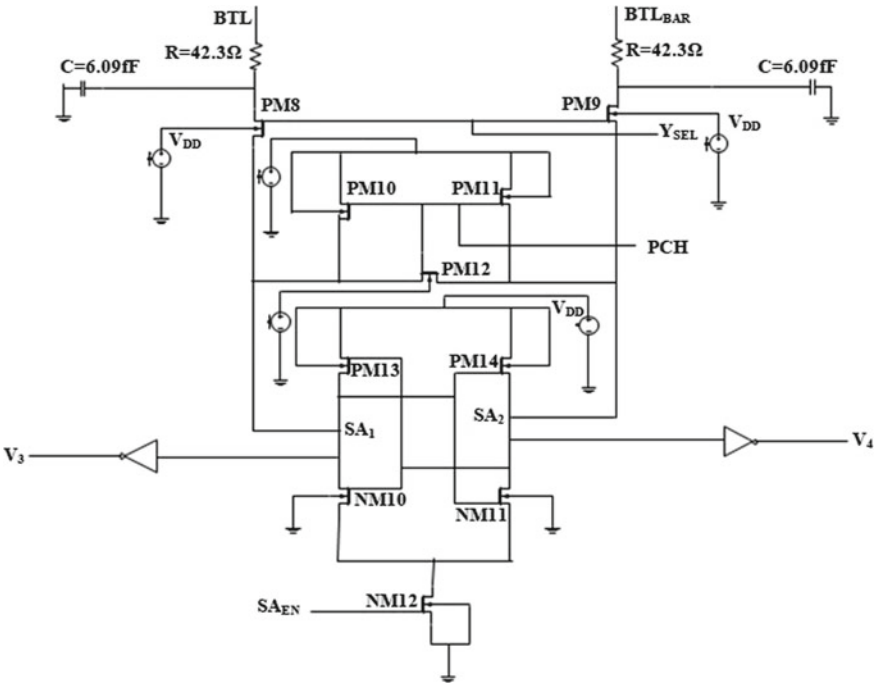

Fig. 4 VMSA schematic

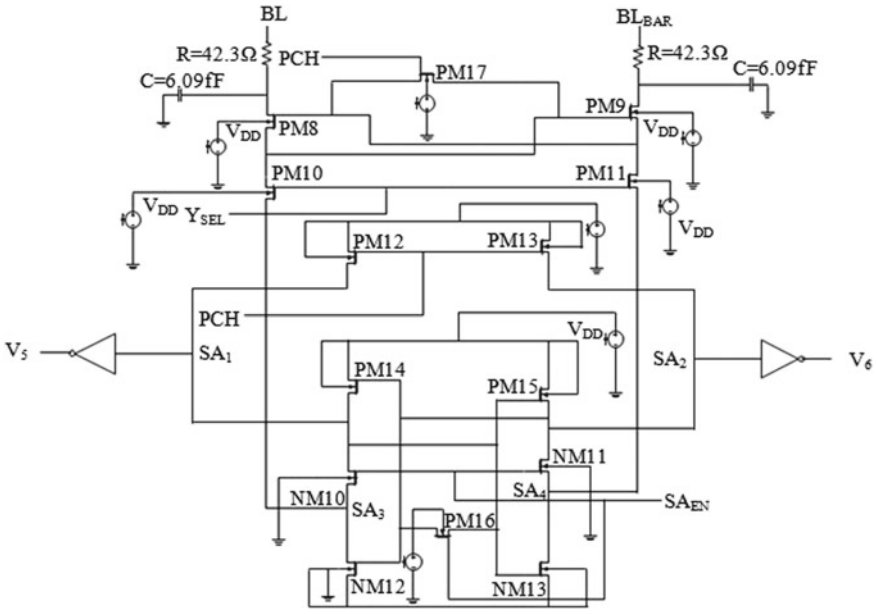

Fig. 5 CMSA schematic

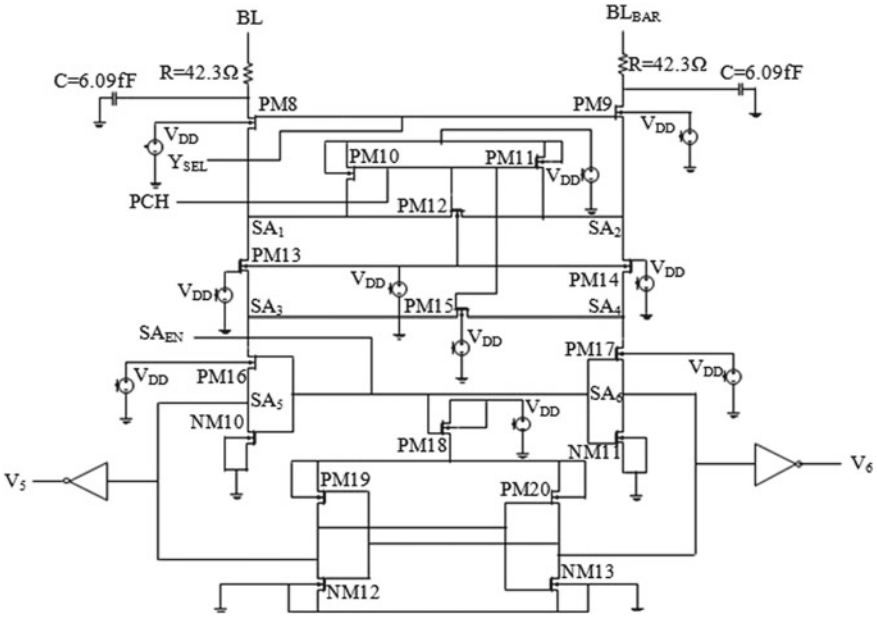

Fig. 6 CTSA Schematic

P_1 and P_2 are biased at potential Vb. In second part, P_7 through N_11 latches made cross-coupled inverters.

2.3.4 Voltage Latch Sense Amplifier

Figure 7 is a VLSA electrical diagram. P_1, P_2, N_1 and N_2 form the inverters. Differential voltage o/p bit line (bl) converted into full-swing o/p by inverter. The internal node of circuit is charged through bit lines (bl). Difference creates on internal nodes by input bit lines operates the electrical design [13].

2.3.5 Current-Latch Sense Amplifier

CLSA is popular due to low power consumption and an automatic power saving scheme as shown in Fig. 8. In read cycle, small difference on bit line (bl) is a data of cell [14]. The two gates n1 and n2 are connected to bl and blb. The serially connected latch circuit is controlled by current flow of two n-mos.

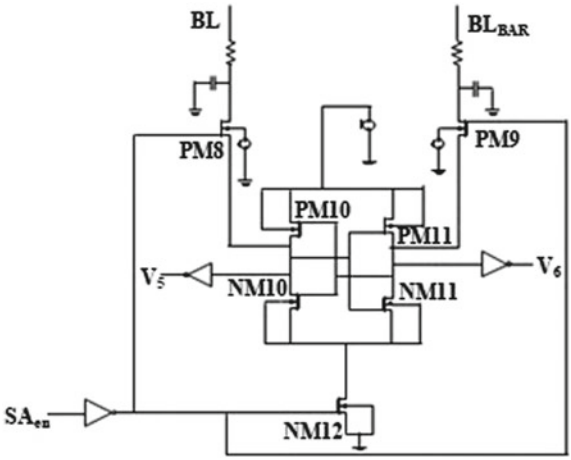

Fig. 7 VLSA schematic

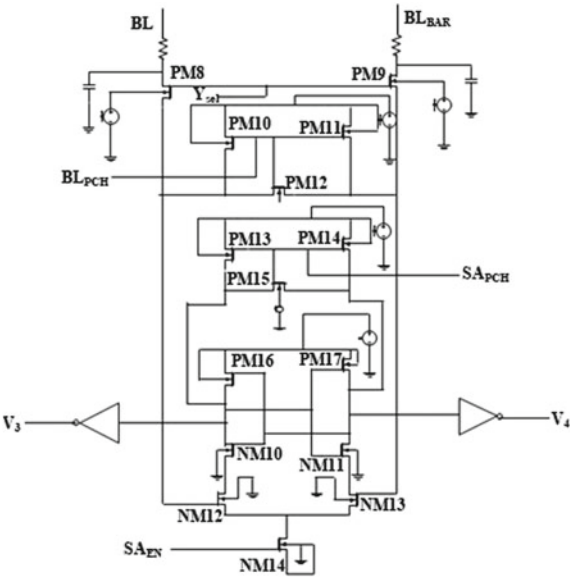

Fig. 8 CLSA schematic

3 Analysis of Result

Figure 10 represents the block structure of Single Bit MTCMOS CACHE MEMORY ARCHITECTURE [15] implemented with MTCMOS SRAM and MTCMOS CTSA (Fig. 9).

Cache memory architecture made of WDC, PCH Circuit, "SRAM" cell and sense amplifier, i.e., CTSA. Every block is evaluated and described below with their outputs [16].

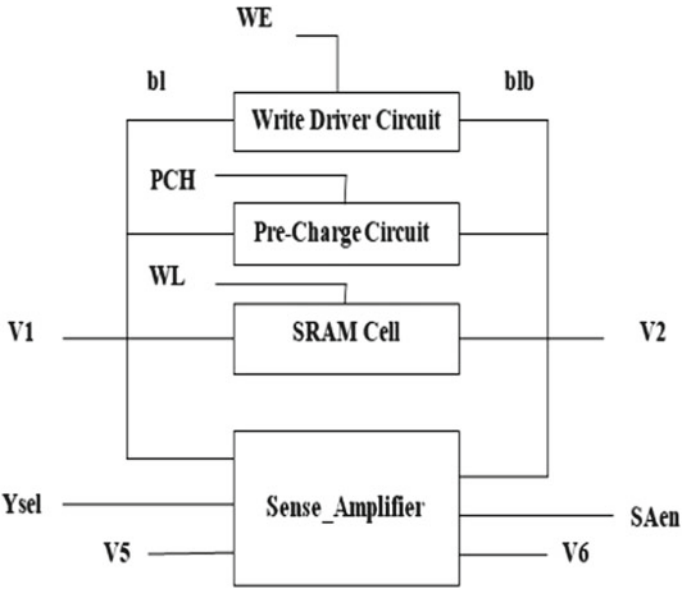

Fig. 9 Block structure of single-bit MTCMOS cache memory architecture

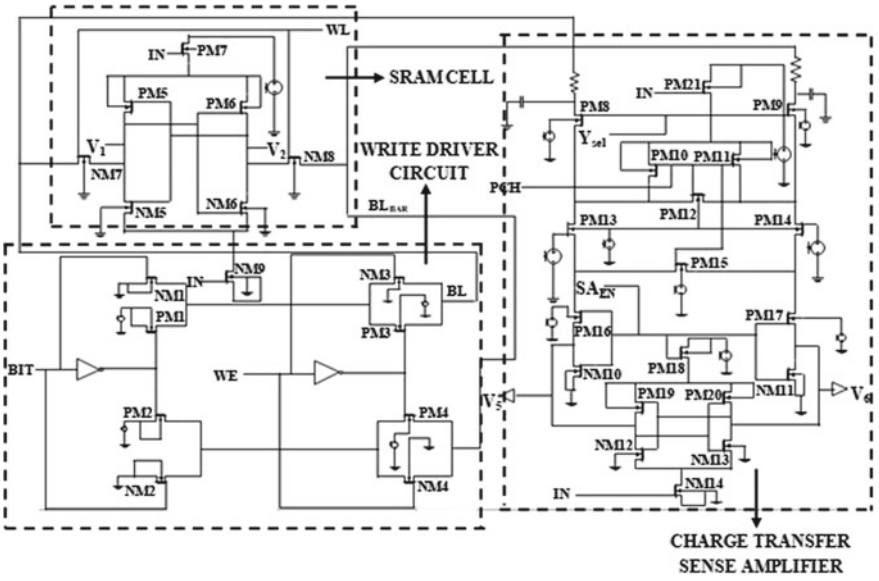

Fig. 10 Circuit Diagram of MTCMOS CACHE MEMORY ARCHITECTURE

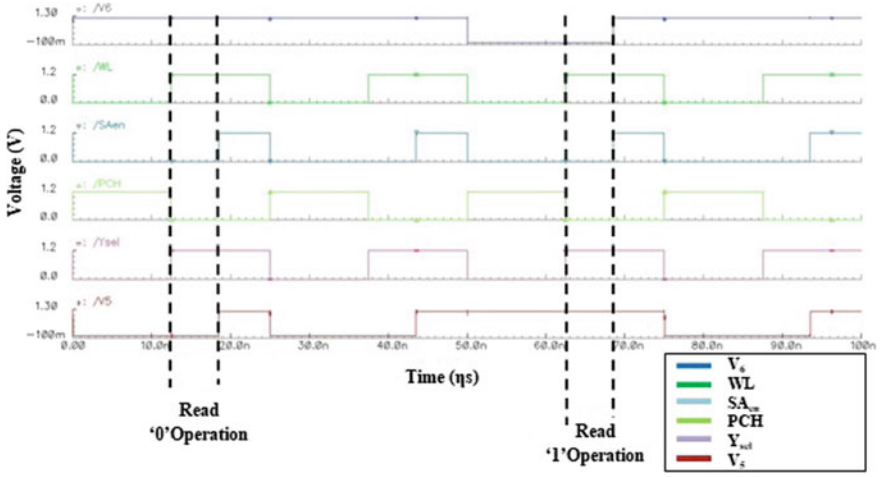

Fig. 11 Output waveform of MTCMOS CACHE MEMORY ARCHITECTURE

Figure 10 shows single-bit MTCMOS CACHE MEMORY ARCHITECTURE. The output from WDC is connected to the bit lines of SRAM Cell. O/p is stored in memory cell when write line (i.e., WL = 1) is enabled. Sense amplifier turns on when Saen = 1 [17]. Figure 13 represents the o/p wave form of "MTCMOS CACHE MEMORY ARCHITECTURE". When bl is charged up to Vdd by PCH circuit, read and write operation can be done. When WE = 1, bit line stored the o/p data, and by charging and discharging the bit lines, write operation can be performed. Now, charge the bit lines up to V_dd (i.e., bl = Vdd), and the SA sensed the change in voltage at o/p points. The o/p matches the data saved in "SRAM" cell, which represent "read 0" and "read 1" operation (Fig. 11).

Table 1 displays the "power dissipation" of SRAM and SRAM with different leakage reduction techniques, whereas Table 2 demonstrates the power dissipation of different sense amplifiers. As today's need is device with low power consumption, so different leakage reduction techniques are applied over different sense amplifiers as shown in Table 3.

From Table 2, conclusion arises that VMSA, CMSA and CTSA consume low power among all five types of sense amplifier, due to this reason, a Single-Bit Cache Memory Architecture is designed using VMSA, CMSA and CTSA, and their power consumption analysis has been seen as shown in Table 4.

From Table 1, conclusion arises that SRAM with MTCMOS technique consumes low power, and from Table 2, conclusion arises that Charge-Transfer sense amplifier consumes lowest power, and from Table 3, conclusion arises that CTSA with MTCMOS technique consume low power. So, now architecture has been designed having SRAM with MTCMOS technique, PCH, WDC and CTSA with MTCMOS technique, and the complete structure is known as "MTCMOS CACHE MEMORY

Table 3 Power dissipation of sense amplifiers using leakage power reduction techniques

S. No.	Technique	SA				
		VLSA (μW)	CLSA (μW)	CTSA (μW)	VLSA (μW)	CLSA (μW)
1	Forced-stack technique	52.94	5.54	2.587	257.102	109.838
2	MTCMOS technique	53.21	5.482	2.59	255.344	64.79
3	Sleep-stack technique	65.19	6.726	2.64	265.625	127.383
4	Sleepy keeper technique	53.18	6.738	2.66	261.103	108.154

Table 4 Power dissipation of CACHE MEMORY with different sense amplifiers

S. No.	Architecture	Power consumption (μW)
1	SRAM with VMSA	266.821
2	SRAM with CMSA	274.296
3	SRAM with CTSA	231.293

Table 5 Conclusion of all tables using different techniques over architecture

Power consumption of SRAM with CTSA in memory architecture	Power consumption of modified SRAM with CTSA in memory architecture	Power consumption of SRAM with modified CTSA in memory architecture	Power consumption of modified SRAM with modified CTSA in memory architecture
231.293 μW	11.30 μW	112.876 μW	2.00 μW

ARCHITECTURE". There is 98–99% decrement in power consumption in new design as shown in Table 4 (Table 5).

4 Conclusion

In presented work, MTCMOS CACHE MEMORY ARCHITECTURE has been implemented with MTCMOS SRAM (i.e., SRAM with MTCMOS_technique) and MTCMOS CTSA (i.e., CTSA with MTCMOS_technique). Analysis concludes that MTCMOS CACHE MEMORY ARCHITECTURE with MTCMOS CTSA offers a much superior performance in terms of reduction in power dissipation. It was found that MTCMOS technique implemented in any circuit gives 75–76% reductions in power dissipation and MTCMOS CACHE MEMORY ARCHITECTURE consumes 98–99% less power as compared to conventional architecture. Furthermore, this

work has been implemented in array form of MTCMOS CACHE MEMORY ARCHITECTURE.

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