Impact of Temperature on DC and Analog/RF Performance for DM-DG-Ge Pocket TFET

Kumari Nibha Priyadarshani, Sangeeta Singh, and Alok Naugarhiya

Abstract This work illustrates the effect of temperature on the performance of dualmetal double-gate Ge pocket TFET with hetero-dielectric. The study reveals that the performance of DM-DG-Ge pocket TFET improves with an increase in temperature. Both the DC and analog/RF parameters improve with increase in temperature, whereas I_{ON}/I_{OFF} decreases with an increase in temperature due to higher increase in OFF current than ON current. The improvement in DC and analog/RF parameters makes the device suitable for operation at the higher temperatures.

Keywords TFET · Temperature · Dual gate · Hetero-dielectric

1 Introduction

TFET has gained huge interest of researchers and industry due to its low-power circuit application, low off-state leakage current, low SS and thus fast switching $[1–8]$ $[1–8]$. The main agenda of TFET is to achieve low SS as 60 mV/decade is the thermionic transport limitation of MOSFET. The transport mechanism of TFET is completely different from MOSFET, and it works on band-to-band tunneling mechanism removing SS limitation. TFET is also immune to short-channel effects. The limitation of TFET is low ION and ambipolar current [\[9\]](#page-6-1). Researchers have found performance improvement with low band gap material, n^+ pocket region, double gate, double metal gate, etc. [\[5,](#page-6-2) [10–](#page-6-3)[12\]](#page-6-4). Further, with low *k* dielectric ambipolar current suppression can be achieved. Dual-metal double-gate Ge pocket TFET (DM-DG-Ge pocket TFET) with hetero-dielectric consists of the advantage of both dual-metal double-gate and hetero-dielectric. This work reports the investigation on performance of DM-DG-Ge pocket TFET at higher temperatures. The study has been done for a wide range of temperatures, viz 250–500 K.

135

K. N. Priyadarshani \cdot S. Singh (\boxtimes) National Institute of Technology Patna, Patna, India e-mail: sangeeta.singh@nitp.ac.in

A. Naugarhiya National Institute of Technology Raipur, Raipur, India

[©] The Author(s), under exclusive license to Springer Nature Singapore Pte Ltd. 2021 V. Goyal et al. (eds.), *Proceedings of International Conference on Communication and Artificial Intelligence*, Lecture Notes in Networks and Systems 192, https://doi.org/10.1007/978-981-33-6546-9_14

In this work, DC and analog/RF performance parameter such as V_{TH} , I_{ON} , I_{ON}/I_{OFF} , SS, g_m , C_{gd} , C_{gg} , f_T , GBW, TGF and TFP analysis has been done with variation in temperature for DM-DG-Ge pocket TFET.

2 Device Structure and Simulation models

2D cross-sectional structure of DM-DG-Ge pocket TFET with hetero-dielectric is shown in Fig. [1.](#page-1-0) The source region is of $Si_{0.5}Ge_{0.5}$, the pocket region is of Ge, and the source and the channel regions are of silicon. With pocket width (L_{pocket}) 3 nm, t_{ox} as 1.2 nm, $L_G = 20$ nm and body thickness (*t*) is 8 nm. The length of auxiliary gate ($L_{\text{auxiliary}}$) and tunneling gate ($L_{\text{tunneling}}$) is $L_G/2$. The oxide material used is HfO₂ under tunneling gate and $SiO₂$ under auxiliary gate. Further, the doping in source region is $N_{\text{source}} = 10^{20} \text{ cm}^{-3}$, in pocket region is $N_{\text{pocket}} = 4 \times 10^{19} \text{ cm}^{-3}$, in channel region is $N_{\text{channel}} = 10^{16} \text{ cm}^{-3}$, and in drain region is $N_{\text{drain}} = 10^{20} \text{ cm}^{-3}$. The work function of gate metal for tunneling gate is ($\Phi_{\text{tunn}} = 4.6 \text{ eV}$) and for auxiliary gate is ($\Phi_{\text{aux}} = 4.2 \text{ eV}$). Mo, Ta and W metals can be used for tunneling gate metal, and Ti–Ni and $IrO₂$ can be used for auxiliary gate metal.

All simulation has been carried out on Atlas Silvaco device simulator [\[13\]](#page-6-5). Silvaco solves Poisson's equation with the current continuity equation self-consistently. Nonlocal band-to-band tunneling has been considered for precise modeling of tunneling. Kane model has also been considered with default value of material parameters. Band gap narrowing, Shockley–Read–Hall recombination and Fermi–Dirac model have also been considered for precise modeling of device. The body thickness of device is 8 nm; hence, quantum confinement effect has not been considered.

3 Result and Discussion

The property of semiconductor material depends on temperature. Thus, operating temperature indirectly influences the performance of device. The dependence of energy band gap on temperature is as depicted in the following equation:

$$
E_{\rm g}(T) = E_{\rm g}(0) - \left(\frac{\alpha T^2}{T + \beta}\right) \tag{1}
$$

where $E_{\varphi}(T)$ is the energy band gap at temperature *T* K. $E_{\varphi}(0)$ is the energy band gap at 0 K, and α and β are fitting parameters of semiconductor material.

Equation 1 shows that the energy band decreases with increase in operating temperature. The carrier transport of device depends on band-to-band tunneling (BTBT) of electron from valence band of source region to conduction band of channel region. Thus, the drain current can be evaluated by Kane model, given by

$$
I_{\rm DS} = D^2 A_{\rm kane} V_{\rm gs} E_{\rm g}^{-1.5} \times \exp\left(\frac{-B_{\rm kane} E_{\rm g}^{-1.5}}{V_{\rm gs} \times D}\right) \tag{2}
$$

Here, *D*, A_{kane} and B_{kane} are constant parameters and E_{g} is energy band gap of material. So, drain current is indirectly dependent on temperature. With increase in temperature, energy band gap of semiconductor decreases, and with decrease in energy band gap, the drain current increases as depicted in Eq. [\(2\)](#page-2-0).

3.1 DC Performance Analysis

With increase in temperature, the drain current increases. Both I_{ON} and I_{OFF} increase, but the increase in ON current is less in comparison with the increase in OFF current. Thus, the I_{ON}/I_{OFF} decreases with increase in temperature. V_{TH} , g_m and SS also improve with increase in temperature. The variation in device parameter with increase in temperature is shown in Table [1.](#page-3-0) With increase in temperature from 250 to 500 K, the decrease in V_{TH} is 4%, increase in I_{ON} is 799.5%, increase in I_{OFF} is ~10⁷, and decrease in I_{ON}/I_{OFF} is ~107. Further, the increase in transconductance (g_m) is 552.7% and improvement in SS is 10.8%.

3.2 Analog/RF Performance Parameter Analysis

Further, the analog and RF parameter analysis with variation in temperature has been done. Figure [2a](#page-3-1) shows the $I_D - V_G$ at $V_D = 0.5$ V for DM-DG-Ge pocket TFET, and it shows the increase in drain current with V_{GS} variation at different temperatures. The ambipolar current is fully suppressed for the DM-DG-Ge pocket TFET as shown in figure. The increase in $I_D - V_G$ with increase in temperature from 250 to 500 K is 799.5%. Figure [2b](#page-3-1) shows the $I_D - V_D$ at $V_G = 0.5$ V for DM-DG-Ge pocket TFET. The figure shows increase in drain current with the drain voltage variation at

Temp (K)	V_{TH} (V)	I_{ON} (μ A/ μ m)	I_{OFF} (pA/ μ m)	I_{ON}/I_{OFF}	gm $(mS/\mu m)$	SS (mV/decade)
250	0.4522258	1.98	5.58×10^{7}	$3.54 \times$ 10^{12}	41.47	11.07
300	0.449525	3.11	2.56×10^{7}	$1.21 \times$ 10^{13}	61.62	15.63
350	0.446228	4.89	3.76×10^{4}	$1.30 \times$ 10^{10}	91.08	17.41
400	0.442189	7.60	1.68×10^{2}	$4.52 \times$ 10^{8}	131.49	17.14
450	0.438105	11.69	3.44×10^{1}	$3.39 \times$ 10 ⁷	188.97	16.06
500	0.434166	17.81	4.02	$4.43 \times$ 10 ⁶	270.61	15.53

Table 1 Device characteristic with variation in temperature

Fig. 2 a $I_D - V_G$ at $V_D = 0.5$ V and **b** $I_D - V_D$ at $V_G = 0.5$ V for DM-DG-Ge pocket TFET

higher temperatures. The analog analysis is done at 1 GHz frequency. The C_{gd} and C_{gg} are shown in Fig. [3a](#page-4-0), b, respectively. Capacitance values are also increasing with increase in the temperature.

Further, Fig. [4a](#page-4-1), b shows g_m and g_d with the variation in temperature, respectively. For analog applications of device in OPAMP, differential amplifier, etc., circuit designer needs device to have higher g_m in order to get higher amplification ($A_V =$ $g_{\rm m}/g_{\rm d} = g_{\rm m}R_{\rm o}$). The $g_{\rm m}$ of the device increases with increase in temperature and thus suitable for higher gain. Lesser g_d value is needed for higher gain. However, g_d increases with increase in temperature. This shows that R_0 decreases with increase in temperature, giving rise to drain current. Figure [5a](#page-4-2), b shows f_T and GBW of device with variation in temperature, respectively. The circuit designer needs the device to work as amplifier for higher frequency. Cut-off frequency f_T is the maximum frequency at which the gain of device becomes unity. After this frequency, the device

Fig. 3 a C_{gd} and **b** C_{gg} at $V_D = 0.5$ V for DM-DG-Ge pocket TFET

Fig. 4 a g_m at $V_D = 0.5$ V and **b** g_d at $V_G = 0.5$ V for DM-DG-Ge pocket TFET

Fig. 5 a f_{T} and **b** GBW at $V_{\text{D}} = 0.5$ V for DM-DG-Ge pocket TFET

Fig. 6 a TGF and **b** TFP at $V_D = 0.5$ V for DM-DG-Ge pocket TFET

could not work as amplifier. f_T is defined as $f_T = g_m/2\pi C_{gg}$. The f_T of DM-DG-Ge pocket TFET increases with increase in temperature. The GBW is the operating frequency and voltage gain product. GBW is defined as $GBW = g_m/2\pi 10C_{gd}$. It is a constant value, for a DC voltage gain of 10; the GBW is shown in the figure. It increases with increase in temperature. Figure [6a](#page-5-1), b shows TGF and TFP of DM-DG-Ge pocket TFET, respectively. It is defined as $TGF = g_m/I_D = \ln(10)$ /SS. SS value is being low in transition region from ON to OFF. The TGF value achieves its maximum and then again decreases. TFP describes power bandwidth trade-off.

and is important parameter for design of moderate to high-speed circuit. It is defined as TFP = $(g_m/I_D) \times f_T$ = TGF $\times f_T$. TFP also increases with increase in temperature.

4 Conclusion

An exhaustive analysis of temperature sensitivity of DM-DG-Ge pocket TFET has been presented in this work. The study reports excellent improvement in DC parameter as well as analog/RF performance parameters with increase in temperature. The study shows improvement in g_m , f_T , GBW, TGF and TFP with operating temperature increase, thus making it suitable for application in higher temperature ranges.

Acknowledgements The authors are grateful to the National Institute of Technology, Raipur, India, for providing the computational resources.

References

1. Seabaugh AC, Zhang Q (2010) Low voltage tunnel transistors for beyond CMOS logic. Proc IEEE 98(12):2095–2110

- 2. Ionescu AM, Riel H (2011) Tunnel field-effect transistors as energy effcient electronic switches. Nature 479(7373):329–337
- 3. Ionescu AM, De Michielis L, Dagtekin N, Salvatore G, Cao J, Rusu A et al (2011) Ultra low power: emerging devices and their benefits for integrated circuits. IEDM Tech Dig: 1611–1614
- 4. Nigam K, Kondekar P, Sharma D (2016) DC characteristics and analog/RF performance of novel polarity control GaAs-Ge based tunnel field effect transistor. Superlattices Microstruct 92:224–231. ISSN 0749–6036
- 5. Boucart K, Ionescu AM (2007) Double gate tunnel FET with high-k gate dielectric. IEEE Trans Electron Devices 54(7):1725–1733
- 6. Kumar MJ, Janardhanan S (2013) Dopingless tunnel field effect transistor: design and investigation. IEEE Trans Electron Devices 60(10):3285–3290
- 7. Leung G, Chui CO (2013) Stochastic variability in silicon double-gate lateral tunnel field-effect transistors. IEEE Trans Electron Devices 60(1):89–91
- 8. Shrivastava V, Kumar A, Sahu C, Singh J (2016) Temperature sensitivity analysis of dopingless charge-plasma transistor. Solid-State Electron 117:94–99
- 9. Avci UE, Rios R, Kuhn KJ, Young IA (2011) Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET. In: 11th IEEE international conference on nanotechnology, IEEE, pp 869–872
- 10. Saurabh S, Kumar MJ (2009) Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor: Theoretical investigation and analysis. Jpn J Appl Phys 48(6R):064503
- 11. Krishnamohan T, Kim D, Raghunathan S, Saraswat K (2008) Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) with record high drive currents and << 60 mV/dec subthreshold slope. In: IEEE international electron devices meeting. IEEE, pp 1–3
- 12. Li W, Woo JC (2018) Optimization and scaling of Ge-pocket TFET. IEEE Trans Electron Devices 65(12):5289–5294
- 13. Atlas AUM (2015) Silvaco international. Santa Clara, CA