Design Optimization of Doping-less InGaAs TFET and GaAs/Si-Heterojunction Doping-less TFET for Potential Breast Cancer Sensing Applications

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Abstract This work demonstrates in-depth comparative analysis for the performance optimization of doping-less InGaAs TFET and GaAs/Si-heterojunction doping-less TFET (GaAs/Si-HJDL-TFET). As doping-less TFET is a prominent device in terms of lower sub-threshold slope (SS)(<60 mV/decade) and it realizes steep switching speed. Lower bandgap materials such as InGaAs are deployed, which results in the narrowing of tunneling width which causes a large amount of carriers that can tunnel across the source-channel junction and thereby increases the drive current significantly. Moreover, to suppress the ambipolar current, heterojunction structure is very helpful. Furthermore, device structure optimization has been achieved with the mole fraction (x) composition variation of $In_{(1-x)}Ga_xAs$ in both the devices. Study reveals that GaAs/Si-HJDL-TFET structure represents enhanced performance in terms of lower SS, minimum threshold voltage and greater I_{ON}/I_{OFF} ratio. Interestingly, the charge sensitive characteristics of the reported device can be deployed for detection of C-erbB-2 protein, the breast cancer bio-marker sensing applications.

Keywords Hetero-junction · Doping-less · Bio-marker

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1 Introduction

As the semiconductor industry is stepping toward the sub-10 nm regime, it imposes more challenges on the conventional MOSFET, when different scaling techniques are applied in terms of increasing the complexity in the fabrication of device and the short channel effects (SCEs) [1]. Various emerging device structures have been investigated to overcome these problems such as DG-MOSFET, SOI MOSFET, junctionless nanowire transistor, gate-all around MOSFET, etc. All the devices listed above employs the thermionic emission as a current gating mechanism, which restricts its sub-threshold slope (SS) to Boltzmann limit, i.e., 60 mV/decade. Therefore, for reducing the SS below 60 mV/decade, the device conduction mechanism has to be different. For the future switching transistor technology, the TFETs have drawn huge attention of researchers because of its ability to achieve SS below Boltzmann limit (60 mV/decade), which works on band-to-band-tunneling phenomenon [2–5] Further, due to its exceptionally low leakage current, lower V_{th} and immunity toward various short channel effects (SCEs), it is a predominant device to be used for the low power application. Moreover, TFET performance is restricted due to its limited ON-state current because of less transmission probability of band-to-band tunneling, random dopant fluctuations (RDFs), ambipolar current, etc. Many device engineering techniques have been employed with TFET to overcome these issues such as dual material TFET, double gate TFET, n^+ pocket doped TFET, hetero-junction TFET, doping-less TFET, [6–15]. It is quite challenging to fabricate TFET at nanoscale dimensions, thus doping-less TFET has been reported to reduce this process. The work function engineering has been done on source and drain side for implementing doping-less TFET [16] by choosing appropriate metal with required work function for source as well as drain electrodes, and electrons and holes carriers are induced in the semiconductor layer beneath these electrodes. n^+ region can be formed toward drain side by incorporating hafnium (Hf) (w.f. = 3.9 eV). On the other hand, side p^+ region can be formed toward source by considering platinum (Pt)(w.f. = 5.93 eV) [17]. Moreover, to reduce the problem of lower I_{ON} current, the hetero-junction DL-TFETs, line charge III-V group compound-based DL-TFET are of great interest, because of the inherently high carrier mobility, composition-dependent bandgap variation and lower effective masses of their carriers [18]. The band tuning of low bandgap (III-V) material-based compounds in the source region has been explored to improve the tunneling current and to reduction of the tunneling width [19–21]. The major disadvantage of using III-V group hetero-junction TFETs is that they realize significantly increased OFF-state current in comparison to conventional Si-TFETs [22] Hence, to suppress the OFF-state current and to increase the ON-state current, device structural optimization along with source material engineering must be done. In this regard, different device structures have been explored such as *L*-shaped/*U*-shaped TFET [23], vertical TFET [24, 25] and source pocket engineered TFET [5]. These concurrent research findings inspired the authors for analysis and optimization of the performance of doping-less InGaAs TFET and GaAs/Si-hetero-junction doping-less TFET (GaAs/Si-HJDL-TFET). Here, the device performance

has been improvised by deploying the parametric sweep optimization. Firstly, the basic Si-TFET structure is replaced with the material $In_{(1-x)}Ga_xAs$ for all regions. Further, another structural variant $In_{(1-x)}Ga_xAs$ only in the source region and GaAs as pocket doped material at source/channel junction and rest regions is of Si material, which shows the improved performance for the later structure. The key focus of this research is to analyze the device DC performance of both the structures and also to analyze the impact of mole fraction (x) variation on different parameters. It is worth mentioning here that the reported charge sensitive characteristics of both the device structure can be used for the detection of C-erbB-2 protein, the breast cancer bio-marker sensing application.

The rest of the paper is ordered as stated below:

Device structure and models of simulation are defined in Sect. 2. Simulation result and discussion are mentioned in Sect. 3. Further, Sect. 4 concludes the research work with some critical findings.

2 Device Structure and Simulation

The two different 2D structures considered for the InGaAs-DL-TFET are shown in Fig. 1a, b. In the first structure, $In_{(1-x)}Ga_xAs$ material, with $x = 0.75$ composition, is selected for designing the InGaAs-DL-TFET structure, which is having a similar bandgap as of Si as depicted in Fig. 1a. Second structure has been implemented by choosing $In_{(1-x)}Ga_xAs$ material, with $x = 0.75$ composition in the source region and GaAs/Si as hetero-channel junction for GaAs/Si-HJDL-TFET realization as shown in Fig. 1b. Doping-less technique has been utilized for both the devices [16], by selecting the desired metal work function above the source as well as drain regions. Due to this work function engineering, the electrons and holes are induced thereby realizing virtual doping. Toward the drain side, n^+ region is formed by selecting hafnium electrode with work function of 3.9 eV and toward source side p^+ region can be formed by choosing platinum (Pt) electrode with work function as 5.93 eV. To avoid the formation of silicide, there must be a space between the drain electrode and source electrode with the semiconductor film. This gap is optimized between

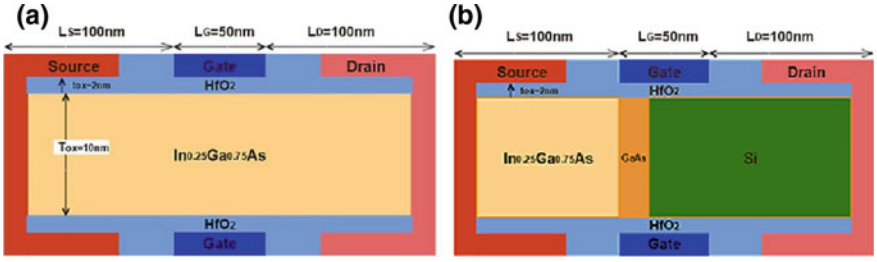

Fig. 1 2D structure of **a** InGaAs-DL-TFET **b** GaAs/Si-HJDL-TFET

Table 1 Simulation parameters for InGaAs-DL-TFET and GaAs/Si-HJDL-TFET

Parameters	InGaAs-DL-TFET(D_1) GaAs/Si-HJDL-TFET(D_2)	
Silicon thickness (T_{Si})	10 nm	10 nm
Gate oxide thickness (T_{ox})	2 nm	2 nm
Gate length (L_G)	50 nm	50 nm
Source length (L_S)	100 nm	100 nm
Drain length (L_D)	100 nm	100 nm
Background doping (N_{in})	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Source work function (ϕ_S(Pt))	5.93 eV	5.93 eV
Drain work function (ϕ_D (Hf))	3.9 eV	3.9 eV
Gate dielectric constant (ε_{ox})	HfO_2 (31)	HfO2 (31)
Source material	$In_{(1-x)}Ga_xAs$	$In_{(1-x)}Ga_xAs$
Channel material	$In_{(1-x)}Ga_xAs$	GaAs/Si (10–40 nm) Hetero-junction
Drain material	$In_{(1-x)}Ga_xAs$	Si

source and channel at 2 nm, whereas at 15 nm between the channel region and drain region. It leads to the enhancement in the ON-state current and reduces the ambipolar effect [27]. The gate oxide thickness value is optimized at 2 nm. TCAD Silvaco ATLAS simulator has been used to accomplish the study of the considered device structures. The models used in the simulation are listed as Shockley–Read–Hall (SRH), concentration and field-dependent mobility, bandgap narrowing model, Fermi model. Non-local BTBT model is used to justify the special profile and to more accurately model the process of tunneling [28]. All the device parameters considered for the device simulation are listed in Table 1.

3 Results and Discussion

This section investigates the comparative analysis of both the structures with the help of exhaustive calibrated 2D-TCAD simulation. Figure 2 shows the comparative analysis of the concentration of carriers of both the structures for OFF state for V_{GS} = 0 V, V_{DS} = 1 V and ON state for V_{GS} = 1 V, V_{DS} = 1 V below the gate oxide along the horizontal cut-line of 1 nm. From this figure, it is evident that both the devices have achieved the required concentration profile similar to the conventional doped TFET by electrostatic doping to realize $p^+ - i - n^+$ charge carrier profile even without metallurgical doping. Figure 3, represents the energy band diagrams of both device structures in OFF state for V_{GS} = 0 V, V_{DS} = 1 V and ON state for V_{GS} = 1 V, V_{DS} = 1 V along with the horizontal cut-line 1 nm below the gate oxide. Here, toward source side, energy barrier gap is lower as compared to drain in both the structures. It can be noted that staggered hetero-junctions [26] are formed at the

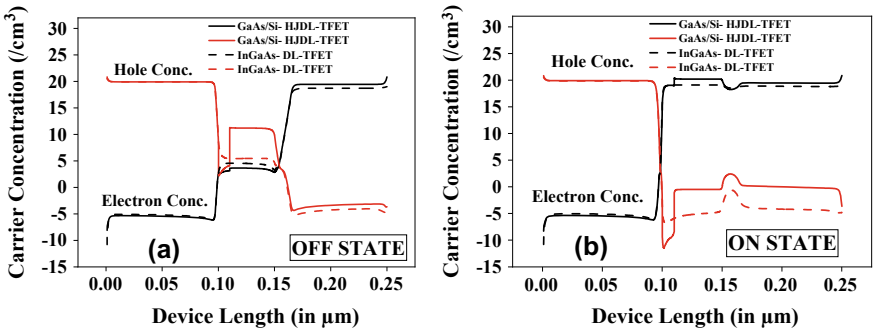

Fig. 2 Carrier concentration of InGaAs-DL-TFET and GaAs/Si-HJDL-TFET **a** OFF state (V_{GS} = 0 V, V_{DS} = 1 V) **b** ON state (V_{GS} = 1 V, V_{DS} = 1 V)

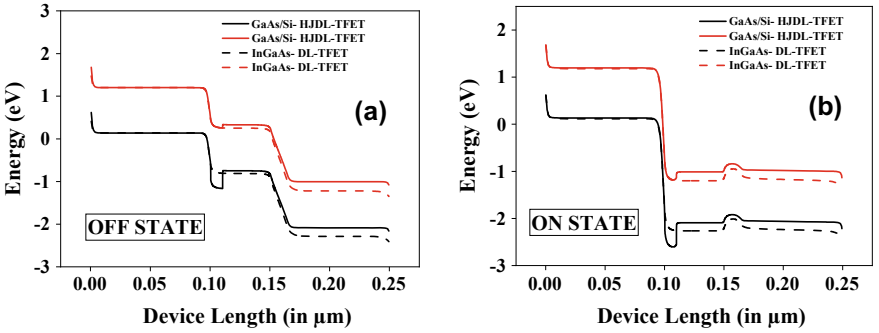

Fig. 3 Energy band diagram of InGaAs-DL-TFET and GaAs/Si-HJDL-TFET **a** OFF state (V_{GS} = 0 V, V_{DS} = 1 V) **b** ON state (V_{GS} = 1 V, V_{DS} = 1 V)

source-channel junction of the HJDL-TFET structure, which improves the OFF-state performance of the device.

The transfer characteristic of both the device structures is shown in Fig. 4. The figure depicts that the I_{ON} current of HJDL-TFET and DL-TFET is almost similar around 0.3 mA/µm but the OFF-state current decreases significantly in HJDL-TFET than other structure. It is because of the fact that in HJDL-TFET is having wider energy bandgap toward drain side as shown in Fig. 3a. The simulated performance parameters like SS, I_{ON} and I_{ON}/I_{OFF} ratio of both the structures under study are mentioned in Table 2. It is observed that I_{ON}/I_{OFF} of the proposed structure HJDL-TFET is approximately four times improved than the DL-TFET. The comparative analysis of the proposed structure with the previous works has also been listed in this table.

In Fig. 5a, the energy band diagrams of InGaAs-DL-TFET are shown in.

which as the mole fraction of material $In_{(1-x)}Ga_xAs$ increases from $x = 0.55$ to $x = 0.7$ in all the regions of structure results in an enhancement in tunneling width leads to the reduction in the tunneling current but OFF-state current also reduces

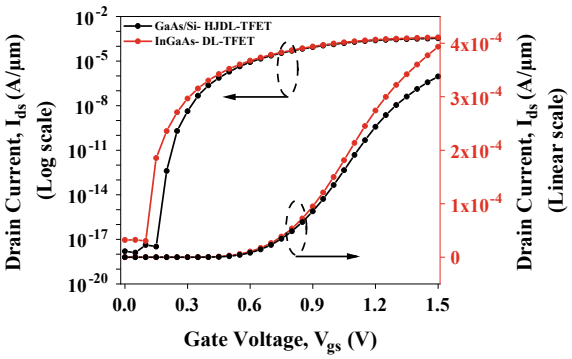

Fig. 4 Transfer characteristics of InGaAs-DL-TFET and GaAs/Si-HJDL-TFET

Table 2 Device performance characteristics for InGaAs-DL-TFET and GaAs/Si-HJDL-TFET at x composition = 0.75 and at $V_{GS} = 1$ V, $V_{DS} = 1$ V

Parameters	D_1	D_2	Sharma et al. [29]	Tripathy et al. [30]
SS (mV/deeade)	9.05	9.82	9.78	26
V_{LH} (V)	0.338	0.374	0.519	0.31
I_{ON}/I_{OFF}	2.21×10^{13}	8.48×10^{13}	2.06×10^{11}	7.5×10^{11}

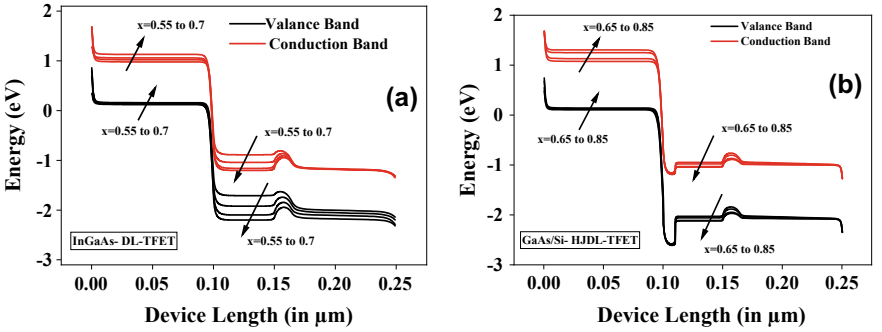

Fig. 5 Energy band diagram of **a** InGaAs-DL-TFET and **b** GaAs/Si-HJDL-TFET with the variation in mole fraction of $In_{(1-x)}Ga_xAs$

with increase in the mole fraction. Figure 5b shows the impact on the energy band diagram of GaAs/Si-HJDL-TFET with the variation in mole fraction of $In_{(1-x)}Ga_xAs$ toward source region from $x = 0.65$ to $x = 0.85$. It can be noticed from the figure that with an increase in the mole fraction x, the tunneling width increases that leads to the reduction in tunneling current and I_{OFF} increases with the increase in mole fraction. In Fig. 6a, b, transfer characteristic of InGaAs-DL-TFET and GaAs/Si-HJDL-TFET has been shown. Here, the variation in the mole fraction of $In_{(1-x)}Ga_x$ As for all the regions of former structure and source region for the later structure are considered. The graph shifts toward the right with the increasing value of x. It shows

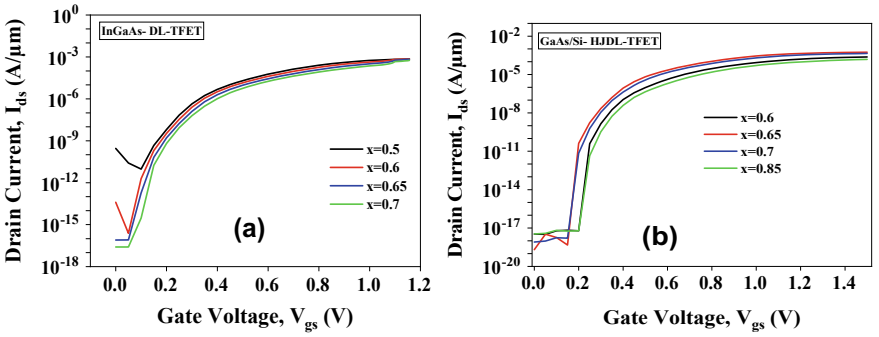

Fig. 6 Transfer characteristics of **a** InGaAs-DL-TFET and **b** GaAs/Si-HJDL-TFET with the variation in mole fraction of $In_{(1-x)}Ga_xAs$

the faster switching operation for a higher value of x. Figure 7 shows the impact on the performance characteristics of InGaAs-DL-TFET with the variation in mole fraction of $In_{(1-x)}Ga_xAs$ in all regions. Figure 7a shows the variation of SS with x and maximum SS as 29 mV/decade has been found for the minimum mole fraction value as $x = 0.5$ and minimum threshold voltage as 0.25 V for the same structure as shown in Fig. 7b and I_{ON}/I_{OFF} ratio (1.96×10^6) is lower for $x = 0.5$ as illustrated in Fig. 7e. Figure 8 shows the impact of mole fraction variation of $In_{(1-x)}Ga_xAs$ toward the source side on the performance characteristics of GaAs/Si-HJDL-TFET. Figure 8a shows the variation of SS with x and minimum SS as 6.3 mV/decade has been found for $x = 0.65$ and minimum threshold voltage as 0.34 V for the same structure as shown in Fig. 8b. Maximum I_{ON} (2.8 mA/μm) and minimum I_{OFF} (2.04×10^{19}) have been achieved at $x = 0.65$ as shown in Fig. 8c, d, respectively. A maximum of I_{ON}/I_{OFF} ratio is for hetero-junction DL-TFET, i.e., for $x = 0.65$ as 1.38×10^{15} which makes this structure as a significant structure among both structures. Moreover, hetero-junction DL-TFET has also been investigated for its charge sensitivity. Figure 9 shows the variation in the device performance characteristics such as SS, threshold voltage and I_{ON}/I_{OFF} ratio. It is to be noted from the figure that this device shows sensitivity toward charged bio-molecules (for positive as well as negative charge), which leads to enhance the suitability of this device structure for the designing of sensor device for charged bio-molecules such as breast cancer cells.

4 Conclusion

Here, two novel TFET device structures, doping-less InGaAs TFET and GaAs/Si-hetero-junction doping-less TFET (GaAs/Si-HJDL-TFET), are analyzed using an exhaustive calibrated TCAD simulation study. These structures are investigated for improving the performance parameters with the variation in mole fraction x of $In_{(1-x)}Ga_xAs$. Among both the structures, GaAs/Si-HJDL-TFET with x = 0.6

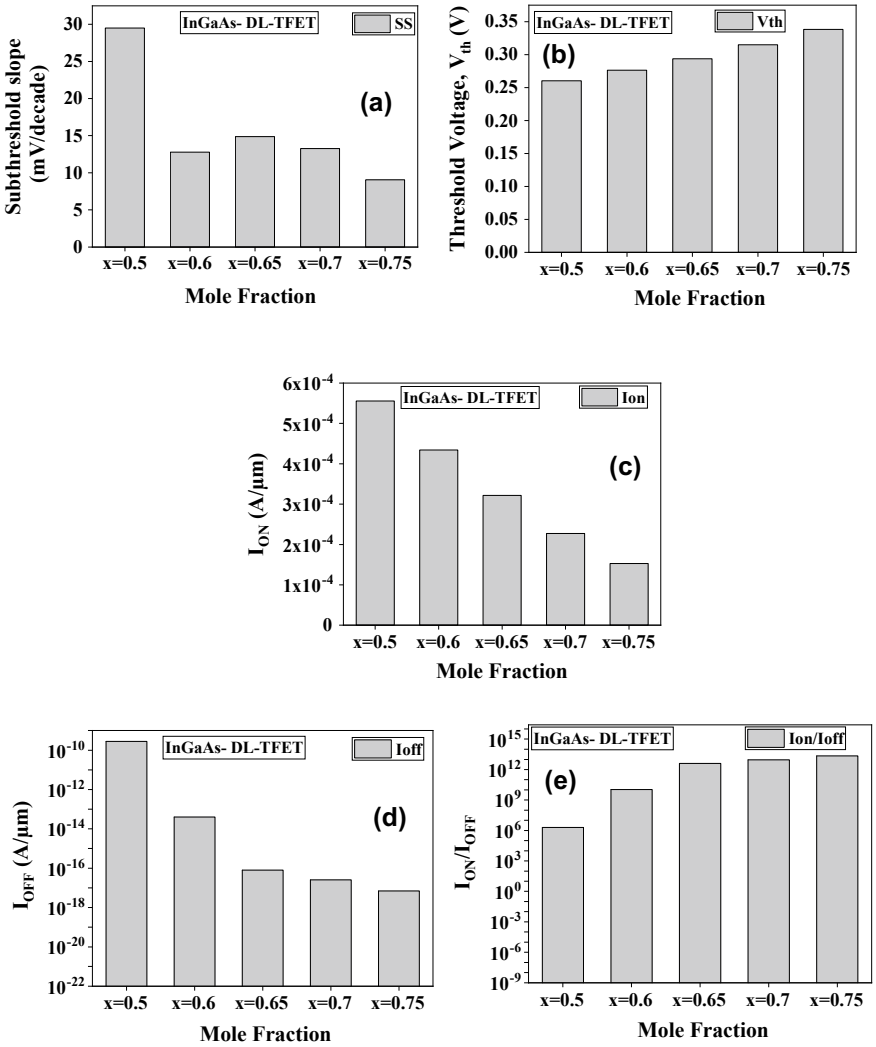

Fig. 7 Performance characteristics of InGaAs-DL-TFET **a** SS **b** V_{th} **c** I_{ON} **d** I_{OFF} **e** I_{ON}/I_{OFF}

shows better performance characteristics such as low threshold voltage (0.33 V), higher I_{ON} (0.2 mA/μm), lower SS (6.3 mV/decade) and higher I_{ON}/I_{OFF} ratio is of (1.38×10^{15}) Furthermore, hetero-junction DL-TFET structures have also been investigated for charge sensitivity. Therefore, GaAs/Si-based hetero-junction DL-TFET with $x = 0.6$ can be used as an application of the fast switching circuits and charge-based bio-molecules such as C-erbB-2 protein, the breast cancer bio-marker detection device.

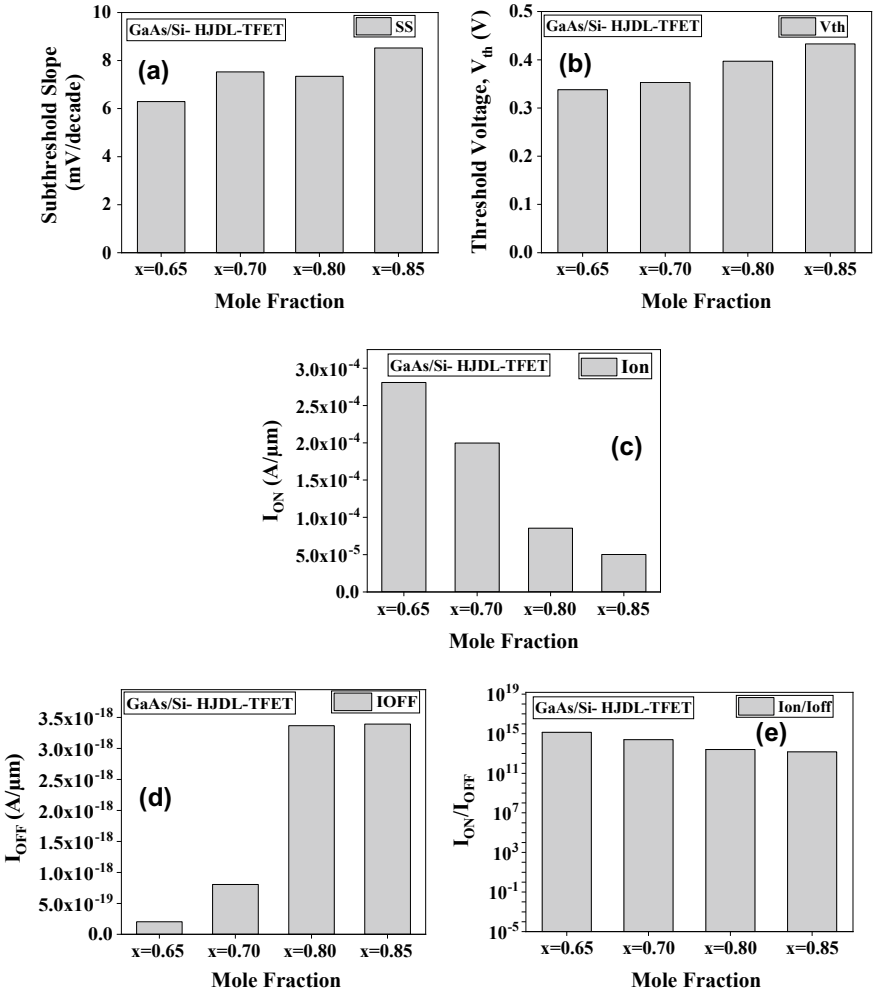

Fig. 8 Performance characteristics of GaAs/Si-HJDL-TFET **a** SS **b** V_{th} **c** I_{ON} **d** I_{OFF} **e** I_{ON}/I_{OFF}

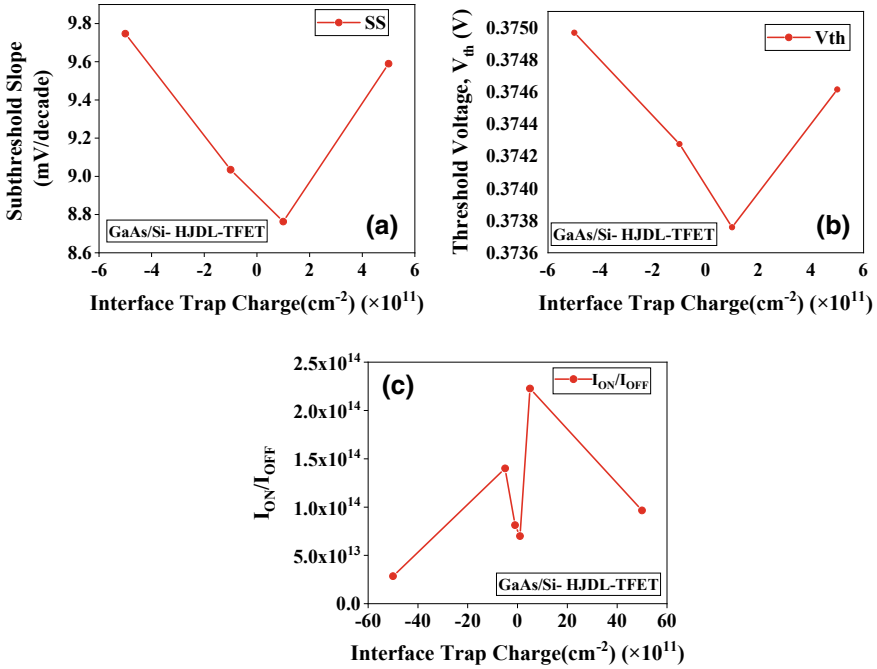

Fig. 9 Performance characteristics of GaAs/Si-HJDL-TFET **a** SS **b** V_{th} (c) I_{ON}/I_{OFF} with the variation of interface trap charges

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