

Design of Current Mode MOS Logic for Low-Power Digital Applications



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Abstract Today, the major limitation of designing of high-speed integrated circuits (ICs) with conventional technology is the delay limiting the switching speed of the gates. As evident from already established logic styles like complementary pass transistor logic (CPL), differential cascode voltage swing logic (DCVSL), etc., the circuit exploits the property of noise reduction due to differential inputs. Ideally current mode circuits have constant current gain with no input impedance and finite output impedance. The current gain of the circuit is set to unity as current amplification leads to higher consumption of static power. MOS current mode logic (MCML) is graced with certain advantages which include low level of noise generation, static power dissipation independent of switching activity, low voltage swing, a weak dependence of propagation delay on fan-out load capacitance, lower power dissipation at higher frequencies, etc., out way the few disadvantages such as elaborated design process and increased number of design parameters. In this paper, we present an in-depth study of MCML base approach in which the analysis of low-power applications is performed at the target data rate of 1 Gbps. Work has been done on a standard CMOS technology of 0.18 μm .

Keywords Current mode · High performance · Low power · MCML · Digital IC

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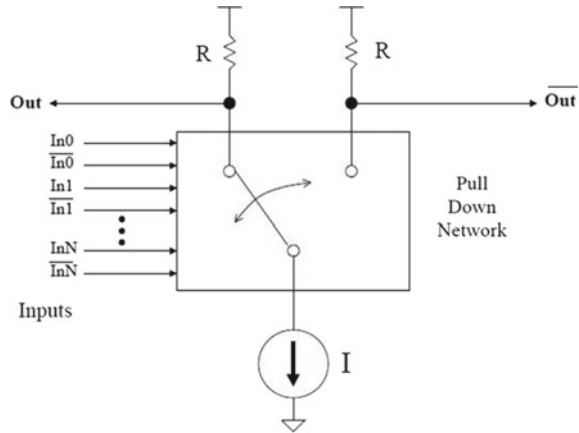
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Fig. 1 Basic MCML gate



1 Introduction

In today's world, demands for power efficient device are increasing exponentially. To make battery life more durable, power efficient device design is the need of the hour. Generally, the total power dissipation of a CMOS device consists of static and dynamic power. The static power dissipation occurs due to leakage in MOSFETS. The dynamic power dissipation occurs due to charging and discharging of capacitive load. To reduce the device size and increase the speed of device technology, scaling is done. With the help of technology scaling, a more number of transistors are embedded in device. Due to this, more functionality is added in the device which improves the performance. But due to addition of more transistors, switching activity increases which results in large dynamic power dissipation. Technology scaling enhances leakage current due to which static power dissipation increases [1]. For high-speed applications, MCML is preferred over other techniques [2, 3]. The MCML techniques suffer from large static power dissipation problem [4]. Owing to its numerous advantages, MCML becomes preferred design over other MOS logic styles [5] for digital circuit applications [6, 7]. MCML gives a reduced output voltage swing compared to CMOS circuits thus making it suitable for higher speed applications. The power dissipation using MCML is independent of its frequency of operation [8]. For higher frequency application, MCML design is preferred due to low power dissipation. Constant current in the supply rails of MCML technique reduces the noise as well as crosstalk owing to low voltage swing. In digital logic circuits, signal integrity improves due to differential nature at the inputs of the MCML.

2 MOS Current Mode Logic Operation

The continental structure of MCML block [8] is shown in Fig. 1 which have three most essential components such as pull-up network, pull-down network, and a constant current source. The PDN accepts only differential inputs, i.e., the true and complemented form of all the signals at the inputs. Current ‘ I ’ is originated by the constant current source while the output voltage swing is determined by the load resistance R . The governing principle of the circuit is current steering [2]. Depending on the concept used, PDN directs the current ‘ I ’ to one of the pull-up devices. The voltage drops across the resistor connected to the current source via PDN is equal to $\Delta V = I \times R$. Theoretically, zero current flows through the other branch. The total voltage swing is determined by the magnitude of the current ‘ I ’ steered and the load devices value.

2.1 Derivation of MCML Gate Performance

The basic MCML block is modeled as RC network [3] shown in Fig. 2. The transient analysis of simplified MCML model based on RC network is based on following assumptions:

1. symmetrical output loads
2. the pull-down network is considered to be an ideal switch shifting from left to right at time $t = 0$.

The MCML circuit based on RC network before and after $t = 0$ depends on switch position that can be modeled as shown in Fig. 3a, b, respectively.

A circuit is assumed to have ‘ N ’ identical gates arranged in linear chain, all having similar load capacitance’s denoted by ‘ C ’. So, the total propagation delay for the chain of gates will be proportional to:

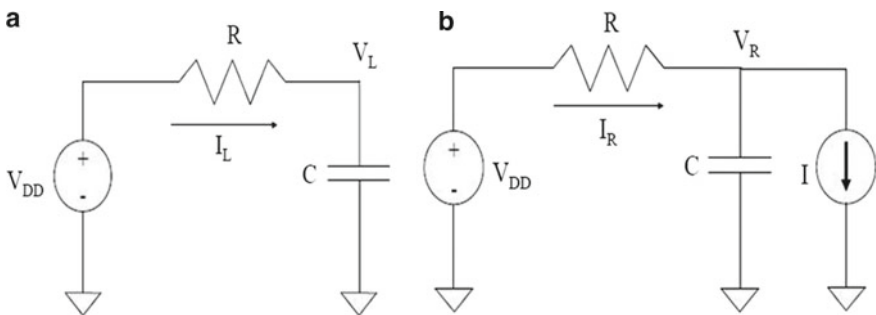
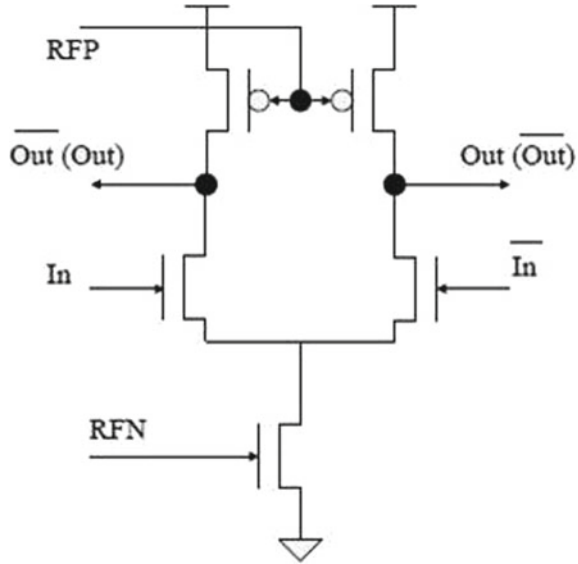


Fig. 2 a, b Equivalent RC model of MCML

Fig. 3 MCML inverter/buffer



$$D_{MCML} = NRC = \frac{N \times C \times \Delta V}{I} \tag{1}$$

In digital circuits, the power dissipation can be categorized into static and dynamic power components [6]. Thus, in case of MCML under first order consideration, the total power dissipation is a constant. Following this assumption, power, power delay product, and energy delay product can be represented as,

$$P_{MCML} = N \times I \times V_{dd} \tag{2}$$

$$PD_{MCML} = NIV_{dd} \times \frac{N \times C \times \Delta V}{I} = N^2 \times C \times \Delta V \times V_{dd} \tag{3}$$

$$ED_{MCML} = N^2 \times C \times \Delta V \times V_{dd} \times \frac{NC\Delta V}{I} = \frac{N^3 \times C^2 \times V_{dd} \times \Delta V^2}{I} \tag{4}$$

The following equations can be used for comparison with static CMOS logic based on parameters such as power, delay, power delay, energy delay:

$$D_{CMOS} = \frac{N \times C \times V_{DD}}{\frac{K}{2} \times (V_{DD} - V_T)^\infty} \tag{5}$$

$$P_{CMOS} = N \times C \times V_{DD}^2 \times \frac{1}{D_{CMOS}} \tag{6}$$

$$PD_{CMOS} = N \times C \times V_{DD}^2 \tag{7}$$

$$E D_{\text{CMOS}} = N^2 \times 2 \times \frac{C^2}{K} \times \frac{V_{\text{DD}}^2}{(V_{\text{DD}} - V_T)^\infty} \quad (8)$$

where k and ∞ are parameters dependent on process and transistor size.

2.2 MCML Inverter

The primary design is the MCML inverter/buffer [2] as shown in Fig. 3. The inverter/buffer circuit structure is topologically identical to MCML which employs differential logic to switching the output or input for sense. The load devices in the circuit are implemented using PMOS transistors. They have a fixed gate voltage and to model as resistors, operated in the linear region. It is desirable to make the width of these transistors as small as possible to increase the linearity and to decrease the capacitance. The RFP voltage is controlled by the variable controlled swing shown in Fig. 3.

The PDN is implemented using differential pair of NMOS transistors. The main goal of the pull-down network is to steer the current from the current source to any part of the branch. Theoretically, all current flows through single path and zero current flows through the other path but in reality, some current also flows through the ‘OFF’ path which causes the reduction in the voltage swing. Although the increase in the transistor width increases the voltage gain, it too results in the increase the parasitic capacitance which leads to a trade off between performance and robustness. Thus, in order to preserve the performance, gain must be kept minimum.

A NMOS transistor working in saturation region with a fixed gate voltage act as a current source. Area and robustness form the main trade-off in selecting the size of the current source device. Preference is given for (non-minimum length) transistor to achieve a high output impedance and better current matching ratio. The voltage at the gate of the current source must be kept a few hundred mv from both the power rails if it is determined by a current mirror.

2.3 MCML Tristate Buffer

To remove the influence of the device from the rest of the circuit is the main concept behind high impedance state. Designing tristate gates in CMOS logic is easy [2] since an output of the CMOS gates is connected to any one of the power rails at a time. Therefore, turning off the paths connecting both the supplies to the output is easy in CMOS. In case of current mode logic, the output is constantly connected to the positive supply via load devices which remains always ON.

A switch-based tristate buffer shown in Fig. 4 has two PMOS pass transistors (M6-M7) as reported in [1, 2].

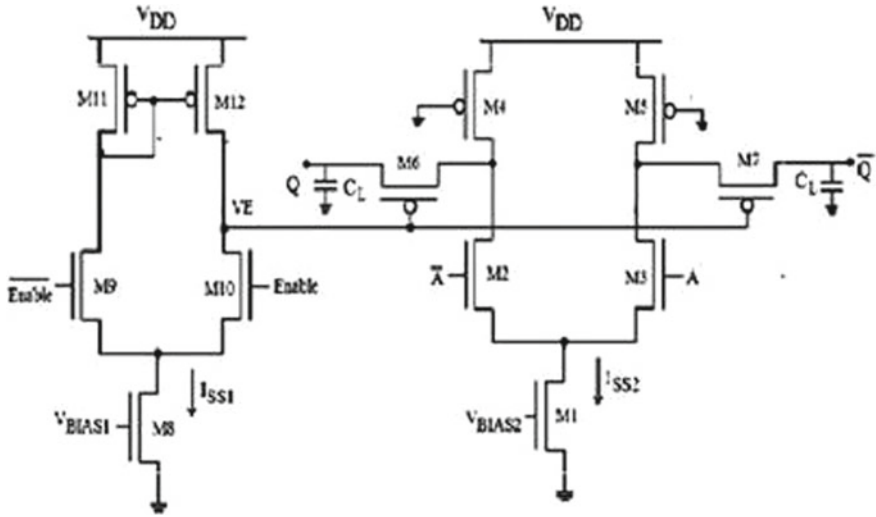


Fig. 4 Switch-based MCML tristate buffer

A low power version of tristate buffer [6] is presented in Fig. 5 which consumes less power as compared to the switch-based tristate buffer by disconnecting the output node from both power supply as well as ground when the buffer is in high impedance state.

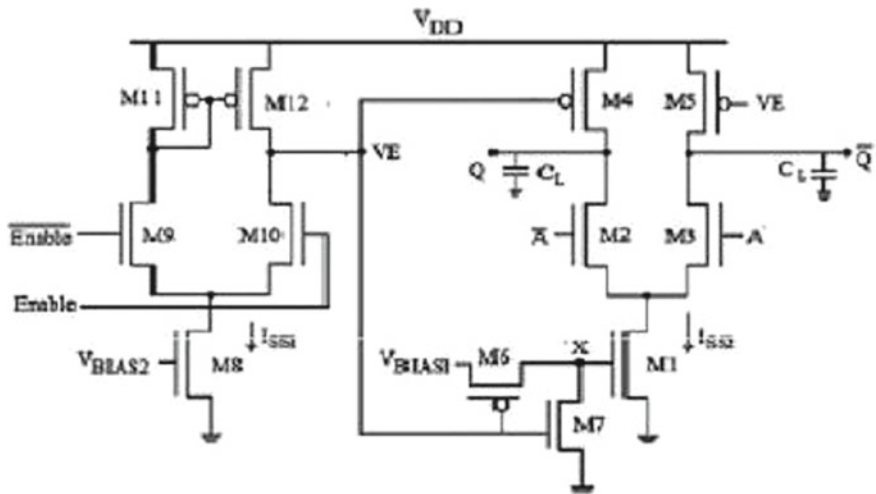


Fig. 5 Low-power MCML tristate buffer

3 Results and Comparison

From Tables 1, 2, and 3, it is observed that the main factors which affect the performance of the gates are their limits on minimum swing at the low current end, but give better propagation delay, good power delay product, and reduced power consumption. With increase in current levels, voltage swing increases in order to attain the gain metric, whereas the propagation delay and the power delay product increase. In order to reduce the capacitance, it is desirable to reduce the width of the transistors but process minimum widths are already achieved.

The performance comparison of the proposed tristate buffers with the existing tristate buffers that are carried out using 0.18 μm gpdK CMOS technology parameters. It is noticed that the propagation delay and the power delay product for the switch-based tristate buffer is reduced by fbgv 88.35% and 70.57%, respectively, and that of the low-power tristate buffer reduces by 93.52% and 74.67%, respectively.

Table 1 Simulation results for MCML inverter

I (μA)	ΔV (mV)	V_{DD} (V)	(W_A/L_A)	$(W/L)_{RFP}$	$(W/L)_{RFN}$	T_p (ps)	PDP (fJ)	Static power (pW)
40	300	1.8	0.5/0.18	0.4/0.18	3.0/0.18	63	4.54	19.9
50	400	1.8	0.5/0.18	0.4/0.18	3.0/0.18	69	6.14	20.49
60	500	1.8	0.5/0.18	0.4/0.18	3.0/0.18	71	7.66	21.13

Table 2 Simulation and comparison results for switch-based tristate buffer [8]

Design	I (μA)	ΔV (mV)	V_{DD} (V)	T_p (ps)	Power (μW)	PDP (fJ)
Switch-based tristate buffer [1]	50	400	1.8	481	435	209
Implemented switch-based tristate buffer	50	400	1.8	56	128	7.16

Table 3 Simulation and comparison results for low-power switch-based tristate buffer [8]

Design	I (μA)	ΔV (mV)	V_{DD} (V)	T_p (ps)	Power (μW)	PDP (fJ)
Low-power tristate buffer [1]	50	400	1.8	340	308	104
Implemented low-power tristate buffer	50	400	1.8	22	78	1.71

4 Conclusion

In this paper, a detailed study of MCML operating principle has been presented along with its application to digital circuit design. The paper also addresses the design methodology of high speed, low-power logic gates, and other digital system design blocks by using the contemporary MCML style which has been proved to be better than the conventional CMOS. The static power dissipation of current mode logic remains the main drawback for many applications which stays a future scope of research.

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