Design of Low-Power Dynamic Type Latch Comparator Using 18 nm FinFET Technology for SAR ADC

B. Hemalatha and Ajay Kumar Dadoria

Abstract There are multitudinous applications of comparator in diversified areas, notably used in data converters. Since many years, single stage, dynamic type latch as well as double tail comparators have been designed using CMOS technology. But there is a trade-off among the energy consumption and time delay. Concurrently, to alleviate the short channel effects of the design, which is based on traditional CMOS, FinFET has loomed as the most assuring surrogate by its enormous gate control characteristic across the channel region. Here, we examined the performance of a latest dynamic type latch comparator, and a modern design of dynamic type latch comparator is proposed in this paper. Furthermore, 18 nm FinFET technology is considered as a platform for the design of this comparator. The proposed comparator has shown splendid performance with respect to energy consumption, delay, in comparison with the other latest comparator through simulation with Cadence.

Keywords Ultra low power · Dynamic latch comparator · FinFET · Inverter · Delay

1 Introduction

Along with the other applications of comparator like in line decoders, level shifters, data receivers, memory sense amplifiers, one of its important applications is in analog to digital converters [1]. Also, in biomedical imaging applications, an extreme data rate, high resolution and high sensitivity-based ADCs are at present highly demanding [2].

Static comparators are now outdated because of noticeable amount of power consumption and limited speed [3]. Some distinguished features of dynamic type latch comparator which made it more attractive are strong positive feedback, high input impedance, negligible static power consumption and rail to rail output swing

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[4]. In a single stage comparator, because the differential input stage and regeneration latch stage are interconnected, it had a trade-off between the offset voltage and energy requirements and along with the relentless kickback noise [5]. A single tail transistor further has constraints in total flow of current by two output nodes, and this also increases the dependence of offset voltage and performance of various ranges of input common mode voltage [6]. An alternative of single tail comparator has emerged by imparting the required segregation between the preamplifier and latch stages. This new double tail architecture has high accuracy, near supply voltage function, high input common mode voltage range, cascading amplifier stage, so on, [7, 8]. With the advancement in the technology, design of high-speed comparators with low supply voltage is more challenging [9]. To continue scaling, the most assuring alternative approach of CMOS-based technology is FinFET which shall be used for the design of high-speed, low-power dynamic type latch comparator. Few characteristics of this multi-gate structure are improved scalability, higher mobility of carriers, reduction of short channel effects, low value of supply and threshold voltages, reduced dopant fluctuations, higher frequency operations, lower leakage of current near sub-threshold operation and good channel control [10]. Device scaling demands for reduction in power supply voltage, low threshold voltage and high transistor density. Drain gating PMOS and drain gating NMOS technique are employed to low-power applications [11, 12]. Aggressive scaling of single gate CMOS faces many challenges in nanoscale technology. So, double gate FinFET (DGFET) is used to mitigate the leakage current higher ON state current when scaling is beyond 32 nm [13]. In this paper, a modern dynamic latch comparator is designed that shows compelling enhancements in power consumption and power delay. The remaining part of this paper is organized as follows: Sect. 2 explains the operation, advantages and disadvantages of the latest dynamic type latch comparator. In Sect. 3, the proposed modern comparator's operation is discussed. In Sect. 4, results analysis and comparison table are given. Finally, the paper is concluded in Sect. 5.

2 Dynamic Latch Type Comparator

The operation, merits and demerits of already existing dynamic comparator which are designed by Hossain et al. [14] will be discussed in this section shown in Fig. 1. As like the conventional comparators, which works with two clock pulses, here in the starting, at the reset phase of the operation CLK1 = 0 and CLK2 = 1, therefore Ftail1 and Ftail2 will be turned OFF, and the source and drain terminals of F3, F4 will be charged to the supply voltage Vdd through F6, F8 and F5, F7. If Outp and Outn terminals are left with any charge from the previous cycle, it will be discharged to ground through F13 and F14. At the evaluation phase of the operation, the clock cycles will be reversed, and therefore, tail transistors Ftail1 and Ftail2 will be turned ON. The operation path of F1 and F2 depends on the input and reference voltages. Then, node Fa discharges faster than the node Fb, when vin > vref and since F7 as well as F8 are OFF, now they do not have the chance to recharge at this evaluation

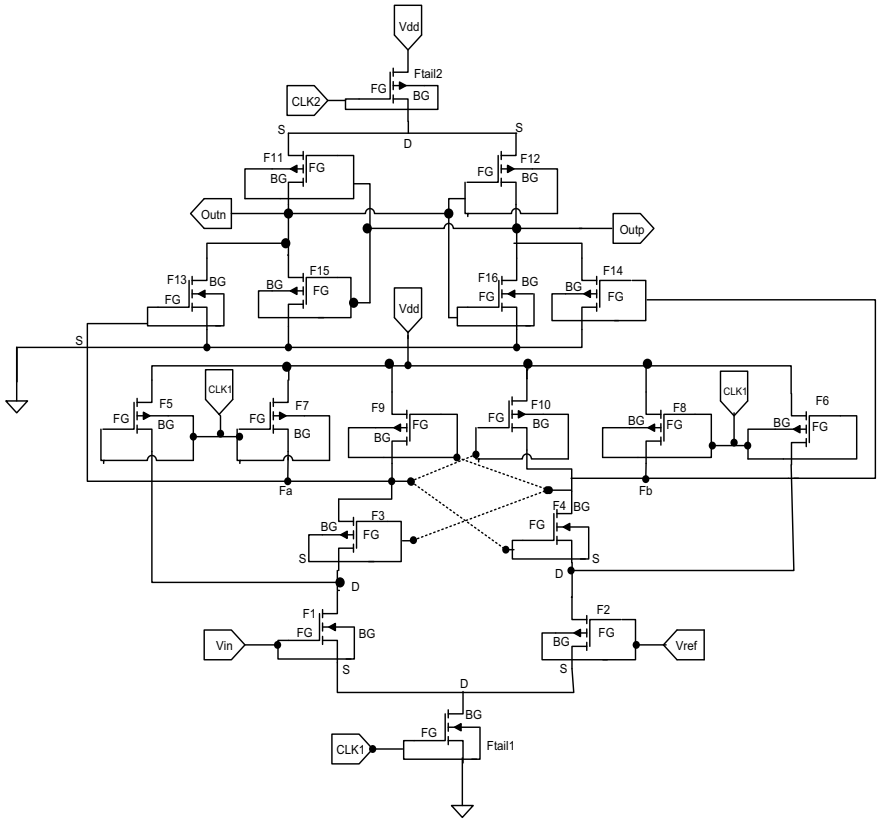

Fig. 1 Circuit diagram of reference dynamic latch comparator [14]

phase. Since Fa is discharged quickly, it will turn OFF F4 and F10. As Fb still holds the charge (Vdd), F9 is turned OFF, and F3 is turned ON in order to expedite node Fa to completely get discharged. Node Fb will be kept ON, as Outp will be discharged to ground through F14. Outp will also turn ON F11 and turn OFF F15, so that Outn will be stayed at Vdd. Outn will cause F12 to turn OFF, so the charging path of OutP is now completely disconnected and turn On F16 to help Outp to be totally discharged.

F3 and F4 in this design are allowing to circumvent the static power consumption by disconnecting the discharge path after reaching decision. The upper tail transistor (Ftail2) inhibits any power consumption during the reset phase of operation. Anyhow, two individual clocks are required, and an appropriate strategy in among them is required to provide the desired accuracy.

3 Proposed Dynamic Latch Comparator

The operation of our proposed dynamic latch type comparator is discussed in detail in this section shown in Fig. 2. Analogous to other conventional comparators, the proposed comparator too works with two individual clock phases. The main idea of this proposed circuit is to prevent the complexity in the coordination of two different clock pulses and to reduce the power consumption. In this circuit instead of using two individual clock pulses, a source CLK is considered. This CLK pulse serves both the phases of the circuit. This CLK is split into two non-overlapping clock pulses, i.e., CLK1 and CLK2. CLK1 is derived from the main source CLK followed by inverter (INV), and CLK2 can be directly taken from the source CLK, but to

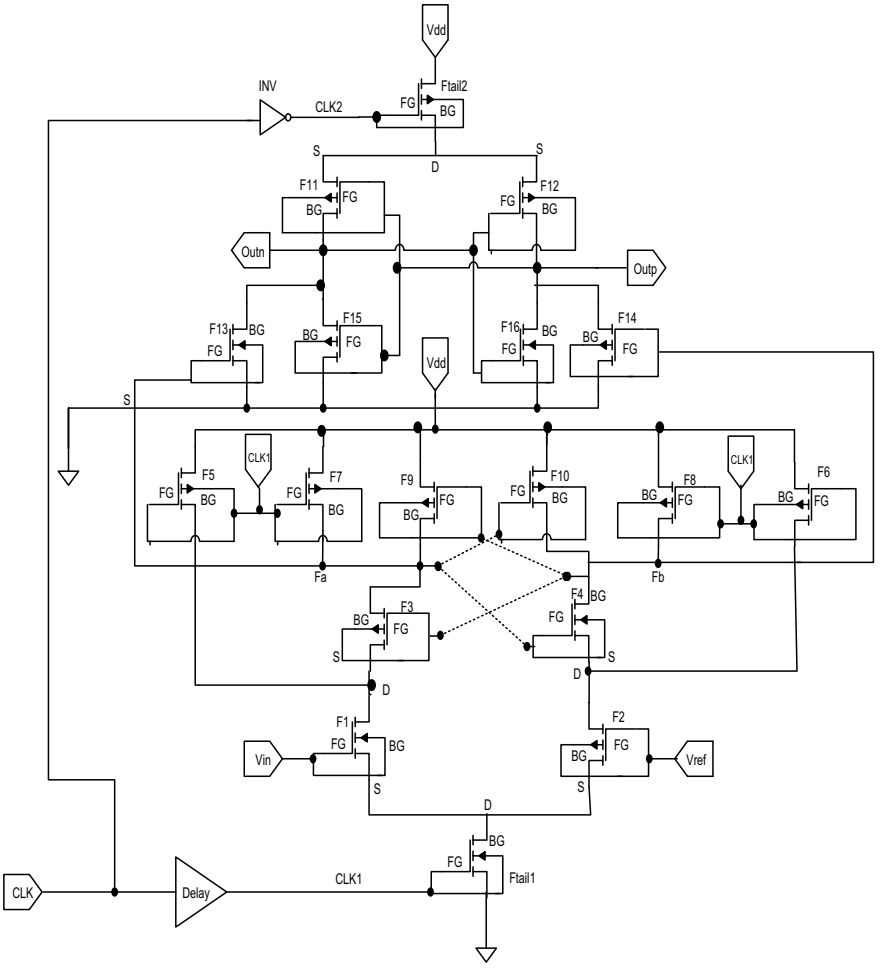

Fig. 2 Circuit diagram of the proposed dynamic latch comparator

match the performance of both the stages, a sufficient delay must be provided. So, CLK2 is derived from the main source CLK followed by a delay circuit. Here, though an additional inverter INV is inserted in the proposed circuit, it will not affect the performance because the power consumed by the inverter compared to the CLK is less.

In the starting, at the reset phase of the operation CLK1 = 0 and CLK2 = 1, therefore, both the tails, i.e., Ftail1 and Ftail2 go to OFF state, and the source and drain terminals of both F3 and F4 will be charged to the supply voltage Vdd through F5, F7 and F6, F8. Now, Outp and Outn will be discharged completely to ground through F13 and F14.

Next at the evaluation phase, both the clock cycles are reversed, CLK1 = 1 and CLK2 = 0, and therefore, both the tails, Ftail1 and Ftail2, go to ON state. Now, the conductance of F1 and F2 depends on the input and reference voltages. If Vin is more than Vref, then node Fa will discharge rapidly than node Fb, and now, F7, F8 are OFF, hence, during this evaluation phase, they will not have the chance to get recharged. Since Fa is discharged quickly, it will turn OFF F4 and F10. As Fb still holds the charge (Vdd), F9 is turned OFF, and F3 is turned ON in order to expedite node Fa to completely get discharged. Node Fb will be kept ON, as Outp will discharge to ground through F14. Outn will stay at Vdd, as Outp turns ON F11 and turns OFF F15. Now, the charging path of Outp is disconnected completely, as Outn causes F12 to turn OFF. F16 will be turned ON to help Outp to totally discharge.

4 Results and Discussion

The proposed dynamic latch comparator is designed, simulated, and the results are plotted with Cadence tool, using 18 nm technology. Figures 3 and 4 show the transient response of the proposed circuit.

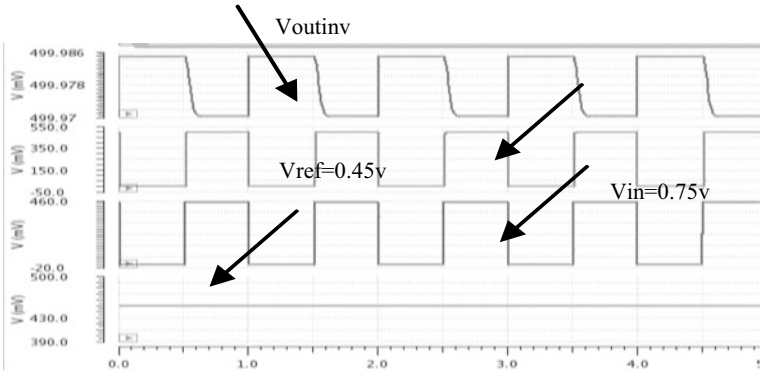

Fig. 3 Input–output waveforms of the proposed dynamic latch comparator

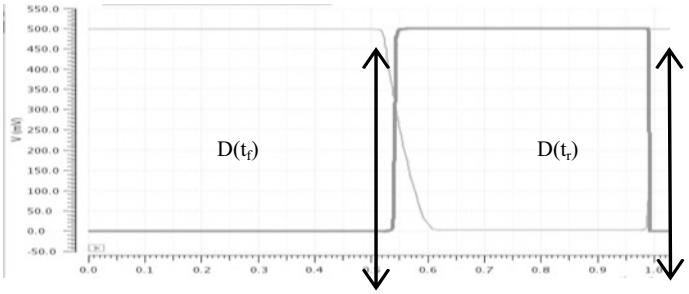

Fig. 4 Transient response of the proposed dynamic latch comparator

Table 1 Summary of comparision of existing and proposed circuits

Parameters	[14]	Proposed
CMOS FinFET technology (nm)	32	18
Supply voltage (V)	0.8	0.75
ΔVin	5	5
Power (μW)	73.36	36
Delay (ps)	12.63	50

Table 1 presents the detailed operational conductance comparison of our proposed dynamic latch type comparator with the existing comparator. The proposed comparator is designed and simulated in 18 nm FinFET technology, operated with a supply voltage of 0.75 V, differential input voltage of 5 V. The average power consumption of our proposed circuit is 36 μW, which is very low compared to existing comparator. The propagation delay is 50 ps. So, by considering all the measuring criteria, our proposed circuit consumes low power, with faster response.

5 Conclusion

This paper presented the design and analysis of modern dynamic latch comparator. 18 nm FinFET PTM models are used to design the proposed circuit. The proposed circuit is designed in 18 nm FinFET technology, and its competency is verified through simulation results which are performed with Cadence Virtuoso. The time delay and average power consumption are found to be very promising compared to the conventional comparators. The average power consumption is reduced by 49.07% compared to conventional comparator.

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