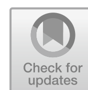
Investigating Effect of Structural Parameters on Static Characteristics of Ultrathin DG MOSFET Using Taur's Model



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Abstract Drain current and pinch-off voltage of ultrathin double-gate MOSFET are analytically calculated based on Taur's model, where the centre potential is derived from Ortiz-Conde formulation. Drain current is computed for different structural parameters in lower nanometric range, and the effect of the high-*K* dielectric is investigated. Pinch-off voltage shift is therefore derived from the simulated findings and compared with the available findings followed by Ortiz-Conde. The result shows a measurable variation in the parameters, and the root cause is explained from the electrostatic point of view. Findings are important for conductance calculation.

Keywords Drain current · Taur's model · Pinch-off voltage · Structural parameters · Ortiz-Conde model · High-*K* dielectric

1 Introduction

Research on multiple-gate MOSFET gets attention in the last decade due to the severe constraint of short-channel effect [1] in low-dimensional devices and thereby requirement of precise gate control [2]. In submicron devices, more precisely when device dimension goes beyond 100 nm, the requirement of lower DIBL and moderate subthreshold slope instigates several novel FET architectures, and double-gate MOSFET is one of the supreme candidates [3–5] among them. One branch of device engineering deals with tunnelling mechanism-based transistors, which results in single-electron transistor [6], tunnel field-effect transistor [7], etc., whereas another arena of research

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is gate engineering where multiple gates, as well as various architectures [8–10], are proposed for controlling electron transport. DG MOSFET is the result of later avenue of research as mentioned, and it offers excellent properties for analog [11] as well as digital [12] applications. Tied-gate architectures are preferred for higher current density [13], whereas independent-gate architecture offers lower threshold voltage [14], and henceforth preferred for low power design.

Inversion layer properties of DG MOSFET are analytically investigated by Palanichamy [15] after the simultaneous solution of Schrödinger and Poisson's equation, whereas weak inversion properties are computed by Bhartia [16] after inclusion of channel length modulation parameter. An explicit model was derived by Zhu et al. [17] following Taur's model, but that is only applicable for undoped structure. Hariharan [18] later included velocity saturation model for submicron device where gate length is considered 200 nm. The effect of the number of gates on drain current is investigated by Yu [19], followed by compact model development [20]. Very recently, Yu published [21] SPICE-compatible model for surface potential computation. In the present paper, drain current of symmetric DG MOSFET is analytically calculated based on Taur's model where centre potential is obtained from Ortiz-Conde analysis. The results are shown the closer agreement of data with published literature. Corresponding pinch-off voltage is calculated for different high-K dielectric and compared with that obtained for conventional SiO_2 material. The results are important for computing conductance of the device.

2 Mathematical Formulation

For long-channel DG MOSFET structure, the solution of 1D Poisson's equation gives [22]

$$\phi(z) = \phi_C - 2\phi_t \ln\left[\frac{t_{\text{sub}}}{2\beta}\sqrt{\frac{qn_i}{2\varepsilon_{\text{sub}}\phi_t}}\cos\left(\frac{2\beta z}{t_{\text{sub}}}\right)\right] \tag{1}$$

where the parameter is defined as [22]

$$\beta = \frac{t_{\text{sub}}}{2}\sqrt{\frac{qn_i}{2\varepsilon_{\text{sub}}\phi_t}}\exp\left[\frac{\phi_0 - \phi_C}{2\phi_t}\right] \tag{2}$$

Here t_{sub} defines the thickness of the substrate, ϕ_C is the quasi-Fermi potential for electrons inside the channel.

Drain current for the device is given by

$$I_{\text{DS}} = \mu_{n\text{eff}}\frac{W}{L}\frac{4\varepsilon_{\text{sub}}}{t_{\text{sub}}}(2\phi_t)2[f(\beta_s) - f(\beta_d)] \tag{3}$$

where

$$f(\beta) = \beta \tan \beta - 0.5\beta^2 + \frac{\varepsilon_{\text{sub}} t_{\text{ox}}}{\varepsilon_{\text{ox}} t_{\text{sub}}} \beta^2 \tan^2 \beta \quad (4)$$

In this case, ϕ_0 denotes the centre potential. In the present work, the value of centre potential is calculated following the Ortiz-Conde formulation [23].

Centre potential according to [23] is defined as

$$\phi_0 = U - \sqrt{U^2 - (V_{\text{GS}} - V_{fb})\phi_{0\max}} \quad (5)$$

where 'U' and $\phi_{0\max}$ are already defined.

In original Taur's model, centre potential is calculated from Eq. (1) with suitable boundary conditions, which is hereby replaced by Eq. (5).

3 Results and Discussion

Based on Eq. (3), we first calculated drain current for symmetric DG MOSFET, and the result is compared with that obtained from Ortiz-Conde model [23]. The result shows a very close agreement in saturation current, but a considerable difference in the active region. It is revealed from Fig. 1a that the slope of the active region is steeper in Ortiz-Conde model, whereas in the present paper, pinch-off voltage is delayed. This is due to the fact that the centre potential in the proposed model is a slowly varying function an affects the both source- and drain-end potentials, whereas in the model [23], the effect is overlooked. However, in the saturation region, the difference becomes negligibly small because of increasing drain voltage, which overcomes the effect of centre potential variation. The comparative study is also performed with the data obtained from Taur's model [24] and represented in Fig. 1b.

In Taur's model, centre potential is calculated directly from the function β [24]. Here that is computed from [23], and a noticeable difference is observed. This is due to the fitting of [23], where the function β, defined in Eq. (2), becomes a function of centre potential, and corresponding total potential function. High-K effect is investigated based on that modification. With the increase of dielectric constant, it is found that drain current decreases, as evident from Fig. 2. This is quite obvious, but another interesting fact that corresponding to the reduction of saturation current, pinch-off voltage takes a right shift.

The effect of dielectric thickness is investigated in Figs. 3 and 4 represent the substrate thickness effect. With the increase of dielectric thickness, current decreases and that is true for the substrate layer width also. Again pinch-off point shifts with the relative change and that is represented in tabular form.

The effect of back-gate voltage is calculated and plotted in Fig. 5. It is seen from the plot that the higher gate voltage leads to delay in pinch-off point due to the

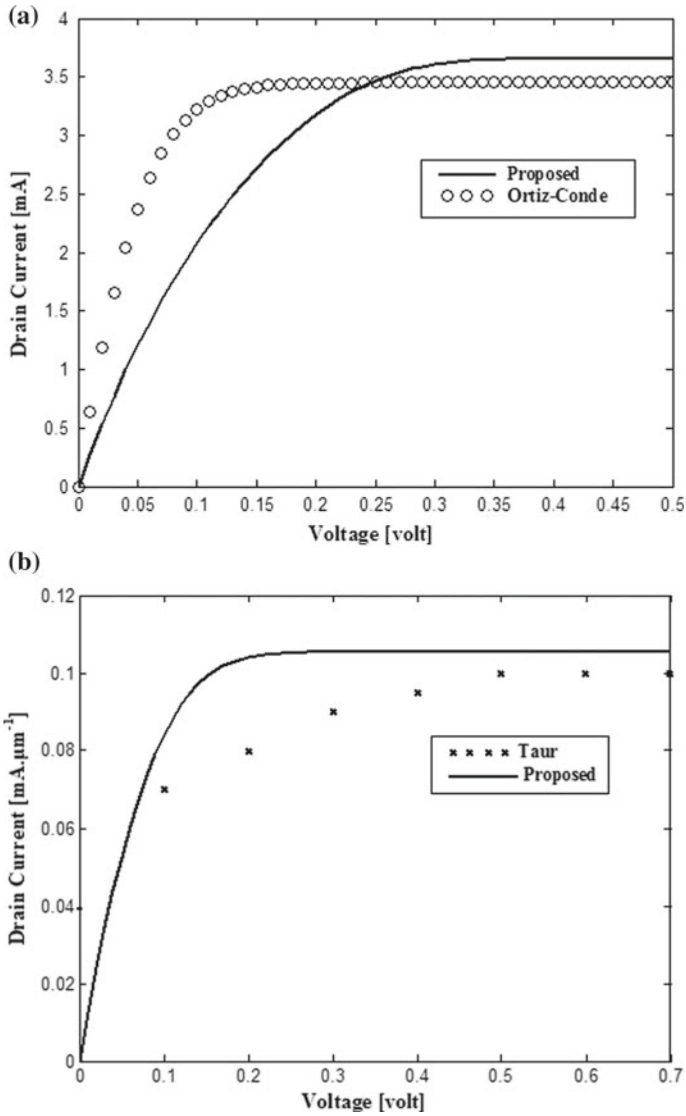

Fig. 1 **a** Comparative analysis of drain current with Ortiz-Conde model [23]. **b** Comparative analysis of drain current with Taur model [24]

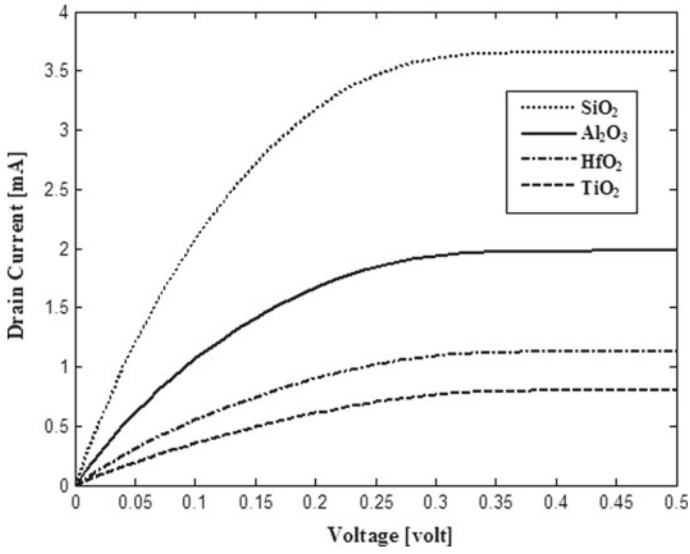

Fig. 2 Effect of high-*K* dielectric on drain current

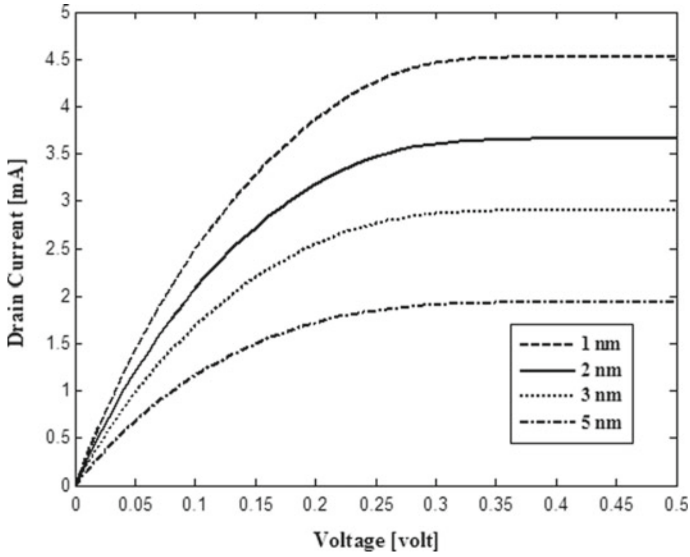

Fig. 3 Effect of dielectric thickness on drain current

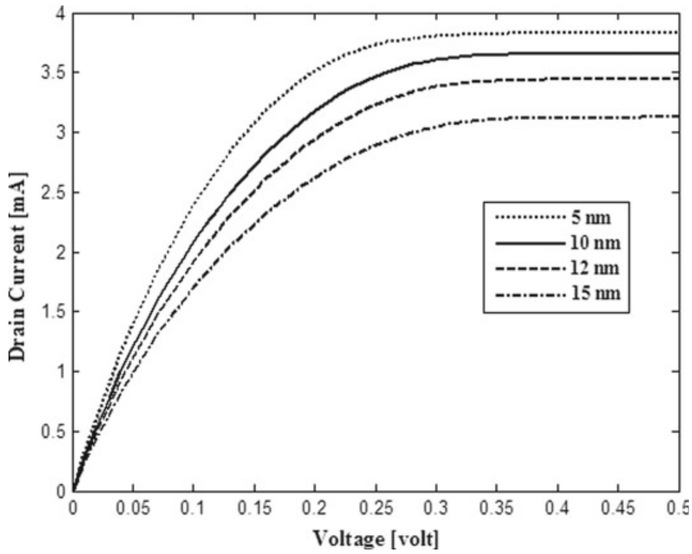

Fig. 4 Effect of substrate thickness on drain current

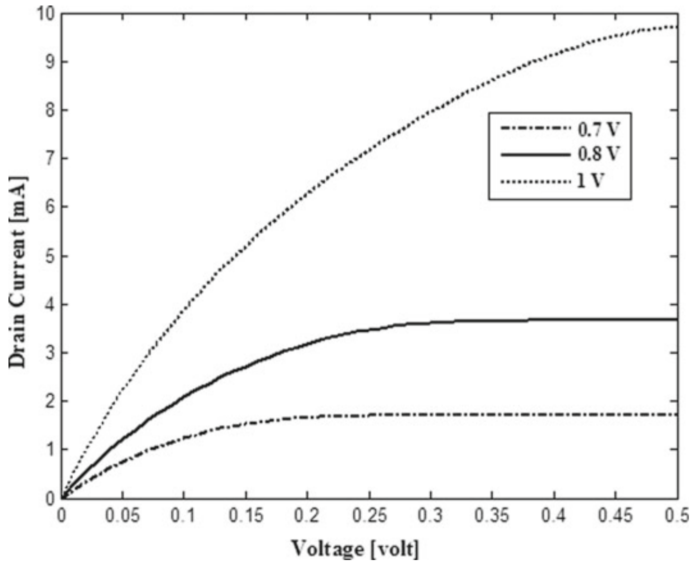

Fig. 5 Effect of back-gate voltage on drain current

Table 1 Pinch-off voltage for different dielectric thickness with two sets of back-gate voltage

t_{ox} (nm)	V_P (volt)							
	SiO_2		Al_2O_3		HfO_2		TiO_2	
	$V_G =$ 0.8 V	$V_G =$ 1 V	$V_G =$ 0.8 V	$V_G =$ 1 V	$V_G =$ 0.8 V	$V_G =$ 1 V	$V_G =$ 0.8 V	$V_G =$ 1 V
2	0.35	0.54	0.35	0.55	0.38	0.59	0.39	0.59
5	0.31	0.51	0.31	0.5	0.35	0.54	0.37	0.54
8	0.27	0.46	0.28	0.45	0.3	0.49	0.33	0.51
10	0.25	0.41	0.26	0.42	0.28	0.44	0.32	0.5

Table 2 Pinch-off voltage for different substrate thickness with two sets of back-gate voltage

t_{sub} (nm)	V_P (volt)							
	SiO_2		Al_2O_3		HfO_2		TiO_2	
	$V_G =$ 0.8 V	$V_G =$ 1 V	$V_G =$ 0.8 V	$V_G =$ 1 V	$V_G =$ 0.8 V	$V_G =$ 1 V	$V_G =$ 0.8 V	$V_G =$ 1 V
5	0.32	0.48	0.31	0.49	0.33	0.52	0.34	0.51
7	0.34	0.49	0.32	0.5	0.34	0.53	0.34	0.53
10	0.34	0.5	0.34	0.51	0.37	0.54	0.37	0.55
15	0.35	0.52	0.35	0.53	0.37	0.54	0.39	0.57

enhancement of the threshold barrier. But it also leads to higher saturation current due to DIBL factor. Corresponding data is shown in Tables 1 and 2.

4 Conclusion

Centre potential, as derived from Ortiz-Conde model, is put into the existing Taur's model, and both drain current and pinch-off voltages are computed from that. The results show a good agreement in the saturation region. The effect of structural parameters and back-gate voltage is calculated, and the shift of pinch-off voltage is vividly reflected from that results. Findings have greater significance for the computation of conductance characteristics.

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