Chapter 20
Stability Analysis of STATCOM in Distribution Networks

Juan Segundo-Ramírez, Aurelio Medina Ríos and Gerard Ledwich

Abstract This chapter presents the stability analysis based on bifurcation theory of the distribution static compensator (DSTATCOM) operating both in current control mode as in voltage control mode. The bifurcation analysis allows delimiting the operating zones of nonlinear power systems and hence the computation of these boundaries is of interest for practical design and planning purposes. Suitable mathematical representations of the DSTATCOM are proposed to carry out the bifurcation analyses efficiently. The stability regions in the Thevenin equivalent plane are computed for different power factors at the Point of Common Coupling (PCC). In addition, the stability regions in the control gain space are computed, and the DC capacitor and AC capacitor impact on the stability are analyzed in detail. It is shown through bifurcation analysis that the loss of stability in the DSTATCOM is in general due to the emergence of oscillatory dynamics. The observations are verified through detailed simulation studies.

Keywords Bifurcation · DSTATCOM · Floquet multiplier · Stability regions

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20.1 Introduction

The transient and steady state response of a power system can be computed by conventional numerical integration methods; this method is known as a Brute Force approach [1]. Therefore the stability of any electric system may be computed through time domain simulations. On the other hand, with bifurcation theory it is possible to predict the system behavior around the operating points without resorting to the numerical integration solution. The results obtained with this analysis can be represented in a bifurcation diagram providing qualitative information about the behavior of the periodic steady state solutions as the parameters vary. In bifurcation points, infinitesimal changes in system parameters can cause significant qualitative changes in periodic solutions. Knowing the set of bifurcation values in the parameter space, it is possible to design an electrical circuit within stable operating conditions, but an important problem is the computation of these bifurcation sets. Upon obtaining the global feature of the bifurcation set, various non-linear phenomena, such as the coexistence of many stable states [2], the jump behavior of periodic responses [3], the phenomenon of hysteresis and the appearance of chaotic states [4], etc., can be observed. In general terms, the construction of a bifurcation diagram consists of the following steps [1, 5]: (1) find a first periodic steady-state solution, (2) based on the first solution, find other equilibrium solutions using a continuation method [1, 5], and (3) determine the stability of each solution.

The bifurcation theory has been used in stability analysis [6] for the demonstration of chaotic motions in the two-degree freedom swing equations. Subsequent applications of this theory have been directed to diverse studies such as voltage collapse [7], subsynchronous resonance [8], voltage source converters [9, 10], ferroresonance oscillations [4], and design of nonlinear controllers [11]. Furthermore, this theory has been applied to assess the dynamical behavior of nonlinear components such as induction motors [3], load models [12, 13], tap changing transformers [14], Flexible AC Transmission Systems (FACTS) [15, 16], and custom power devices [17, 18]. In addition, bifurcation theory has been used to analyze the stability of power converter and nonlinear switched circuits. In [19, 20] a wide collection of results related to nonlinear phenomena in power electronics is presented.

Conventional stability analyses in power systems are basically based on brute force approach and eigenanalysis. In these analyses, the system is modeled using root mean square (rms) quantities and the network dynamics are neglected. In this chapter, the power system is represented through instantaneous quantities, the network transients are taken into account and the electric sources voltage are assumed to be sinusoidal.

20.2 DSTATCOM

The basic purpose of the DSTATCOM is to compensate the load in such a way that at the PCC the source current and the PCC voltage are balanced and sinusoidal. The DSTATCOM can compensate the load, correct the power factor and reduce the

harmonic content in the network. This device can even regulate the voltage at the connection bus. There are important differences between the DSTATCOM and the STATCOM. The STATCOM injects almost sinusoidal a balanced three-phase current, whereas the DSTATCOM must be able to inject an unbalanced and harmonically distorted current in order to balance and eliminate the harmonic distortion in the source current. Therefore, the compensation algorithm and the control are significantly different between DSTATCOM and STATCOM. Additionally, there are two operating modes of the DSTATCOM associated to the control scheme and compensation algorithm. These operating modes are named voltage control mode and current control mode.

In order to cancel-out unbalance or harmonics in the line current, the voltage source converter that constitutes the DSTATCOM must be able to inject currents in one phase independently of the other two phases. From this point of view the structure of a DSTATCOM is very important. The DSTATCOM structure adopted in our analysis is shown in Fig. 20.1. This structure contains three H-bridge Voltage Source Converters (VSC) connected to a common DC storage capacitor. Each VSC is connected to the network through a transformer. The purpose of the transformers is to provide isolation between the inverter legs and prevents the DC capacitor from being shorted through switches of the different inverters. The converter allows three

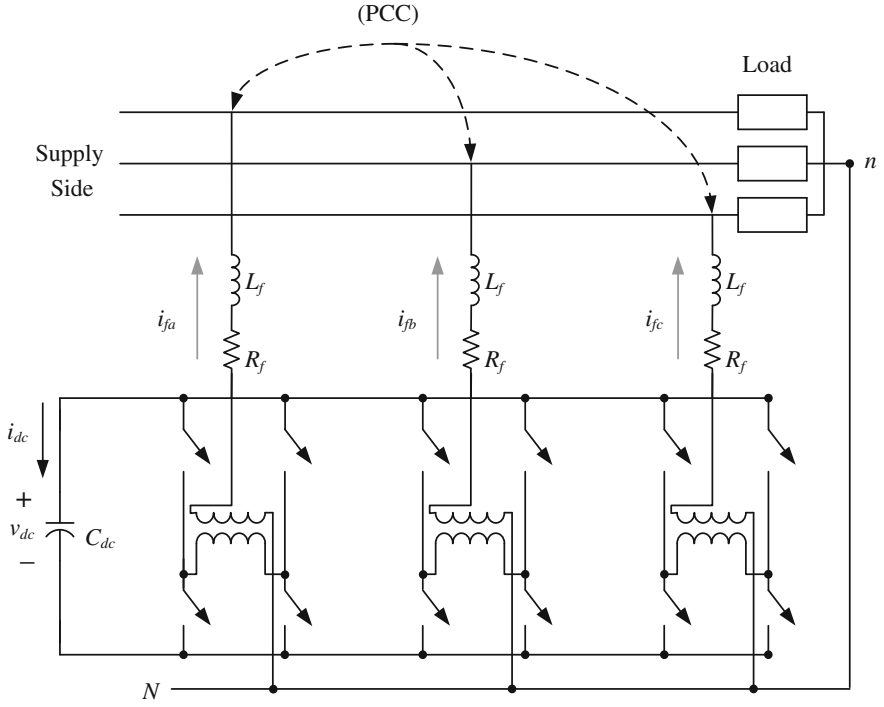

Fig. 20.1 Structure of the DSTATCOM

independent current injections. It is to be noticed that due to the presence of transformers, this topology is not suitable for canceling any DC component in the load current [21]. The inductance L_f represents the leakage inductance of each transformer and additional external inductance, if any. The switching losses of an inverter and the copper loss of the connecting transformer are represented by a resistance R_f. For more details about this structure please see [21]. This converter topology with a hysteresis modulation technique is used in this chapter for the DSTATCOM operating in voltage and current control mode; however, other topologies or modulation techniques can be used.

Now, let us consider the following nonlinear system periodically excited with a T-periodic function (20.1), which can describe the dynamic behavior of the equivalent circuit of the compensated system shown in Fig. 20.2.

$$\dot{\mathbf{x}}(t) = \mathbf{f}(t, \mathbf{x}; \mathbf{M}) \tag{20.1}$$

where $\mathbf{x}$ and $\mathbf{f}$ are n-dimensional vectors and $\mathbf{M}$ is a m-dimensional parameter vector. In particular, for the electric system shown in Fig. 20.1, the dynamic system is

$$\frac{d}{dt}\begin{bmatrix} i_s \\ v_t \\ i_l \\ i_f \\ r \end{bmatrix} = \begin{bmatrix} -\frac{R_s}{L_s} i_s - \frac{1}{L_s} v_t + \frac{v_s}{L_s} \\ \frac{1}{C_{fil}} i_s - \frac{1}{C_{fil}} i_l + \frac{1}{C_{fil}} i_f \\ -\frac{R_l}{L_l} i_l + \frac{1}{L_l} v_t - K_3 \frac{i_l}{L_l r^{m+2}} \\ -\frac{R_f}{L_f} i_f - \frac{1}{L_f} v_t + \frac{V_{dc}}{L_f} u \\ \frac{K_3}{K_2} \frac{i_1^2}{r^{m+3}} - \frac{K_1}{K_2} r^{n-1} \end{bmatrix} \tag{20.2}$$

Please notice that in (20.2) each variable is a three-phase variable. The nonlinear load is an Electric Arc Furnace (EAF); however, a different load can be connected to the PCC. The dynamic behavior of the v–i characteristic of the EAF is described by the differential equation introduced in [22]. This differential equation is based on the principle of energy balance.

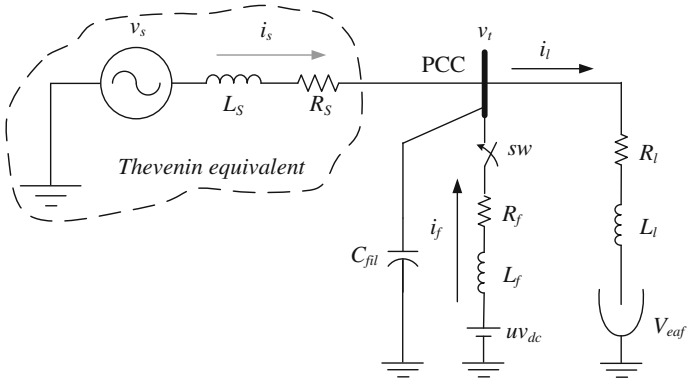

Fig. 20.2 Compensation of a weak system with an EAF

It is possible to represent the different stages of the arcing process by simply modifying the parameters of m and n in the EAF. The complete set of combinations of these parameters for different stages of the electric arc can be found in [22].

20.2.1 Simplified Representation of the DSTATCOM

In the detailed model, the switching devices, the modulation process and the DC capacitor dynamic are explicitly represented. The switching elements are modeled as ideal switches. This model sometimes requires very short time steps to well represent the commutation process; thus, the simulation time can be considerably long. If we are not interested in the switching phenomena, we can use a source having the average value computed upon a switching period. With the simplified model, one can simulate the system using a larger time step and consequently a smaller simulation time. Of course, these simplifications have to be accurate enough to preserve the information of interest. Here, two ways for obtaining simplified representations of the DSTATCOM are developed. The first one is to assume the converter as a set of ideal current or voltage sources. The second one is to assume a zero hysteresis band for the modulation technique, which is called smooth hysteresis band approach.

20.2.1.1 Ideal Sources

For this approach, the converter can be replaced by three ideal current or voltage sources, depending on the case. The link between the DC side and the AC side of the converters is well represented using the energy preservation principle. This modeling approach is equal to suppose an instantaneous response of the power electronic converters without commutation harmonics; in other words, this approach assumes that the DSTATCOM converters follow perfectly the control references.

20.2.1.2 Smooth Hysteresis Band Approach

In the ideal sources approach we assume an instantaneous response of the converter to generate the reference currents or voltages. However, this approach does not take into account neither the switching control nor the converter structure. The smooth hysteresis band approach is simpler than the ideal sources approach, since it is possible to obtain the simplified model from the detailed model in a straightforward way. In addition, this approach takes into account the converter structure and the switching control.

This model is based on the assumption that the hysteresis band shown in Fig. 20.3 is decreased until $h = 0$, as a consequence the harmonic distortion introduced by the commutation process no longer exists. The hysteresis curve in the

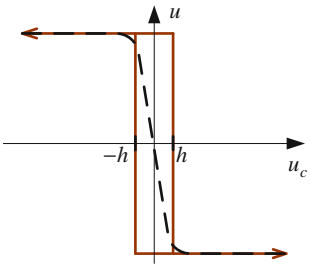

Fig. 20.3 Hysteresis modulation technique and the smooth hysteresis approximation

detailed model can be replaced for a sigmoid function or a hyperbolic tangent. The approximation of the hysteresis curve using the sigmoid function is defined as

$$u = \frac{2}{1 + e^{4u_c/h}} - 1 \tag{20.3}$$

The approximation through the hyperbolic tangent is defined as

$$u = -\tanh(u_c/h) \tag{20.4}$$

here, u_c is a continuous function defined as the controlled current or voltage obtained from measurements minus the reference signal. Figure 20.3 shows the hysteresis function represented with solid lines and the smooth hysteresis curve is drawn with dashed lines.

20.2.2 DSTATCOM Operating in Current Control Mode

In the current control mode, the DSTATCOM compensates for any unbalance or distortion in the load; thus, a balanced current from the system for any unbalance or harmonic distortion in the load is drawn [23]. One of the most important issues for the load compensation is the generation of the reference compensator currents. There are several techniques proposed [24, 25]. However, most of these methods assume that the voltage at the PCC is stiff. Unfortunately this is not a valid assumption for the most practical applications. In this chapter, the computation of the reference currents will be done using instantaneous symmetrical components [26]. For a more realistic case, the source is not assumed to be stiff.

20.2.2.1 Compensation Algorithm and Control

In (20.2), u is the control signal constrained between +1 and −1. Once the reference currents are generated, they are tracked-down in a hysteresis band current control scheme. The control signal is computed through,

$$u = hys\left(i_f - i_f^*\right) \tag{20.5}$$

where i_f^* is the reference compensation current. These are given by [26],

$$\begin{aligned} i_{fa}^* &= i_{la} - \frac{v_{ta} + (v_{tb} - v_{tc})\beta}{\sum_{x=a,b,c} v_{tfx}^2}\left(P_l^{av} + P_{loss}\right) \\ i_{fb}^* &= i_{lb} - \frac{v_{tb} + (v_{tc} - v_{ta})\beta}{\sum_{x=a,b,c} v_{tfx}^2}\left(P_l^{av} + P_{loss}\right) \\ i_{fc}^* &= i_{lc} - \frac{v_{tc} + (v_{ta} - v_{tb})\beta}{\sum_{x=a,b,c} v_{tfx}^2}\left(P_l^{av} + P_{loss}\right) \end{aligned} \tag{20.6}$$

where β is computed based on the desired power factor. In (20.6), P_l^{av} is the average power drawn by the load, P_{loss} is the power loss due to R_f, and v_{tfx} is the fundamental component of v_{tx}, for $x = a, b, c$.

The hysteresis function hys is defined by,

$$hys(w) = \begin{cases} 1 & for \quad w \leq -h \\ -1 & for \quad w > h \end{cases} \tag{20.7}$$

where 2 h is the hysteresis band.

The power loss P_{loss} is computed through the proportional controller [23], i.e.,

$$P_{loss} = K_{pdc}\left(v_{dc}^* - v_{dc}^{av}\right) + K_{idc}\int \left(v_{dc}^* - v_{dc}^{av}\right) dt \tag{20.8}$$

where v_{dc}^* is the reference DC voltage, v_{dc}^{av} is the average voltage across the DC capacitor.

To compute β, we introduce a simple *proportional-integral* control given by,

$$\beta = K_{p\beta}\left(\beta_t^* - \beta_t\right) + K_{i\beta}\int \left(\beta_t^* - \beta_t\right) dt \tag{20.9}$$

where

$$\beta_t^* = \frac{1}{\sqrt{3}}\tan\left(\cos^{-1}(PF^*)\right) \tag{20.10}$$

$$\beta_t = \frac{1}{\sqrt{3}}\tan\left(\cos^{-1}(PF)\right) \tag{20.11}$$

and PF* is the desired reference power factor at the PCC bus and PF is the measured power factor at PCC.

20.2.2.2 Simplified DSTATCOM Model

The ideal switch model has some disadvantages [27]. One way to mitigate the adverse effects on the simulation related to the switching process is to use a small integration time step to carry-out the simulation. However, it takes long simulation time. The source of numerical problems for the integration process arises from the discontinuities and the non-differentiability introduced by the ideal switch model [20, 28], and one way to avoid these problems is to smooth the switching transitions.

In Fig. 20.4 the schematic representation of the simplified DSTATCOM model in current control mode is shown. Figure 20.5 shows the schematic representation of the DC link model. The power balance between the DC and AC side can be given as,

$$\begin{aligned} P_{dc} &= v_{dc} i_{dc} \\ &= i_{fa} v_{ta} + i_{fb} v_{tb} + i_{fc} v_{tc} + R_f\left(i_{fa}^2 + i_{fb}^2 + i_{fc}^2\right) + L_f\left(i_{fa}\frac{di_{fa}}{dt} + i_{fb}\frac{di_{fb}}{dt} + i_{fc}\frac{di_{fc}}{dt}\right) \end{aligned} \tag{20.12}$$

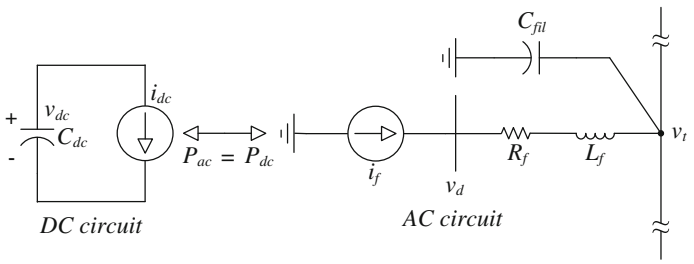

Fig. 20.4 Schematic representation for the simplified model

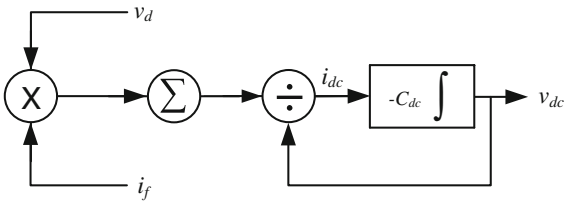

Fig. 20.5 DC link model

where

$$\frac{di_{fa}}{dt} = -\frac{\Delta\left(\frac{dv_{ta}}{dt} + \left(\frac{dv_{tb}}{dt} - \frac{dv_{tc}}{dt}\right)\beta + (v_{tb} - v_{tc})\frac{d\beta}{dt}\right) + \frac{d\Delta}{dt}}{\Delta^2}\left(P_l^{av} + P_{loss}\right) + \frac{di_{la}}{dt} - \frac{v_{ta} + (v_{tb} - v_{tc})\beta}{\Delta}\left(\frac{dP_{dc}}{dt} + \frac{dP_{loss}}{dt}\right) \tag{20.13}$$

$$\frac{di_{fb}}{dt} = -\frac{\Delta\left(\frac{dv_{tb}}{dt} + \left(\frac{dv_{tc}}{dt} - \frac{dv_{ta}}{dt}\right)\beta + (v_{tc} - v_{ta})\frac{d\beta}{dt}\right) + \frac{d\Delta}{dt}}{\Delta^2}\left(P_l^{av} + P_{loss}\right) + \frac{di_{lb}}{dt} - \frac{v_{tb} + (v_{tc} - v_{ta})\beta}{\Delta}\left(\frac{dP_{dc}}{dt} + \frac{dP_{loss}}{dt}\right) \tag{20.14}$$

$$\frac{di_{fc}}{dt} = -\frac{\Delta\left(\frac{dv_{tc}}{dt} + \left(\frac{dv_{ta}}{dt} - \frac{dv_{tb}}{dt}\right)\beta + (v_{ta} - v_{tb})\frac{d\beta}{dt}\right) + \frac{d\Delta}{dt}}{\Delta^2}\left(P_l^{av} + P_{loss}\right) + \frac{di_{lc}}{dt} - \frac{v_{tc} + (v_{ta} - v_{tb})\beta}{\Delta}\left(\frac{dP_{dc}}{dt} + \frac{dP_{loss}}{dt}\right) \tag{20.15}$$

$$\Delta = \sum_{x=a,b,c} v_{tfx}^2 \tag{20.16}$$

20.2.2.3 Comparative Analysis of Models for the DSTATCOM in Current Mode

In this section, the performance of the simplified model presented in the previous section is compared against the detailed model where the voltage source inverter based on the three H-bridge inverter is used. The test system is shown in Fig. 20.2. The system and the DSTATCOM parameters are given in Table 20.1. The hysteresis band for the detailed model is $h = 1$ A.

Initially, for $t < 0$ the switch *sw* is open and the electric circuit is in periodic steady-state. At $t = 0$ s the switch *sw* is closed and the DSTATCOM starts the compensation with the DC capacitor pre-charged at 1,200 V. Selected waveforms are presented in Fig. 20.6. Figure 20.6a shows the compensation current i_{fa}, while

Table 20.1 System parameters of the DSTATCOM in current mode

System	DSTATCOM
Voltage ($\|V_s\|$): 440 V (peak), sinusoidal and may contain harmonics, exhibit sags and swells, and possible unbalance.	Voltage controllers gains of DC capacitor loops: $K_{pdc} = 80$, $K_{idc} = 500$.
Feeder impedance (R_s, L_s): $1 + j7.54\ \Omega$	β control loop gains: $K_{p\beta} = 0.5$, $K_{i\beta} = 300$.
AC capacitor (C_{dc}): 70 μF	DC capacitor(C_{dc}): 1,500 μF
Feeder load impedance (R_l, L_l): $0.5 + j3.77\ \Omega$	Interface circuits (R_f, L_f): $0.05 + j3.77\ \Omega$
EAF constants: $K_1 = 15$, $K_2 = 0.05$, $K_3 = 800$, $m = 0$ and $n = 2$.	Reference value of DC capacitor voltage: 1,200 V

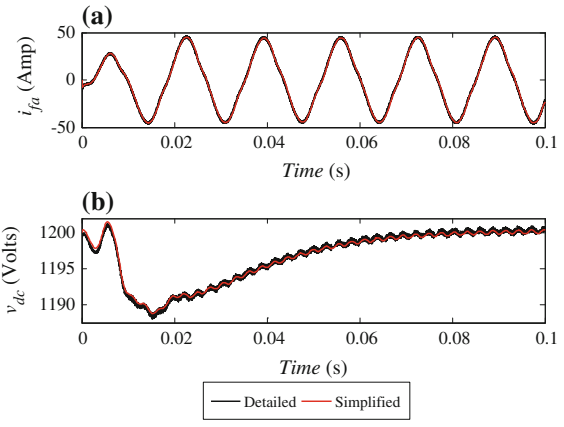

Fig. 20.6 Comparison in the time domain between the detailed and the simplified model for **a** compensation current i_{fa} and **b** DC capacitor voltage v_{dc}

Fig. 20.6b shows the DC voltage v_{dc} with the simplified model and with the detailed model for an integration step size of 65 and 1 μs, respectively. A good agreement between the two models has been achieved, even though the simplified model has a considerably larger integration step size (125 times).

20.2.3 DSTATCOM Operating in Voltage Control Mode

Here, the control strategy proposed in [29] is used. With this algorithm, the DSTATCOM operates as a voltage regulator to maintain constant the voltage of a specified bus (PCC). The magnitude of the bus voltage is pre-specified while its phase angle is generated from a DC capacitor control loop. A deadbeat controller for the inverter is used for voltage tracking. With this algorithm, the DSTATCOM can compensate the terminal voltage, for any distortion or unbalance in the load or in the voltage source.

20.2.3.1 Simplified DSTATCOM Model

In the simplified model, the three H-bridge converters are replaced by three controllable voltage sources. The main advantage of this model is to allow larger integration steps with high precision and reliability. In Fig. 20.7, the schematic representation for the simplified model of DSTATCOM operating in voltage mode is shown. This model is based on the assumption that $v_{tx} = v_{tx}^*$, where v_{tx}^* is the reference terminal voltage. Figure 20.8 shows the schematic representation of the DC link model.

The reference terminal voltage v_{tx}^* is

$$v_{tx}^* = V_m \sin(\omega t - \delta - \phi_x) \tag{20.17}$$

and δ is computed using a proportional-integral controller described by,

$$\delta = K_{p\delta}\left(P_{sh} - P_{sh}^*\right) + K_{i\delta}\int \left(P_{sh} - P_{sh}^*\right) dt \tag{20.18}$$

P_{sh} is the instantaneous power reference in the shunt link and P_{sh}^* is its reference; P_{sh} is given by

$$P_{sh} = v_{ta}i_{fa} + v_{tb}i_{fb} + v_{tc}i_{fc} \tag{20.19}$$

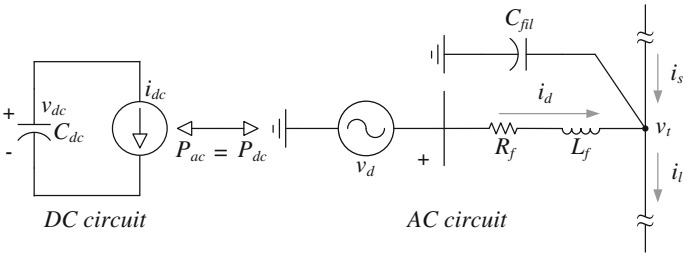

Fig. 20.7 Schematic representation for the simplified model

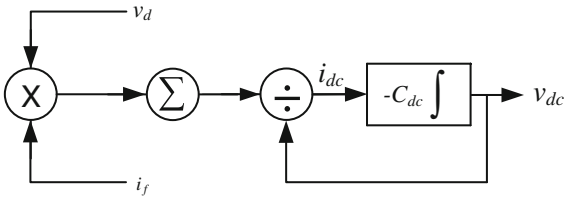

Fig. 20.8 DC link model

P_{sh}^{*} is obtained as,

$$P_{sh}^{*} = K_{pdc}\left(v_{dc}^{average} - v_{dc}^{*}\right) + K_{idc}\int \left(v_{dc}^{average} - v_{dc}^{*}\right)dt \tag{20.20}$$

where v_{dc}^{*} is the reference DC voltage, $v_{dc}^{average}$ is the average voltage across the DC capacitor. The converter terminal voltage is given by,

$$v_{dx} = R_f i_{dx} + L_f \frac{di_{dx}}{dt} + v_{tx} \tag{20.21}$$

The current injected by the compensator is calculated by,

$$i_{dx} = -C_{fil} V_m \sin(\omega t - \delta - \phi_x)\left(\omega - \frac{d\delta}{dt}\right) + i_{lx} - i_{sx} \tag{20.22}$$

The first derivative of i_{dx} is computed as,

$$\frac{di_{dx}}{dt} = \frac{d(i_{lx} - i_{sx})}{dt} - C_{fil} V_m \left(\sin(\omega t - \delta - \varphi_x)\frac{d^2\delta}{dt^2} + \cos(\omega t - \delta - \varphi_x)\left(\omega - \frac{d\delta}{dt}\right)^2\right) \tag{20.23}$$

The dynamic capacitor voltage is given by,

$$C_{dc}\frac{dv_{dc}}{dt} = -\frac{i_{da}v_{da} + i_{db}v_{db} + i_{dc}v_{dc}}{v_{dc}} \tag{20.24}$$

where

$$x =$$
$$\phi_a = 0,\ \phi_b = 2\pi/3,\ \phi_a = -2\pi/3$$

$$\frac{d\delta}{dt} = K_{p\delta}\left(\frac{dP_{sh}}{dt} - K_{pv}\frac{dv_{dc}^{average}}{dt}\right) + K_{i\delta}\left(P_{sh} - P_{sh}^{*}\right) \tag{20.25}$$

$$\frac{d^2\delta}{dt^2} = K_{p\delta}\left(\frac{d^2P_{sh}}{dt^2} - K_{pv}\frac{d^2v_{dc}^{average}}{dt^2}\right) + K_{i\delta}\left(\frac{dP_{sh}}{dt} - K_{pv}\frac{dv_{dc}^{average}}{dt}\right) \tag{20.26}$$

Table 20.2 System parameters of the DSTATCOM in voltage mode

System Parameters	DSTATCOM
Voltage (V_s): 440 V (peak), sinusoidal and may contain harmonics, exhibit sags and swells, and possible unbalance	Voltage controllers gains of DC capacitor loops: K_{pdc} = 154, K_{idc} = 3,500
Feeder impedance (R_s, L_s): 1 + j7.54 Ω	δ control loop gains: $K_{p\delta}$ = 27e−6, $K_{i\delta}$ = 8e−3
AC capacitor (C_{ac}):70 μF	DC capacitor(C_{dc}): 1,500 μF
Feeder load impedance (R_l, L_l): 0.5 + j3.77 Ω	Interface circuits (R_f, L_f): 0.05 + j3.77 Ω
EAF constants: K_1 = 15, K_2 = 0.05, K_3 = 800, m = 0 and n = 2	Reference value of DC capacitor voltage: 1,200 V

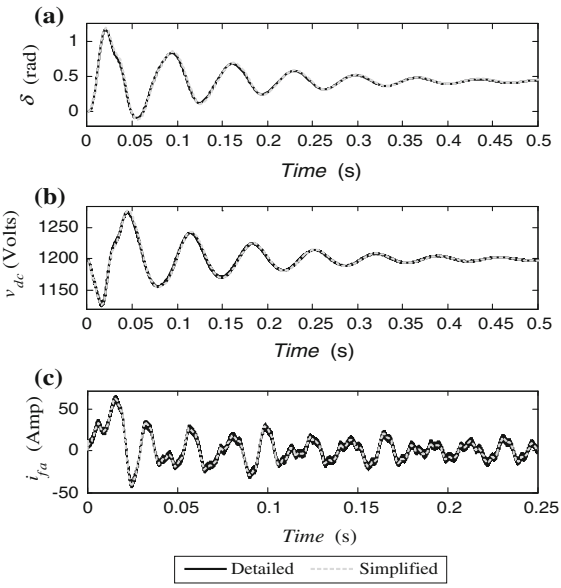

Fig. 20.9 Comparison in the time domain between the detailed and the simplified model for **a** phase angle δ, **b** DC capacitor voltage v_{dc}, and **c** compensation current i_{fa}

20.2.3.2 Comparative Analysis of Models for the DSTATCOM in Voltage Control Mode

In this section, the performance of the simplified DSTATCOM model is compared against the detailed model. The system parameters and the DSTATCOM parameters for the circuit shown in Fig. 20.2 are given in Table 20.2. The hysteresis band for the detailed model is h = 10.

Initially, the electric system is in periodic steady state and the switch sw is open. At t = 0 s, the switch sw is closed, thus, the DSTATCOM starts to regulate the terminal voltage v_t at the PCC bus. Figure 20.9a shows the results comparison for the phase angle δ, Fig. 20.9b shows the comparison for the voltage across the DC

capacitor v_{dc}, and Fig. 20.9c for the compensation current ifa. The results show a very good agreement between the simplified model and the detailed model, with an integration step size of 60 and 1 μs, respectively. An excellent agreement between the two models is achieved, even though the simplified model has a considerably larger integration step (60 times).

20.2.4 Comparison of the Simplified Modeling Approaches

20.2.4.1 DSTATCOM Operating in Current Mode

A comparison between the detailed model and the simplified model based on the ideal source approach is shown in Fig. 20.10. The compensator current i_{fa}, the terminal voltage v_{ta}, and the DC voltage capacitor v_{dc}, are shown in Fig. 20.10a, b, and c respectively.

The same comparison for the simplified model based on the hyperbolic tangent approach is presented in Fig. 20.11. For this numerical experiment, the hysteresis band has been selected as $h = 5$ A. Observe that the DC voltage capacitor computed with the ideal current source models has a small error. This error is because this model assumes that the DSTATCOM generates the compensation currents instantaneously. The model based on the hyperbolic tangent gives much better solutions since it is not based on this assumption.

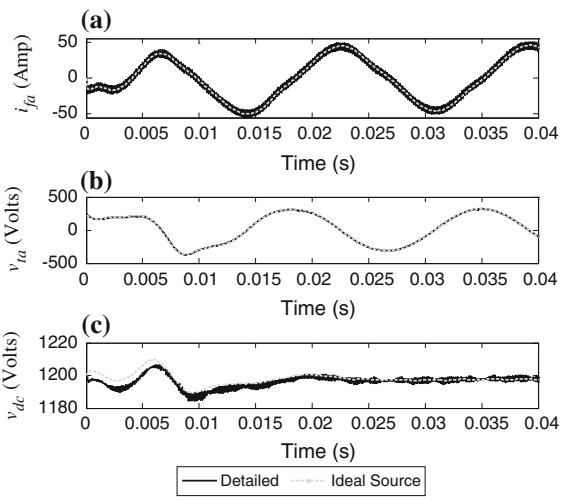

Fig. 20.10 Comparison in the time domain between the detailed and the simplified model based on the ideal source approach for **a** compensation current i_{fa}, **b** terminal voltage v_{ta}, and **c** DC capacitor voltage v_{dc}

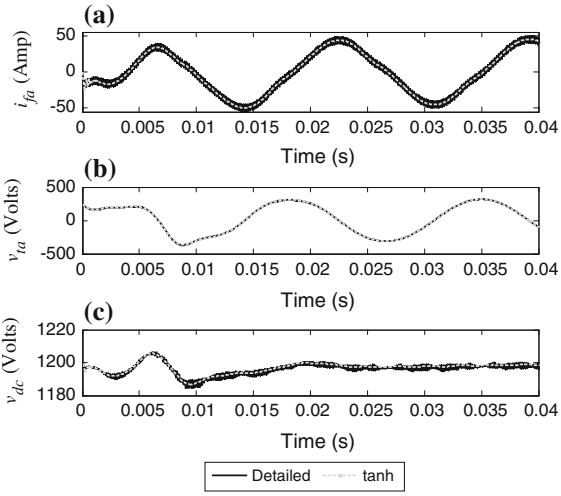

Fig. 20.11 Comparison in the time domain between the detailed and the simplified model based on the smooth hysteresis band approach for **a** compensation current i_{fa}, **b** terminal voltage v_{ta}, and **c** DC capacitor voltage v_{dc}

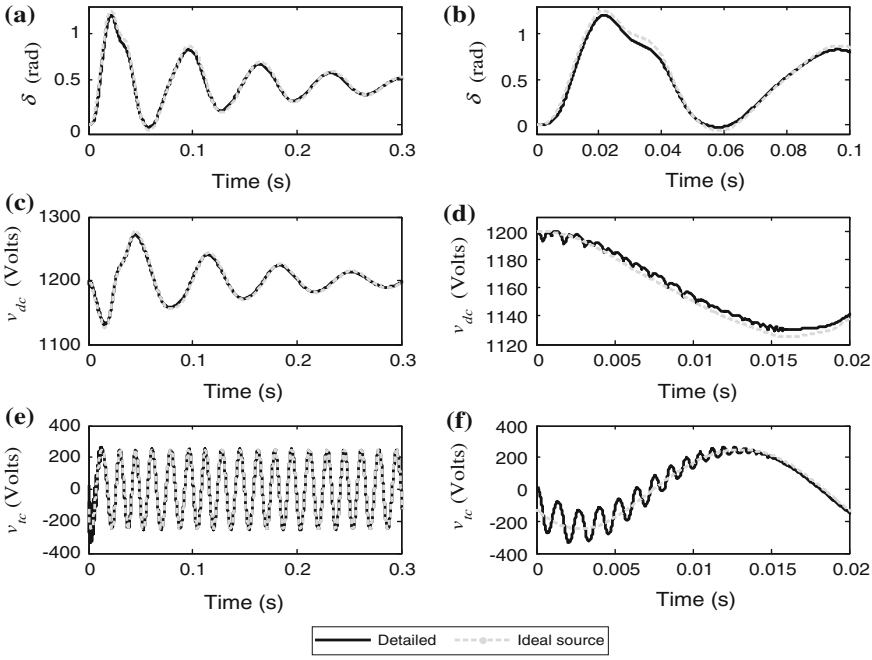

Fig. 20.12 Comparison in the time domain between the detailed and the simplified based on the ideal source approach for **a** phase angle δ, **b** phase angle δ during the first 0.02 s, **c** DC capacitor voltage v_{dc}, **d** DC capacitor voltage v_{dc} during the first 0.02 s, **e** terminal voltage v_{tc}, and **f** terminal voltage v_{tc}

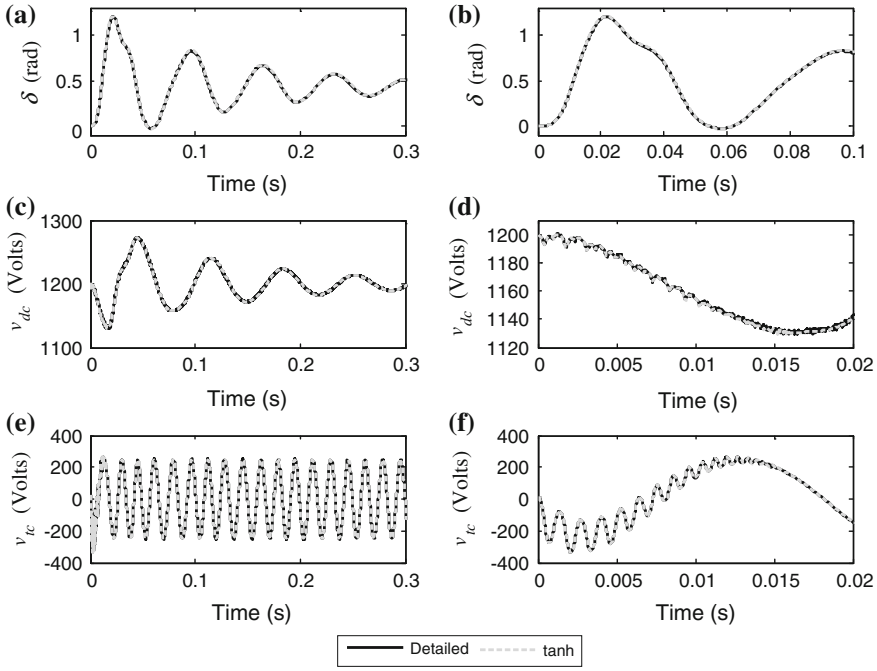

Fig. 20.13 Comparison in the time domain between the detailed and the simplified based on the smooth hysteresis band approach for **a** phase angle δ, **b** phase angle δ during the first 0.02 s, **c** DC capacitor voltage v_{dc}, **d** DC capacitor voltage v_{dc} during the first 0.02 s, **e** terminal voltage v_{tc}, and **f** terminal voltage v_{tc}

20.2.4.2 DSTATCOM Operating in Voltage Mode

The solution comparison for the DSTATCOM operating in voltage mode for the phase angle δ, the DC capacitor voltage v_{dc}, and the terminal voltage v_{ta} are presented in the Fig. 20.12a, c and e respectively. Observe from Fig. 20.12b, d and f that for this particular case, the solution obtained with the simplified model based on ideal voltage sources is not accurate during the first cycles.

The same comparison for the simplified model based on the hyperbolic tangent is presented in Fig. 20.13. Please notice that the initial transients can be accurately reproduced with the simplified model based on this approach.

The presented simplified models allow the fast computation of the periodic steady state solution by time domain simulations and by the application of an iterative method such as the Newton method. This method computes the periodic steady state solution despite its stability and it is commonly used as the corrector in the continuation methods for tracing bifurcation diagrams. Due to the discontinuity of the detailed model, the Newton method presents convergence issues and becomes difficult the construction of stability regions. To tackle these issues, the previously presented simplified models can be used instead. In particular, the fastest

and best suited modeling approach was that based on ideal sources, therefore, this will be used for the bifurcation analysis and the detailed models will be used to corroborate the computed stability regions.

20.3 Stability Analysis of Periodic Steady State Solutions

Continuation schemes are used to determine how the solutions of a system vary with a given parameter. Implementing a predictor–corrector scheme, a continuation algorithm can trace the path of an already established solution as the parameters are varied. XPPAUTO [30] is a software package widely used for this purpose; however, this software has not been used in the presented analyses since it has convergence problems to trace the bifurcation diagrams of periodically forced nonlinear-switched systems. In this chapter, the sequential method [5] is used as the predictor; in this method, the periodic solution determined in the previous step is used as an initial guess for the periodic solution to be determined in the next step. After the third point, an extrapolation method based on the cubic spline is used as a predictor. The Newton method based on the direct exponential expansion (DEE) process [31] is used as the corrector.

The stability of a periodic solution is computed from its Floquet multipliers; they describe the stability near the limit cycle of interest. Floquet theory is based on the observation that a periodic solution can be represented through a fixed point of an associated Poincaré map. Consequently, the stability of a periodic solution can be determined by computing the stability of the corresponding fixed point of the Poincaré map. The Floquet multipliers are the eigenvalues of the Jacobian of this Poincaré map obtained in the DEE method. Stable periodic solutions correspond to Floquet multipliers inside the unit circle; on the other hand, unstable periodic solutions have at least one Floquet multiplier outside the unit circle. Therefore, loss of stability is encountered when a multiplier leaves the unit circle; this can occur in three different ways: A fold bifurcation is encountered when a single real Floquet multiplier crosses the unit circle at +1. The flip bifurcation or period-doubling bifurcation takes place when a single real Floquet multiplier crosses the unit circle at −1. At this bifurcation point, the prevailing solution branch becomes unstable and a new branch is born. Solutions on this new branch have twice the period of the previous limit cycle. The generalized Hopf bifurcation or Neimark bifurcation is found when two complex conjugated Floquet multipliers leave the unit cycle.

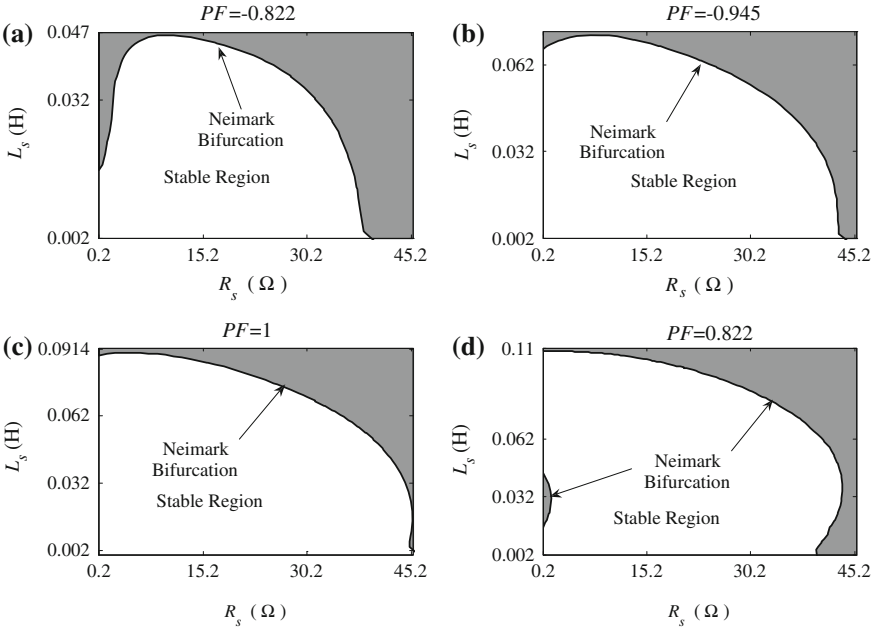

Fig. 20.14 Stability regions for the DSTATCOM operating in current control for different power factors at the terminal bus with $|V_s|$ = 440 V

20.3.1 Stability Analysis of the DSTATCOM in Current Control Mode

20.3.1.1 Stability Regions in the L_s-R_s Plane

The network of Fig. 20.2 has been represented through its Thevenin equivalent. The network upstream from the PCC towards the source side may contain different feeders and loads. Thus, the radial line and the source shown in figure is a Thevenin representation of the upstream network, where v_s, R_s, and L_s represent the Thevenin equivalent looking towards the left into the network. Since the Thevenin equivalent can change at any time depending on the load at left side of the PCC, it is desirable to assess a set of v_s, R_s, and L_s, for which the DTATCOM performance is stable.

For the electric system shown in Fig. 20.2, only the Neimark bifurcation was located in the parametrical-space used in this analysis. In analogy with the Hopf bifurcation, a bifurcation is expected at a critical value, as the limit cycle losses its stability, so that an attracting torus is born; this is the secondary Hopf bifurcation or a Neimark bifurcation. Besides, the bifurcated solution can be either stable and supercritical or unstable and subcritical [5].

Figure 20.14 shows the bifurcation set on the R_s–L_s plane. This Figure shows the stability regions for different power factor corrections with $|V_s|$ = 440 V, where $|V_s|$

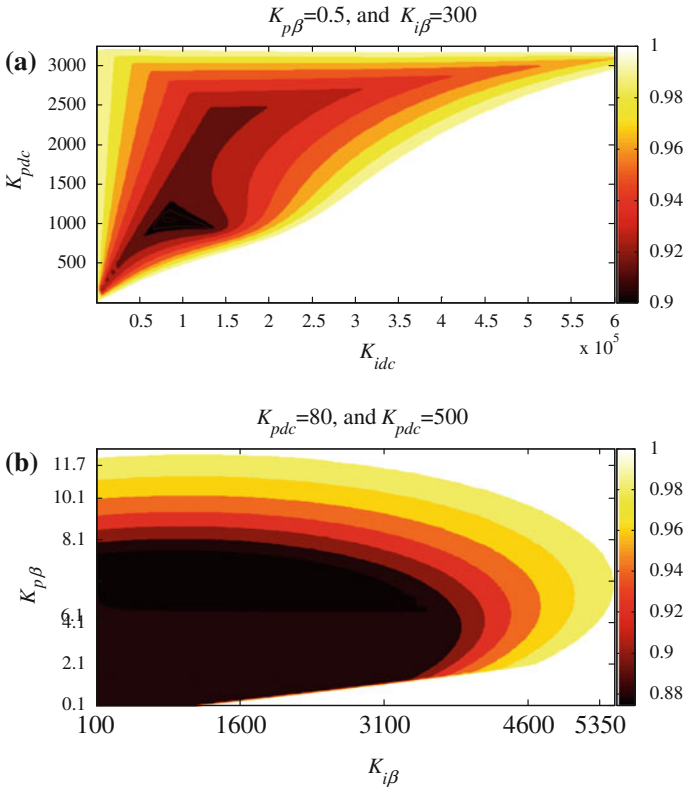

Fig. 20.15 Stability regions for the DSTATCOM operating in current control mode in **a** the K_{idc} – K_{pdc} space, and **b** $K_{i\beta}$ – $K_{p\beta}$ space

is the peak value. The solid line represents the Neimark bifurcation set. Inside the contour line the solutions are T-periodic and the gray zones represent the unstable regions. The stable region in the R_s–L_s plane changes according to the power factor at the PCC. For instance, Fig. 20.14d shows that for a 0.822 lead power factor, an unstable region within the stable region exists. In a practical distribution system, the set (R_s, L_s) is smaller than those stable sets computed through the bifurcation analysis, which means that for all the possible operating points the DSTATCOM operating in current control mode will properly compensate.

20.3.1.2 Stability Regions in the Gains Plane

In this section, the stability region in the K_{idc} – K_{pdc} space, and in the $K_{i\beta}$ – $K_{p\beta}$ space, as well as the contour lines for different Floquet multipliers are computed. Figure 20.15a shows the stability regions in the K_{idc} – K_{pdc} space, and Fig. 20.15b shows the stability regions in the $K_{i\beta}$ – $K_{p\beta}$ space. Also, in these figures, contour

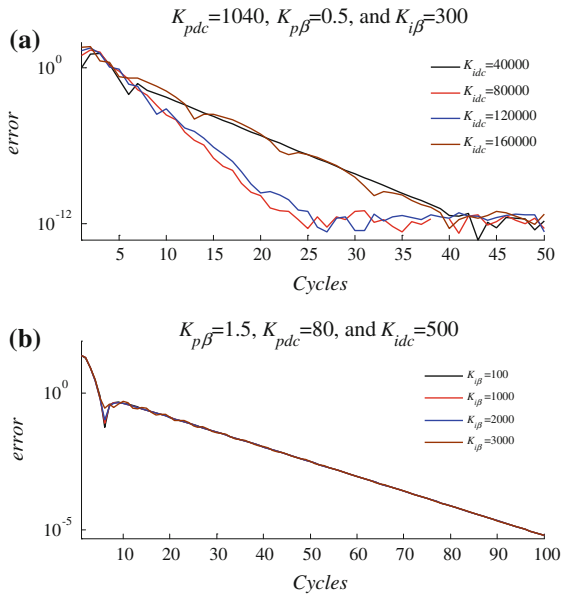

Fig. 20.16 Convergence errors for different gains in the DSTATCOM controllers. **a** For DC capacitor voltage controller. **b** For power factor controller

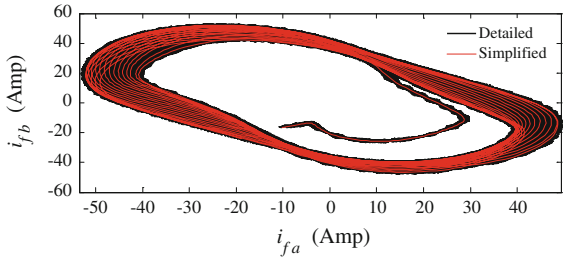

Fig. 20.17 Quasiperiodic solution for $K_{p\beta} = 0.5$, $K_{i\beta} = 300$, $K_{pdc} = 1{,}040$, and $K_{idc} = 2.5 \times 10^5$. i_{fa} versus i_{fb}

lines are presented for different Floquet multipliers to show the different speed of response. For example, from the Fig. 20.15a, it is easy to notice that the pair of gains $K_{idc} = 80{,}000$ and $K_{pdc} = 1{,}040$ give the fastest response. The implementation of this set of gains in a physical controller depends on the precision available in the hardware and software employed.

Figure 20.16a shows time domain simulations of the convergence error for $K_{pdc} = 1{,}040$ and different K_{idc}. It can be observed that this agrees with the bifurcation diagram of Fig. 20.15a. From Fig. 20.15b, it is easy to notice that in the stable region, there is an important area for which the maximum Floquet multiplier

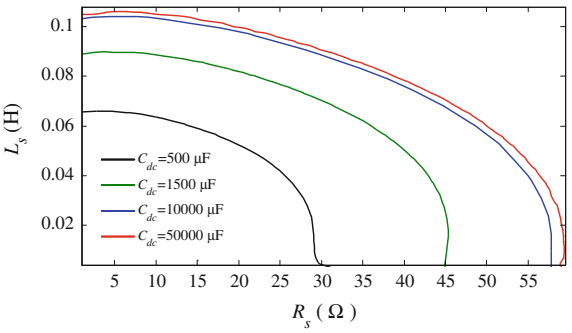

Fig. 20.18 Comparison between the stability regions for different DC capacitors

is constant. This means that for this area, the speed of response should be almost the same. To corroborate this observation, the convergence error for $K_{p\beta} = 1.5$ and different $K_{i\beta}$ is shown in Fig. 20.16b. As expected, the convergence error is almost the same in this area.

Figure 20.17 shows the torus solution for compensation current i_f for $K_{p\beta} = 0.5$, $K_{i\beta} = 300$, $K_{pdc} = 1{,}040$, and $K_{idc} = 2.5 \times 10^5$. This operating point corresponds to a quasiperiodic solution. Please notice that the detailed model and the simplified model are in very good agreement, even in the unstable regions.

20.3.1.3 DC Capacitor Impact on the Stability

The impact of the DC capacitor size in the stability regions in the $R_s - L_s$ plane is qualitatively shown through bifurcation analysis. This analysis shows that the stable region increases asymptotically as the DC capacitor size increases, thus, the size of the DC capacitor can be chosen to suit the load demand. Figure 20.18 shows the stability regions in the $R_s - L_s$ plane for different DC capacitor sizes.

20.3.1.4 AC Capacitor Impact on the Stability

The purpose of the capacitor filter C_{fil} is to provide a path for the switching harmonic current introduced by the DSTATCOM. However, it is shown in [23], that this passive filter has an important impact on the DSTATCOM performance and on its stability. High capacitances in the capacitor filter provide a low impedance path for the harmonic currents. However, there are three problems related to high capacitances. The first one is the cost, the second one is that the speed of response becomes slower, and the third one is that the stable region decreases as the capacitance becomes larger. This is shown in Fig. 20.19, where the stability region in the $R_s - L_s$ plane has been computed for three different capacitor filters.

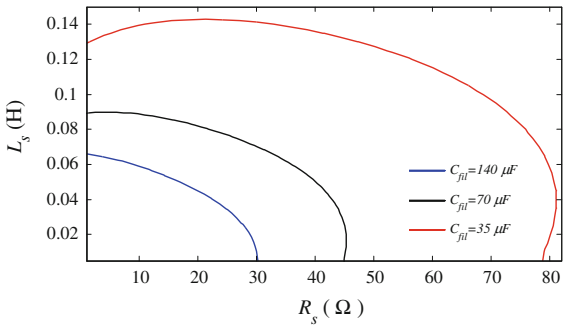

Fig. 20.19 Comparison between the stability regions for different AC capacitors

20.3.2 Bifurcation Analysis for DSTATCOM in Voltage Control Mode

In this section, the bifurcation theory is applied to the same system to assess the stability regions of the electric system including the DSTATCOM operating in voltage control mode. In the section to follow, bifurcation diagrams in the Thevenin space are computed to show the set of L_s, R_s, and v_s (derived from Thevenin reactance) for which the DSTATCOM contains stable solutions. The stability regions on the gains space are calculated through bifurcation theory, and the set of gains for the fastest speed response of the DSTATCOM is obtained from this analysis. Besides, the gains impact on the stability regions in the Thevenin space is analyzed. Finally, the AC and DC capacitors size impact on the stability in the Thevenin space is analyzed.

The simplified DSTATCOM model based on ideal sources is used in this analysis; however, the solutions will be compared against the detailed DSTATCOM model to validate the results. The simplified model is used in this analysis rather than the detailed model basically because the detailed model does not allow the correct implementation of the shooting method during the correcting process in the computation of the bifurcation branches through the continuation methods.

20.3.2.1 Stability Regions in the $R_s - L_s$ Plane

The Fig. 20.20 shows the bifurcation set on the $L_s - R_s$ plane for different Thevenin voltages. The dotted line represents the Neimark bifurcation set. Inside the contour line the solutions are T-periodic, and the dark zone is the unstable region. The stability region for $|V_s| = 350$ V, $|V_s| = 400$ V, and $|V_s| = 440$ V, are shown in Fig. 20.20a–c, respectively. In Fig. 20.20d a comparison is presented between the different stability boundaries; the stability region decreases as the source voltage becomes smaller. Also, Fig. 20.20a–c can be seen as bifurcation diagrams in the Thevenin space.

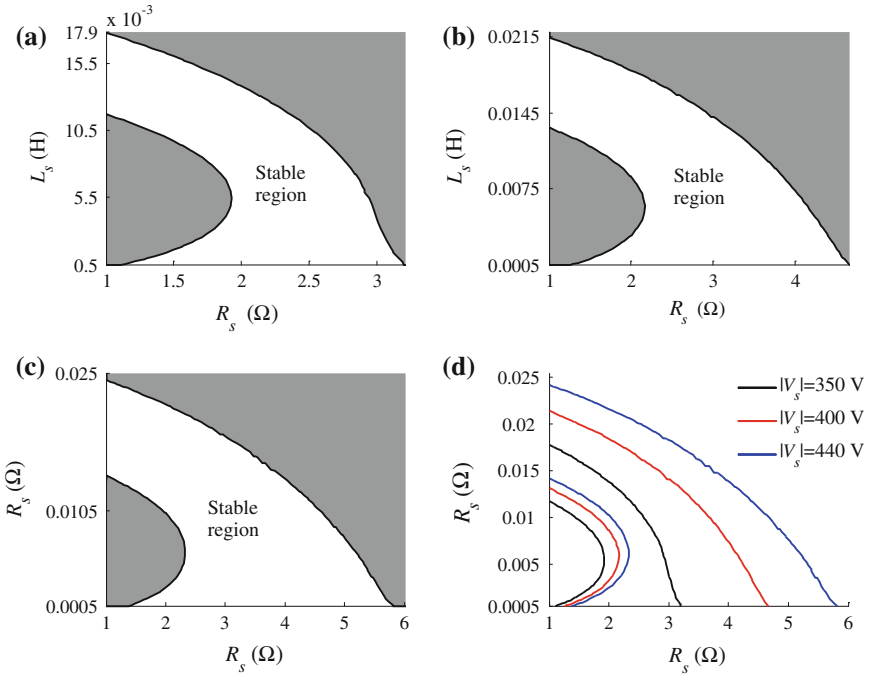

Fig. 20.20 Stability regions for the DSTATCOM operating in voltage control in the $L_s - R_s$ plane for different Thevenin equivalent voltages; **a** $|V_s| = 350$ V, **b** $|V_s| = 400$ V, and **c** $|V_s| = 440$ V and **d** comparison of the stability boundaries

Figure 20.20d shows that the only region for which the DSTATCOM properly operates in the Thevenin space for $|V_s|$ is from 350 to 440 V; between the inner stability boundary of $|V_s| = 440$ V and the outer stability boundary of $|V_s| = 350$ V. In this region, the DSTATCOM can compensate any disturbance from the network.

20.3.2.2 Stability Regions in the Gains Plane

The dynamic behaviour of the DSTATCOM in transient state is strongly related to the gain of the PI controllers; therefore, an important task to do deals with the proper gains assessment. In addition, the set of gains has an important impact on the DSTATCOM steady state performance, since they modify the stability regions. In this section the stability region in the $K_{idc} - K_{pdc}$ space, and in the $K_{i\delta} - K_{p\delta}$ space are computed, as well as the contour lines for different Floquet multipliers, with the purpose of assessing the set of gains for which the fastest speed of response is obtained. Figure 20.21b in the $K_{idc} - K_{pdc}$ space. Also, in these figures, contour lines are presented for different Floquet multipliers to show the different speed of response. Figure 20.22a shows the convergence error for different pairs of gains $K_{i\delta}$

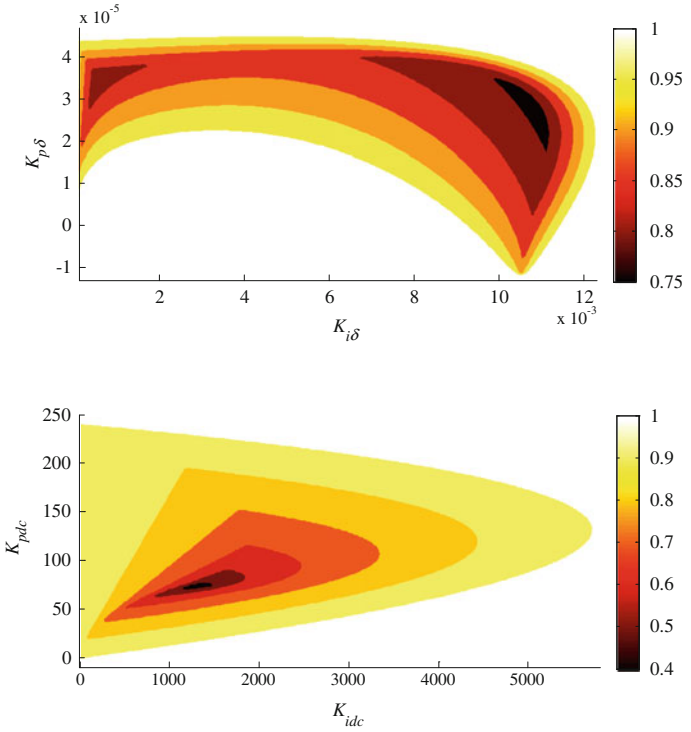

Fig. 20.21 Stability regions for the DSTATCOM operating in voltage control mode. (*Top*) $K_{i\delta}$ –$K_{p\delta}$ space. (*Bottom*) K_{idc} –K_{pdc} space

– $K_{p\delta}$. In Fig. 20.22a, the convergence error for $K_{p\delta} = 30 \times 10^{-6}$, and different $K_{i\delta}$ are shown. From this figure, we can see that the fastest response is around $K_{i\delta} = 10.5 \times 10^{-3}$ and $K_{p\delta} = 30 \times 10^{-6}$. Figure 20.22b shows the convergence error for $K_{pdc} = 74$, and different K_{idc}. From this figure, it is easy to see that the fastest response is around $K_{pdc} = 74$ and $K_{idc} = 1{,}320$. These results are in agreement with the bifurcation analysis illustrated in Fig. 20.21.

As mentioned previously, the gains of the controller have a direct impact on the system stability. However, it is not known how the size of the stable region in the Thevenin space varies as the gains are varied. To investigate the effect of the gains variation in the stability of the system, a bifurcation analysis is carried-out to assess the stable and unstable regions for different sets of gains. In particular, the stability region obtained for $K_{idc} = 1{,}320$, $K_{pdc} = 74$, $K_{i\delta} = 8 \times 10^{-3}$, and $K_{p\delta} = 27 \times 10^{-6}$ with $|V_s| = 440$ V is compared against that shown in Fig. 20.20c. This comparison is shown in Fig. 20.23; it can be noticed that the size of the stable regions significantly change as we change the set of gains. Figure 20.23 has been computed using the parameters given in Table 20.2; only the gains are varied.

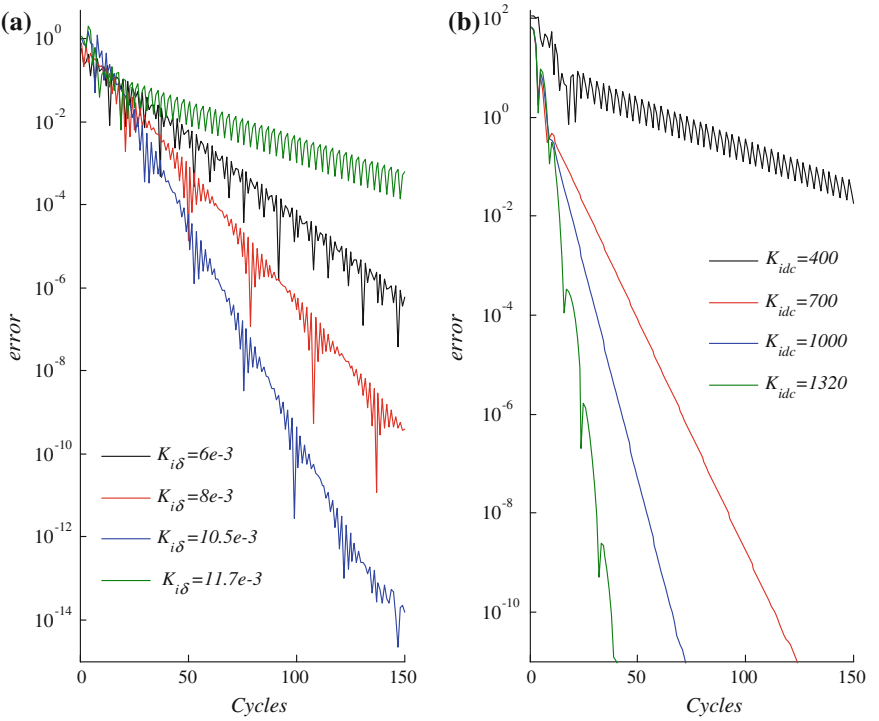

Fig. 20.22 Convergence errors for different gains of the DSTATCOM controllers. **a** For δ controller. **b** For the DC capacitor voltage controller

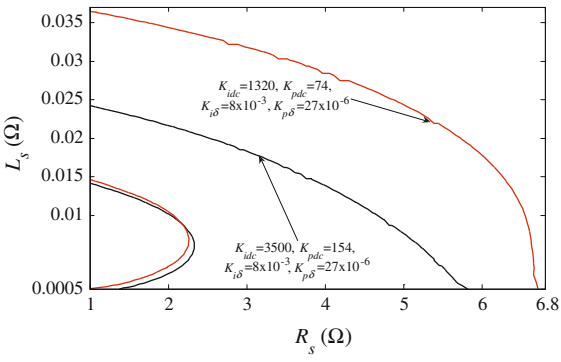

Fig. 20.23 Comparison between the stability regions for two sets of gains

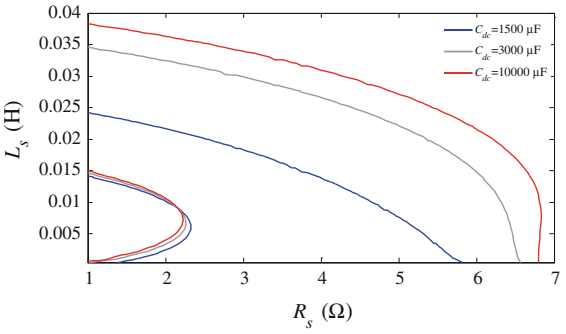

Fig. 20.24 Comparison between the stability regions for different DC capacitors

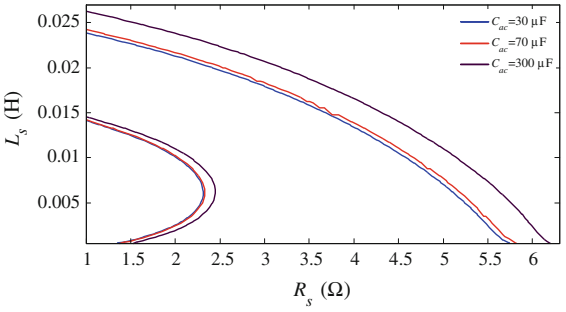

Fig. 20.25 Comparison between the stability regions for different AC capacitors

20.3.2.3 DC Capacitor Impact on the Stability Region

The DC capacitor is a very important element in the design of DSTATCOM, as it stores the energy necessary to compensate the load during disturbances. In steady state, the DSTATCOM has to provide the active power fluctuation and the reactive power demanded by the system, in order to maintain the voltage at the PCC bus. Thus, the DC capacitor size is important for the compensator performance, i.e., larger capacitances the storage more energy, consequently the DSTATCOM could bear larger and more severe disturbances. This observation suggests that the stable region increases as the DC capacitor size becomes larger. To corroborate this, a comparison between the stability regions for different DC capacitor sizes is presented in Fig. 20.24. It can be seen that the stable regions on the $L_s - R_s$ asymptotically increases as the DC capacitor becomes larger. Please notice that even the inner unstable region decreases as the AC capacitor size increases. Figure 20.24 has been computed using the parameters given in Table 20.2. From this analysis, the DC capacitor size can be selected to suit the load demand. Obviously, the selected DC capacitor size also depends on its cost.

20.3.2.4 AC Capacitor Filter Impact on the Stability Region

The main purpose of the AC capacitor filter is to drain the harmonic currents coming from the DSTATCOM converters. A small AC capacitor size presents high impedance to the harmonic currents; in consequence, the harmonic currents are not efficiently drained. For a large AC capacitor size, the harmonic currents are efficiently drained; however, there are some problems with a large AC capacitor filter. For instance, the transients in a capacitor increase as its size increases. To assess the AC capacitor filter impact on the stability, the stable regions in the Thevenin plane have been compared for three different AC capacitors; this comparison can be seen in Fig. 20.25. From this figure, it easy to notice that the AC capacitor has a positive impact on the stability, since the stable region on the L_s–R_s plane increases as the AC capacitor becomes larger. However, it should be noticed that not only the outer boundary increases; the inner boundary becomes larger as well. Basically, the AC capacitor filter size has a positive effect on the stability because the AC capacitor acts as reactive power compensator as well, and this action reduces the reactive power injected by the DSTATCOM to maintain the reference terminal voltage. Figure 20.25 has been computed using the parameters of Table 20.2.

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