Filter and Closed Loop Control Technology of Piezoelectric Drivers

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Abstract. The sluggish, nonlinearity of piezoelectric drivers will greatly reduce the pointing accuracy of a precision tracking system for inter-satellite laser communication, and affect link stability. In order to solve the problem of sluggish, nonlinearity, external interference and badly dynamic response performance of piezoelectric drivers. This paper provides a close loop algorithm which was combined with Butterworth filtering algorithm and PID control algorithm. First, the realization method of PID control algorithm was analyzed based on FPGA processor. Then, in order to solve the influence of noise on the sensor signal, the design and simulation of Butterworth filter algorithm was introduced. Finally, the test was carried out on the hardware platform. Experimental results indicate that the closed loop algorithm effectively solves the sluggish and nonlinearity problems, and pointing accuracy is increased from 6urad to 3urad. It can satisfy laser communication system requirements of higher precision.

Keywords: Computer vision · Edge detection · Geometric figure · Curve fitting · Sub pixel

1 The Introduction

Space laser communication has the characteristics of wide band and narrow beam, which is suitable for high rate and anti-interference communication [1]. Laser communication has unique advantages in satellite communication, and will be more and more fully confirmed. The narrow laser beam leads to many technical challenges in the beam alignment, so the most important thing is the acquisition, pointing, tracking, APT technology of long distance and high precision beam [2]. One of the key problems is the control technology of precision tracking system. The most remarkable characteristics of fine tracking control are high servo bandwidth and tracking accuracy but small dynamic range [3]. It can further effectively suppress the coarse tracking residuals and has a strong ability to suppress the vibration of wide power spectrum [4, 5], so as to ensure fast and high precision alignment and tracking. The final tracking accuracy of the composite axis APT subsystem mainly depends on the tracking accuracy of the fine tracking servo unit, so the fine tracking unit is the core unit of the composite axis APT system. However, the precision of the fine tracking actuator as well as its own characteristics will certainly become the factors that cannot be ignored affecting the precision of the fine tracking system and even the whole system.

In order to improve the execution accuracy of the piezoelectric fine tracking actuator, it is necessary to solve the unique hysteresis and nonlinearity of the piezoelectric actuator at first [6–10]. In order to solve these problems, many control algorithms have been proposed at home and abroad, such as the compound control algorithm based on Fuzzy-PID [11]. Many improved PID algorithms [12–16], such as adaptive reverse control and neural network control, have compensated the deficiencies of PID control to a certain extent. However, in practical engineering applications, PID control algorithm is still the control method adopted in most occasions due to its advantages of simple structure, high reliability and fast speed [17].

In this paper, through the analysis of the characteristics of piezoelectric fine tracking actuator, a filtering closed-loop control algorithm based on FPGA processor combining Butterworth filtering algorithm and PID control algorithm is proposed. Through experimental verification, the algorithm successfully solves the hysteresis, nonlinear and other problems of piezoelectric fine tracking actuator. Combined with FIR filtering algorithm, it effectively solves the problem that the fine tracking actuator is susceptible to external interference and noise.

2 Design of Filtering Closed-Loop Control Algorithm

2.1 PID Control Algorithm Design

Digital PID is the traditional continuous PID discretization, easy to achieve in the computer. This controller adopts incremental digital PID controller, which is a form of PID control. The closed-loop control of the system can be realized by adjusting the three parameters of the PID controller: proportion, integral and differential.

The basic structure of a typical control system includes input, sampling, controller, controlled object and output, as shown in Fig. 1.
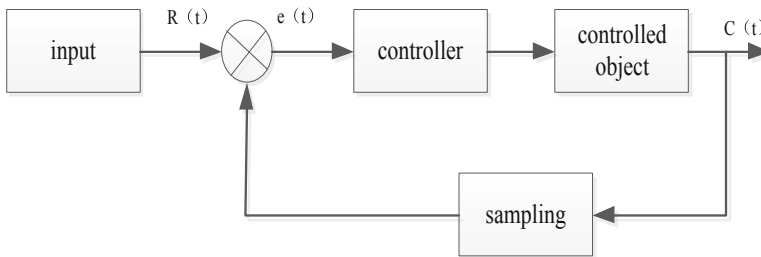

Fig. 1. Typical control system basic structure

Wherein, R(t) is the input set value, C(t) is the actual output value, e(t) is the deviation signal. The control deviation is composed of the input set value and the actual output value, that is, $e(t) = R(t) - c(t)$.

PID control algorithm in the actual application is divided into position PID control algorithm and incremental PID control algorithm. The control theories of the two are the same, but there are differences after digital quantization. This paper uses incremental

digital PID controller. Incremental PID control means that the output of the controller is the increment of the control quantity. The control algorithm formula is as follows.

$$\Delta u(k) = u(k) - u(k-1) \tag{1}$$

$$\Delta u(k) = K_p(e(k) - e(k-1)) + K_i Te(k) + \frac{K_d[e(k) - 2e(k-1) + e(k-2)]}{T} \tag{2}$$

In the above types, T is the sampling period, k is the sampling sequence number, k = 1, 2, ..., e(k − 2) e(k − 2), e(k − 1)e(k − 1) and e(k)e(k) is the system deviation signals obtained at the time of (k − 2) (k − 2), (k − 1)(k − 1) and k respectively.

In this paper, "input quantization" refers to the Angle value given by the upper computer, which is input to the PID controller. After calculation by the PID controller, the output value is converted into analog value by the DA conversion module and input to the controlled object - the piezoelectric fine tracking actuator. The sampling module -AD sampling module converts the analog value to the digital value of the piezoelectric fine tracking actuator. As the input of Pid controller, the digital value and the given value of the Angle are calculated. It obtains the amount of error for PID control.

This paper uses FPGA to realize incremental PID control algorithm. The specific design process is as follows:

1) Read the instruction and state, and read the PID control coefficient;
2) Convert instructions and states to single-precision floating-point numbers;
3) Double axis parallel floating-point subtraction operation, to find the error;
4) Calculate the error increment based on the error in the previous step;
5) Calculate the increment of error increment based on the increment of error in the previous step;
6) Floating-point multiplication of PID coefficient and corresponding error and error increment and Increment of error increment in parallel;
7) Complete the parallel sum of three items in two steps to get the control increment;
8) Sum the control increment and the previous control output to get the new control output. Update the State Correlation Register at the same time.
9) Judge whether the output exceeds the maximum output range to prevent the overshoot of the control output from being too large.
10) Convert the floating-point control output into unsigned 16-bit data, and send it to the output register for DA control program to read. Return 1) proceeds to the next control loop.

2.2 Butterworth Filter Design

The signals collected by AD usually have high-frequency noise, which affects the control accuracy. The maximum operating frequency of the controlled object in the system is 1kHz, so digital filters are required to suppress high-frequency noise. S second-order Butterworth filter is used to filter the high-frequency noise signals collected by AD to ensure the reliability of the system control,. The design process of digital filter is as follows:

1) Determining the cut-off frequency and sampling frequency of filter. The sampling frequency of the filter is 200 kHz, and the cut-off frequency is designed to be 2 kHz.
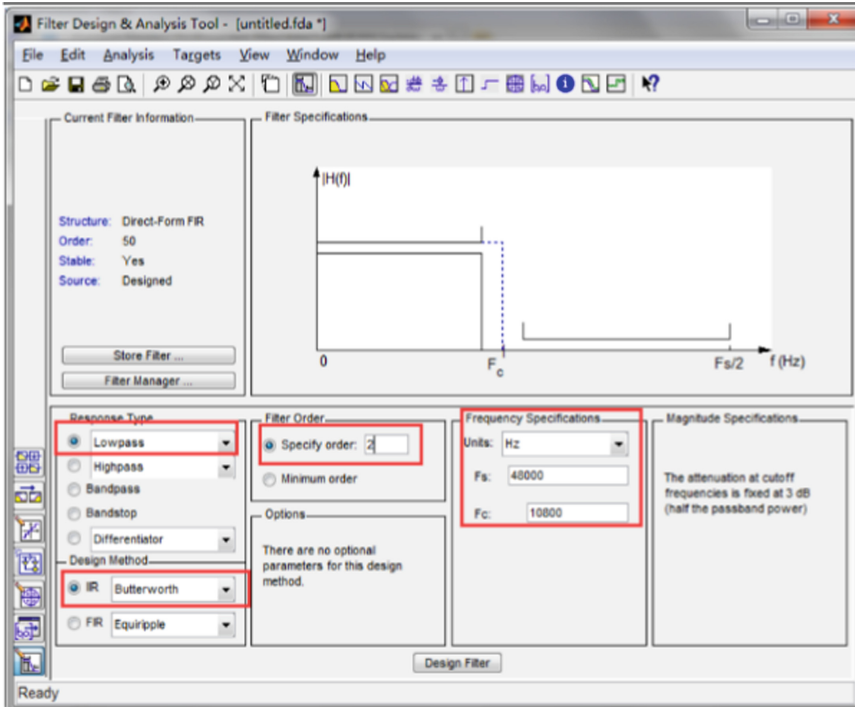2) Obtain the second-order Butterworth filter coefficients through Matlab FDATOOL, as shown in Fig. 2;

Fig. 2. MATLAB tool interface of the filter design

3) To ensure the accuracy of the filter design, the coefficients are expressed by double precision floating-point numbers. Convert the double precision floating-point number to hexadecimal floating-point number;
4) convert the filter coefficients into discrete input the expressions (3) and (4).

$$y1k = n1 * x1k + n2 * x1k\_1 + n3 * x1k\_2 - d2 * y1k\_1 - d3 * y1k\_2 \quad (3)$$

$$y2k = n1 * x2k + n2 * x2k\_1 + n3 * x2k\_2 - d2 * y2k\_1 - d3 * y2k\_2 \quad (4)$$

5) Perform the arithmetic operation of computational polynomial sequentially, calculate the five-term floating-point multiplication at the same time, and complete the calculation of the output value through the summation of three floating-point numbers. The polynomial operation is performed by performing steps 1 and 2 sequentially.

It is important to note that the Xilinx ISE environment cannot perform floating-point arithmetic directly. Therefore, IP Core resources in the Xilinx ISE environment need to be called to perform floating-point arithmetic, as shown in Fig. 3.
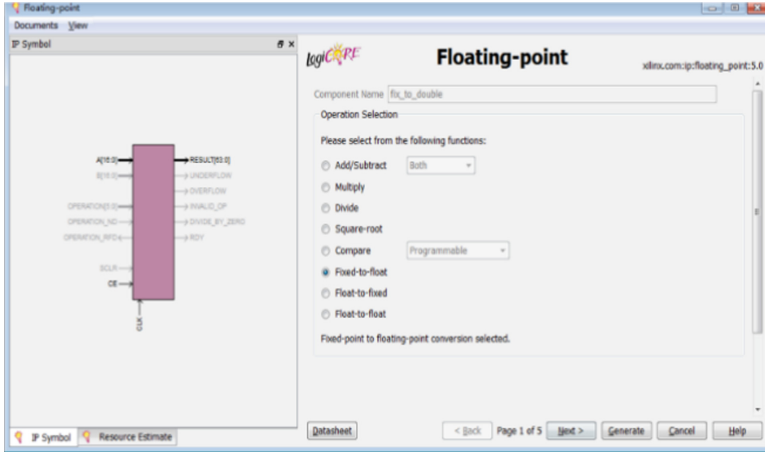

Fig. 3. The interface of XILINX ISE IP Core

The filter is simulated and verified: a step excitation 0×8000 is input to the filter module to check whether the output can converge as expected. The simulation results are shown in Fig. 4 below.
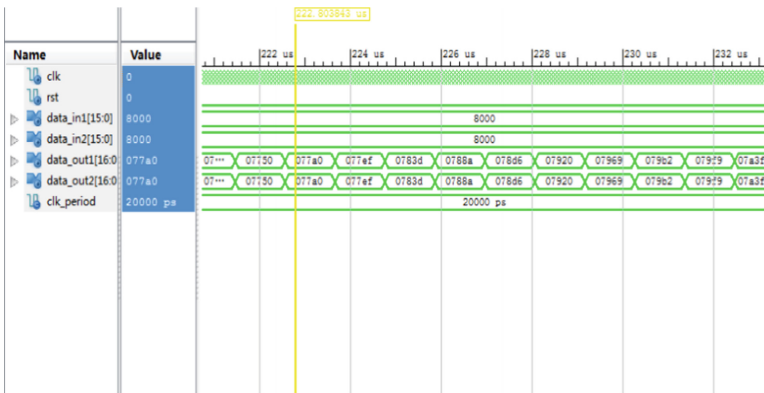

Fig. 4. The results of filter

3   Test Verification and Result Analysis

A piezoelectric deflector driving control board with FPGA is used as the main control board. S-330.2 piezoelectric deflector from PI Company is selected as the controlled

object. The self-developed ground inspection equipment is used as the instruction input and acquisition equipment. The static pointing accuracy, mechanism nonlinearity, sinusoidal dynamic response and system bandwidth of the piezoelectric deflector were tested in the closed-loop operation mode. The test system is shown in Fig. 5 below.
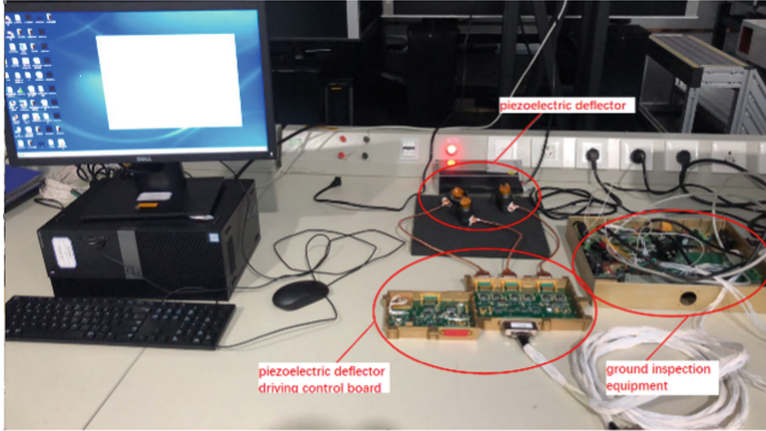

Fig. 5. The experimental system

The digital quantity 32768 was sent by ground inspection equipment, and the software without filter was used for testing. The piezoelectric deflector sensor feedback was collected, as shown in Fig. 6. The software with Butterworth filter was used for testing, and the piezoelectric deflector sensor feedback was collected, as shown in Fig. 7. The ordinate represents the digital quantity of sensor feedback collected by AD.
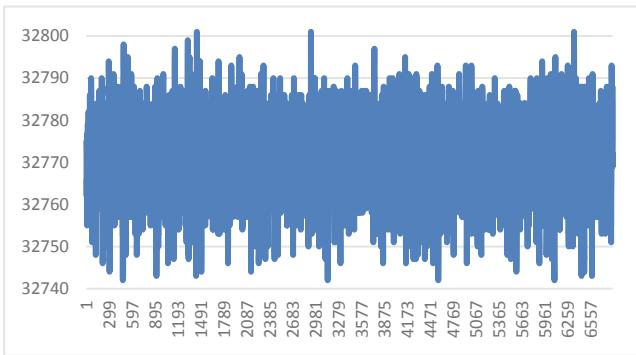

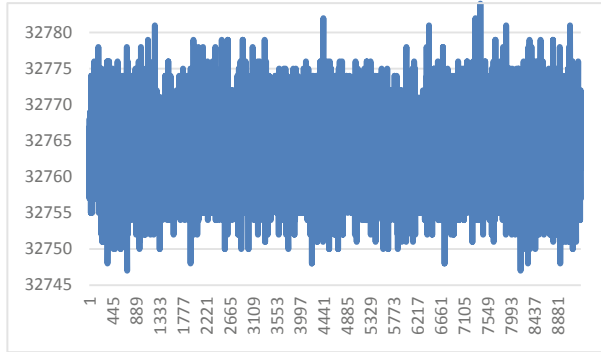**Fig. 6.** The sensor feedback of Piezoelectric without filter

Fig. 7. The sensor feedback of Piezoelectric with Butterworth filter

The ground inspection was used to send 0–65535 instructions to the deflector every 500 digital quantities to collect the piezoelectric deflector sensor feedback, and the nonlinear curve was drawn as shown in Fig. 8. The abscissa innate in the figure represents the sending of instructions (digital quantities), and the ordinate represents the digital quantities collected by the sensor feedback from AD.
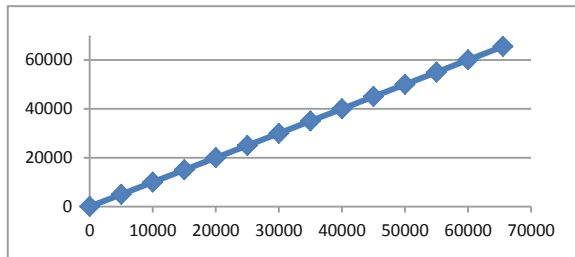

Fig. 8. The nonlinear curve

The 500 Hz sine wave generated by the piezoelectric mechanism is shown in Fig. 9. Where the blue line is the instruction, the red line is the feedback, the abscissa represents the number of points collected, and the ordinate represents the digital quantity of sensor feedback collected by AD.

The system was tested by sweeping frequency of 1–1 kHz. The curve is shown in Fig. 10, where the abscissa represents the instructions sent (digital quantity) and the ordinate represents the digital quantity fed back by the sensor collected by AD. The frequency sweep curve in Fig. 10 is systematically identified, and the result is shown in Fig. 11.

It can be seen from the above test results that the feedback accuracy of piezoelectric deflector sensor collected by the software with Butterworth filter is twice as high as that without the use of filter, indicating that the filter design can effectively reduce the sensor noise of piezoelectric deflector and improve the execution accuracy of the mechanism. It can be seen from Fig. 8 that the PID control algorithm can significantly improve
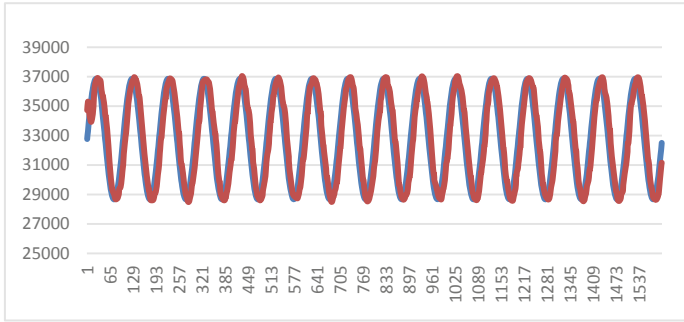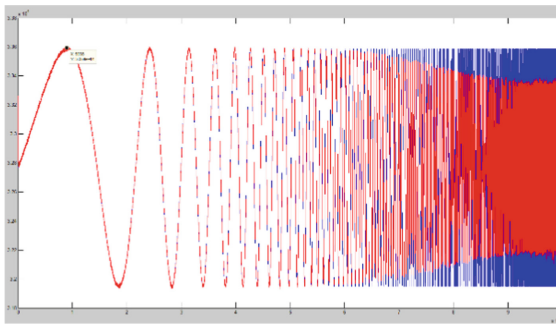
Fig. 9. The curve of dynamic sine wave

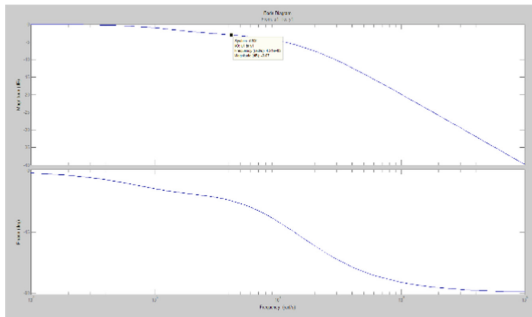**Fig. 10.** The sweep chart

Fig. 11. The frequency response curve of system recognizes

the nonlinear and hysteretic problems of the piezoelectric deflecting mirror. Figure 9, 10 and 11 shows that this filtering closed-loop control algorithm does not affect the dynamic response of the system, and the −3 dB bandwidth of system is 630 Hz, which is consistent with the given value in the manual.

4 Conclusion

This paper provide a filtering closed-loop control algorithm based on FPGA processor, which combines Butterworth filter algorithm with incremental PID control algorithm, and implements the software. The hardware platform is built in the laboratory, and the algorithm is tested and verified. The test results show that, the closed-loop control algorithm effectively solves the problems of hysteresis and nonlinearity of the fine tracking actuator, and the pointing accuracy is improved from 6urad to 3urad, which meets the high precision requirements of laser communication system for the fine tracking actuator.

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