Improved Non-isolated DC-DC Boost Converter with High Gain Capability for Renewable Energy Microgrids

Sunkara Udaykiran, V. Bharath Kumar, and Y. V. Pavan Kumar

1 Introduction

Due to the emergence of the industrial revolution and rapid population growth, the ease of energy consumption was increased to a greater extent. So there is a need to increase the production of energy by using renewable energy sources such as solar panels, fuel cells etc. But the magnitude of output voltage that is obtained from these solar panels is considerably less, which is not required to produce sufficient energy from microgrids. Here comes the importance of high gain DC-DC boost converters. These high gain converters will boost the magnitude of voltage to desired levels to produce a sufficient amount of energy.

1.1 Problem Statement

The conventional boost converter configuration as shown in Fig. 1 is able to scale up the voltage level 2 times more than that of the input voltage. It comprises a MOSFET, diode, inductor and capacitor. The MOSFET will act like a switch that requires controlled gating pulses for its operation.

The working of the conventional boost converter is as follows,

S. Udaykiran · V. Bharath Kumar · Y. V. Pavan Kumar (✉)
School of Electronics Engineering, VIT-AP University, Amaravati 522237, Andhra Pradesh, India
e-mail: pavankumar.yv@vitap.ac.in

S. Udaykiran
e-mail: sunkara.udaykiran@vitap.ac.in

V. Bharath Kumar
e-mail: bharath.18bec7093@vitap.ac.in

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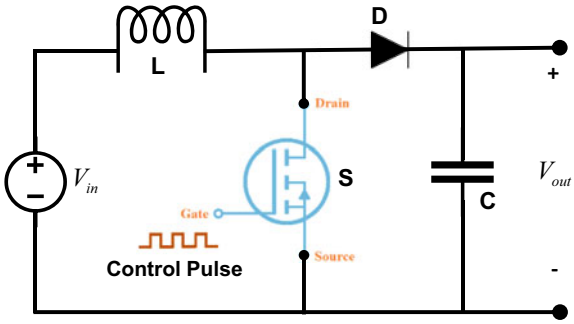

Fig. 1 Basic DC-DC boost converter circuit

– When the switch is on, the inductor gets charged up with the help of supply voltage. Here the voltage across the inductor (V_L) and supply voltage (V_{in}) will be the same as they are in parallel.
– When the switch is off, the current flow path will flow through the inductor, diode and capacitor. So according to basic network rules, the voltage measured across the inductor is shown by Eq. 1.

$$V_C = V_{out} = V_{in} + V_L \tag{1}$$

As the voltage across the inductor (V_L) and supplied voltage (V_{in}) are equal, Eq. 1 can also be represented as shown in Eq. 2.

$$V_{out} = V_{in} + V_{in} = 2V_{in} \tag{2}$$

So as per the input–output relation, the conventional boost converter can scale up 2 times that of the input voltage. The gain of the traditional boost converter is only 2, which is not suitable for renewable energy applications.

1.2 Literature Survey

Several kinds of high gain boost converter topologies already existed in literature [1]. But, there are a few drawbacks associated with them like a higher number of components, high switching frequency and voltage gain for the existed topologies in the literature.

The topology that is demonstrated in [2] has less no of components, but it has a high switching frequency of 40 kHz. It requires a high amount of cost for the topologies having a higher switching frequency. A topology that was shown in [3] has the disadvantage of having a greater number of components and a high switching frequency used in its configuration. Besides, it has a greater advantage of producing

a higher voltage magnitude of around 20 times that of input voltage. A topology which is described in [4] has a greater benefit because of having a higher gain of 25, But it also shows its disadvantages of having a high switching frequency of 118 kHz and more components used. The topology which is demonstrated in [5] has the advantage of having a gain of 20 in producing voltage levels. Despite having a higher gain, this topology requires more no of components and a higher switching frequency of 46 kHz for its operation. There exists one topology as depicted in [6] that is not suitable for renewable energy applications, as it takes a greater no of components of about 22 and a higher switching frequency of 100 kHz.

A topology which was shown in [7] will have a weak point of having less gain value of only 2 and a higher switching frequency of 100, Besides, it shows its advantage in having less no of components. The topology which is shown in [8] has the advantage of having less no of components used for its construction and less switching frequency of about 10 kHz. Besides, it can only produce output voltage levels of 2 times more than the input voltage. The topology which is described in [9] can produce an output voltage magnitude which is 30 times more than the input voltage. Although it is having a minimal number of components needed to build switching frequency. A topology which is shown in [10] was chosen as the worst topology because of having a number of components required of almost 33, But it requires less amount switching frequency of 10 kHz. The topology which was demonstrated in [11] has a higher amount of switching frequency of about 200 kHz, which is not advisable for any application. This topology is having a considerable gain value of 10. The topology shown in [12] has the disadvantage of having more number of components and a considerable voltage gain value of 10. The topology shown in [13] has the disadvantage of having less gain of about 9 and more no of components required for its construction.

1.3 Paper Contribution and Organization

The topologies which are having less number of component count have more switching frequency. Subsequently, the topologies which are having more gain value require more no of components to build. So there is a tradeoff between the number of components, gain values and switching frequency. The objective of the proposed work is to develop one unique boost converter topology, which produces a high gain compared with conventional topologies. Further, the proposed topology is best suitable for renewable energy applications. Additionally, the proposed topology was compared with some considerable conventional topologies in terms of total no of components, voltage gain and performance indices.

2 Description of the Proposed Topology

The proposed topology had designed and simulated in Simulink as shown in Fig. 2. The proposed topology consists of five energy storing elements, i.e., two inductors and three capacitors, it also consists of one MOSFET and one resistor used for switching and load purposes respectively. The specifications of the circuit are, the input voltage $V_{in} = 10$ V; switching frequency $f_s = 10$ kHz; the values of passive elements are tabulated below in Table 1.

By simulating the circuit, it is observed that the output voltage $V_{out} = 181.8$ V, from that it is determined that the gain of the circuit is 18.19 which means the output is approximately 18 times that of the input value.

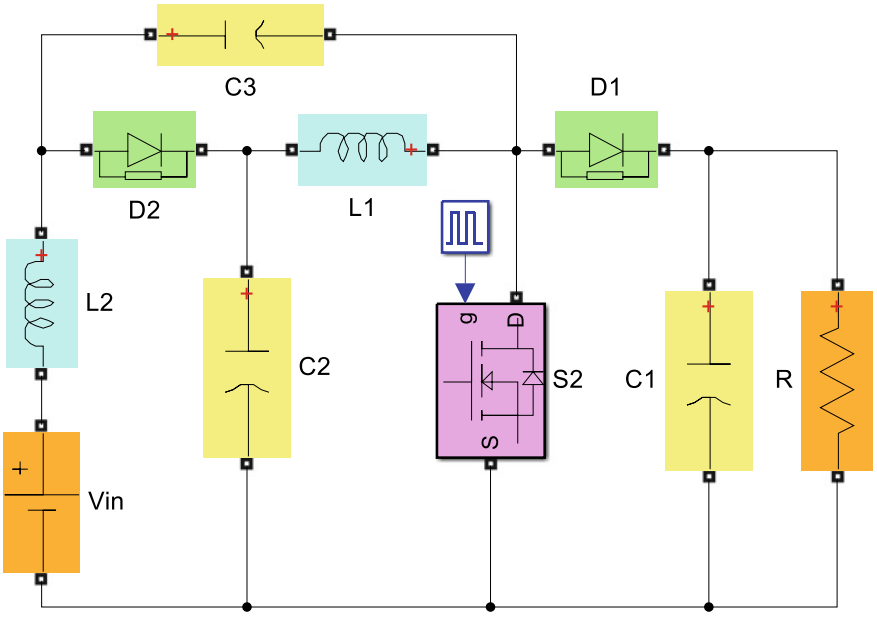

Fig. 2 Proposed DC-DC boost converter circuit

Table 1 Component specifications

Specification	Conventional topologies		Proposed topology
	Topology-1 [12]	Topology-2 [13]	
Resistance (Ω)	58	1000	58
Capacitance (μF)	$C_0, C_1, C_2 = 25$	$C_1, C_2, C_3, C_4, C_5 = 25$	$C_1, C_2, C_3 = 25$
Inductance (mH)	$L_1 = 0.5, L_2 = 0.1$	$L_1 = 1.2$	$L_1 = 0.2$, L2 $= 0.2$

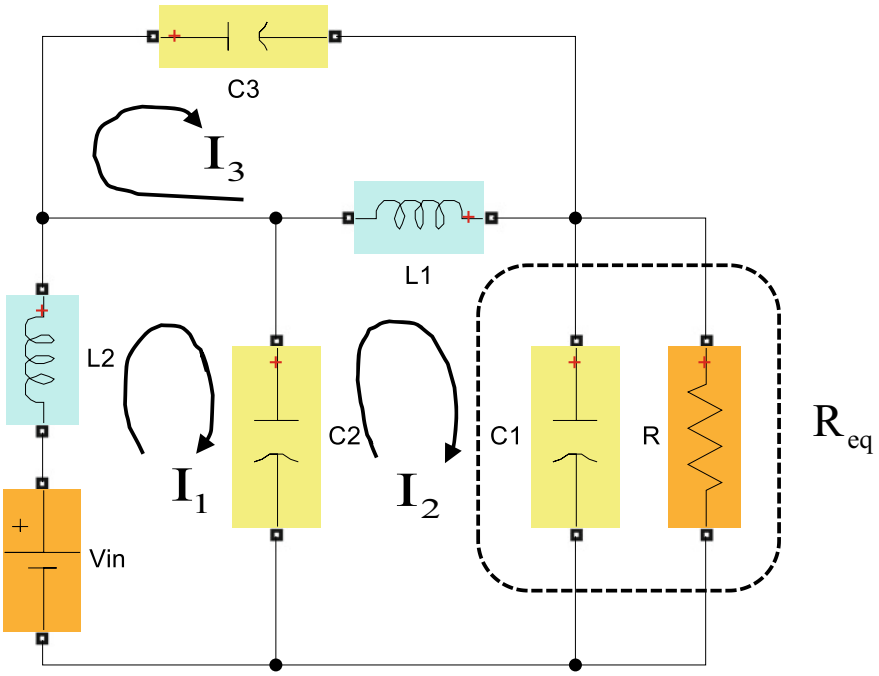

Fig. 3 Simplified circuit of the proposed topology when the switch is in the ON state

The output equation of the proposed topology has been derived by linearizing the circuit. When the switch is turned on, the equivalent circuit is shown in Fig. 3. Applying Kirchhoff's voltage law for the 3 loops, we get,

The KVL equation for loop 1 is given by Eq. 3.

$$V_{in} = I_1 L_2 s + \frac{1}{C_2 s}(I_1 - I_2) \tag{3}$$

The KVL equation for loop 2 is given by Eq. 4.

$$\frac{1}{C_2 s}(I_2 - I_1) + L_1 s(I_2 - I_3) + I_2 R_{eq} = 0 \tag{4}$$

The KVL equation for loop 3 is given by Eq. 5.

$$\frac{1}{C_3 s} I_3 + L_1 s(I_3 - I_2) = 0 \tag{5}$$

By rearranging Eqs. (3)–(5) with respect to current I_1, I_2, I_3 the following equations are obtained as shown in Eqs. 6–8.

$$V_{in} = \left(L_2 s + \frac{1}{C_2 s}\right) I_1 - \left(\frac{1}{C_2 s}\right) I_2 \tag{6}$$

$$-\left(\frac{1}{C_2 s}\right) I_1 + \left(\frac{1}{C_2 s} + L_1 s + R_{eq}\right) I_2 - (L_1 s) I_3 = 0 \tag{7}$$

$$-(L_1 s) I_2 + \left(\frac{1}{C_3 s} + L_1 s\right) I_3 = 0 \tag{8}$$

The matrix representation of Eqs. (6)–(8) is shown in Eq. 9.

$$V_{in} = \begin{bmatrix} \left(L_2 s + \frac{1}{C_2 s}\right) & -\frac{1}{C_2 s} & 0 \\ -\frac{1}{C_2 s} & \frac{1}{C_2 s} + L_1 s + R_{eq} & -L_1 s \\ 0 & -L_1 s & \frac{1}{C_3 s} + L_1 s \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{9}$$

The resultant product $I_2 \times R_{eq}$ will give the output equation of the proposed topology. Here I_2 can be found by using the crammers rule as mentioned in Eq. 10.

$$I_2 = \frac{\Delta_2}{\Delta} \tag{10}$$

Here Δ represents the determinant of the matrix. As per the crammers rule, the value Δ_2 can be found as Eq. 11. Similarly, Δ can be found as Eq. 12.

$$\left.\begin{aligned} \Delta_2 &= \begin{vmatrix} \left(L_2 s + \frac{1}{C_2 s}\right) & V_{in} & 0 \\ -\frac{1}{C_2 s} & 0 & -L_1 s \\ 0 & 0 & \frac{1}{C_3 s} + L_1 s \end{vmatrix} \\ \Rightarrow \Delta_2 &= V_{in}\left[-\frac{1}{C_2 C_3 s^2} \quad \frac{-L_1 s}{C_2 s}\right] = V_{in}\frac{[-1 - L_1 C_3]s}{C_2 C_3 s^2} \end{aligned}\right\} \tag{11}$$

$$\left.\begin{aligned} \Delta &= \begin{vmatrix} L_2 s + \frac{1}{C_2 s} & -\frac{1}{C_2 s} & 0 \\ -\frac{1}{C_2 s} & \frac{1}{C_2 s} + L_1 s + R_{eq} & -L_1 s \\ 0 & -L_1 s & \frac{1}{C_3 s} + L_1 s \end{vmatrix} \\ \Rightarrow \Delta &= \frac{(R_{eq} L_1 L_2 C_2 C_3)s^4 + [L_1 L_2 (C_2 + C_3)]s^3 + (L_2 C_2 + L_1 C_3) R_{eq} s^2 + (L_1 + L_2)s + R_{eq}}{C_2 C_3 s^2} \end{aligned}\right\} \tag{12}$$

So, I_2 can be found by dividing Δ_2 and Δ. The resultant I_2 is as Eq. 13.

$$I_2 = \frac{V_{in}(-s[1 + L_1 C_3])}{(R_{eq} L_1 L_2 C_2 C_3)s^4 + [L_1 L_2 (C_2 + C_3)]s^3 + (L_2 C_2 + L_1 C_3) R_{eq} s^2 + (L_1 + L_2)s + R_{eq}} \tag{13}$$

Thus, the final output voltage equation of the proposed topology is given as Eq. 14.

$$V_{out} = \frac{V_{in}(-s[1 + L_1C_3])R_{eq}}{(R_{eq}L_1L_2C_2C_3)s^4 + [L_1L_2(C_2 + C_3)]s^3 + (L_2C_2 + L_1C_3)R_{eq}s^2 + (L_1 + L_2)s + R_{eq}} \tag{14}$$

Table 1 comprises values of the passive components of conventional topologies and proposed topology. Here for the comparison purpose, all the capacitor ratings are taken the same. Inductor ratings of the proposed topology are less compared to ratings of conventional topologies. All three ratings of the proposed topology don't exceed the ratings of conventional topologies. The design equations for the calculation of inductance and capacitance are given in Eqs. 15 and 16.

$$L = \frac{D(1 - D)R}{2f} \tag{15}$$

$$C = \frac{D}{2fR} \tag{16}$$

3 Simulation Results and Discussion

From Fig. 4, it is found that the settling time is 30 ms and the output voltage is 181.9 V. In the zoom-in graph, it is observed that the change of voltage is slow because of capacitors. It is known that the capacitor doesn't allow the sudden change in voltage because that saw tooth graph had occurred in the output graph. The voltage of the saw-tooth is fluctuating between 168.7 and 181.8 V. Here maximum voltage is considered as the output of the circuit.

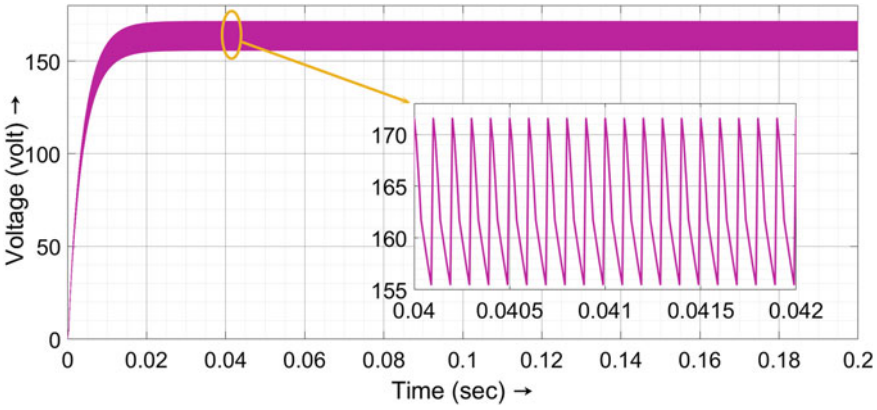

Fig. 4 Output of the proposed topology

3.1 Conventional Versus Proposed Topology Analysis

The simulation models of conventional topologies are shown in Figs. 5 and 6. From Table 2, it is found that the total number of components of the proposed topology is less than conventional topologies. Here, the majority number of switches is one and the number of diodes is very less compared to conventional topologies which leads to a decrease in the cost of the circuit.

Tables 2 and 3 comprise the input voltage (V_{in}), output voltage (V_{out}), number of components, duty cycle, switching frequency, and the gain of circuits. Here proposed topology is compared with conventional topologies. The input voltage, switching frequency, and duty cycle are considered the same for all three topologies so that comparison will be good. It is observed that gain is high for the proposed topology compared to the other two topologies, and almost the sum of gains of two conventional topologies is equal to the proposed topology's gain.

From Table 4, it is summarized that conventional topology—2 has peak-overshoot at 104 V. So, it is not preferred. There is no peak-overshoot in the output response of conventional topology-1 as shown in Fig. 7 and the proposed topology. Settling

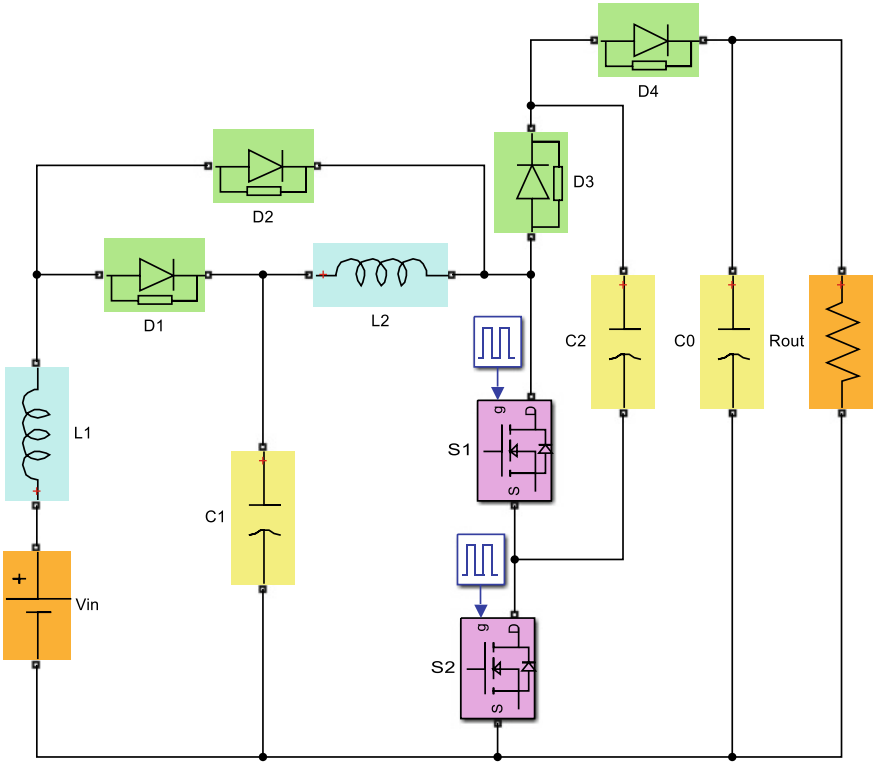

Fig. 5 Conventional topology-1 [12]

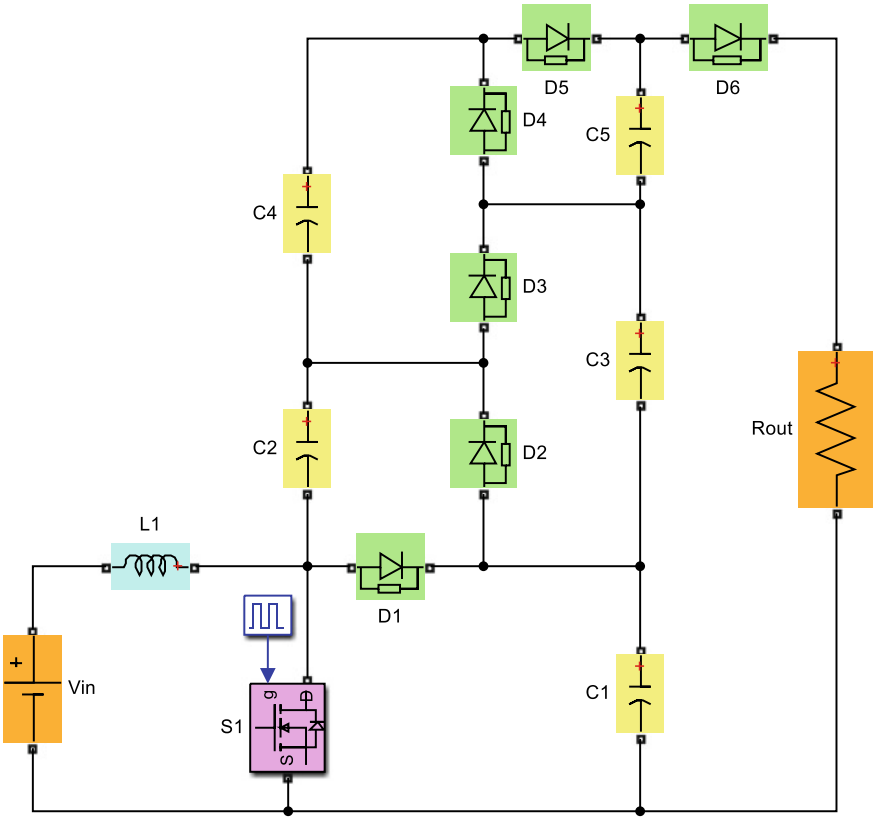

Fig. 6 Conventional topology-2 [13]

Table 2 Comparison of number of components used in conventional and proposed topologies

Topology	Number of sources	Number of switches	Number of capacitors	Number of inductors	Number of diodes	Total
Conventional topology-1 [12]	3	2	3	2	4	14
Conventional topology-2 [13]	2	1	5	1	6	15
Proposed topology	2	1	3	2	2	10

Table 3 Analysis of output responses of conventional and proposed topologies

Topology	V_{in} (V)	V_{out} (V)	Switching frequency (kHz)	Duty cycle	Gain
Conventional topology-1 [12]	10	105.3	10	0.6	10.53
Conventional topology-2 [13]	10	70.02	10	0.6	7
Proposed topology	10	181.8	10	0.6	18.18

time is less for proposed topology, so it is good compared to conventional topologies. Delay time and rise time are high for the proposed topology and low for conventional topology-2 as shown in Fig. 8. The comparative response of conventional, as well as proposed topologies, is given in Fig. 9 for better visualization.

Table 4 Analysis of the transient performance of conventional and proposed topologies

Topology	Delay time (ms)	Rise time (ms)	Peak overshoot (%)	Peak-time (ms)	Settling time (ms)
Conventional topology-1 [12]	1.46	6.89	0	0	25
Conventional topology-2 [13]	5.03	2.01	48.8	3.5	40
Proposed topology	3.02	8.61	0	0	30

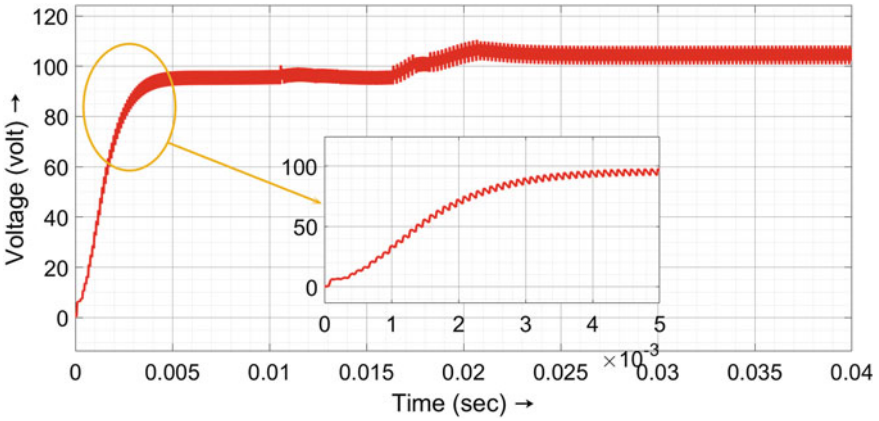

Fig. 7 Output of conventional topology-1

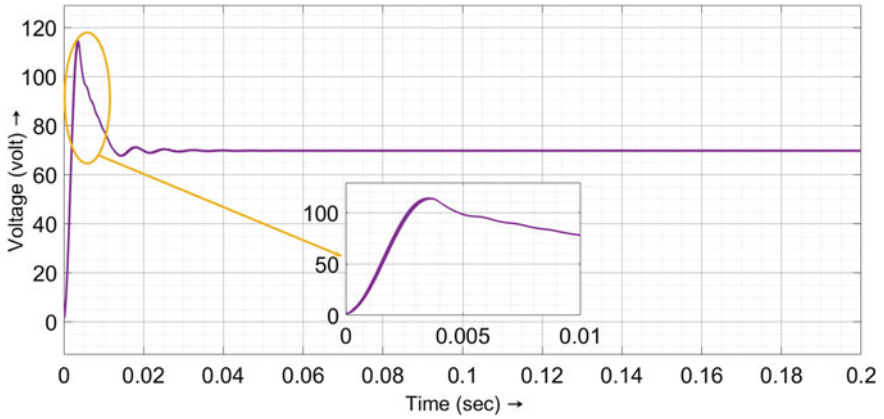

Fig. 8 Output of conventional topology-2

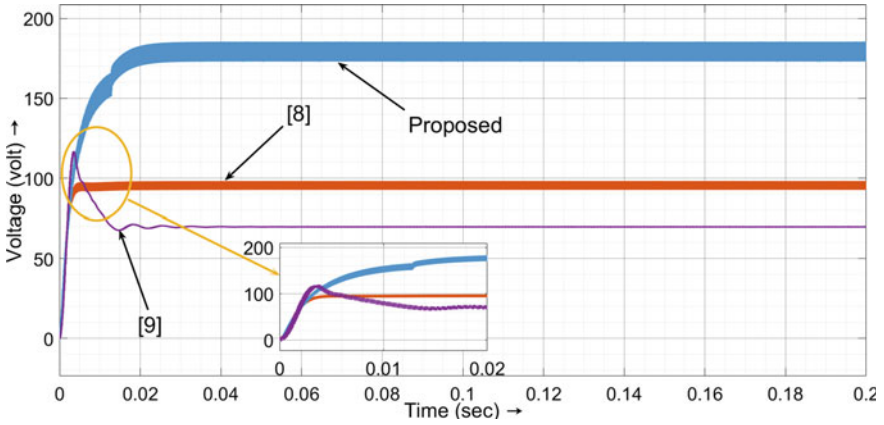

Fig. 9 Comparison of responses produced by conventional and proposed topologies

4 Conclusion

Thus, this paper considers the following factors to look at the best circuit, those are gain, number of components, switching frequency, duty cycle, and number of sources. For the desired circuit following criteria should be followed, the gain should be high, the number of components should be less, and switching frequency should be less. From the summary of Tables 2, 3 and 4, it is observed that the proposed topology satisfies the maximum criteria that are given as follows.

– High gain
– Less number of components
– Less switching frequency

– Less settling time
– No peak-overshoot
– Low cost.

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References

1. S. Uday Kiran, P. Manoj Kumar, Y.V. Pavan Kumar, Comprehensive analysis on critical factors for the operation of advanced high gain DC-DC converters used in renewable energy applications. Int. J. Renew. Energy Res. **11**(3), 1449–1459 (2021)
2. A.S. Ansari, J.S. Moghani, A novel high voltage gain non coupled inductor SEPIC converter. IEEE Trans. Industr. Electron. **66**(9), 7099–7108 (2019)
3. Y. Qin, Y. Yang, S. Li, Y. Huang, S.C. Tan, S.Y. Hui, A high efficiency DC/DC converter for high-voltage-gain, high-current application. IEEE J. Emerg. Sel. Top. Power Electron. **8**(3), 2812–2823 (2020)
4. M.L. Alghaythi, R.M.O. Connell, N.E. Islam, M.M.S. Khan, J.M. Guerrero, A high step-up interleaved DC-DC converter with voltage multiplier and coupled inductors for renewable energy system. IEEE Access **8**, 123165–123174 (2020)
5. V. Marzang, S.H. Hosseini, N. Rostami, P. Alavi, P. Mohseni, S.M. Hashemzadeh, A high step-up nonisolated DC-DC converter with flexible voltage gain. IEEE Trans. Power Electron. **35**(10), 10489–10500 (2020)
6. P. Mohseni, S.H. Hosseini, M. Maalandish, A new soft switching dc-dc converter with high voltage gain capability. IEEE Trans. Industr. Electron. **67**(9), 7386–7398 (2020)
7. A. Ponniran, A.A. Bakar, M.U. Wahyu, M.S. Kamarudin, M.A. Chulan, K. Kamit, M.H. Sahabudin, Y. Yunus, F.A. Khalid, M.A. Hamzah, Volume reduction consideration in multilevel DC-DC boost converter, in *4th IET Clean Energy and Technology Conference*, Kuala Lumpur, Malaysia (2016)
8. A.N. Natsheh, J.G. Kettleborough, J.M. Nazzal, Analysis, simulation and experimental study of chaotic behaviour in parallel connected dc-dc boost converters. Chaos Solitons Fractals **39**(5), 2465–2476 (2009)
9. Z. Saadatizadeh, P.C. Heris, M. Sabahi, E. Babaei, A DC–DC transformerless high voltage gain converter with low voltage stresses on switches and diodes. IEEE Trans. Power Electron. **34**(11), 10600–10609 (2019)
10. E. Babaei, H.M. Maheri, M. Sabahi, S.H. Hosseini, Extendable nonisolated high gain dc-dc converter based on active–passive inductor cells. IEEE Trans. Industr. Electron. **65**(12), 9478–9487 (2018)
11. A.J. Sabzali, E.H. Ismail, H.M. Behbehani, High voltage stepup integrated double boost-sepic dc-dc converter for fuel-cell and photovoltaic applications. Renew. Energy **82**, 44–53 (2014)
12. V. Marne, K. Vadirajacharya, *Performance Verification of DC–DC Boost Converter. Computing, Communication and Signal Processing, Advances in Intelligent Systems and Computing,* vol. 810 (Springer Nature Singapore, 2019), pp. 661–667
13. H.T. Priya, A.M. Parimi, U.M. Rao, Performance evaluation of high voltage gain boost converters for DC grid integration, in *IEEE, International Conference on Circuit, Power and Computing Technologies [ICCPCT]*, Nagercoil, India (2016)