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Shailendra Kumar
Bhim Singh
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Recent Advances in Power Electronics and Drives

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A New 51-Level Asymmetrical Inverter Circuit with Reduced Number of Components

V. Thiyagarajan

1 Introduction

The concept of Multilevel inverters (MLIs) technology has been quickly evolving in the field of power electronics recently, with a lot of scope for growth. MLIs are extremely trustworthy, high-quality power converters which help to interconnect the DC system with an AC system. MLIs offer the capacity to handle the growing demand for higher power ratings while also improving power quality and lowering harmonic distortion [1, 2]. MLIs are best suited for high-voltage and high-power conversion systems because they can provide a high-quality stepped AC voltage waveform from various connections of power semiconductor switches (PSSs) and single/multiple DC voltage sources (DCVSs) while operating at a low switching frequency [3]. MLIs not only achieve large power ratings, but they also allow renewable energy sources to be used. Photovoltaic, wind and fuel cell can all be used as sources and easily integrated into an MLI system for a high-power application. Because of their high-voltage operation capability, low switching losses, great efficiency, low dV/dt stress and low electromagnetic interference, MLIs are gaining more and more popularity [4]. Flying capacitor MLIs, diode-clamped MLIs and cascaded H-bridge (CHB) MLIs are the three classic types of MLIs. However, all of these classic topologies have drawbacks that make them inappropriate for industrial drive applications, such as a higher number of PSSs, DCVSs, balancing diodes and balancing capacitors [5, 6]. Based on the level of DCVSs, MLIs are further divided into the symmetric multilevel inverter (SMLI) and asymmetric multilevel inverter (ASMLI). AMLIs, on the other

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hand, have DCVSs of varying magnitude, whereas SMLIs have equal magnitude DCVSs [7, 8]. As a result of the reduction in the number of bridges utilized in the ASMLI structure, a significant reduction in size and a simpler control system can be noted as important outcomes. However, delivering different DCVSs might be quite expensive, making the MLI topologies difficult to implement [9, 10].

In recent years, many researchers are striving to build an effective and more efficient structure of MLIs that contain a lesser number of circuit components and larger output voltage levels, enhancing their efficiency, reliability and, eventually, reducing the size and cost of the output filter [11, 12]. Topological improvements, use of asymmetrical isolated DCVSs and a combination of both topological improvements and use of asymmetrical DCVSs are the most common techniques to minimize component count. Gautam et al. [1] proposes an inverter structure made up of cascading basic units without an H-bridge circuit. The enormous number of bidirectional PSSs in this inverter circuit increases its conduction losses. As a result, the MLI structure is less efficient and unsuitable for high-voltage applications. Furthermore, in comparison to traditional topologies, this MLI structure has a limited amount of redundant switching states, therefore basic units under fault conditions cannot be bypassed. Jayabalan et al. [2] proposes a new multilevel inverter structure with multiple bidirectional PSSs in each basic unit. Although the total switching component count in this MLI is lower than in traditional MLI structures, the voltage stress across the PSSs and power losses are higher than in a few recently developed MLI structures due to the usage of multiple bidirectional PSSs. The cost of this inverter circuit rises as the number of DCVSs grows. Another asymmetrical MLI suggested in the literature [3] has four DCVSs and nine PSSs as its basic unit. A cascaded connection of the necessary number of basic units must be formed to generate a very large number of voltage steps at the output. The modularization is lost in the asymmetric mode due to unequal DCVSs, but the suggested MLI structure can still be extended with a proportionate factor. The polarity generation switch, which operates at the fundamental switching frequency, is subjected to additional voltage stress than the level generation switch. The use of the H-bridge in modular MLI has been presented in [4], however, it yields fewer levels with a higher input source count. Also, the quantity of IGBTs in this arrangement is very high and their cost is considerable because of the wide variety of DC sources. The suggested inverter structure in [5] can provide more steps at the output by adding a large number of DCVSs and switching devices. Furthermore, H-bridge PSSs must have a greater voltage rating. In [6] is presented a new 51-level inverter topology for high-voltage and high-efficiency applications. The switching loss was attempted to be reduced by minimizing the number of PSSs required. The suggested control method is easily adaptable to high-power and high-voltage MLIs. A new ASMLI structure is designed in [7] to reduce the cost, voltage stress on PSSs and switching losses. The presented MLI aims to minimize the DC sources and PSSs

which reduce both implementation costs and total standing voltage (TSV). It presents a new module for cascade MLIs that eliminates the need for a negative voltage level generator circuit. Using four unequal DCVSs and 10 PSSs, each module can generate 25 distinct voltage levels. This paper aims to present a new 51-level ASMLI structure with five DCVSs and 12 PSSs. The organization of this paper is as follows: Sect. 2 presents the suggested 51-level inverter topology. Section 3 presents the comparison study. Simulation results are presented in Sect. 4 and the conclusion is given in Sect. 5.

2 Suggested 51-Level MLI Circuit

The suggested 51-level inverter structure with asymmetric DCVSs is shown in Fig. 1. The suggested inverter consists of two parts: a basic unit and Tri-Level Circuit (TLC). The basic unit of the suggested MLI consists of four DCVSs and eight PSSs. The TLC unit consists of a single DCVS and four PSSs. The basic unit is connected in series with the TLC. Here, the full-bridge inverter with four PSSs and one DC input source acts as a TLC which creates three output steps, $-V_x$, 0 and V_x, respectively. The main objective of TLC is to increase the output voltage step while simultaneously reducing the required number of PSSs and their voltage rating. Some of the sample positive and negative output levels obtained for the suggested inverter circuit are shown in Fig. 2. In order to prevent short circuit of DCVSs, the following switching combinations should not be turned ON simultaneously: (T_1, T_4), (T_2, T_3), (S_1, S_2), (S_1, S_3), (S_6, S_8), (S_7, S_8). The maximum number of PSSs turned ON to create any output level is equal to five PSSs which is a very less number as compared with other topologies. To obtain the 51-level output voltage, i.e., 25 positive levels, 25 negative levels and a zero level, the magnitudes of the DCVSs are chosen in the ratio as $V_x : V_1 : V_2 : V_3 : V_4 = 1 : 3 : 3 : 9 : 9$. The maximum amplitude of the obtained output voltage is given by $V_{o,\max} = V_x + V_1 + V_2 + V_3 + V_4 = 25V_{dc}$.

3 Comparison Study

In this section, different asymmetric type 51-level inverter topologies are compared based on the required number of switching devices, DCVSs, ON-state PSSs and total standing voltage (TSV) value of the PSSs. The comparative results of the suggested inverter circuit with other latest inverter circuits are presented in Table 1. The inverter

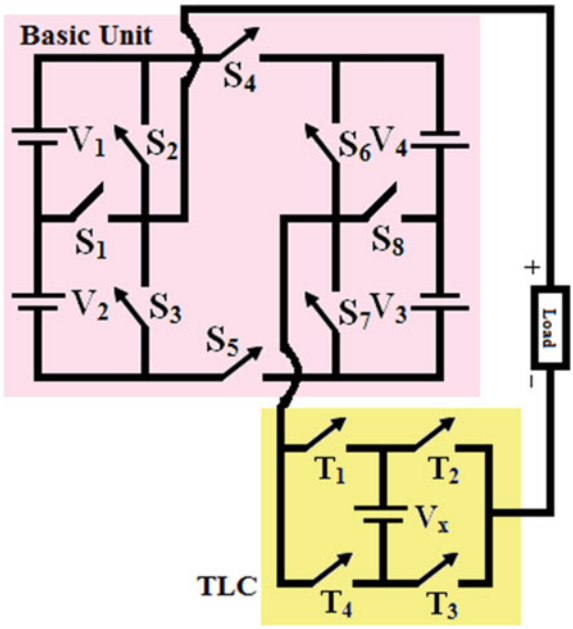


Fig. 1 Suggested inverter topology

circuit presented in [1–7] has inbuilt capability to obtain the negative output voltage steps without using a half-bridge unit. The topologies presented in [1, 2] and [3] require 14, 13 and 12 DCVSs respectively to create 51-output levels. In addition, the required number of switching devices and TSV value are also very high for these inverter circuits as compared with the presented 51-level inverter circuit. The TSV value is $162V_{dc}$ for the inverter circuit presented in [1]. The TSV value for the suggested inverter is $112V_{dc}$, which is also lesser than other topologies presented in the literature. It is noteworthy that the cost of the MLI topologies increases with the increase in the number of circuit components and increase in the TSV value. In this regard, the cost and size of the suggested 51-level inverter circuit is very less as compared with the other presented topologies.

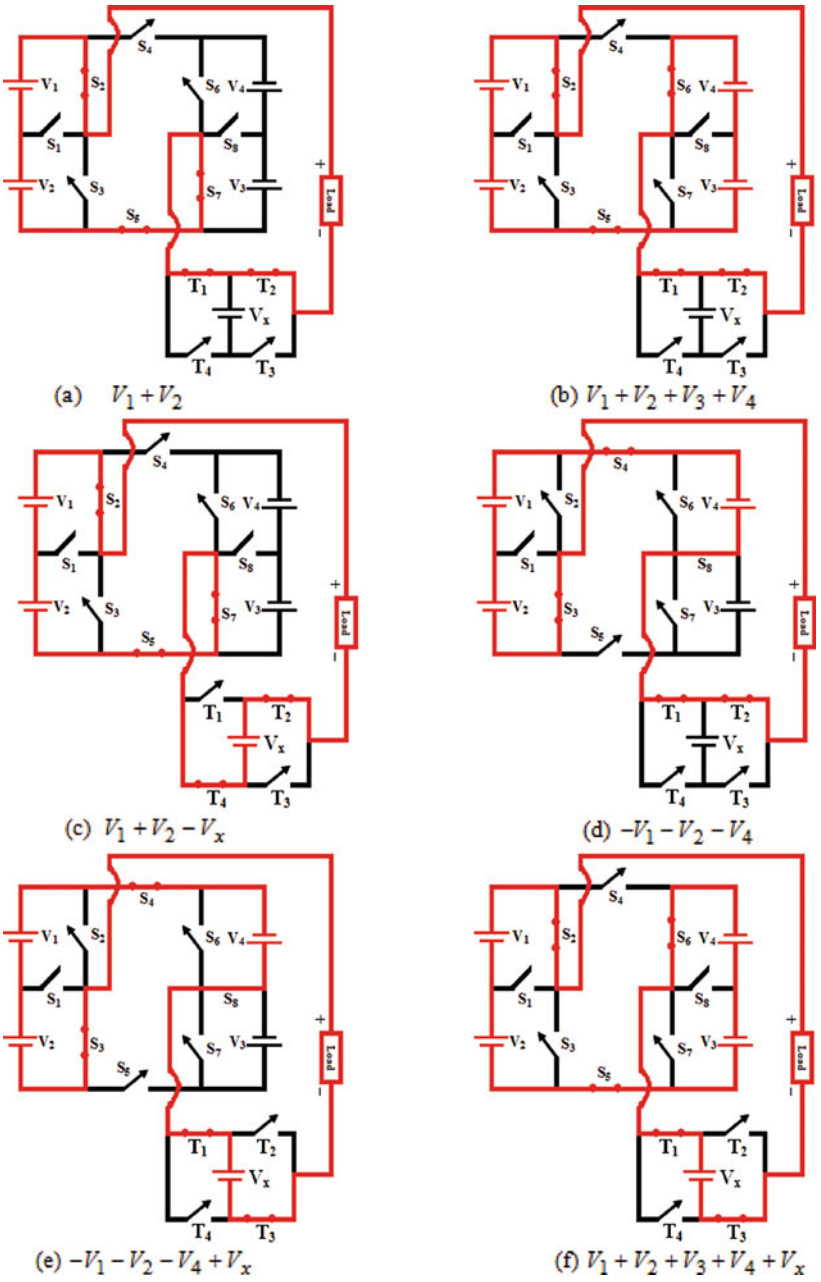


Fig. 2 Various output voltage levels

Table 1 Comparative analysis

Topology	Negative level	No. of sources	No. of switches	ON-state switches	TSV
[1]	Inherent	14	18	6	$162V_{dc}$
[2]	Inherent	13	32	8	$175V_{dc}$
[3]	Inherent	12	38	10	$125\ V_{dc}$
[5]	Inherent	6	14	8	$125V_{dc}$
[6]	Inherent	6	12	5	$112V_{dc}$
[7]	Inherent	5	12	6	$114V_{dc}$
Proposed	Inherent	5	12	5	$112V_{dc}$

The switching losses of the inverter circuit depend on the number of conducting PSSs required to create the desired output levels. The inverter circuit presented in [3] requires 10 conducting PSSs, and eight conducting PSSs are required for the MLI structure presented in [2, 5]. In this regard, the suggested 51-level inverter circuit has good efficiency with minimum switching losses as it requires only five conducting PSSs to create the desired output voltage levels.

4 Simulation Results

The simulation analysis of the suggested asymmetrical 51-level inverter circuit is carried out using MATLAB Simulink software. The DC voltage magnitude is selected as $V_x = 5\,\text{V}$; $V_1 = V_2 = 15\,\text{V}$ and $V_3 = V_4 = 45\,\text{V}$ and hence the maximum voltage magnitude obtained is 125 V. Most of the control approaches discussed in the literature [1–8] have set their primary goal as the reduction of overall loss and improvement of harmonic profile. Among the two basic types of control methods, the fundamental frequency switching method can outperform than high-frequency switching methods. In this paper, a simple PWM technique is used in which the reference sine waveform is compared with the constant magnitude carrier signals to generate the required switching pulses. The amplitude of the carrier signals is obtained using the formula:

$$V_{Ck} = V_m\left(\frac{k-0.5}{\frac{N_L-1}{2}}\right) \text{ where, } k = 1, 2, 3..., N_L \tag{1}$$

where N_L is the number of voltage steps and V_m is the magnitude of the reference sinusoidal signal.

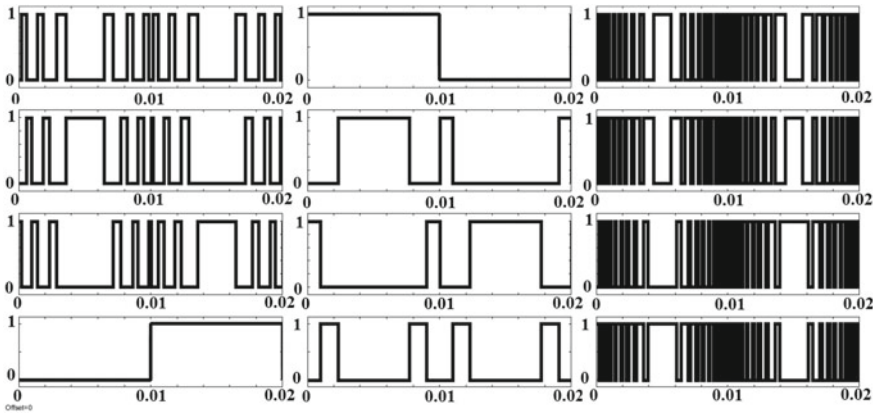


Fig. 3 Switching pulses

Figure 3 shows the switching pulses generated for the suggested 51-level asymmetrical inverter circuit. It is noted that switch S_4 is conducted during the negative cycle only and switch S_5 is conducted during the positive cycle only. Figure 4 shows the voltage stress across each PSSs of the suggested 51-level inverter circuit. The voltage stress across switch S_1 is 15 and is 30 V for the PSSs S_2 and S_3. The maximum voltage stress of 120 V is obtained across the PSSs S_4 and S_5, respectively. The voltage stress across the PSSs S_6 and S_7 is equal to 90 V and for the switch S_8, this value is equal to 45 V. The voltage stress for the PSSs T_1, T_2, T_3 and T_4 in the tri-level circuit (TLC) is very minimum as compared with the PSSs in the basic unit and the voltage stress magnitude is equal to 5 V. Hence, the total standing voltage (TSV) across the PSSs of the suggested 51-level inverter circuit is equal to 560 V. The 51-level load voltage and load current waveforms, and total harmonic distortion (THD) of the load voltage for the various load parameters are shown in Fig. 5, Fig. 6, Fig. 7, Fig. 8 and Fig. 9, respectively.

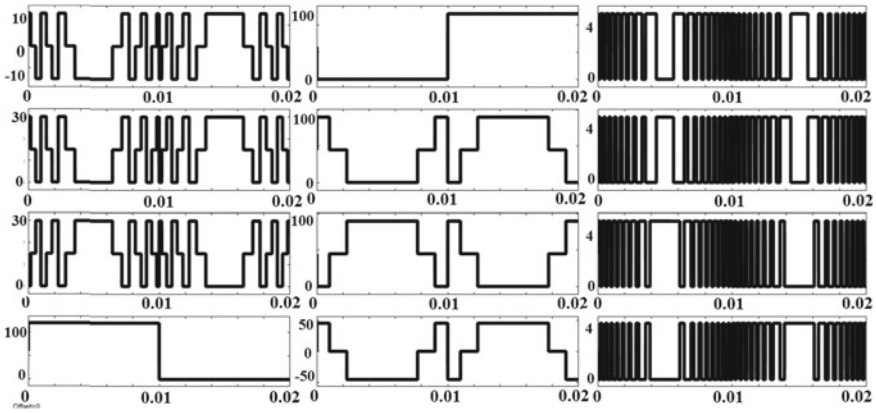
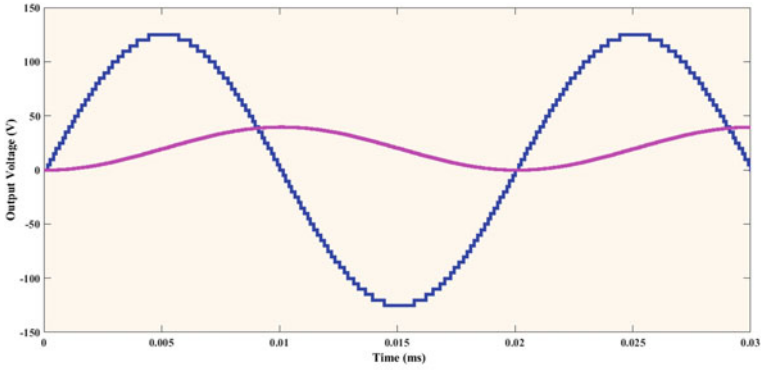


Fig. 4 Voltage stress across the PSSs



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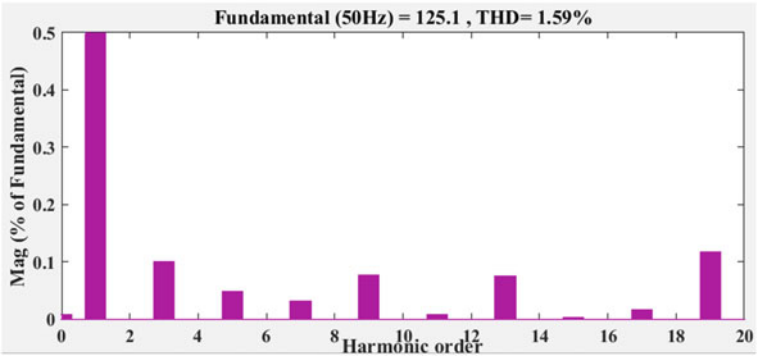

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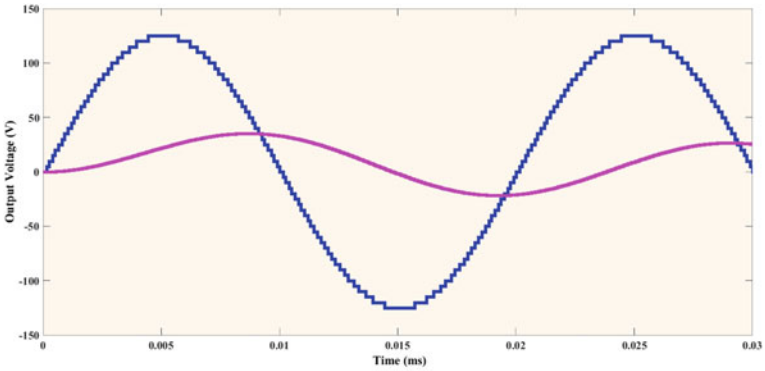
Fig. 5 Simulation results with $R = 0\ \Omega$, $L = 200$ mH **a** output waveform **b** TED



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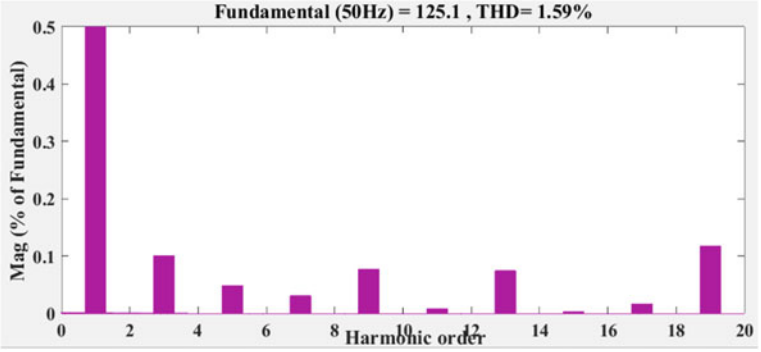


(b)

Fig. 6 Simulation results with $R = 15\ \Omega$, $L = 150$ mH **a** output waveform **b** TED

As anticipated, the output voltage is of the stepped waveform closely resembling the sinusoidal waveform with minimum THD. The THD values of both the voltage and current waveforms of the suggested 51-level inverter circuit for various load parameters are given in Table 2. For pure resistive load with $R = 75\ \Omega$, the THD of both 51-level output voltage waveform and load current waveform are equal to 1.59%. Furthermore, it is noticed that the THD of the load current waveform varies between 0.1 and 1.59% as the load power factor varies from 0 to 1.

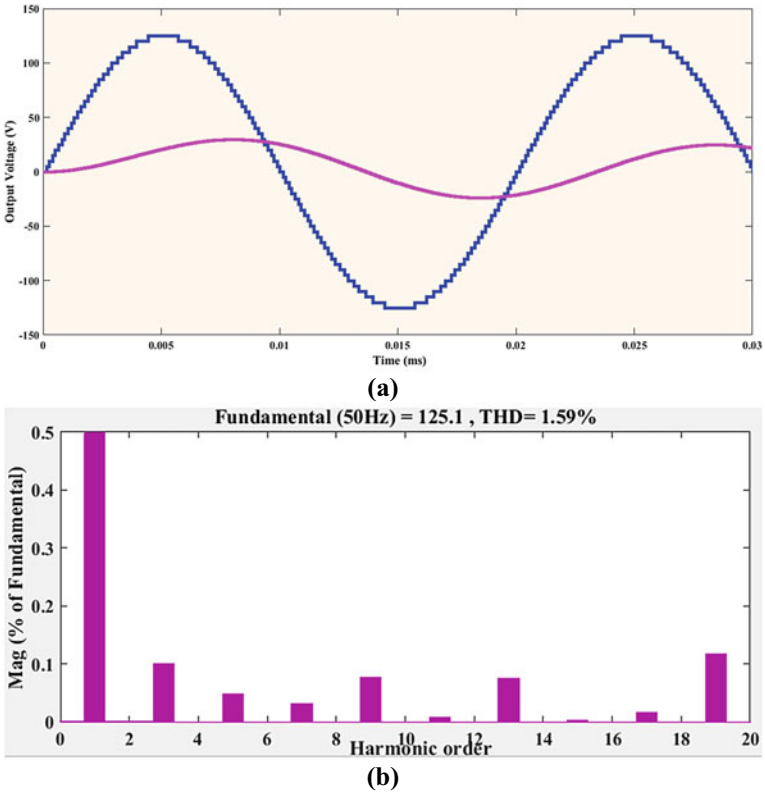
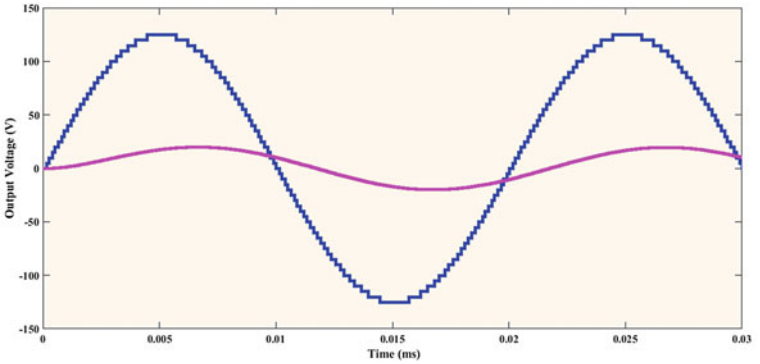


Fig. 7 Simulation results with $R = 25\ \Omega$, $L = 140$ mH **a** output waveform **b** TED

5 Conclusion

This article presents a new inverter module for 51-level operation that reduces the number of PSSs and DCVSs. The suggested inverter circuit has several merits including the reduced switch count, less blocking voltage of PSSs and ability to build negative output levels, not including any additional PSSs and DCVSs. The advantages of the suggested 51-level inverter circuit are confirmed through the latest comparable MLI topologies. In addition, the suggested 51-level inverter offers better efficiency and lesser switching losses. At last, the simulation results of the 51-level inverter obtained using MATLAB Simulink software is presented.



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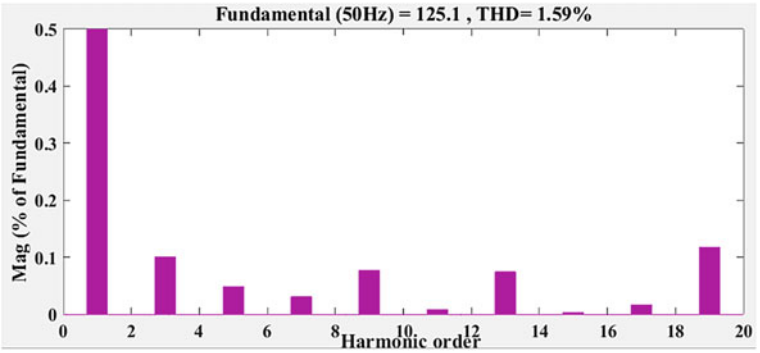

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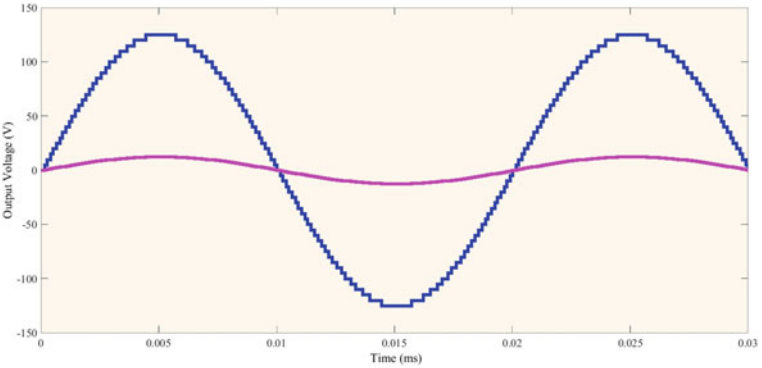
Fig. 8 Simulation results with $R = 45\ \Omega$, $L = 110$ mH **a** output waveform **b** TED



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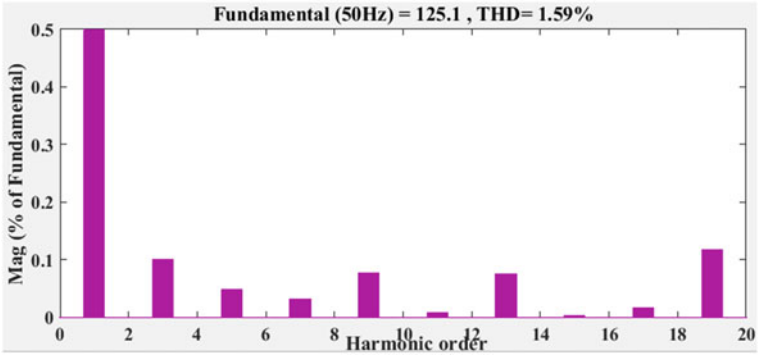

(b)

Fig. 9 Simulation results with $R = 75\ \Omega$ **a** output waveform **b** TED

Table 2 25-level inverter—load variation analysis

Load parameters		Power factor	Load voltage THD (%)	Load voltage current (%)
R (Ω)	L (mH)			
0	200	0	1.59	0.10
15	150	0.3	1.59	016
25	140	0.5	1.59	0.24
45	110	0.8	1.59	0.31
75	0	1	1.59	1.59

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Compact Power Supply for Induction Heating in Shrink Fitting

Akash Metha, Prashant Indalkar, Krithika Kamath, Pranav Samant, and Mini Rajeev

1 Introduction

Electric heating is one of the cleanest and reliable heating methods used in a variety of day-to-day applications such as industrial and domestic applications. Induction Heating (IH) systems possess the advantage of fast and precise heating as compared to conventional heating methods. Moreover, due to recent advancements in power electronics, it is easier to achieve the compactness of these heating systems. There are two forms of electrical heating—Resistance heating and Induction heating. The former is a direct method of heating which offers high efficiency, but suffers from the disadvantage of slow heating. The latter is a contactless method which offers high efficiency along with fast, reliable and localized heating [1]. Therefore, IH is more popular as compared to resistance heating.

The phenomenon of contactless heating, employing the principle of Faraday's law of electromagnetic induction, causes an electromagnetic force to be induced in the conducting material to be heated. This causes circulating eddy currents in the conducting material which heats it up. Figure 1 shows the block diagram of the IH circuit. Single phase, 230 V, 50 Hz AC supply is initially converted to DC using a rectifier-filter circuit. The filtered DC output is converted to high-frequency AC using an inverter circuit. In order to improve overall efficiency, a resonant circuit is

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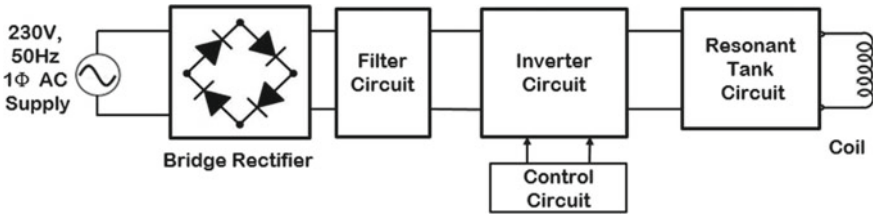


Fig. 1 Block diagram of induction heating

employed, which works at a high frequency in the order of kHz. Although operating at higher frequencies provides fast heating, it also results in an increase in switching losses. This disadvantage can be overcome by employing Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) which are also known as soft switching techniques.

The objective of this work is to design a portable, compact-sized power supply, having an output wattage of 1 kW for IH. To achieve this, a parallel quasi-resonant Inverter, employing only a single switch is selected. At a 1 kW power level, IH is used for applications such as Shrink Fitting, Induction Bonding and Induction Cooking.

The paper is organized as follows: Sect. 2 comprises various applications of IH, and Sect. 3 provides a brief survey of the converters used in IH. The detailed description of the selected inverter topology and its design is covered in Sect. 4, and simulation results and hardware results are shown in Sect. 5 and Sect. 6, respectively. Conclusion and reference are there at the end.

2 Applications of Induction Heating

Various applications of induction heating are discussed in this section. The application selected for this work is also elaborated on in detail.

2.1 Industrial Applications

Induction heating has a unique feature of providing localized heat which can be used to shape metals, metal coatings and for various other industrial applications like Forging, Brazing, Annealing, Surface hardening, etc. These applications may require high operating temperatures ranging from 200 to 1200 °C and hence may have higher power demand [2].

2.2 Domestic Applications

IH also has many domestic applications in appliances like Induction cookers, Electric hot plates, Induction stoves, Induction heaters, etc. These applications usually are of low power (500 W to 3 kW), and the compactness of appliances is the desired quality in such applications.

2.3 Medical Applications

Induction Heating being a clean, fast and portable heat source finds its application in the medical field as well. It is used for the manufacturing and sterilization process of medical instruments. It can be also used for cancer treatment in order to remove unwanted cells, thereby protecting the healthy cell in the body. It is carried out at a temperature of about 50 °C with a non-contact, accurate and proper power control mechanism [3].

2.4 Shrink-Fitting

The concept of expansion of metal when heated and contraction when cooled is utilized in Shrink-fitting. It is used for fitting or removing parts like rusted bolts, bearings, motor housing rings, gears and many more. Benefits of IH in such applications include high-speed operation, accuracy, energy efficiency and temperature control. This is achieved at a temperature of 150–300 °C at a frequency ranging from 10 to 300 kHz as per requirement. This application can also be used in Petrochemical industries as there is no flame involved in heating. This paper further discusses the resonant converter for IH in shrink-fitting applications [4].

3 Brief Survey of Converters Used in Induction Heating

Various topologies are proposed for IH application by researchers. A brief survey of these topologies is presented in this section.

3.1 Multi-output Voltage Source Inverter

Figure 2a shows the Multi-Output Half-Bridge VSI Converter. This topology is used for multi-output and multi-source systems. Domestically used induction heaters are

one of the examples which require multiple output power for different kinds of load. It employs at least three switches in half-bridge and more than three in full-bridge configuration. This again affects the compactness of the device and requires a cost-effective alternative to compete in the recent domestic Induction heating market [1, 2].

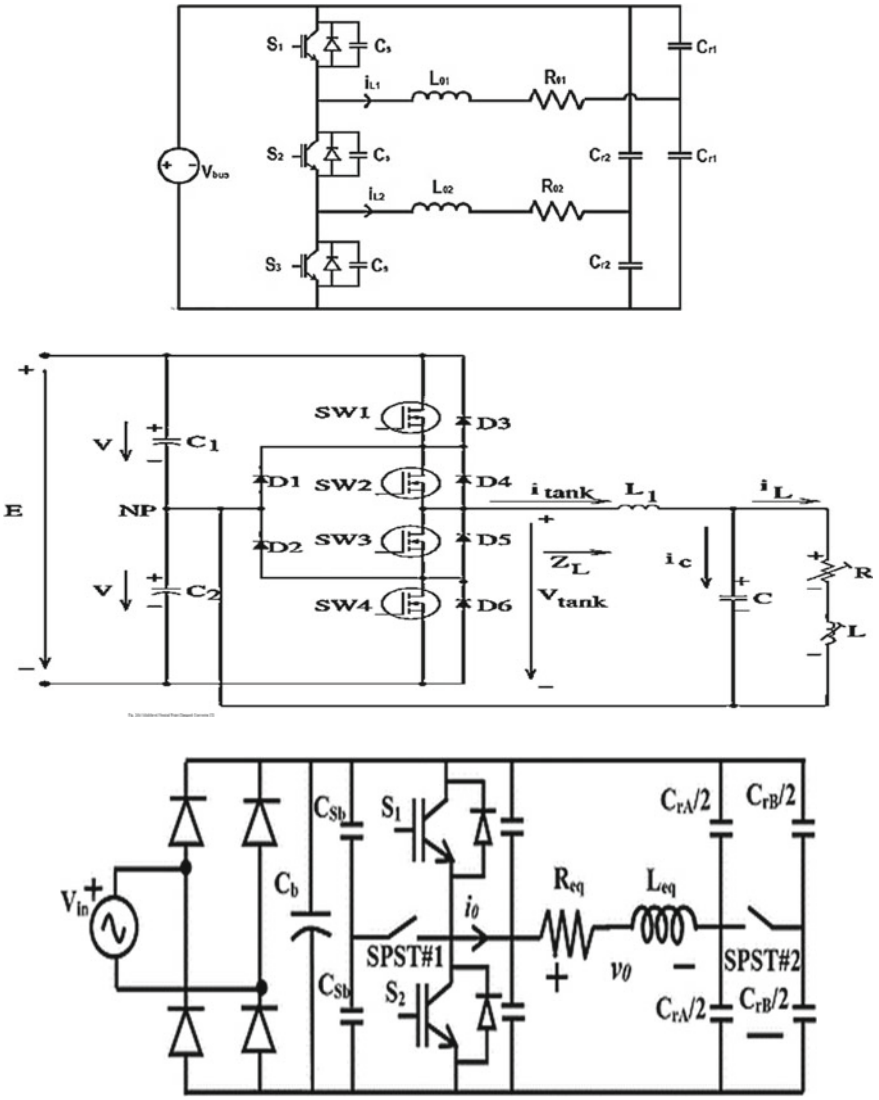


Fig. 2 **a** Multi-output half-bridge VSI converter [1]. **b** Multilevel neutral point clamped converter [5]. **c** Dual-mode resonant inverter [6]. **d** Interleaved boost AC-AC converter [6]. **e** Active clamped single switch VSI [7]

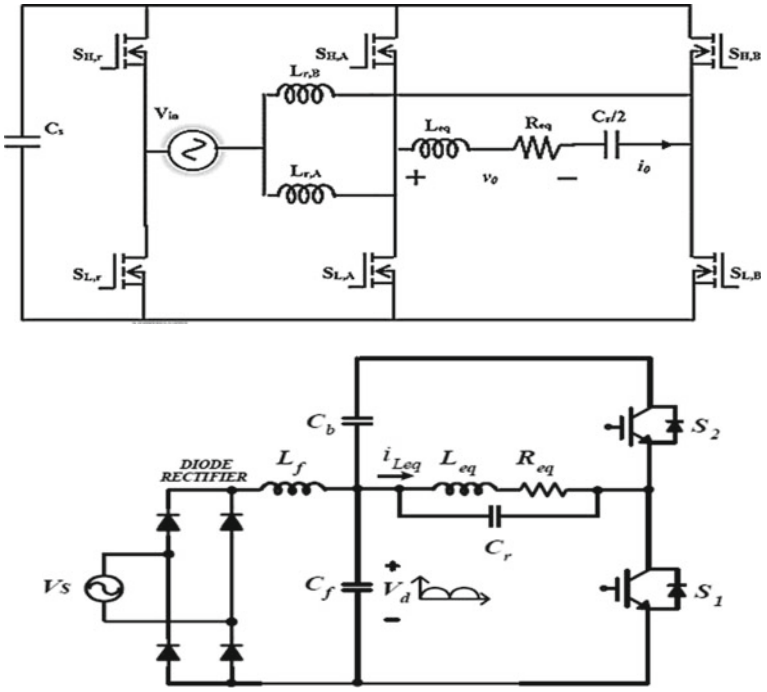


Fig. 2 (continued)

3.2 Multilevel Neutral Point Clamped (MNPC) Inverter Topology

Figure 2b shows the MNPC Converter. This topology maintains high efficiency by keeping the phasor difference between voltage and current to approximately zero at different loading conditions thereby ensuring maximum power transfer. This eventually reduces voltage stress on the switches, which in turn reduces the switching losses and helps to achieve high efficiency. It can be used with an LLC tank circuit to enhance its ability for short-circuit handling and current gain [5].

3.3 Dual-Mode Resonant Inverter

Dual-Mode Resonant Inverter topology shown in Fig. 2c is used to improve the efficiency of the system when operated at low power. This is achieved by replacing the resonant capacitor with an electromagnetic relay under low-load conditions. Under rated conditions, the inverter operates in class D operation, while under low-load conditions, it would switch over to class E inverter [6].

3.4 Interleaved Boost AC-AC Converter

Figure 2d shows an Interleaved Boost AC-AC Converter used for high-power induction heating applications in which low-frequency supply is directly converted to high-frequency AC without any DC link. It makes use of a boost inductor to limit current thereby increasing voltage which then also helps to reduce current ripple as well as conduction losses [6].

3.5 Single-Switch Resonant Inverter

Active Clamped Single-Switch VSI: Figure 2e shows the circuit diagram of the Active Clamp Converter. It incorporates two switches, one for inverter operation and the other for auxiliary purposes. It can also be used with ZVS or ZCS; but the use of two switches again affects its compatibility and increases complexity [7–9].

Single-Switch Voltage Source Inverter: Single-Switch VSI topology houses a single semiconductor switch along with a resonant tank circuit to improve overall efficiency and can be operated using either ZVS or ZCS technique to reduce switching losses. The inverter topology which is described in this paper is a type of single-switch VSI. Figure 3 shows the IH power supply circuit [1, 10].

4 Selected Resonant Converter and Its Design

This section elaborates on the design of the selected resonant converter. The selected topology is a single-switch parallel quasi-resonant converter as shown in Fig. 3. A 230 V, 50 Hz AC power supply, when given to a full-bridge rectifier, gives output with ripples of twice the supply frequency, i.e.,100 Hz. This rectified output is then provided to a LC circuit where the value of L and C is taken as per the ripple required, followed by a single switch parallel quasi-resonant inverter circuit. The details of the inverter are mentioned in the subsequent subsections.

The inverter topology comprises a parallel resonant circuit and a single switch, which operates at a switching frequency of 50 kHz. A Silicon Carbide MOSFET is

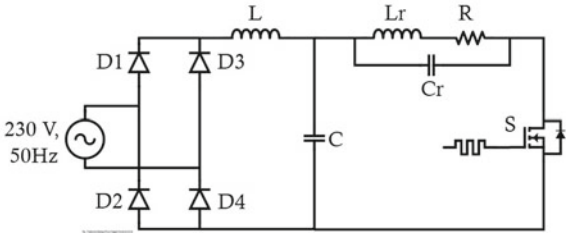


Fig. 3 Induction heating power supply circuit [11, 12]

used to improve the overall efficiency of the converter circuit. The use of a single switch makes the circuit simple and eliminates the problem of short circuits caused by insufficient dead time. Moreover, the size of the heat sink and the cost of the circuit is also reduced. This is because of the phenomenon of turning the switch on at zero voltage conditions [12], which helps to reduce the switching losses at high frequencies to a considerable extent.

4.1 Modes of Operation

Mode 1 (t0–t1): Initially, the switch (S) is turned on and the resonant inductor (Lr) charges with positive polarity as shown in Fig. 4a. Since the inductor doesn't allow a rapid change in the current (low di/dt), Lr and switch current start rising gradually to their peak value. Initially, the resonant capacitor current has a transient peak. These transient peak charges the resonant capacitor (Cr) with the polarity as shown in the figure. Thereafter, the resonant capacitor acts as an open circuit once it gets fully charged. The DC link capacitor (C) discharges through Lr, thereby causing the switch current to be the summation of the DC link capacitor current and filter inductor current.

Mode 2 (t1–t2): In mode 2, the absence of a gate pulse turns off the switch (S). This reduces the switch current to zero and the switch voltage rises gradually. Since Cr doesn't allow a sudden change in voltage (low dv/dt), it discharges through Lr in the direction as shown in Fig. 4b. Hence, Lr gets charged during this process. The supply current has only one path, i.e., through C.

Mode 3 (t2–t3): The charged Lr now discharges through Cr. Thus, Cr charges to $2Vi$ due to the charge stored in Lr. During this period, the switch voltage rises to $3Vi$ and the supply current continues to flow through C.

Mode 4 (t3–t4): Up to this instant, energy stored in Lr is completely utilized to charge Cr. Cr now starts discharging through inductor Lr as shown in Fig. 4d. This in turn charges Lr and hence, the voltage across the switch starts reducing.

Mode 5 (t4–t0): Once Cr has completely discharged, Lr starts discharging through capacitor (C) in the direction as shown in Fig. 4e. The reason is that, the value of C is higher than Cr, hence C offers low reactance as compared to that offered by Cr ($Xc < Xcr$). The discharging of inductor (Lr) through capacitor (C) makes the anti-parallel diode across the switch conduct and hence zero voltage condition is achieved.

Mode 6 (t0): This zero voltage condition across the switch can be utilized to achieve zero voltage switching (ZVS) in order to reduce turn-on switching losses.

Waveforms pertaining to different modes are presented in Fig. 5.

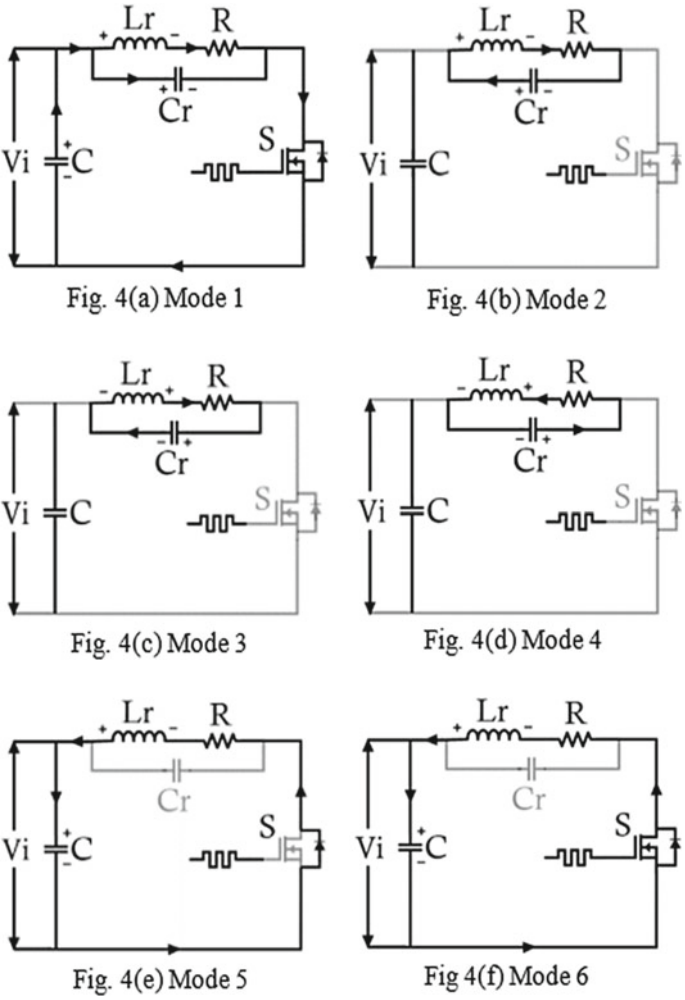


Fig. 4 **a** Mode 1. **b** Mode 2. **c** Mode 3. **d** Mode 4. **e** Mode 5. **f** Mode 6

4.2 Design of Resonant Circuit

This sub-section deals with the design of the quasi-resonant circuit. Table 1 lists the parameters considered for the design.

Design of Resonant Inductor: The value of the resonant inductor can be calculated from the Q factor as given below [13]

$$Lr = \frac{Q * Rl}{2\pi * fr} \tag{1}$$

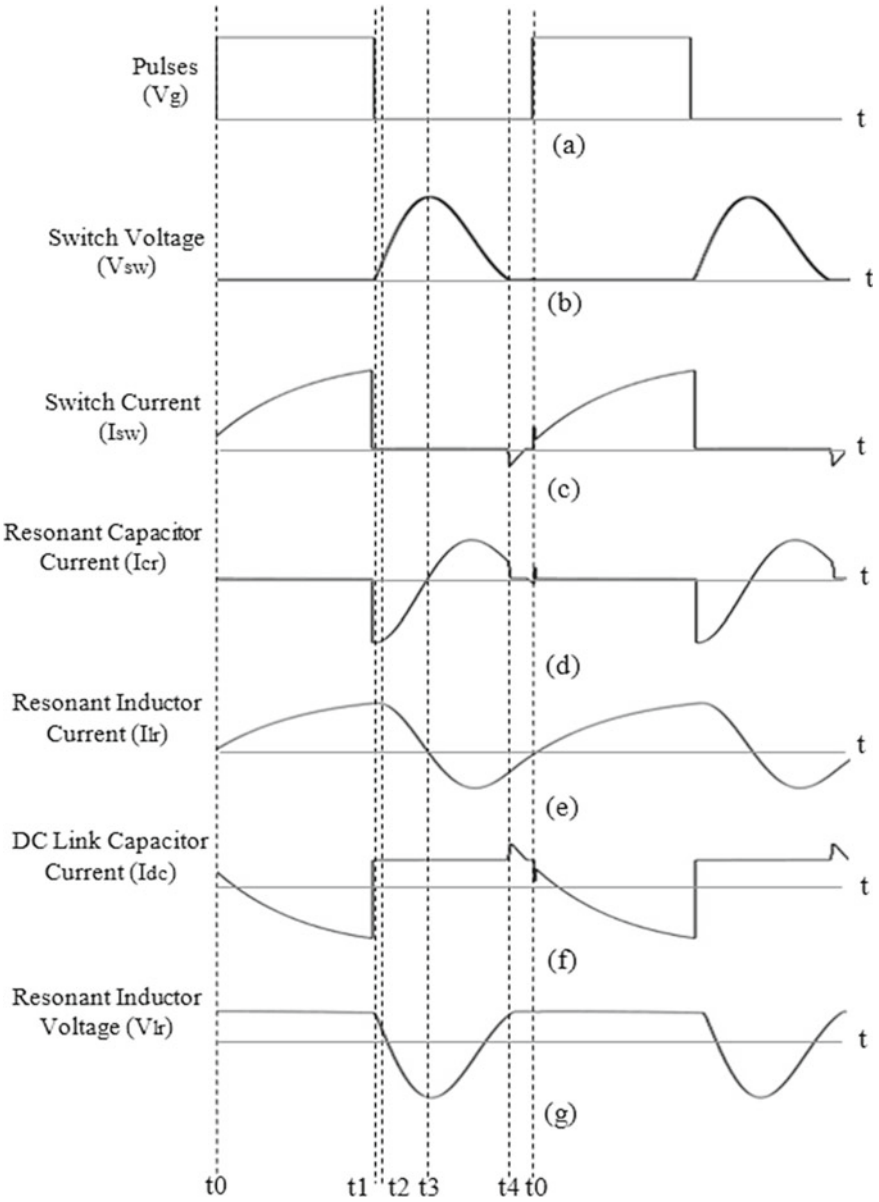


Fig. 5 Waveform pertaining to different modes

Table 1 Design parameters

Sr. No.	Parameters	Values
1	V_{input} (RMS)	230 V
2	Output power (P_{out})	1 kW
3	Switching frequency (fs)	50 kHz
4	Resonant frequency (fr)	80 kHz
5	Equivalent resistance (R_l)	20 Ω

where

Q = Quality Factor,
Rl = Equivalent Resistance and
fr = Resonant Frequency.
Assuming the value of the Q factor as 3, we get Lr as 119.36 μH.

Design of Resonant Capacitor. Resonant frequency for the parallel resonant circuit is given by [13]

$$fr = \frac{1}{2\pi}\sqrt{\frac{1}{Lr * Cr} - \frac{Rl^2}{4Lr^2}} \tag{2}$$

After substituting the required values, we get.
Resonant Capacitor (Cr) = 31.41 nF ≈ 32 nF.

Design of working coil. An air-core inductor can be designed using the H. A. Wheeler formula as given below [14]

$$L = \frac{r^2 * N^2}{(9r + 10l)} \tag{3}$$

where

L—Inductance of coil in μH,
r—Radius of coil in inches,
l—length of coil in inches and
N—Number of turns.
Here, $l > 0.8r$ is required to satisfy Eq. (3).
Figure 6 shows the design consideration used for the working coil.
Take radius (r) of the coil (as per requirement) = 1.5 in.
and Length (l) of the coil (as required) = 3 in.
Thus, from Eq. (3), we get
$N = 48.67 \approx 49$ turns.
For calculating the wire gauge,

$$\text{Diameter of a conductor in inches } (d) = \frac{length\ of\ coil(l)}{No.\ of\ turns(N)} \tag{4}$$

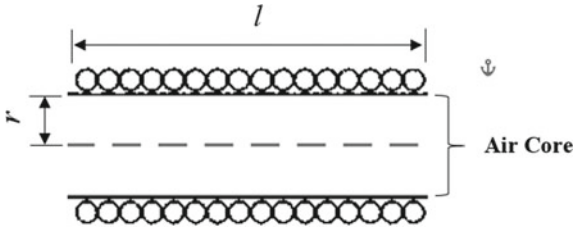


Fig. 6 Design consideration used for working coil

Thus, we get d as 0.064 in. and accordingly, 16 SWG wire size is selected.

This approximation of conductor size then increases the length of the coil from 3 to 3.11 in. (0.064 * 49).

5 Simulation Results

The simulation of the system is carried out in MATLAB/SIMULINK. Results are shown in this section. The values of the parameters presented in Table 2 are used for simulation.

A single phase, 230 V, 50 Hz supply is used as source, followed by a bridge rectifier, along with an inductor (L) filter. Apart from this, a DC link capacitor (C) is used to help achieve ZVS operation. A working coil is connected in parallel with the resonant capacitor (Cr). An IGBT is used as a switching device. The frequency of pulses given to the gate terminal of IGBT is 50 kHz, with a duty cycle of 50%. The waveforms presented in Fig. 7 show a simulated waveform of supply voltage, supply current, resonant inductor voltage, resonant inductor current, switch voltage and switch current, respectively.

Figure 8 shows the circuit simulation model of the selected topology. As shown in Fig. 5c, the reverse current through the switch is due to the inductor discharge current during Mode 4, and this current passes through the anti-parallel diode of IGBT. The voltage across the switch is zero, and hence, ZVS is obtained during this instant. Figure 9 shows the output power waveform. The output power is around 950 W and the input power is 700 W. The power factor obtained is 0.9967 leading, as shown

Table 2 Simulated parameters

Sr. No.	Parameters	Values
1	Filter inductor	2 mH
2	DC link capacitor	3.3 μF
3	Working coil	119.36 μH
4	Resistance	20 Ω
5	Resonant capacitor	32 nF
6	Switching frequency	50 kHz

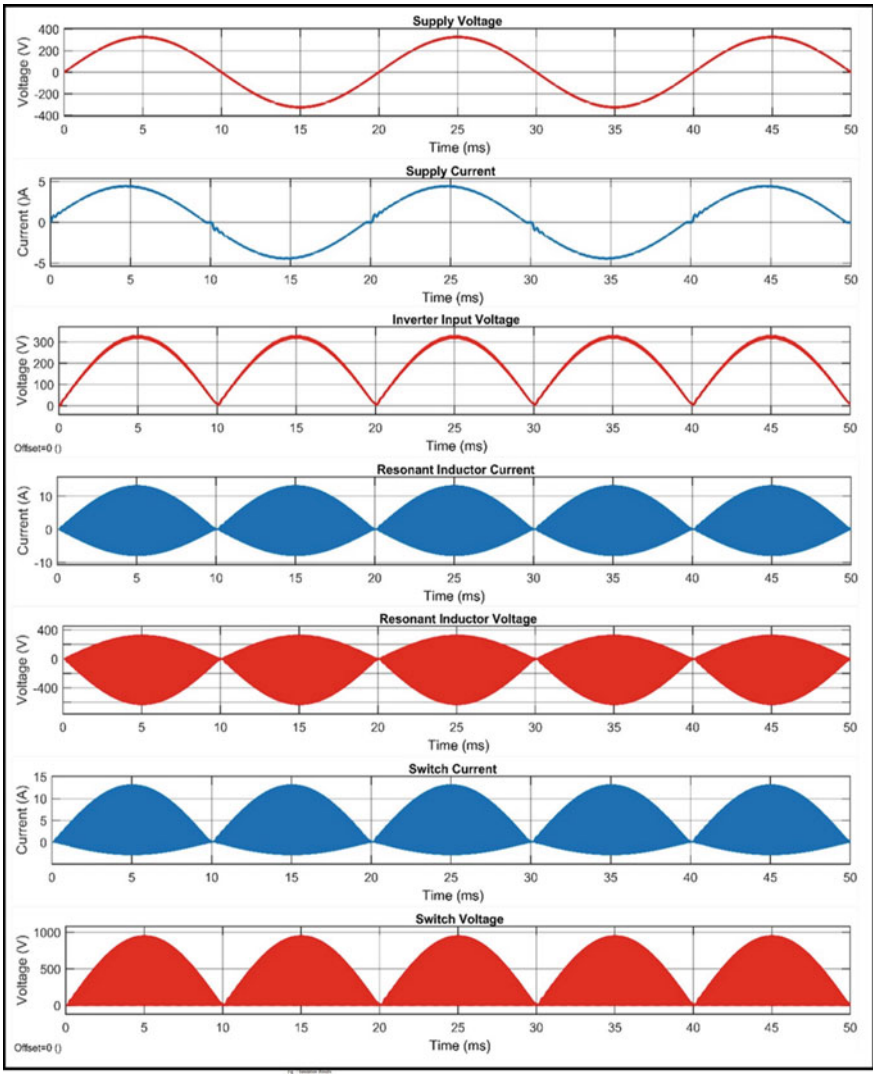


Fig. 7 Simulation results

in Fig. 8. This means that the device is behaving as a capacitive load for a 50% duty cycle and 50 kHz switching frequency. The FFT analysis of the input current is carried out and results are presented in Fig. 10. The Total Harmonic Distortion (THD) of 2.04% is observed, which is below permissible limits.

Based on the simulation results, it is observed that in order to achieve proper resonance, resonant frequency should be higher than the switching frequency for proper ZVS operation to take place. This also helps in reducing the size of the resonant filter. Hard switching can still occur in a resonant tank circuit even with a

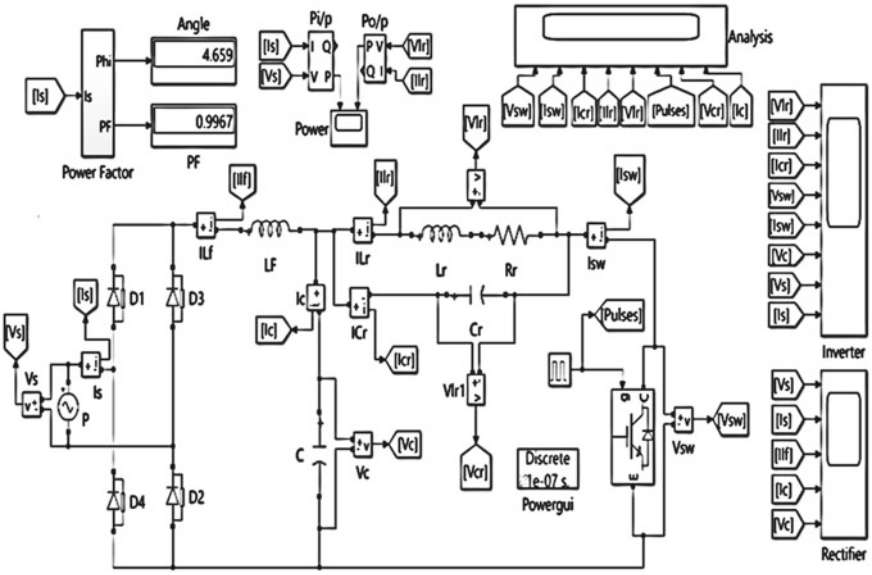


Fig. 8 MATLAB simulation

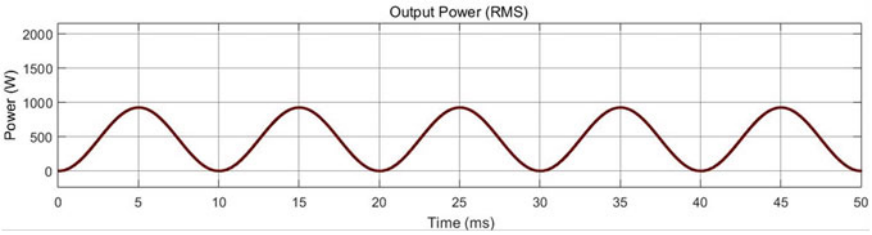


Fig. 9 Output power

higher resonant frequency, due to improper selection of duty cycle. This may occur due to duty cycle (D) being too low or too high, and thus it plays a very vital role in converter operation, especially for ZVS switching. Therefore, the value of the duty cycle used for simulation should be in the range of 0.45–0.55. A duty cycle of 0.5 is chosen for this simulation.

6 Hardware Results

Hardware implementation of the selected converter and its results are presented in this section. The hardware part comprises the control circuit and power circuit. Switch-control circuit consists of driver IC HCPL3120, which has an in-built optocoupler.

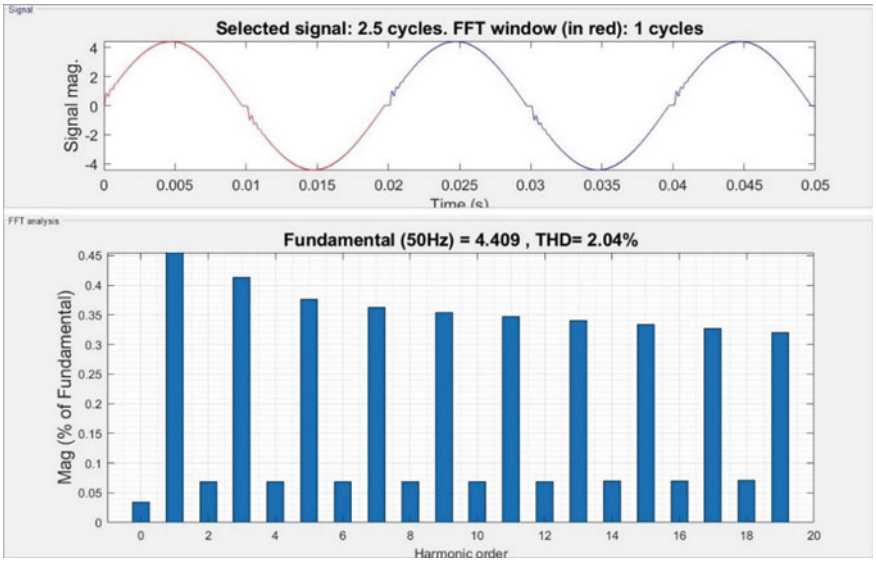


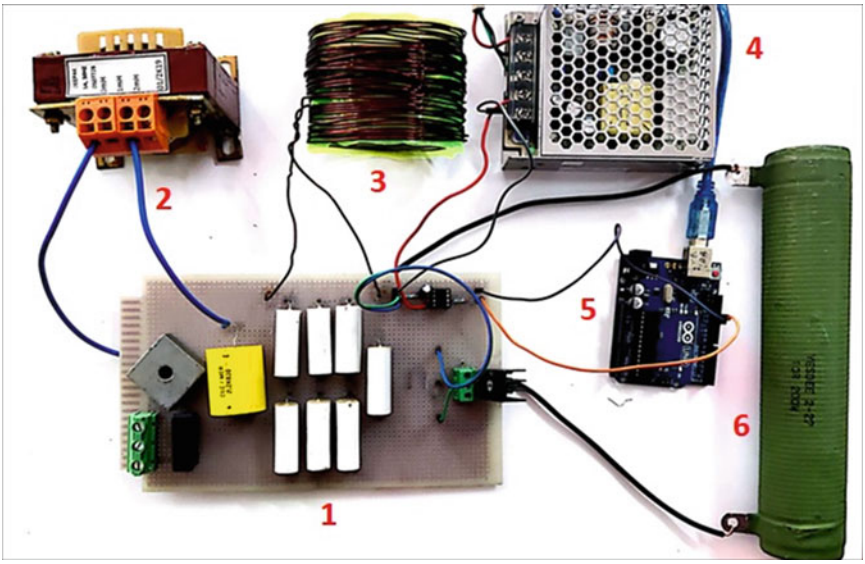
Fig. 10 FFT analysis of supply current

The power circuit consists of a rectifier, resonant circuit and inverter circuit. The circuit was first tested with IGBT (G4PH50UD) on a reduced voltage of 110 V using an auto-transformer with a 230 V, 50 Hz AC supply. Later, when IGBT was replaced by SiC MOSFET (SCT2280KE), the current through the working coil was observed to have increased for the same voltage level of 110 V, indicating an increase in output power and efficiency. A photograph of the laboratory setup is shown in Fig. 11. List of components for hardware implementation is presented in Table 3.

In case of IGBT, ZVS condition is achieved at a switching frequency of 45 kHz whereas in the case of SiC MOSFET, it is achieved at 40 kHz. Both waveforms were observed through DSO and are presented in Fig. 12a, b, where ZVS can be observed. An increase in switch current from 3.2 A in IGBT to 4A in SiC MOSFET is observed. A metal piece was used as the target material for IH. The heating effect was higher in the case of SiC MOSFET as compared to IGBT as the on-state losses in SiC MOSFET are lesser.

7 Conclusion

Simulation and hardware results of single switch parallel quasi-resonant converter, utilizing the concept of Induction Heating and suitable for Shrink-fitting application, are presented in this paper. The design of the supply system using a resonant converter is discussed in detail and validated for a reduced voltage level of 110 V by the hardware results obtained. Zero Voltage Switching was achieved and heating of



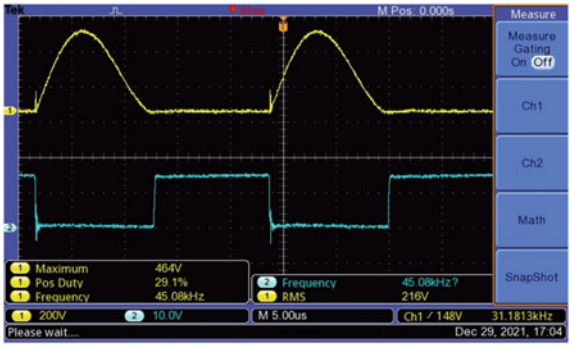
1. Circuit; 2. Filter Inductor; 3. Working Coil; 4. DC Power Supply; 5. Arduino; 6. Resistor

Fig. 11 Hardware implementation of selected converter

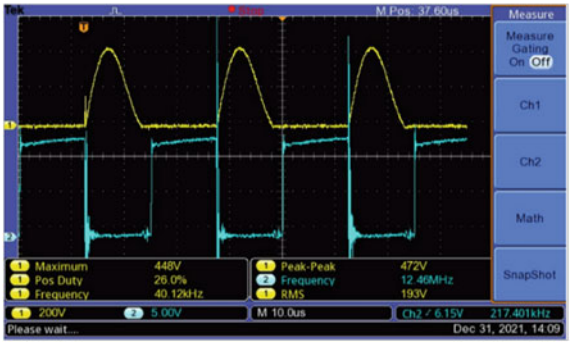
Table 3 List of components and parameters in prototype

Sr. No.	Components	Values
1	Supply voltage	110 V, 50 Hz
2	Bridge rectifier (KBPC5010)	2500 V, 50 A
3	DC link inductor	2 mH
4	DC link capacitor	2.2 μF
5	Working coil	385 μH, 0.2 Ω
6	Resistance	10.6 Ω
7	Resonant capacitor	32 nF
8	Switching frequency	40 kHz
9	Resonant frequency	50 kHz
10	SiC MOSFET (SCT2280KE)	1200 V, 14 A
11	HCPL3120	–

the target material was observed. Results were compared by using IGBT and SiC MOSFET as switching devices. Output power was higher in the case of SiC MOSFET as expected, thereby improving the efficiency of the system. A compact power supply can be constructed for Induction heating in shrink-fitting applications by means of zero voltage switching with wide-band gap devices.



(a) IGBT



(b) SiC MOSFET

Fig. 12 Switch voltage and pulses at ZVS condition

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Investigation on Physics-Based Models of Lithium Ion Batteries in Electric Vehicle Applications: A Review

P. Aruna, V. Vasan Prabhu, and V. Krishna Kumar

1 Introduction

The important emphasis is to increase the functionalities of BMS used in EV to guarantee secure and reliable operation and prevent the battery from running outside of its safe operating parameters. The ability of BMS to precisely monitor internal battery states is critical for sensible operational strategies and reliable fault diagnostics [1]. A well-managed Li-ion battery can reduce battery cell aging, prevent cell failures, and prevent catastrophic fires/explosions caused by overcharging, discharging, high temperature; internal and external short circuits of the cells, and other stressed operating conditions. Battery indicators such as State of Charge (SOC) and State of Health (SOH) are frequently employed in present BMS algorithms to specify the energy stored and the degree of battery degradation [2]. Nevertheless, the internal states of the battery cannot be measured directly and the only directly quantifiable values are the surface temperature, terminal voltage, and current which are measured by standard sensor technology. Thus efficient mathematical models describing the electrical and thermal dynamics of a battery cell are pivotal, allowing smart controls to accomplish maximum energy and power from the lithium batteries without premature aging of cells [1]. The real-time dynamics of the cell can be determined by using these models. The well-known existing general battery models; mathematical model, electrochemical model, and equivalent circuit-based model have been defined in the literature for various applications. The properties of lithium ion batteries predicted and described using mathematical models are based on empirical formulas and stochastic

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techniques. It is very challenging to transfer and execute those models on generic circuit modeling tools to evaluate the performance of the battery as they do not have direct relationships with physical data. The intercalation of lithium in the electrolyte and electrodes represented by the electrochemical model is computationally intensive and cannot be implemented in the on board of BMS without simplification [3]. The SOC of the lithium ion battery is usually estimated using Equivalent-Circuit Models (ECM), which are frequently employed. But the intrinsic chemical reactions occurring within the cell are not represented by this model and hence these models produce poor predictions of aging. If the evolving dynamic features due to battery degradation are not adequately taken into account, the estimation of battery performance becomes inaccurate [4]. The BMS with PBMs of the battery will provide the valuable internal information for the prediction of aging and extended lifetime. At the same time, the arduous PBMs being constructed from basic thermodynamic and electrochemical principles are highly complex in computation and cognitive for EV applications. This paper reviews the recent reduced order PBMs of lithium ion batteries.

1.1 Difference Between Empirical Models and Physics-Based Models

The word "empirical model" refers to models that are developed by observation and experimentation and are able to describe the performance of the system within a limited working range accurately. When it comes to the processes that occur in the system, the empirical models have no physical significance. They merely change the input of the system to forecast the output in order to mimic the behavior of the original system. The advantage of empirical models over physics-based models is that they are easier to build and analyze. On the other hand, PBMs, which are derived from the electrochemical properties of lithium-ion cells, describe the internal dynamics of the system which is extremely complicated. Even though this model is difficult to create and compute, it provides a more accurate picture of thermal behavior [5], dendritic growth [6], chemical evaporation [7], and other phenomena. These models can also be utilized to develop reduced-order models that can be employed efficiently in BMS for hybrid and electric vehicles after they have been evaluated for usefulness (HEVs and EVs) [8].

2 Continuum Porous-Electrode Model

The most extensively used PBM of lithium-ion battery cells is the continuum porous-electrode model. The term "continuum" refers to averaging the underlying physics over a set of homogeneity assumptions. The term "porous-electrode" denotes the

fact that electrodes are made up of numerous microscopic particles. The holes or porosity between these particles are filled with electrolyte. The fundamental physics of charge conservation, mass conservation, and rate of reaction equations are utilized to model and explain the internal features of lithium-ion battery cells. These equations are defined by five separate time and space varying variables represented as Partial Differential Equations (PDE) [7].

- The first PDE models distribution of lithium in the solid electrode particles leading to the concentration of lithium $Cs(x, r, t)$ at the electrodes surface $Cs(x, t)$, where "x" represents a spherically symmetric reference frame "t" denotes the function of time and "r" represents the radial dimension inside of that spherical particle.
- The second PDE models the diffusion of electrons depending on the rate of production of it and it is represented by "$Ce(x, t)$".
- The third PDE models the diffusion of electronic charge balance and particle behavior leading to the forecasting of solid potential denoted by "$\Phi s(x, t)$".
- The fourth PDE models the balancing of ions in the electrolyte leading to the forecasting of the potential of the electrolyte given by "$\Phi e(x, t)$".
- The fifth PDE coordinates all four PDEs and it models the rate of transference of lithium between the electrodes and electrolyte is represented by "$j(x, t)$".

This shows that the study of the diffusion of lithium ion is important for determining the behavior of a cell. Figure 1 represents an inside look at a lithium ion cell.

The diffusion has the effect of transporting lithium from high-concentration areas to low-concentration areas and the leveling out the concentrations over time are shown in Fig. 2. The rate of diffusion is approximated by discrete approximation as shown in Eq. (1). It states that at any location in space, the future concentration is equal to the current concentration plus diffusivity multiplied by the time difference Delta t, multiplied by the central difference estimate of the second derivative. The Octave code is developed to simulate linear diffusion of lithium using this discrete approximation and by assuming the parameters shown in Table 1. The computations are performed in a Jupyter notebook using octave code [7].

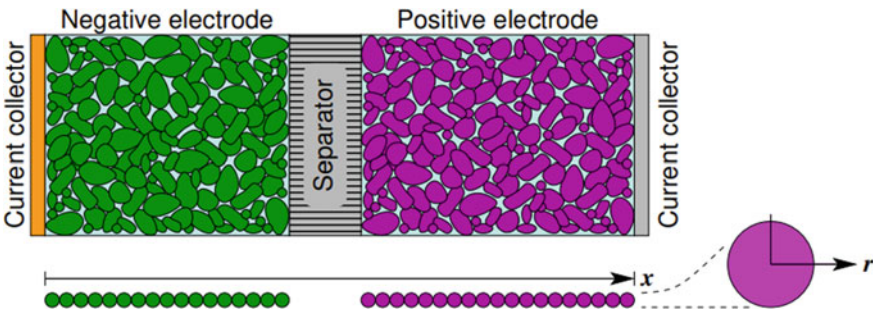

Fig. 1 An inside look at a typical Lithium ion cell [7]

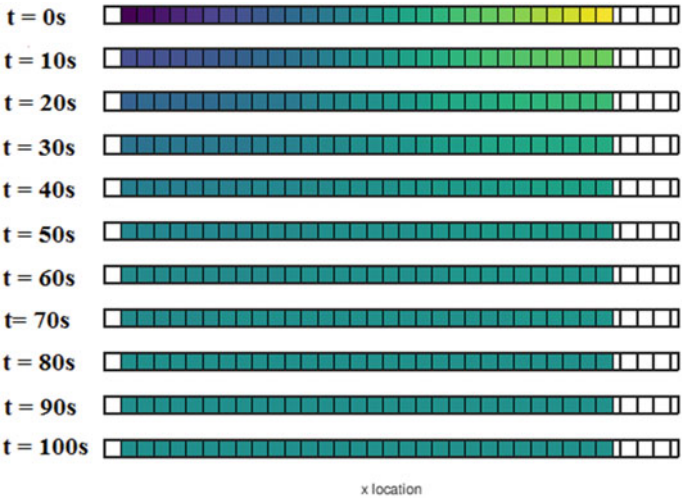

Fig. 2 Linear diffusion of lithium ions

Table 1 The parameters of linear diffusion

Parameters	Values
Initial concentration gradient C	1:30 in moles/m^3
Diffusivity D	3 m/s
Time step, dt	0.1 s
Spatial resolution dx	1 m
Simulation time	100 s

$$c(x, t + \Delta t) = c(x, t) + D\Delta t \frac{c(x + \Delta x, t) - 2c(x, t) + c(x - \Delta x, t)}{(\Delta x)^2} \quad (1)$$

A color gradient is being plotted in Fig. 2 to show the concentration of lithium at various positions in the one-dimensional space. The leftmost concentration has a value of one at time zero and the value of the rightmost concentration is 32. Low concentrations are depicted as in this diagram. High concentrations are shown in greenish-yellow color, whereas low concentrations are shown in a purple color and medium concentrations are shown as light aqua color. As time progresses, Lithium goes from one state to another. This diffusion mechanism transports from high-concentration locations to low-concentration areas. Hence, the sharpness of greenish-yellow, aqua, and purple colors gets reduced and when the simulation gets over, the concentration is evenly identical at every place. The simulated result shows that the diffusion is nothing but the movement of lithium from higher concentration to lower concentration areas. In a real-time BMS, evaluating these PDE equations

requires more computations than is feasible. Hence there is a need for approximating these equations. One of the approximation methods is Single-Particle Reduced Order Model (SPROM) which is explained in the next section.

3 Single-Particle Reduced Order Model

The dynamic contribution of diffusion is the most important as the lithium diffusion inside solid particles is the slowest process in a cell. Therefore, a single-particle model (SPROM) of a cell can be considered, by representing a typical particle as a single spherical particle within the electrode. The change in lithium concentration throughout the interior of this spherical electrode particle will be simulated using a finite volume method. The particle is divided into spherical shells of equal thickness to model the varying concentrations at different spots in the particle which will resemble an onion. So that there will be an inner core, an outer ring, a third ring, a fourth ring, and so on. Each of these rings has the same thickness, but when the radius expands, the volume of each of these shells grows as well. As the concentration of electrolytes and their potential dynamics are not taken into account in PBMs, SPROM is a good learning tool for understanding the response of lithium ion cells to various input stimuli for estimating the SOC. In this method, a PDE-based state estimation approach that makes use of lithium conservation, marginal stability, and invariability of output function for getting convergent estimates is used [9]. This SPROM is also simulated in the octave environment. At each time step of the simulation, the transportation of lithium from one shell to another is calculated and then the concentrations inside each of these shells is updated based on that calculation of lithium mobility. The amount of lithium in the outermost shell of the particle will be updated by the electrical current delivered to the terminals of the overall battery cell. The simulation is performed by considering Nr as the number of shells in radial direction and Rs as the radius of the particle, then

$$\text{Width of the shell } dR = \frac{Rs}{Nr} \tag{2}$$

$$\text{Volume of the innermost shell } dV_1 = \frac{4}{3}\pi (dR)^3 \tag{3}$$

$$\text{Surface area of the innermost shell, } Sa_1 = 4\pi (dR)^2 \tag{4}$$

$$\text{Volume of nth shell, } dV_n = \frac{4}{3}\pi (ndR)^3 - \frac{4}{3}\pi ((n-1)dR)^3 \tag{5}$$

$$\text{Surface area of nth shell, } Sa_n = 4\pi (ndR)^2 \tag{6}$$

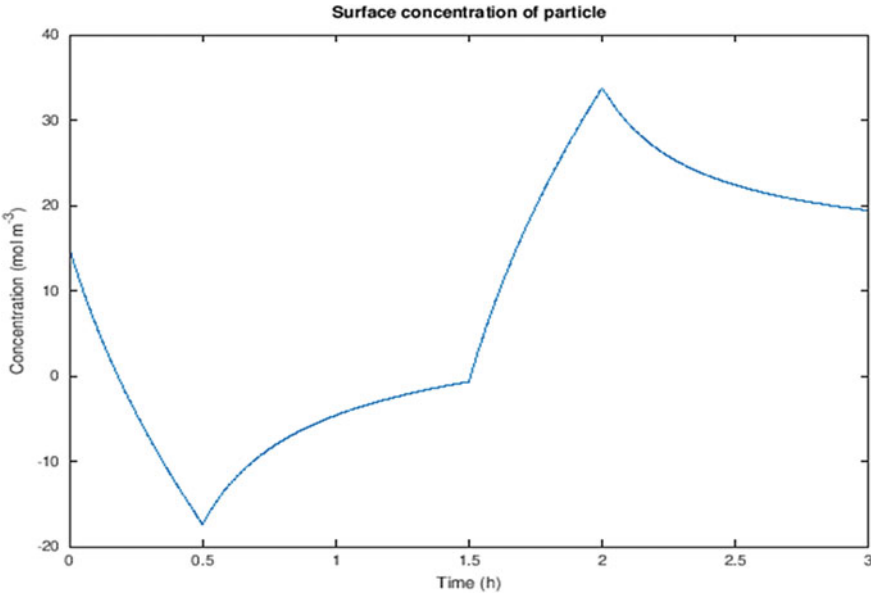

Fig. 3 Radial symmetric diffusion in a single negative-electrode particle

Using the Eqs. (2)–(6) the construction of a single-particle, as the particle is discharged, rested, charged, and rested is simulated. The output of radial symmetric diffusion in a single negative-electrode particle is shown in Fig. 3.

Even though the SPROM technique provides a better understanding of physics-based models working, it lacks sufficient resolution to allow us to predict or replicate the processes that cause degradation. As a result, this model is called a zero-dimensional model to regulate degradation. It averages the entire electrode down to a single typical spatial point, which is insufficient to manage degradation because degradation is spatially variable. It varies at different points in the cell; therefore there is a need for at least a one-dimensional model that represents the cross section between the current collector and the separator border on one side and the separator boundary on the other.

4 Doyle–Fuller–Newman (DFN) Model

An extensively used electrochemistry-based model is the DFN model [10]. Figure 1 depicts the modeling of a Li-ion cell using DFN. In this model, the Concentrations and potentials are expressed in the radial direction r and in the x dimension. Hence, it is known as a pseudo-two-dimensional model [11]. The negative-electrode, separator,

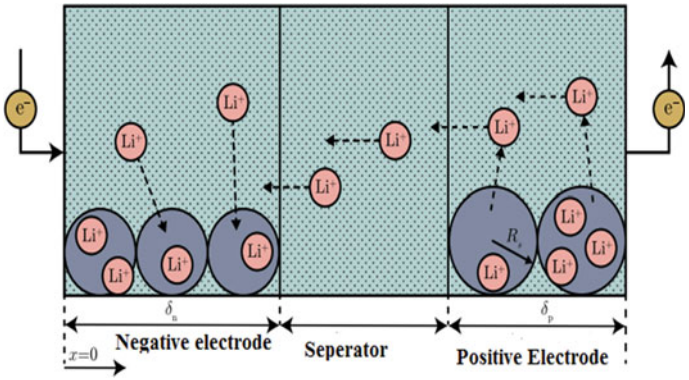

Fig. 4 Modeling of lithium ion cell using DFN approach (11)

and positive electrode are the three sections of the cell in the x dimension. This model is considered as a consistent physics-based modeling tool for lithium-ion batteries. Its flaws in predicting battery dynamics at high discharge rates, operating temperatures, and most significantly, the reason behind aging process is not fully addressed. The battery's operating regimes, which result in violations of the approximations and limits that contributed to the creation of the DFN model, are not well documented in the literature [12] (Fig. 4).

Some of the fundamental assumptions of the DFN model are outlined in [13]. The particle geometry is the most important of them all. According to experiments [14], the practical battery electrodes feature non-spherical particle morphologies that display polydispersity. Furthermore, the effective transport qualities are calculated based on an empirical relationship that is only dependent on the electrolyte volume percent. Electrode topology and morphology, on the other hand, have a major impact on these effective qualities [15]. In single-particle models [16] such constraints may be magnified significantly. Hence, even if their performance is accurate in comparison to the DFN model, the end results of such control-oriented models may not accurately reflect real-world battery response. Research efforts have not fully addressed the problem of determining the optimal operating conditions for the models in use so far. Lack of awareness of model usage may lead to its implementation for the inappropriate application unless this is rectified. Hence there is a necessity to imply the ROM for modeling the electrochemical reactions occurring within the cell optimally in discrete-time space.

5 Reduced Order Models Using Discrete Realization Algorithm (DRA)

In order to model the internal dynamics of a lithium-ion cell, the transfer functions of reaction flux $j(z, t)$, the over potential $\eta(z, t)$, and the solid surface concentration Cs, $e(z, t)$ which are the cell variables that are firmly bonded together, solid potential in an electrode $\Phi s(z, t)$, electrolyte potential $\Phi e(x, t)$ and lithium concentration in the electrolyte $Ce(x, t)$ must be converted into reduced order models optimally in discrete-time with the Eqs. (7) and (8).

$$x(t + T_S) = Ax(t) + Bi_{app}(t) \tag{7}$$

$$y(t) = Cx(t) + Di_{app}(t) \tag{8}$$

where T_S is the sampling period of the discrete-time ROM, $x(t)$ is the "state" vector of the model at time t, $y(t)$ is the "output" vector of the model at time t, i_{app} is the applied cell current and A, B, C, and D are matrices [17]. As the outputs and states of ROM are effective only at the integer multiples of the sampling periods, the Discrete Realization Algorithm (DRA) that relies on Hoe Kalman algorithm [18] is used for generating optimal ROM in discrete-time space from the pulse response of discrete-time system.

The description of the algorithm in detail as follows [19]

Step 1: The continuous-time impulse response is approximated by sampling the continuous-time transfer function in the frequency domain at a high rate Fs which is then converted into the inverse discrete Fourier transform (IDFT).

Step 2: The continuous-time impulse response forms the continuous-time step response which further computes the time pulse response in discrete form by assuming that the input is linked to the sample and hold circuit.

Step 3: Using the deterministic Hoe Kalman algorithm, a state space in discrete realization is generated. The reduced-order A, B, and C matrices from the discrete-time pulse-response sequences in Step 2 are returned by this algorithm. The sorted singular values of the Hankel matrix produced as part of the procedure are used to establish the system's order. The initial value theorem is used to find the D matrix.

Step 4: The state-space system is transformed to the required final form using similarity transformation if necessary.

The discrete-time realization procedure is utilized to generate an optimal reduced-order discrete-time state-space model from these transfer functions so that the constraints of nonlinear optimization approaches can be mitigated. Also, the nonlinear modifications to the linearized model are also offered so that the accuracy of the model can be improved. The DRA method is simulated using octave code and the results are shown in Figs. 6, 7, 8, and 9. The main purpose is to compare the accuracy of the ROM predictions of internal electrochemical variables at different locations in the cell to the "truth" values provided by a pre-computed simulation of the PDE model.

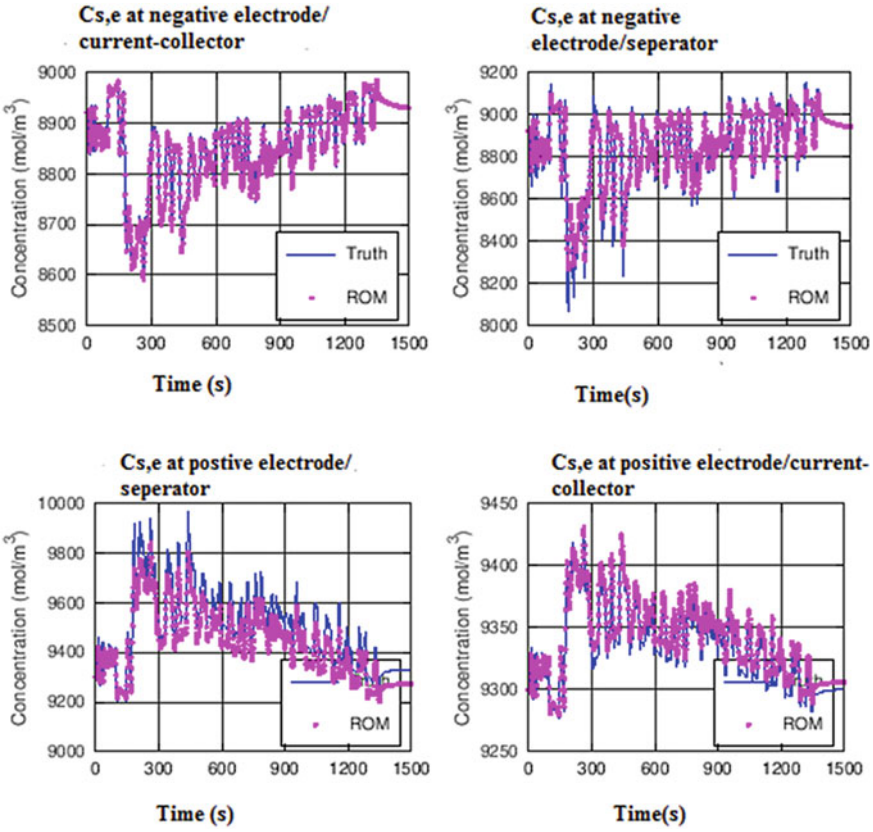

Fig. 5 Solid surface concentration at four locations in the cell

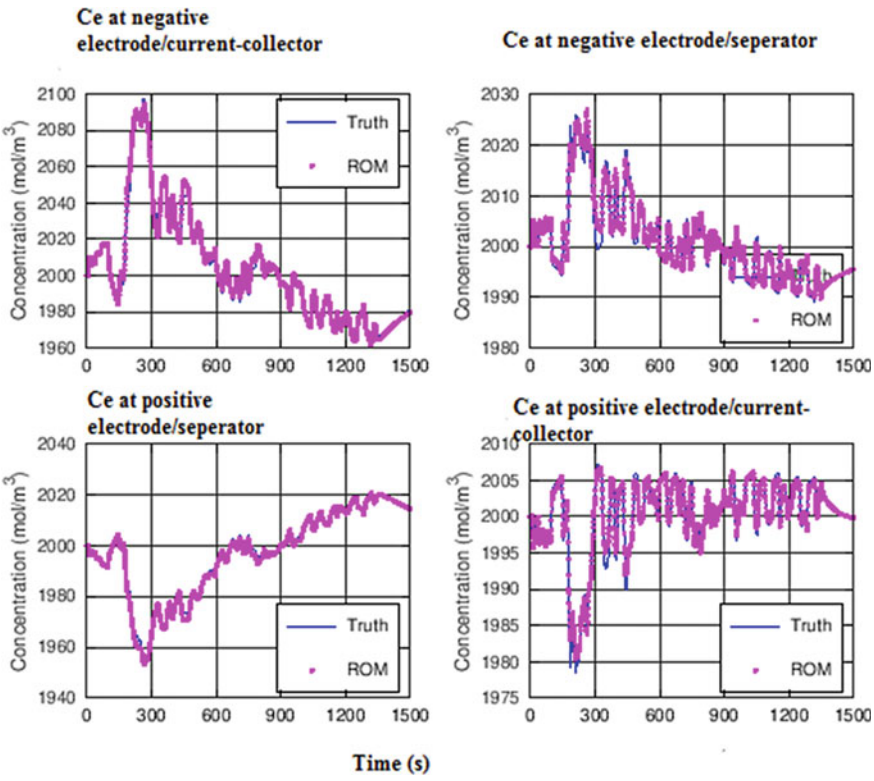

Fig. 6 Electrolyte concentration at four locations in the cell

6 Hybrid Model

ROMs are required for the computation of real-time battery controllers to be efficient. The best control-based ROMs are low-order and preserve electrochemical measures that are important for regulating battery performance and extending battery life. The greatest candidates for producing desired ROMs are physics-based models (PBMs). There are several techniques for creating ROMs from Full Order Models (FOM) each with its own set of advantages and disadvantages.

The comparison of SPM and PBROM is as follows:

- SPM does not provide enough electrochemical data to estimate SOH.
- SPM cannot be used to manage lithium plating since it can't predict local over potential.
- At low SOC and medium to high C-rates, SPM produces poor estimates.

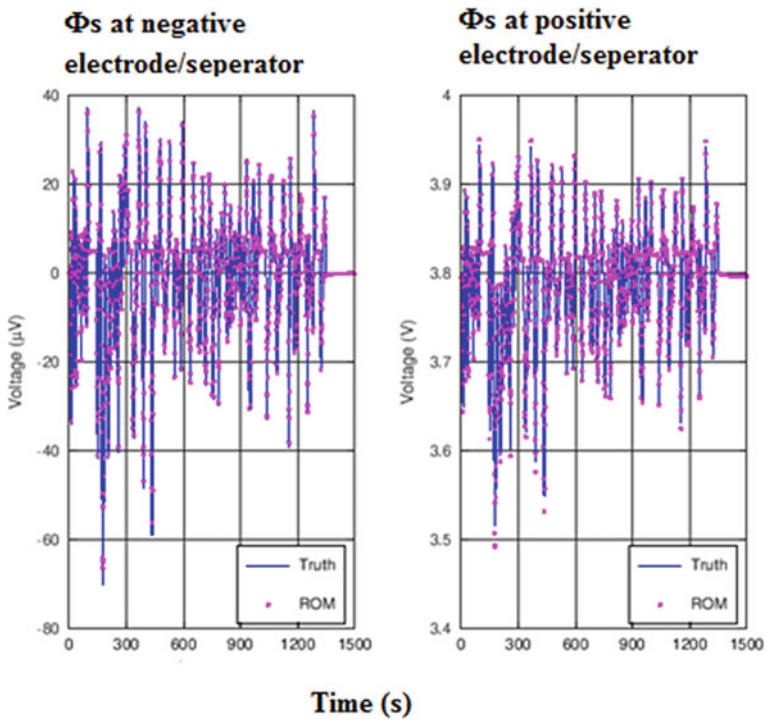

Fig. 7 Solid potential

- Most electrochemical dynamics are preserved in PBROM, although it is computationally heavier than SPM (due to output mixing) and loses accuracy at high C-rates.

It is postulated that the best qualities of SPMs and PBM-ROMs can be combined to create a better SPM known as enhanced SPM (eSPM). SPM accurately depicts concentration profiles throughout particle radius, whereas PBM-ROM catches electrolyte dynamics and electrode-length dependencies that the SPM misses. Combining these features into a single, low-order model could result in improved accuracy with only a little increase in processing cost [20]. The hybrid model is in the theoretical stage and it will be developed further in the future using machine learning algorithms.

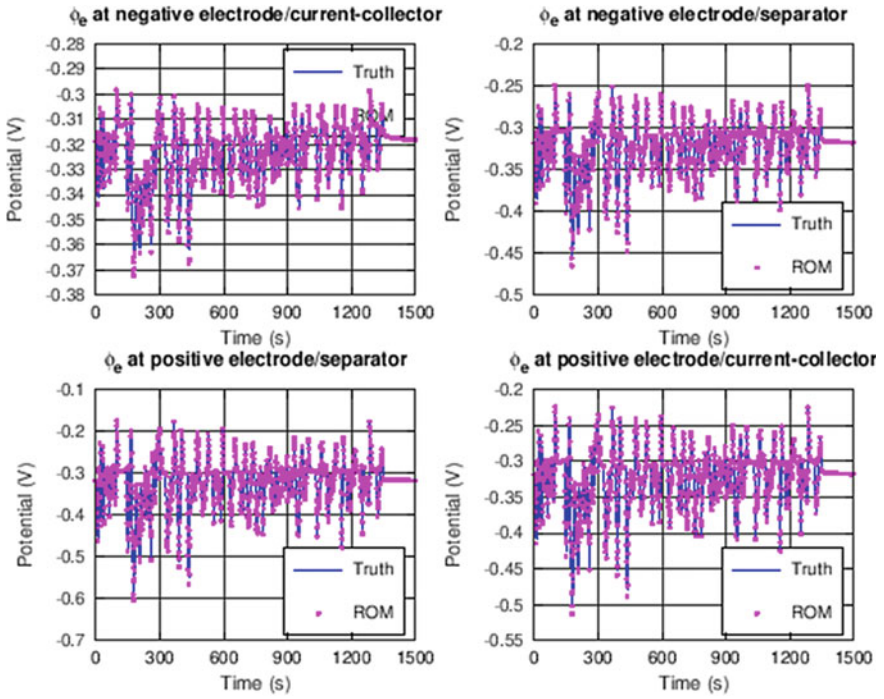

Fig. 8 Electrolyte potential at four locations in the cell

7 Conclusion

There is a need to address the efficient implementation of optimal power controls, tuning the various aging mechanisms of the lithium batteries, and cost considerations. Also, there is a necessity to identify systems that give well-defined physics-based model parameter values, excellent parameterized models of the cells to match the real-time mechanisms occurring within the cell. A lot of research is going on to improve the PBROM for predicting the degradation of the cell. Thus this paper presents a review of existing PBM and future models like hybrid modeling to make the Battery Management systems more accurate.

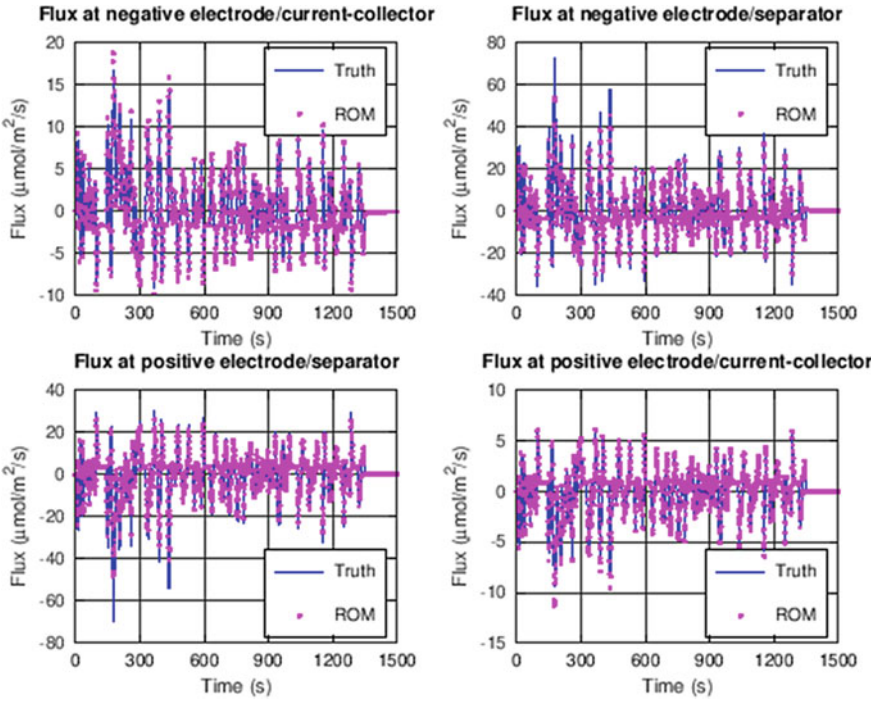

Fig. 9 Flux from solid to electrolyte at four locations in the cell

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A Transformerless High Step up Dual Inductor Based DC-DC Converter for Fast Charging Application

Yash Vardhan Bhargava, R. Aravind, Kashish Noori, Divyakumar Gupta, Sivaprasad Athikkal, and Ravi Eswar Kodumur Meesala

1 Introduction

Pollution due to transportation is a major challenge at present. Air pollution and global warming have triggered a need for sustainable development means of existence [1]. In this regard, researchers have reported that more than 66% of the world's pollution is contributed by thermal plants and conventional transport (CT). More precisely, 24% is credited to CT [2]. Therefore, sustainable alternatives to CT are the dire need of the hour. Electric Vehicles (EVs) have proved to be an effective solution to the transportation problem. Elimination of carbon emissions renders them completely eco-friendly. This has caused a drastic increase in demand for EVs [3]. Apart from this, they can also be integrated with renewable energy sources (RESs) [4]. Despite these advantages, the requirement of longer charging times for EVs is hindering their

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commercial popularity [5]. Consequently, methods that can facilitate electric vehicle fast charging (EVFC) are being rigorously investigated. Figure 1 shows the role of the proposed MDC in the EV charging infrastructure. Multiport DC-DC converters (MDCs) have various advantages such as high gain [5], lower component count [6], ability to interface multiple sources independently [7], and high efficiencies that make them well suited for such applications. A novel three-port converter (TPC) with a non-isolated (NI) structure is reported in [8], which is capable of Single Input Single Output (SISO), Single Input Double Output (SIDO), and Double Input Single Output (DISO) operation. Its advantages are the use of simple buck-boost topologies, etc., and use of single-inductor (SI). Chen et al. [9] discussed the principle of deriving novel topologies based on traditional SISO topologies namely buck, boost, and buck-boost. Multiple Input Multiple Output (MIMO) cells are devised based on inductor current flow. Integration of these cells with the traditional topologies will result in novel converters. Another high-gain novel MDC is proposed in [10], where capacitor—diode voltage multiplier cells have been used. The incorporated four inputs and two outputs converter is fault resistant to contingency faults but used more number of passive components. Researchers in [11], presented an MDC topology, which is developed by integrating buck and super-lift Luo converter. The converter is SIDO type. Positive output super-lift converter is used for step-up mode. The lower number of components is used, while enabling both step-up and down operations. The converter is mostly suited for low power applications. Another novel NI MDC is proposed by authors Elham et al. [12], in which power transfer from all inputs to all other outputs is possible. It has the advantages of high gain and soft switching. Despite the reduction in the number of switching devices, the MDC suffered from high magnetic losses. A DISO novel NI MDC is reported in [13]. The proposed converter is capable of providing high gain and bi-directional operation. An actively switched LC (ALC) circuit for obtaining high output voltage levels is a notable feature. The usage of more number of components is a drawback. Similar to [8], a NI TPC is proposed in [6]. In the research, hard switching is addressed. The converter is capable of generating high output gain, suitable for RES applications. Coupled inductors are used to achieve the high gain. SISO, DISO, and SIDO modes of operation are allowed. Higher number of devices and inclusion of a transformer made the converter bulkier. A group of dual input converters are proposed in [14–17] where the detailed circuit analysis has been explained.

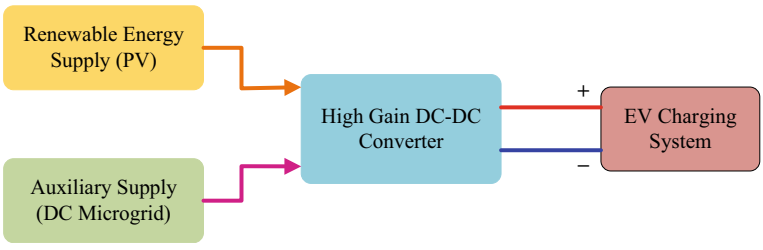

Fig. 1 Introduced MDC in EV fast-charging infrastructure

In this paper, a NI high-gain MDC is presented. The converter utilizes an ALC network along with series-coupled inductors (SCL) in order to attain high output voltage levels. The topology is derived from keeping switching devices to a minimum, to enhance the converter efficiency. The converter allows the interaction of both the voltage sources to the load, which can be varied by variation of switching patterns. The proposed converter has advantages such as high output voltage gain and integration of various energy sources, making them ideal for EV fast-charging applications. Converter topology, modes of operation and static voltage expression, etc. are discussed. The rest of the paper structure is as follows, Sect. 2 designates the projected topology, Sect. 3 presents the modes of operation and the analytical waveforms, and Sect. 4 presents the simulation waveforms and results. Lastly, Sect. 5 concludes the paper.

2 High Gain Non-isolated Converter

The presented converter topology is exposed in Fig. 2. S_1 and S_2 are the two sources or inputs to the converter. The resistor here serves as the load or the output. S_{W1}, $S_{W2,}$ and S_{W3} are the power electronic switches. Whereas D_1, D_2, $D_{3,}$ and D_4 are the power diodes. These provide a freewheeling path and ensure the desired direction of current flow. C_1 and L_a constitute the ALC tank circuit and L_a and L_b together with diode D_1 form the SCL arrangement responsible for high gain. Capacitor C_2 is used to feed the load during isolation from the source. The modes of operation and their mathematical formulation is performed in the forthcoming sections. The proposed boost MDC has four modes of operation for one complete switching cycle as shown in the analytical waveforms given in Fig. 3. The respective modes and the equivalent circuit for each case are described below. Also, the equations for inductor voltage and capacitor current equations are derived in the following text.

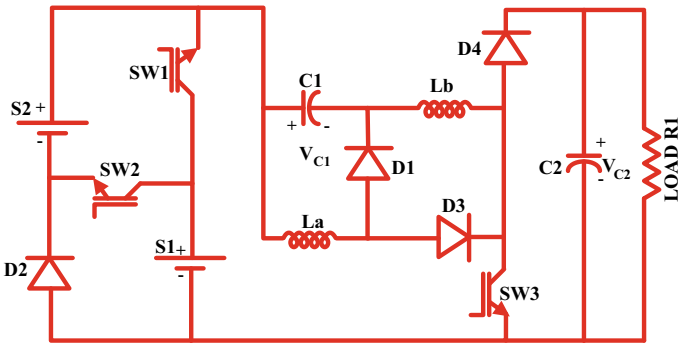

Fig. 2 Circuit diagram for presented converter

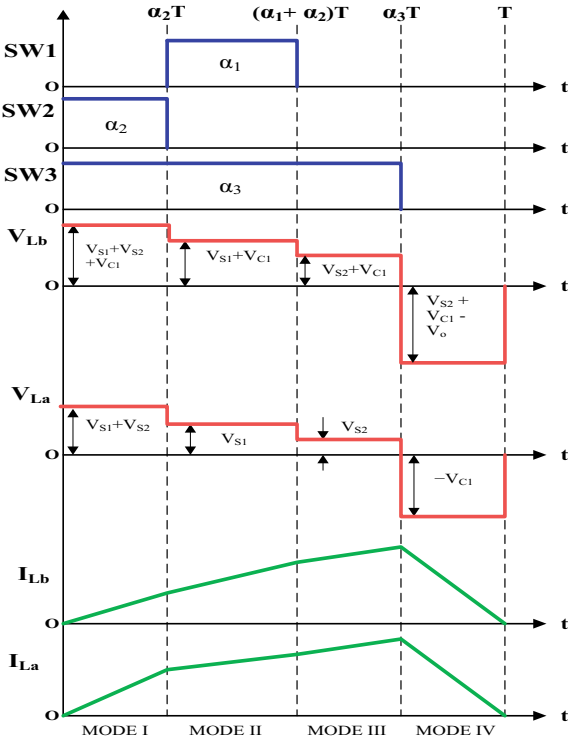

Fig. 3 Analysis waveform for presented converter

2.1 State 1

This state starts at t = 0, when S_{W2} is turned ON, causing both the sources S_1 and S_2 to operate in series and charge the inductors L_a and L_b. Meanwhile, the load is supplied by C_2 and the inductor currents increase further. The current path flow from S_1 and S_2, and flows through C_1 to charge L_b and through L_a, S_{W3}, and D_3. After this mode, L_a is charged to $(V_{S1} + V_{S2})$ and L_b is charged to $(V_{S1} + V_{S2} + V_{C1})$. This mode lasts for $\alpha_2 T$ duration. Figure 4a portrays state 1. The steady-state inductor voltages are described by the following equations.

$$V_{Lb} = V_{S1} + V_{C1} \tag{1}$$

$$V_{La} = V_{S1} + V_{S2} \tag{2}$$

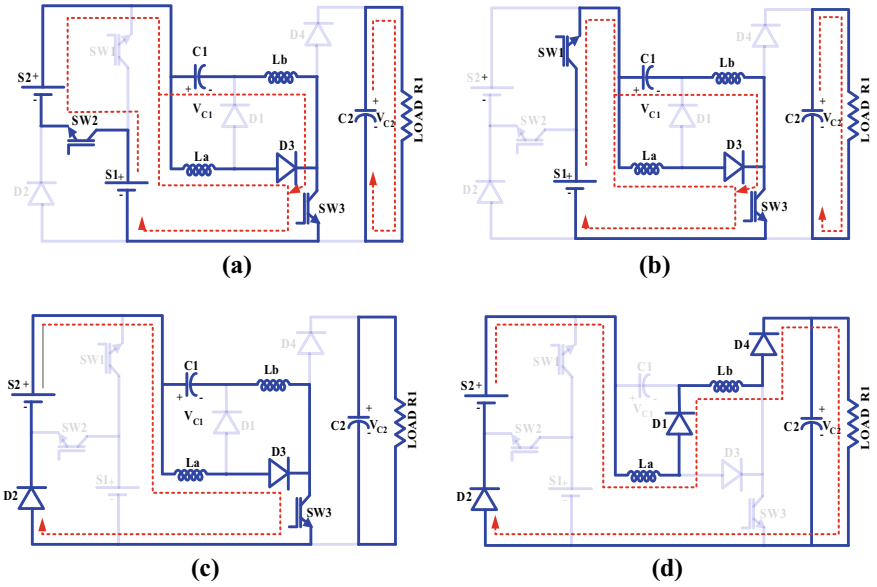

Fig. 4 Working states of the converter **a** state 1 **b** state 2 **c** state 3 **d** state 4

2.2 State 2

In this state, switch S_{W1} and S_{W3} is operated. S_1 charges L_a and L_b with C_1. So, both inductor currents increase with a slope greater than zero. Meanwhile, the load is supplied by capacitor C_2. The current flows from S_1 to L_b and C_1 through S_{W1} and S_{W3}. Meanwhile current flows from S_1 to L_a through S_{W1}, D_3, and S_{W3}. At the end of this state, at $t = \alpha_1 T$, L_a is charged to V_{S1}, and L_b is charged to $(V_{S1} + V_{C1})$. S_{W1} is operated for time $\alpha_1 T$, at a duty cycle of α_1. Figure 4b depicts state 2 operations. By applying KVL, we obtain the expressions for the inductor voltages of both inductors.

$$V_{Lb} = V_{S1} + V_{S2} + V_{C1} \tag{3}$$

$$V_{La} = V_{S1} \tag{4}$$

2.3 State 3

This state begins, when S_{W2} is turned OFF, here the inductor L_a is charged to V_{S2} by source S_2 and inductor L_b is charged to $(V_{S2} + V_{C1})$ by S_2. The inductor currents reach their respective peaks in this state. The current flow from S_2 to L_a through D_3

and S_{W3}, whereas the other flow path, is from S_2 to L_b through C_1 and S_{W3}. This mode lasts for $(\alpha_3 - \alpha_1 - \alpha_2)$T. Only S_{W3} is ON and the load is fed by C_2. Figure 4c depicts this state. The steady-state inductor voltage equations are as follows.

$$V_{Lb} = V_{S2} + V_{C1} \tag{5}$$

$$V_{La} = V_{S2} \tag{6}$$

2.4 State 4

In this state, all switches are in OFF state, S_2 along with inductors L_a and L_b are interfaced to the load through diode D_4. The entire energy accumulated in the previously charging modes appears across the load in the form of high output voltage. C_1 clamps L_a, which causes it to appear in series with L_b resulting in high gain. C_2 is also replenished while the load is supplied. This state lasts for $(1 - \alpha_3)$ T. This is shown in Fig. 4d. The inductor voltage equations for this state are as follows:

$$V_{Lb} = V_{S2} + V_{C1} - V_o \tag{7}$$

$$V_{La} = -V_{C1} \tag{8}$$

3 Analysis of the Converter

In this section, steady-state output voltage expression is derived using Eqs. (1)–(8) of Sect. 2. Further, analytical waveforms for the four modes of converter operation are discussed. This is followed by a software simulation of the proposed converter.

Steady-state output voltage expression:

To derive the output voltage expression, inductor volt-sec balance [14, 15] is employed. According to the inductor volt-sec balance for inductor L_a,

$$[\alpha_1 V_{S1} + \alpha_2(V_{S1} + V_{S2}) + (\alpha_3 - \alpha_1 - \alpha_2)V_{S2} + (1 - \alpha_3)(-V_{C1})] \times T = 0$$

Simplifying, yields V_{C1}

$$V_{C1} = \frac{V_{S1}(\alpha_1 + \alpha_2) + V_{S2}(\alpha_3 - \alpha_1)}{(1 - \alpha_3)} \tag{9}$$

Similarly, for inductor L_b,

$$[\alpha_1(V_{S1} + V_{C1}) + \alpha_2(V_{S1} + V_{S2} + V_{C1}) + (\alpha_3 - \alpha_1 - \alpha_2)(V_{S2} + V_{C1}) + (1 - \alpha_3)(V_{S2} + V_{C1} - V_o)] \times T = 0$$

Simplifying yields

$$V_{S1}(\alpha_1 + \alpha_2) + V_{C1} + V_{S2}(1 - \alpha_1) = (1 - \alpha_3)V_o \tag{10}$$

Now, substituting for V_{C1} gives the expression for V_o

$$V_o = \frac{V_{S1}(\alpha_1 + \alpha_2)(2 - \alpha_3) + V_{S2}(1 - 2\alpha_1 + \alpha_1\alpha_3)}{(1 - \alpha_3)^2} \tag{11}$$

4 Simulation Results

MATLAB/Simulink software has been used for the simulation of the introduced converter. In this section simulation waveforms of all the passive elements, namely. load, inductors, and capacitors along with the power switches and the diodes are presented. Table 1 presents the simulation parameters.

The simulation waveforms of the load voltage and current across R_1 are shown in Fig. 5a. The output voltage obtained across R_1 is 200 V and the current across it is 1.4 A. The corresponding input sources are 24 V for S_1 and 12 V for S_2. The inductor voltage and current waveforms obtained are shown in Fig. 5b, c. The voltage across L_a is 36 V in the first mode, 24 V in the second and 12 V in the third mode. In the last mode, it discharges with a voltage of 48 V. L_b showcases higher voltages than L_a as it is being charged with C_1. The voltage across it is 80 V for the first stage, 66 V for the second, 56 V for the third, and in the final stage, the voltage across it is 150 V. The maximum and minimum currents through L_a were 17.1 A and 16.95

Table 1 Simulation/Experimental parameters

Simulation parameters		
S. No.	Parameters	Specification
1	Input voltages (V_{S1}, V_{S2})	24 V, 12 V
2	Inductor (L_a and L_b)	5 mH
3	Switching frequency (f_s)	20 kHz
4	Duty ratio (D_a, D_b, D_c)	50 and 35%
5	Capacitors (C_1, C_2)	470 μF
6	Output voltages (V_{01})	200 V
7	Load resistors (R_{01})	250 Ω

A respectively. Therefore, the resultant current ripple (peak to peak) was 0.15 A. Similarly, for L_b, the maximum current was 5 A and the minimum current was 4.6 A, yielding a peak-to-peak current ripple of 0.4 A. The voltage and current waveforms for the three switches S_{W1}, $S_{W2,}$ and S_{W3} are presented in Fig. 6a–c. S_{W1} is exposed to a stress of 12 V for the first mode, zero in the second mode, and −12 V for the third and fourth modes. For S_{W2}, it experienced no stress in the first mode, −12 V in the second and −24 V in the third and fourth modes. The third switch S_{W3} is exposed to a stress of 200 V (i.e., V_O), only in the final stage of converter operation. The average current stress through all the switches is 10 A. The voltage and current waveforms for the diodes are shown in Fig. 7a–d. Since diode D_1 conducts only in the final stage, it suffers voltage stresses of 24 V in the first, 12 V in the second and third modes. As D_2 conducts for the third and fourth stages, it is exposed to a stress of −150 V for the initial two stages. Now, as D_3 is in operation for the first three out of four modes, it suffers voltage stresses of 80 V in the first, 66 V in the second, and 56 V in the third mode. Voltage stress across D_4 remains at 200 V till it conducts in the last stage of operation.

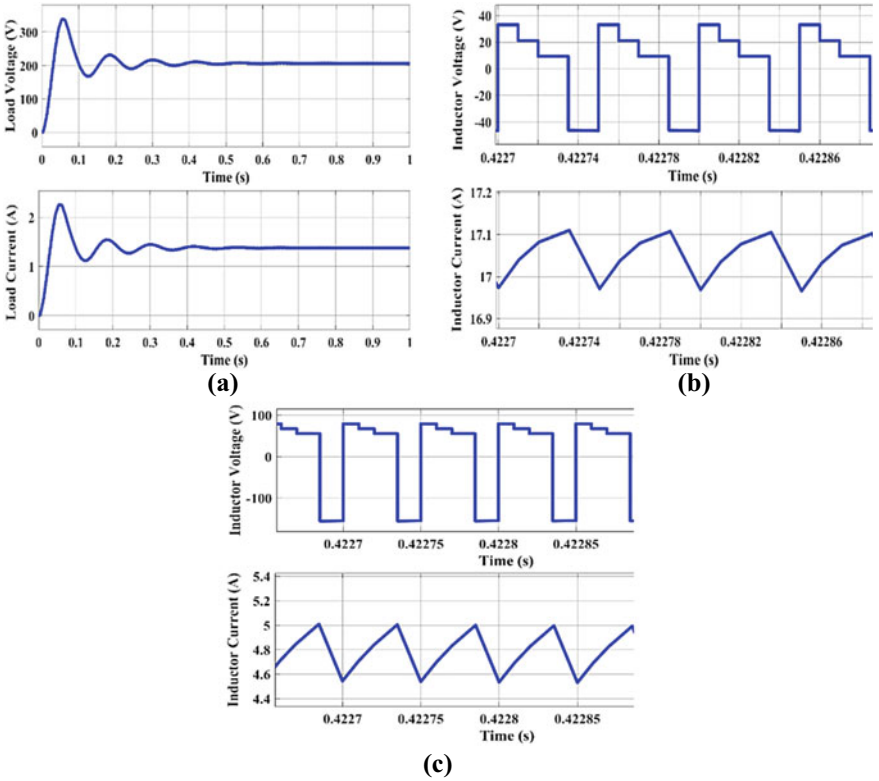

Fig. 5 Simulation waveforms of voltage and current **a** load **b** inductor (L_a) **c** inductor (L_b)

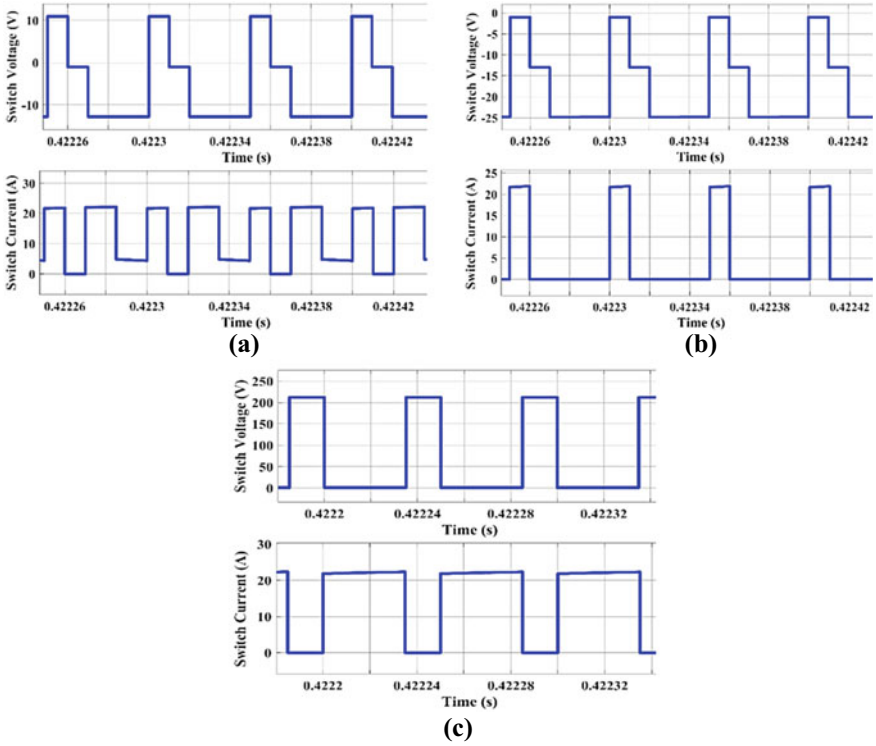

Fig. 6 Simulation waveforms of voltage and current **a** switch S_{W1} **b** switch S_{W2} **c** switch S_{W3}

The variation of output voltage with respect to the duty ratios α_1 and α_2 are displayed in Fig. 8a, b. The graphs show that the converter is well capable to produce higher output voltage even for a duty ratio range of less than 0.8. The comparative analysis of the presented converter is completed in terms of number of components (active and Passive), number of energy sources and ports of output with other projected converter topologies and is cited in Table 2. The disclosed comparison reveals that the presented converter has lower number counts when compared to other different topologies with higher voltage conversion ratio, the possibility to integrate the input sources in series and parallel manner and hence reduces the overall complexity of the circuit.

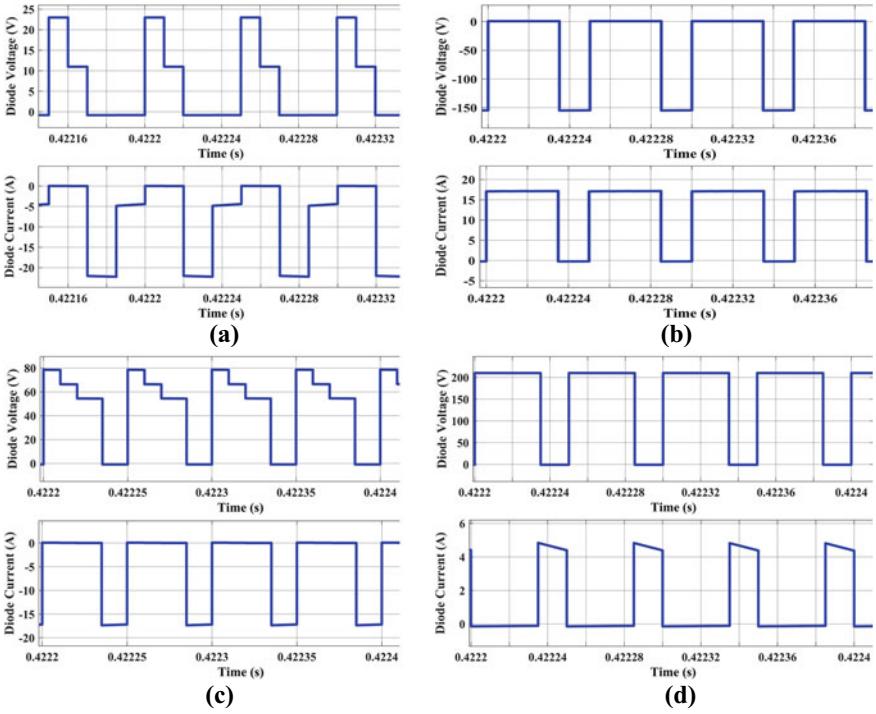

Fig. 7 Simulation waveforms of voltage and current **a** diode D_1 **b** diode D_2 **c** diode D_3 **d** diode D_4

5 Conclusion

A high-gain MDC was presented in this paper. The converter catered to two inputs and one output (DISO). ALC and SLC are employed to achieve high gain at the output port. It has various advantages of high output voltage gain, the capability of interfacing both sources independently, and the absence of electromagnetic components. The topology of the converter is flexible to incorporate a further number of input and output ports. Along with the steady-state output voltage expression, a software simulation of the converter is also performed. The presented converter holds a good voltage conversion ratio when compared to other reported topologies which make it suitable for EV fast-charging application. The reduction of the component count and addition of another port to make the existing converter a TPC are the scope of further works.

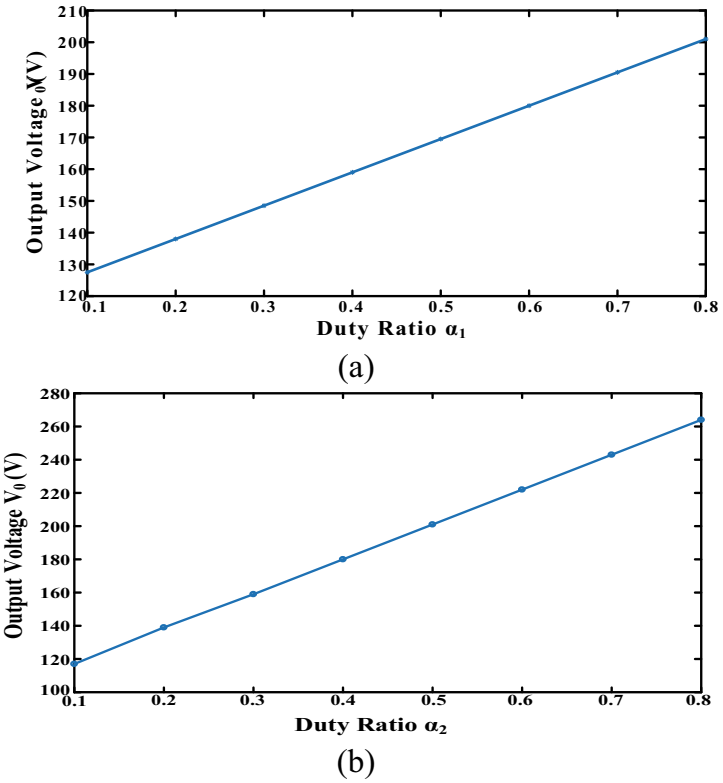

Fig. 8 Output voltage for different duty cycles **a** α_1 **b** α_2 for the presented converter

Table 2 Comparison table with other converters

Component and efficiency comparison					
S. No.	Parameters	Presented converter	[10]	[12]	[14]
1	Switch counts	3	2	2	4
2	Diode counts	4	4	3	0
3	Inductors counts	2	2	3	1
4	Capacitors counts	2	3	4	1
5	Total elements	11	11	12	6
6	Output voltage levels	1	1	1	1
7	Input Sources	2	2	2	2
8	Possibility of series operation of the input sources	Yes	No	No	Yes
9	Voltage conversion ratio	High	Medium	High	Low
10	Reported efficiency (%)	97.8	96.82	95.9	94

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A High Efficiency Isolated Bidirectional Reduced-Switch DC-DC Converter for Electric Vehicle Applications

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1 Introduction

Bidirectional converters are essential for a wide variety of applications such as electric vehicles that require power flow from source to load and vice versa [1–4]. They also provide a flexible power processing interface for such recent steadily emerging electric automotive systems [5–7]. A typical bidirectional DC-DC converter system has a full bridge power stage on one side, which is isolated from another full bridge power stage on the other side, by a linear transformer preferably operating at high frequency [8]. Such High-Frequency Transformers (HFTs) provide galvanic isolation, which is a mandatory standard for many multi-source systems, as it ensures personnel safety, noise reduction, and proper operation of protection systems [9], by preventing system transients at one side of the circuit from passing to the other side. Floating inputs and outputs of such isolated converters are beneficial for multiple applications, as voltages and currents can be drawn from either side of the circuit since they have separate ground connections.

Dual Active Bridge Converters (DABC) are the most commonly used DC-DC converters due to their high reliability. But they have disadvantages like high device stresses and considerable switching losses, as they have a total of 8 switches together in the front-end and back-end H-bridges. Several researches were done to develop an efficient isolated bidirectional converter topology with reduced components. Comparisons were made among several common isolated bidirectional converters [10, 11] based on their volume, weight, failure rate, efficiency, and reliability. It was found that an isolated bidirectional half bridge converter is the best choice. But

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even with a half bridge topology, the converters required a large number of switches, inductors, capacitors, and even transformers.

Topologies were developed for high-power density and high-frequency applications with integrated inductors and capacitors [12–15], and with interleaved structures [16–18]. However, this scenario has imposed challenges such as high switching losses, high degradation of inductance and capacitance, and potentially large voltage imbalances across the components. Matrix transformer integrated bidirectional converter topologies were also designed in some works [17, 19–21], but they have the disadvantage of a complex architecture. In some other works, although soft switching was achieved for half bridge structures with small signal analysis of Zero Voltage Switching (ZVS) topologies [22, 23], the size and volume of the converters were huge due to the use of several large inductors. Also, such resonant converters have the disadvantage of requiring additional inductances to account for leakage of the linear transformers used in them. Some simpler half bridge DC-DC converter structures were also developed for bidirectional power flow, but instead of using an isolating transformer, inductors were used to connect the two half bridges on either side [14, 24]. Thus, galvanic isolation was missing in the structure. A most recent topology for isolated bidirectional converters was modeled with built-in filters [1]. But the structure required 2 linear transformers which add to the size, volume, and cost of the model.

In this work, a new topology for an isolated bidirectional DC-DC converter is presented, with high efficiency and a reduced number of switches in a bridge structure. It requires only a single switch each in the front-end and back-end H-bridges. Compared to conventional bidirectional converters, the converter proposed in this paper is more advantageous with its less number of switches, naturally simplifying the driving and control circuitry also. An HFT is used for isolation, the primary of which is connected across the front-end H-bridge and the secondary is connected across the back-end H-bridge.

This paper consists of the following sections: Sect. 2 describes the proposed circuit configuration and design, Sect. 3 describes the different modes of operation of the converter, Sect. 4 consists of the simulation results obtained, Sect. 5 gives comparable results to a recent similar topology, and finally, Sect. 6 gives a conclusion of the paper.

2 Proposed Configuration

2.1 Circuit Diagram

The circuit diagram of the novel Isolated Bidirectional Reduced-Switch Converter (IBRSC) structure consists of a single transformer, two H-bridges, and a single DC source ‘Vin’ as shown in Fig. 1. The primary winding of the isolation transformer is connected across the front-end H-bridge, and the secondary winding of the transformer is connected across the back-end H-bridge.

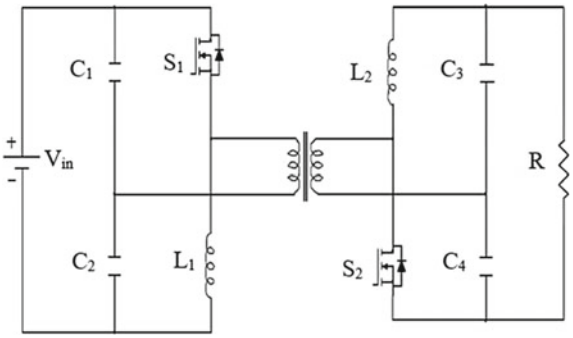


Fig. 1 Circuit diagram of the proposed IBRSC

The front-end H-bridge consists of a switch 'S_1' and an inductor 'L_1' on one leg, and two capacitors 'C_1' and 'C_2' on the other leg. Similarly, the back-end H-bridge also consists of a switch 'S_2', an inductor 'L_2', and two capacitors 'C_3' and 'C_4'. A PET is used for the isolation of the two bridges.

2.2 *Design of Components*

All the components were designed for the converter to operate in Continuous Conduction Mode (CCM); that is, the DC component of the current is assumed to be always greater than the peak of the current ripple [23]. This is because, CCM is more advantageous in terms of reducing the peak and RMS currents of the system for the same output power, and thereby helps in achieving higher efficiencies.

Inductor Design

Inductor design was done based on current ripple calculation [25]. In this topology, a current ripple of 3% through the inductor is assumed to be tolerated [26]. Here, $L_1 = L_2 = L$, since voltage and current through both the inductors are equal.

Based on current ripple calculation, inductor current ripple is given as

$$\Delta i_L = \frac{(V_{in} - V_{out}) \times D \times T}{L} \tag{1}$$

where 'ΔiL' is the maximum peak of inductor current ripple (in Amperes), 'L' is the inductance value (in Henry), 'V_{in}' is the input voltage (in Volts), 'V_{out}' is the output voltage (in Volts), 'D' is the duty ratio, and 'T' is the time period (in seconds).

Capacitor Design

Capacitor design was done based on voltage ripple calculation [25]. Here $C_1 = C_2 = C_3 = C_4 = C$, since the input and output currents of the converter are the same.

Considering a conventional value of 75 mV [26] as the maximum peak of voltage ripple, the capacitor design equation is

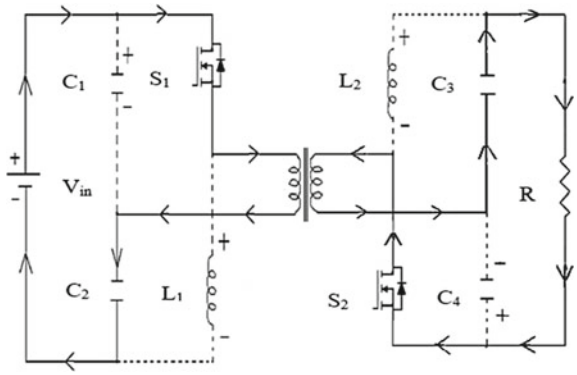


Fig. 2 Mode 1

$$C = \frac{I_{out} \times D \times (1 - D) \times 1000}{f \times V_{pmax}} \tag{2}$$

where 'C' is the capacitance (in microfarads), 'I_{out}' is the output current (in Amperes), 'D' is the duty ratio, 'f' is the frequency (in kilohertz), and 'V_{pmax}' is the maximum allowable peak ripple voltage (in Volts), assumed to be a conventional value of 0.075 V.

3 Modes of Operation

There are four modes of operation for the novel converter in the powering cycle.

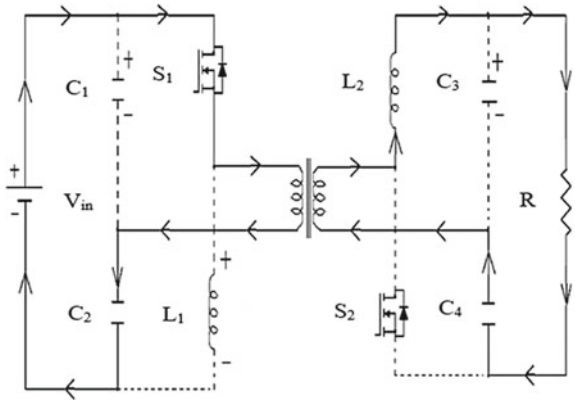
3.1 Mode 1

The mode 1 of the converter where both the switches 'S_1' and 'S_2' are switched ON is shown in Fig. 2. In the primary side of the transformer, capacitor 'C_1' and inductor 'L_1' charges, while capacitor 'C_2' discharges. In the secondary side of the transformer, inductor 'L_2' and capacitor 'C_4' charges, while capacitor 'C_3' discharges.

3.2 Mode 2

Mode 2 of the converter where switch 'S_1' is ON and switch 'S_2' is OFF is depicted in Fig. 3. In the primary side of the transformer, capacitor 'C_1' and inductor 'L_1'

Fig. 3 Mode 2

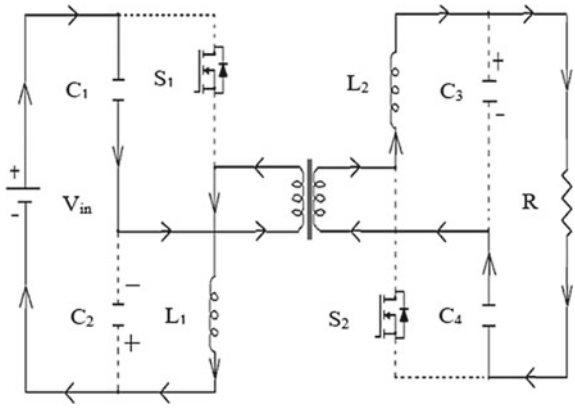


charges, while capacitor 'C_2' discharges. In the secondary side of the transformer, inductor 'L_2' and capacitor 'C_4' discharges, while capacitor 'C_3' charges.

3.3 Mode 3

Mode 3 of the converter where both the switches 'S_1' and 'S_2' are switched OFF is shown in Fig. 4. In the primary side of the transformer, capacitor 'C_1' and inductor 'L1' discharges, while capacitor 'C_2' charges. In the secondary side of the transformer, inductor 'L_2' and capacitor 'C_4' discharges, while capacitor 'C_3' charges.

Fig. 4 Mode 3



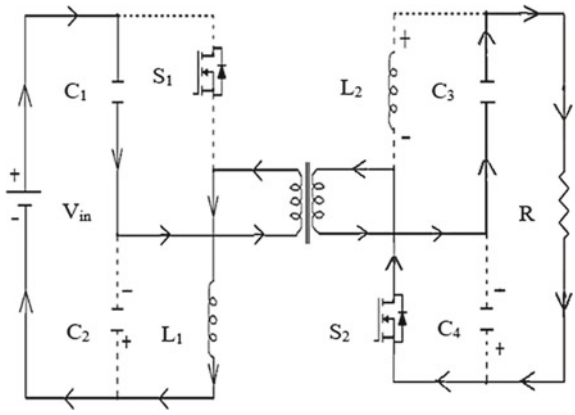


Fig. 5 Mode 4

3.4 Mode 4

Mode 4 of the converter where switches 'S_1' is OFF and 'S_2' is switched ON is shown in Fig. 5. In the primary side of the transformer, capacitor 'C_1' and inductor 'L_1' discharges, while capacitor 'C_2' charges. In the secondary side of the transformer, inductor 'L_2' and capacitor 'C_4' charges, while capacitor 'C_3' discharges.

When the load side voltage becomes higher than the source side, the converter enters into a regeneration mode of operation in the same 4 modes with reverse power flow from the load to the source. Thus, in the powering modes or forward power flow modes, IBRSC acts as a buck converter, and in the regenerative modes or reverse power flow modes, IBRSC acts as a boost converter. Hence, IBRSC is realized with bidirectional power flow in a bridge structure with just two switches.

4 Simulation Results

To verify the structure and working of the designed converter, the topology was simulated using MATLAB/Simulink and the results were studied.

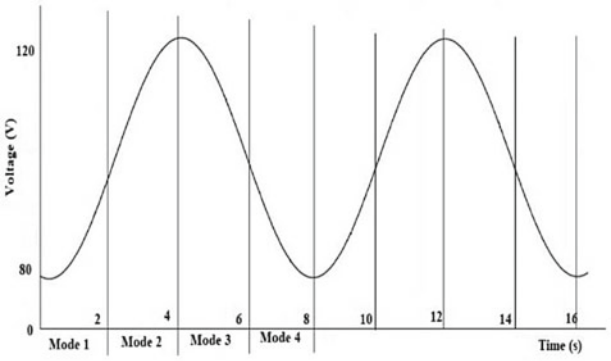
Converter specifications like input voltage, switching frequency, load resistance, duty ratios ('D_1' is the duty ratio of the switch S_1 and 'D_2' is the duty ratio of the switch S_2), etc. used for the simulation are given in Table 1. The design values of the inductors and capacitors were calculated using Eqs. (1) and (2).

The graphs obtained for voltages across the four capacitors C_1 ('V_{C1}'), C_2 ('V_{C2}'), C_3 ('V_{C3}'), and C_4 ('V_{C4}') are shown in Figs. 6, 7, 8, and 9 respectively. Also, the currents through the two inductors L_1 ('I_{L1}') and L_2 ('I_{L2}') are shown in Figs. 10 and 11, respectively. The charging and discharging operations of all the capacitors and inductors are seen accordingly in the corresponding four operating modes.

The novel DC-DC converter topology can be designed for three applications; 'Isolation' mode, 'Buck' mode, and 'Boost' mode operation.

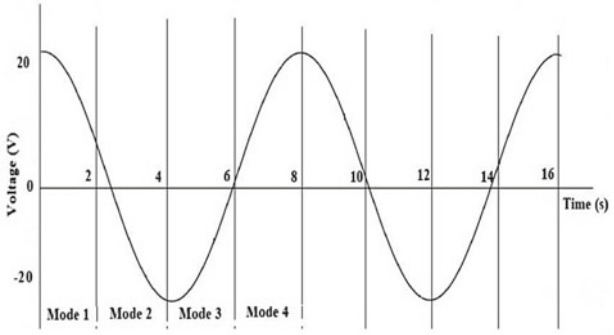
Table 1 Simulation parameters

Specification	Value
Input voltage (V)	100
Switching frequency (kHz)	100
Power rating (kW)	2
Duty ratio D_1: D_2	0.5: 0.5
Load resistance (Ω)	50
Inductors (mH) ($L_1 = L_2$)	8.29
Capacitors (μF) (C1 = C2 = C3 = C4)	66.66



Modes	State of C_1
1	Charging
2	Charging
3	Discharging
4	Discharging

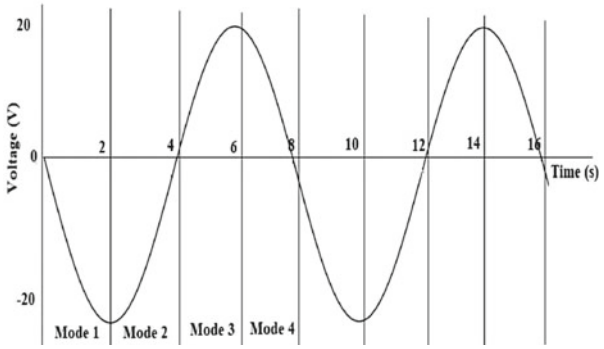
Fig. 6 Voltage across capacitor C_1



Modes	State of C_2
1	Discharging
2	Discharging
3	Charging
4	Charging

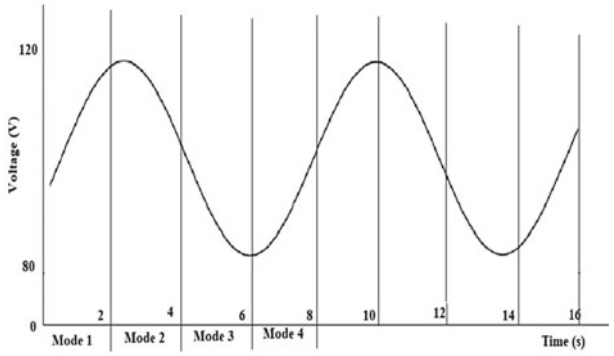
Fig. 7 Voltage across capacitor C_2

In isolation mode operation, the input voltage is transferred to the output side without any stepping up or stepping down. This is obtained when the duty ratio of both the switches is 0.5; that is, $D_1 = D_2 = 0.5$, where 'D_1' is the duty ratio of switch S_1 and 'D_2' is the duty ratio of switch S_2. This means that for 50% of the total time period 'T', switch S_1 is ON, and for the other 50% of T, switch S_2 is turned ON.



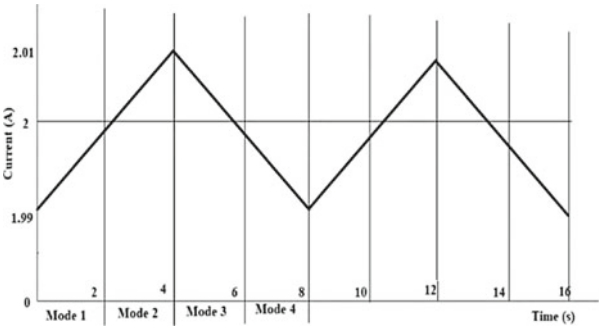
Modes	State of C_3
1	Discharging
2	Charging
3	Charging
4	Discharging

Fig. 8 Voltage across capacitor C_3



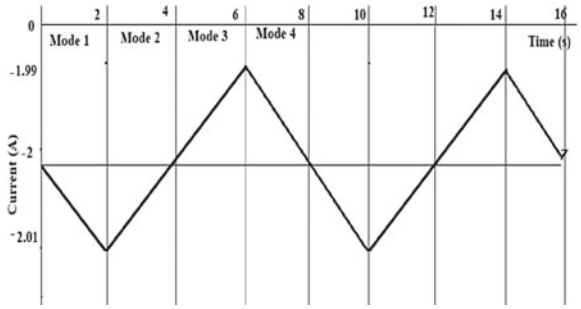
Modes	State of C_4
1	Charging
2	Discharging
3	Discharging
4	harging

Fig. 9 Voltage across capacitor C_4



Modes	State of L_1
1	Charging
2	Charging
3	Discharging
4	Discharging

Fig. 10 Current through inductor L_1



Modes	State of L_2
1	Charging
2	Discharging
3	Discharging
4	Charging

Fig. 11 Current through inductor L_2

In isolation mode, the output voltage is obtained to be equal to the input voltage applied. In buck mode operation, the voltage applied at the input side is reduced at the output side; that is, the voltage is stepped down at the output. This can be obtained by keeping the duty ratio of switch S_1 less than that of switch S_2; that is, $D_1 < D_2$, which means that the switch S_1 is kept ON for a time less than that of S_2 out of the total T. In boost mode operation, the applied voltage is boosted to a higher voltage at the output side. This can be obtained by keeping the duty ratio of switch S_1 greater than that of switch S_2; that is, $D_1 > D_2$, which means that the switch S_1 is kept ON for a time higher than that of S_2 out of the total T. This variation in the ratio of output voltage to input voltage obtained versus duty ratios applied to the two switches is depicted in Fig. 12.

The values of output observations obtained from the simulation of the converter in the three modes: isolation, buck, and boost are given in Table 2. Isolation mode was obtained with the duty ratios D_1: $D_2 = 0.5$: 0.5, buck mode was obtained with

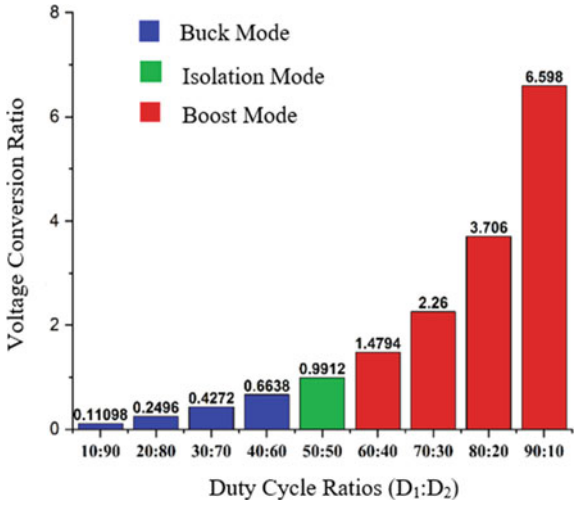


Fig. 12 Voltage conversion ratio versus duty cycle ratios

Table 2 Output observations

Specification	Isolation mode	Buck mode	Boost mode
Output voltage (V)	99.58	64.86	148.81
Output current (A)	1.99	1.29	2.97
Input current (A)	1.99	0.85	4.46
Efficiency (%)	99.38	98.47	99.07

Table 3 Calculated parameters

Specification	Value
Output voltage ripple (%)	5.308
Output current ripple (%)	5.494
Inductor current ripple (%)	3.016
Capacitor voltage ripple (mV)	59.94

the duty ratios D_1: $D_2 = 0.4$: 0.6, and boost mode was obtained with the duty ratios D_1: $D_2 = 0.6$: 0.4.

Efficiency ('η') is calculated as

$$\eta = \frac{V_o \times I_o}{V_{in} \times I_{in}} \times 100\% \tag{3}$$

where 'V_o' is the output voltage, 'I_o' is the output current, 'V_{in}' is the input voltage, and 'I_{in}' is the input current. From the output observations given in Table 2 and Eq. (3), efficiencies of the converter in all 3 modes were validated and were found to be satisfyingly high.

The calculated values of important parameters like current and voltage ripples of the converter in isolation mode are given in Table 3. The output voltage and current ripples of the converter were also found to be very small values of around 3–5%, which is tolerable [10]. The inductors were designed for a current ripple of 3%, and the capacitors were designed for a maximum ripple voltage (V_{pmax}) of 75 mV. From the simulations, the obtained inductor current ripple was 3.01%, and the capacitor voltage ripple value was around 60 mV. Both ripples were within the tolerance level [25, 27], thereby validating the design.

5 Comparison Results with a Recent Similar Topology

Dual-Active-Half-Bridge (DAHB) converters are the most recently developed isolated bidirectional DC-DC converters to be used for EV applications. One such recent design is a DAHB with built-in filters realized with features like high-power

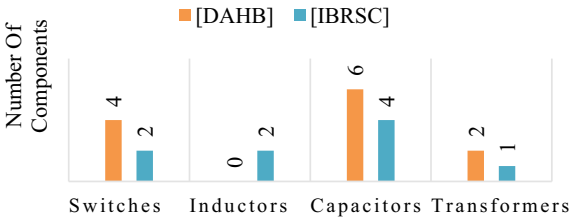


Fig. 13 Comparison of the number of components of IBRSC with the DAHB converter

density, high-power efficiency, and low noise performance [1]. This topology is compared against the novel IBRSC presented in this paper.

A comparison between the number of components used in the DAHB converter and in this novel IBRSC is shown in Fig. 13. It is seen that the number of switches and capacitors required for the DAHB converter is higher than that required for IBRSC. IBRSC requires two additional inductors when compared to the DAHB converter, but it requires only a single transformer whereas the DAHB converter requires two transformers. Transformers add hugely to the weight, cost, and complexity of a converter. Thus, in overall, it can be concluded that IBRSC is more advantageous than the DAHB converter, when considering the number of components required for realizing the topologies.

A comparison of the efficiencies of both the topologies in boost mode, isolation mode, and buck mode is shown in Fig. 14. It is seen that except in buck mode, IBRSC always has a higher efficiency than the DAHB converter, and in buck mode, both the converters have a very high efficiency close to 99%. In boost mode, the efficiency of IBRSC is found to be significantly higher than the DAHB converter. This is because the dual active bridge converter uses 8 switches and its corresponding driver and control components in its circuitry, and hence boosting up of the input voltage by maintaining high efficiency is difficult to attain.

A comparison between the input voltage required for a defined output for both the converter topologies is shown in Fig. 15. It is seen that for all the four different output voltage levels considered, IBRSC always requires a lesser input voltage for obtaining the required output voltage.

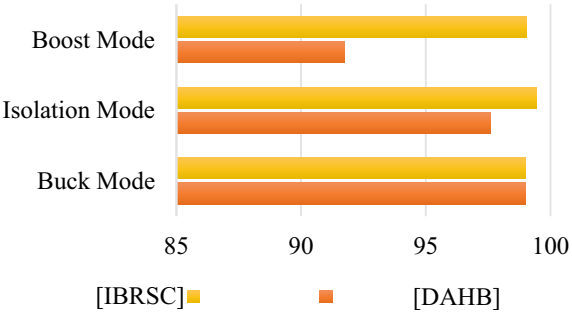


Fig. 14 Comparison of efficiencies of IBRSC and [1] in all three modes of operation

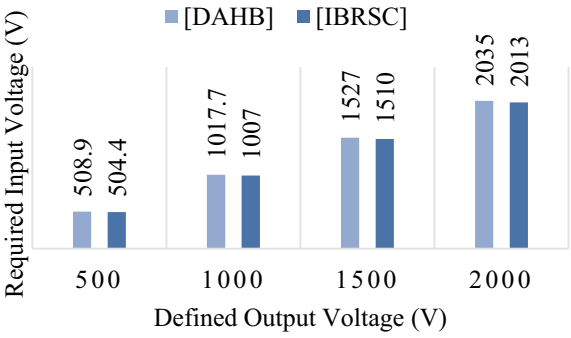


Fig. 15 Comparison of input voltage required for a defined output for both the topologies

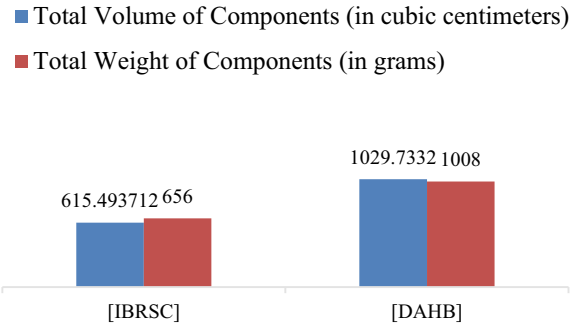


Fig. 16 Comparison of total volume and weight of the components required for both the topologies

A comparison between the total volume and weight of all the components used for realizing both the converter topologies is shown in Fig. 16. It is clearly seen that IBRSC has a way smaller volume and weight when compared to the DAHB converter.

6 Conclusion

In this paper, a new topology for an isolated DC-DC converter is presented with a dual bridge structure, having just one switch, two capacitors, and an inductor each in the front-end and back-end H-bridges, along with a high-frequency transformer for isolation of the bridges. Simulations were done to verify the structure and working of the converter. The converter showed more than 98% efficiency in isolation, buck, and boost operations, with very low voltage and current ripple values of less than 5%. A comparison study of the proposed converter (IBRSC) with a recent similar half bridge converter topology (DAHB) was also done which showed the benefits of the proposed topology. It was seen that the number of components of the proposed converter is way lesser, thus helping in simplifying the driver and control circuitry. An efficiency comparison of the two topologies showed that the proposed topology has

very high efficiency in buck, boost, and isolation operating modes, whereas DAHB has lesser efficiencies in boost and isolation modes. The input voltages required to produce a definite output voltage are also found to be lesser for the proposed IBRSC. Finally, a comparison of the total volume and weight of the components required for both the topologies also showed that the proposed topology is more advantageous.

As a future work, efforts can be made to design an efficient high-frequency transformer for the proposed isolated converter. Emerging technology like planar transformers can be incorporated into this design to further reduce the practical losses of the converter. The design of a simple driver and control circuitry for this reduced-switch topology can also be attempted to further analyze the converter.

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Comparative Analysis of Resonant Converter Topologies for Multiple Load Light Emitting Diode Applications

Aswini Patakamoori, Ramanjaneya Reddy Udumula, Tousif Khan Nizami, and Ravi Eswar Kodumur Meesala

1 Introduction

Lighting loads consume nearly 20% of the total electrical energy generated every year across the globe [1]. Electrical energy can be saved with the effective use of lighting sources. Therefore, traditional lighting sources such as incandescent lamps and fluorescent lamps are being replaced by LEDs which have several advantages such as high luminous intensity, long life span, compact size, environment friendly, and controllable in both color and light [2, 3]. LED driver circuit is a significant component in LED systems in order to provide a constant power supply to lamps [4, 5]. The driver circuits can be AC fed or DC fed based on the availability of an electrical input source [6–8]. Numerous works can be found in the literature related to AC fed LED driver circuits with effective input current regulation, Power Factor Correction (PFC), and improved dimming characteristics [9–25].

DC power distribution improves the efficiency and reliability of the system by eliminating AC to DC conversion stage, which is more significant in LED lighting systems. Hence, DC-DC converter topologies are finding wide interest in LED lighting technology. Various conventional DC-DC converter topologies are given

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in [26, 27]. Here the converters are classified as (i) non-isolated and (ii) isolated converter topologies. Non-isolated topologies presented in [28–34] achieve high efficiency and good dimming characteristics with high voltage gain. High-power LED driver circuits require galvanic isolation to prevent direct current flow between input and output to avoid electric shock. The isolated converter topologies discussed in [35–40] are able to provide galvanic isolation between input and output with improved efficiency and wide range dimming. The size of the LED driver should be compact subjected to low-cost requirements [41]. When these non-isolated and isolated topologies are designed for high-power applications, the size of passive components is more, which results in the bulk size of the converter and more losses. The size of passive components can be reduced by increasing the switching frequency of the devices. But the high frequency of switching devices creates high device stresses and high Electro Magnetic Interferences [EMI] [42]. This will reduce the efficiency of the LED driver circuit.

To overcome these disadvantages, soft switching converters are attracting more attention in high-power LED applications, such as street lighting and industrial lighting [43, 44]. These converters enable Zero Voltage Switching (ZVS) and Zero Current switching (ZCS). The ZVS turn on and ZCS turn off of switching devices reduce the switching losses in the driver circuit. This helps in attaining high efficiency, high frequency of operation, high-power capability, and high reliability [45].

Resonant converter topologies are categorized mainly into three types [46], based on the number of elements in the resonant tank as (i) Two-element resonant converters, (ii) Three-element resonant converters, and (iii) Multi-element resonant converters. Two-element converters such as Series Resonant Converter (SRC) [47–51] and Parallel Resonant Converters (PRC) [52, 53] are simple topologies with simple operation and analysis. But these topologies are not suitable for high-power applications as SRC cannot control the output voltage at no load condition and is not able to supply output voltage greater than input voltage making it suitable for step-down applications. Whereas PRC exhibits poor current regulation and is less efficient in light load conditions [54, 55]. To overcome the limitations of two-element resonant converter topologies, three-element resonant converter topologies are developed [56]. There are 36 different configurations in three-element resonant converter topologies [57, 58]. Among all those LLC, LCC, CLL, and LCL are the most popular topologies [59–68]. Multi-element resonant converters consist of more than three elements in a resonant tank. But the increase in the component count can increase the complexity of the system. Hence, multiple element resonant converter applications are limited [69].

Three-element resonant converters found more interest in LED driver applications due to improved features over SRC and PRC. A high-frequency resonant LLC converter proposed for LED driver applications in [70] achieved an efficiency of 87% with high-power density. A high voltage gain single-stage LLC converter presented in [71] is well suitable for automobile applications. The reduced component count of the converter with an integrating switch between two parts of the converter decreased the cost of the converter. This converter gives an efficiency of 92% at full load. A coupled inductor-based buck LLC converter is presented for automotive applications

in [72]. The passive resonant circuit enables soft switching. Charging the capacitor up to an input voltage during the resonance reduced the voltage stress of the components. The Buck-Boost LLC converter presented for automobile applications in [73] operates in a wide voltage range. ZVS for both primary side and secondary side switches is obtained through an optimized dual-phase shift modulation technique.

The two-stage resonant converter presented in [74] with a buck converter at the first stage and CLL resonant converter working at the series resonant frequency achieved a high-efficiency operation for a wide load range. This converter gives superior current balance with a magnetizing inductance in an unbalanced load condition. The dimming feature is obtained easily with the regulation of the first stage. A multiple load LED driver presented in [75] contains the CLL converter in the primary side of the transformer and charge balance capacitors in the secondary of the transformer. This topology eliminates the use of magnetic components and achieved ZVS turn on of primary side switching devices and ZCS turn of secondary side switching devices. This topology obtained a good current balance in each LED. A CLCL DC-DC resonant converter proposed for two-stage LED driver system in [75] achieves ZVS turn on and quasi ZCS turn off. The optimal design considerations provide good soft switching performance and reduced voltage stress of the switching devices.

A Half bridge LED driver circuit with variable inductor control presented in [76] allows independent current control of multiple LED arrays for providing inherent open circuit and short circuit protection. A Half Bridge LED driver circuit proposed in [77] reduced the conduction losses with asymmetrical secondary windings of the transformer and switching losses with optimized dead time interval. In a full bridge resonant converter [78], the LED lamp is supplied by two series-connected voltage sources. The converter achieved ZVS which resulted in the reduction of switching losses and improved efficiency. The lamp current is controlled by center tapped rectifier in this driver circuit. In high-power applications, multiple loads are being used to achieve high luminous intensity. Many resonant converters topologies are presented for multiple load LED lighting applications in recent years.

This article presents the comparison of a few multiple load resonant converter topologies proposed for street lighting, automotive lighting, and smart lighting applications. The simulation results for a few full bridge topologies to realize the performance of soft switched converters. The article is organized as follows; Sect. 2 explains the classification of LED driver topologies based on input electrical source. The operation principle of the converters is discussed in Sect. 3. Section 4 includes extensive simulation results performed for a few soft switched full bridge LED driver topologies and performance comparison of topologies. Finally, the performances have been evaluated and conclusions are drawn in Sect. 5.

2 Classification of LED Drivers

The LED driver topologies can be classified into three groups based on the nature of the electrical input source, as AC fed LED drivers, DC fed LED drivers, and PV or battery fed LED drivers (Fig. 1).

In passive AC fed LED drivers, the LED current is regulated simply through passive components such as series resistors, coupled inductors, and coupled capacitors. The operation of these circuits is simple; however, the massive size of the passive components results in less efficiency and poor power factor. The limitations of passive topologies are overcome by switched mode AC fed LED driver topologies. These topologies give controlled current regulation, Power Factor Correction (PFC), and shock prevention with isolation between input and output.

Single-stage switched mode AC fed LED driver topologies are suitable for low-power applications, since the AC-DC conversion circuit itself performs PFC and current regulation. This does not provide satisfactory PFC. On contrary, in two-stage switched mode AC fed LED driver topologies, PFC is performed in the first stage and the second stage is designed for current regulation. This improves the reliability and power capability of these converters. The increased component count constrained the

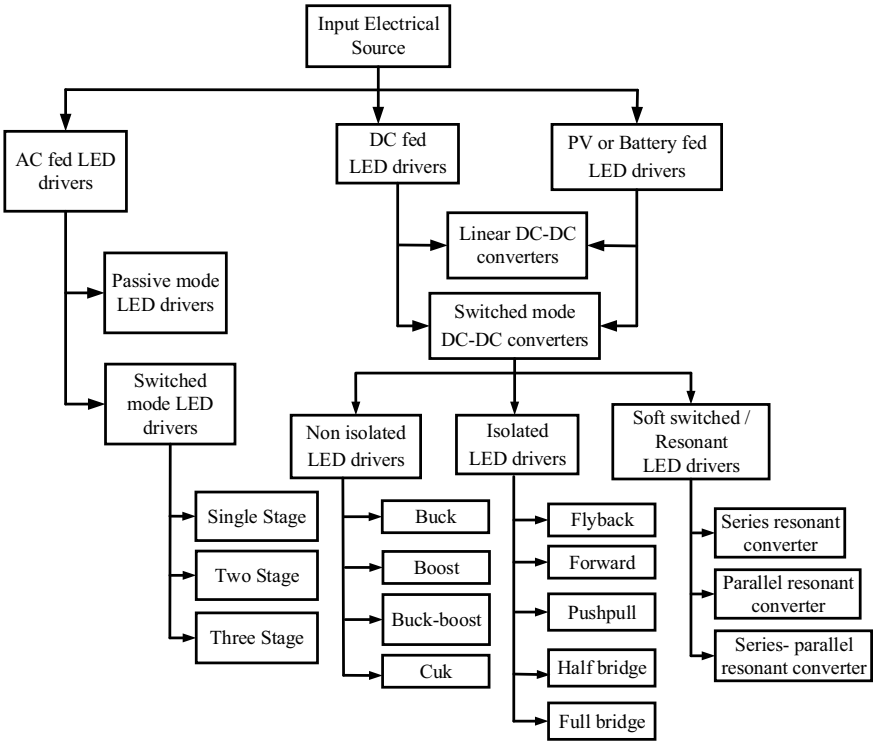

Fig. 1 Classification of LED drivers

application of two-stage topologies. To hammer this limitation, the PFC and DC-DC conversion stages are integrated into integrated two-stage switched mode AC fed LED driver topologies. But in the case of multiple LED load applications, galvanic isolation is required. Hence, three-stage topologies are introduced with galvanic isolation in the first stage, and the remaining two stages perform PFC and current regulation, respectively.

DC fed LED driver topologies and PV or battery fed LED driver topologies are again classified into linear DC-DC converters and switched mode DC-DC converters. In linear DC-DC converters, series resistors are employed to regulate the LED current. These LED driver topologies are simple in operation but the generation of more heat causes poor efficiency and uncontrolled operation limited the application of linear DC-DC converters. To realize the controlled operation of the LED lamps, switched mode DC-DC LED driver topologies are designed. Switched mode LED driver topologies are again classified into non-isolated DC-DC LED driver topologies, isolated DC-DC LED driver topologies, and resonant or soft switching LED driver topologies. Non-isolated LED driver topologies are in turn classified as Buck, Boost, Buck-Boost, and Cuk converters. Further isolated LED driver topologies are classified into Flyback, Forward, Push–pull, Half bridge, and Full bridge topologies. Non-isolated topologies are suitable for low-power applications. Whereas in high-power and multiple load applications, galvanic isolation is required. Isolated topologies give good performance in these applications.

In the DC to AC conversion stage, the transformer for providing isolation between input and output in isolated LED driver topologies increases the losses and component count. The resonant LED driver topologies resolve these limitations. Depending on the LC tank circuit connection between input and output, soft switching converters are categorized into series, parallel, and series–parallel resonant converters. Through ZVS turn on and ZCS turn off in switching devices, these converters provide high efficiency, high-power capability, high frequency of operation, and high reliability. A few resonant LED driver topologies presented for multiple load LED lighting applications are discussed in the next section.

3 Multiple Load Resonant LED Driver Topologies

3.1 Three-Leg Resonant LED Driver Topology [79]

The circuit diagram for three-leg resonant LED driver topology presented for smart lighting applications is shown in Fig. 2. The first two legs of the circuit form the full bridge circuit to power LED lamp-1 and the full bridge circuit formed by the first and third leg supplies LED lamp-2. The switches in two legs are operated simultaneously with a high switching frequency and 50% duty ratio. The third leg switches are also operated for 50% duty ratio but with a low switching frequency. Both LED lamps of different power ratings are supplied through the series resonance concept. This

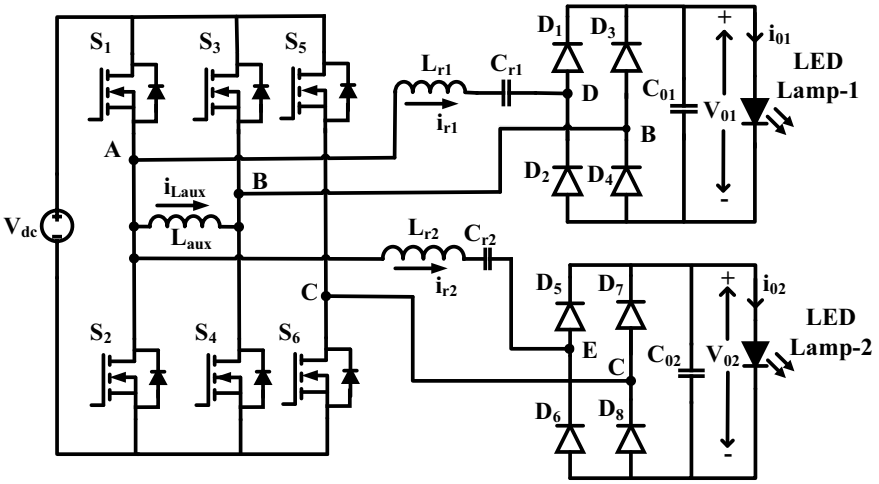

Fig. 2 Three-leg resonant LED driver topology [79]

converter allows individual current regulation and independent dimming with high efficiency.

3.2 Multi-channel LED Driver Topology Based on Switch Controlled Capacitor (SCC) [80]

The precise current sharing control multi-channel SCC LED driver circuit presented in [80] is shown in Fig. 3. This circuit has a transformer with a single primary side and multiple secondary sides with a half bridge rectifier. In each unit, one SCC module, one resonant inductor, and two filter capacitors are connected. Two LED lamps are supplied by each unit. Current regulation and dimming are obtained in each channel through the charging and discharging of the SCC module. This driver circuit achieved current sharing between two LED channels effectively.

3.3 Two-Channel LED Driver with Automatic Current Balance [81]

A Soft switching two-channel LED driver with an automatic current balance is proposed in [81]. The circuit diagram for this topology is given in Fig. 4. In this topology, two half bridge circuits are connected in series to form a stack bridge. The two switches of each half bridge circuit are turned on complimentarily. The square wave output is obtained at the mid-point of the stack bridge by controlling

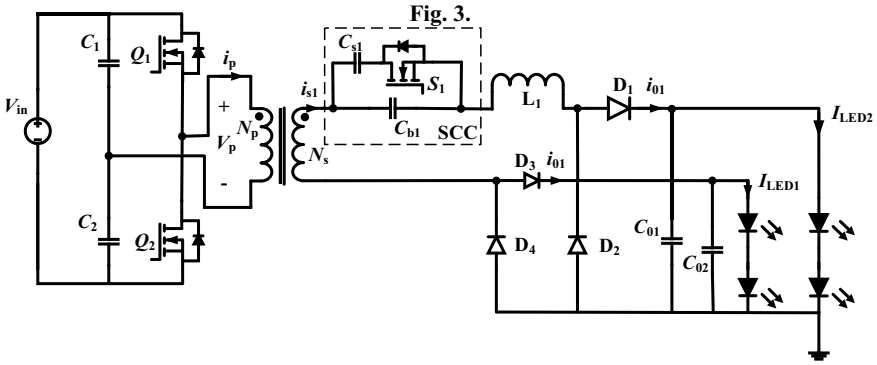

Fig. 3 Multi-channel LED driver topology based on the switch-controlled capacitor (SCC) [80]

the state of the four switches in two half bridge circuits. The inductor L_r acts as a resonant tank. This topology attains ZVS in Continuous Conduction Mode (CCM) and ZCS in Discontinuous Conduction Mode (DCM). The ampere-second balance approach resulted in the automatic current balance of the LED lamps. Stack bridge configuration reduced the switching losses.

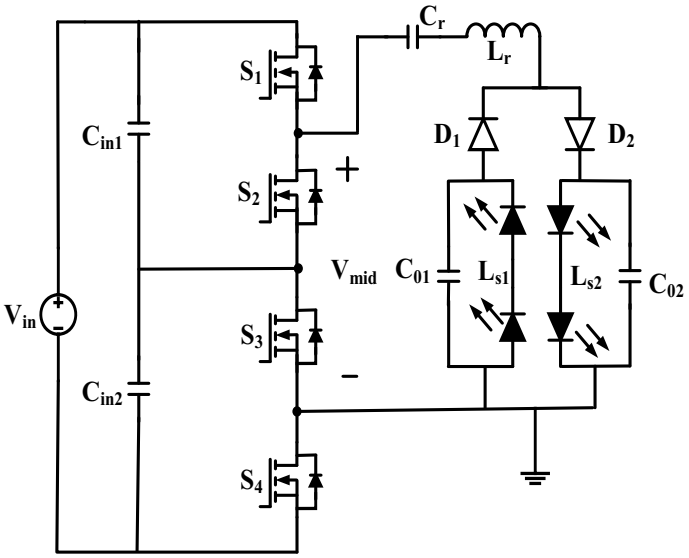

Fig. 4 Two-channel LED driver with automatic current balance [81]

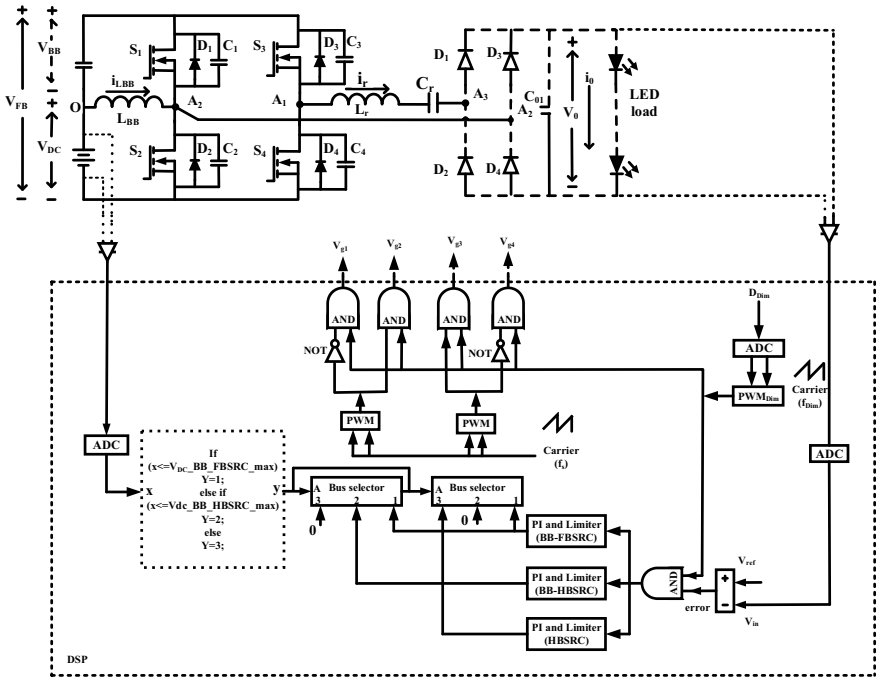

Fig. 5 Non-isolated wide input SRC topology [82]

3.4 *Non-isolated Wide Input Series Resonant Converter (SRC) Topology [82]*

The circuit diagram for a Non-isolated Wide Input Series Resonant Converter (SRC) topology is shown in Fig. 5. This resonant converter can be reconfigured into three different topologies such as Buck-Boost integrated Full Bridge converter (BBFBSRC), Buck-Boost integrated Half bridge converter (HBSRC), and Conventional HBSRC to produce three different voltage gains. It operates for wide input voltage ranges while maintaining the soft switching. The transition from one topology to another topology is achieved smoothly by the PI controller based on input voltage without any additional components. Reduced switching losses and wide voltage range operation make this converter more suitable for automotive applications.

3.5 *Soft Switched Full Bridge LED Driver Topology [83]*

The circuit diagram of the soft switched full bridge converter is shown in Fig. 6. In this driver circuit configuration, the series combination of LED lamp and inductor is connected in parallel with the switch. Inductors L_1, L_2, L_3, and L_4 provide continuous

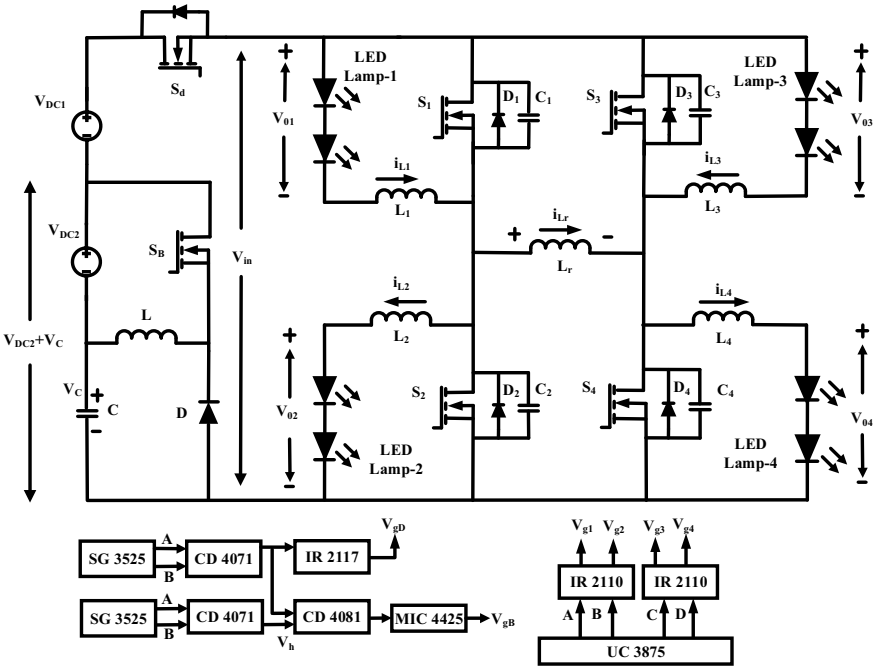

Fig. 6 Circuit diagram of soft switched full bridge LED driver [83]

current to the lamps. Inductor L_r is used to achieve ZVS in all four switches. Switches S_1 and S_2 are alternately turned on and off at a switching frequency $f_s = \frac{1}{T}$ with a 50% duty ratio, to avoid short circuits between the switches. Similarly, S_3 and S_4 are alternately turned on and off with the same switching frequency and duty ratio. By using a low-frequency gate signal, the switch S_d enables dimming control in all LED lamps. Input voltage variations are handled by the Buck-boost converter at the input side of the driver circuit. This topology achieved ZVS which improves the efficiency by reducing switching losses. Hence, the switching devices are carrying only small currents, and the current stress in the devices is also reduced significantly. This topology is highly suitable for street lighting applications.

3.6 Ripple-Free Full Bridge LED Driver Topology [84]

An efficient ripple-free full bridge LED driver with ZVS is proposed in [84]. The connection diagram for this converter is given in Fig. 7. This full bridge configuration cancels out the ripple voltage in LED lamps by using the interleaving technique. The connection of inductors and LED lamps to obtain ripple cancelation in LED lamps is shown in Fig. 7. Allowing more ripple in the inductor reduced the size of the

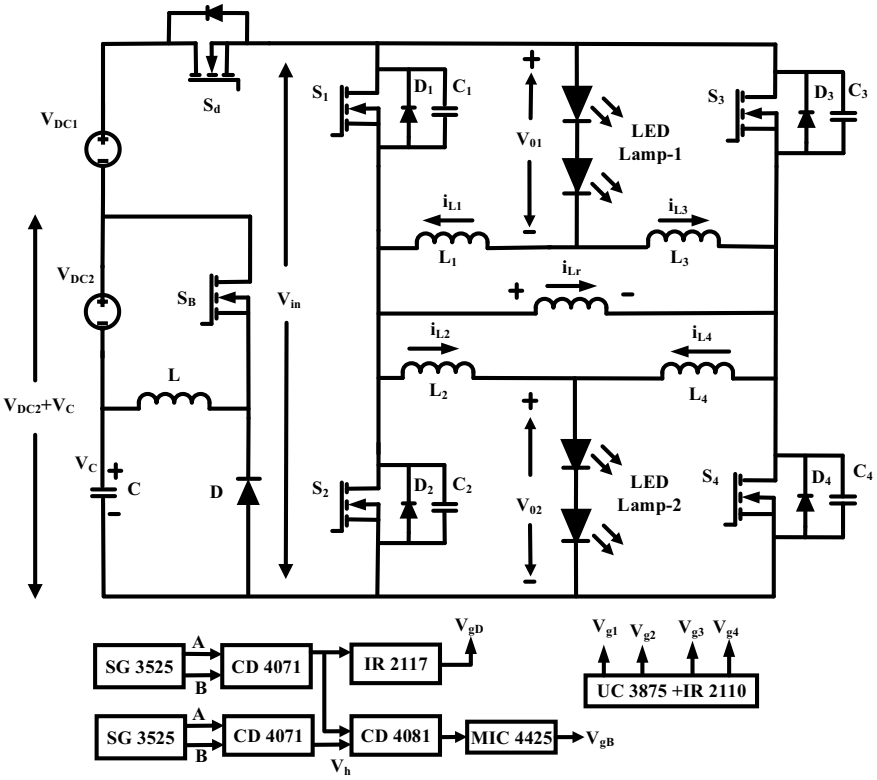

Fig. 7 Circuit diagram of an efficient ripple-free LED driver with ZVS [84]

inductor. Due to this, the size and cost of the driver circuit are reduced. High-efficiency dimming control is achieved through S_d by using the on–off control method. Input voltage variations are controlled by the Buck-boost converter. This driver circuit is suitable for PV or battery fed street lighting applications.

4 Results and Discussions

The two soft switched full bridge topologies are simulated in MATLAB Simulink environment to give an idea about the performance of soft switching converters. The simulation parameters used for the two topologies are given in Table 1. Figures 8, 9, 10, 11 and 12 represent the simulation results for soft switched full bridge converter [83]. In soft switched full bridge topology, ZVS is achieved through resonant inductor L_r in all the four switches. Figure 8, describes the switching pulses of the switch-1 in soft switched full bridge converter. Here we can observe ZVS turn on in the switching device. As all lamps are identical, results are shown for a single lamp.

Figure 9 represents the voltage across lamp-1 and Fig. 10 represents the current through lamp-1. From these waveforms, we can observe that this driver circuit is able to give a continuous supply to LED lamps. And also, we can observe the small ripple content of 1.29 V in voltage waveform and the ripple current of 0.13 A. In general, high ripple factors reduce the efficiency and lifetime of the driver circuit; this in turn affects the performance of LED lamp by decreasing its luminous intensity. The component count of this circuit is comparatively less as it is able to run four loads with four switches, four inductors, and one resonant inductor. Figures 11 and 12 show the voltage and current waveforms of topology with 20% dimming. This shows that high-efficiency dimming is achieved in a wide range.

Figures 13, 14, 15, 16 and 17 represent the simulation results for ripple-free full bridge converter [84]. The switching pulses for ripple-free full bridge converter are shown in Fig. 13. This shows ZVS turn on of switches in this topology. The voltage across lamp-1 and current through Lamp-1 are shown in Fig. 14 and Fig. 15,

Table 1 Simulation parameters

Parameter	Soft switched full bridge driver circuit	An efficient ripple-free full bridge driver circuit
DC input voltage, V_{in}	66 V	31.2 V
Switching frequency, f_s	200 kHz	200 kHz
Duty ratio, D	0.5	0.5
L_1, L_2, L_3, L_4	577 μH	71 μH
L_r	120 μH	130 μH
LED operating current, i_{LED}	550 mA	550 mA
LED operating voltage	3.3 V	3.3 V
Number of lamps	4	2
Number of LEDs	80 (10 LEDs in single string, two parallel strings in one lamp)	48 (12 LEDs in single string, two parallel strings in one lamp)

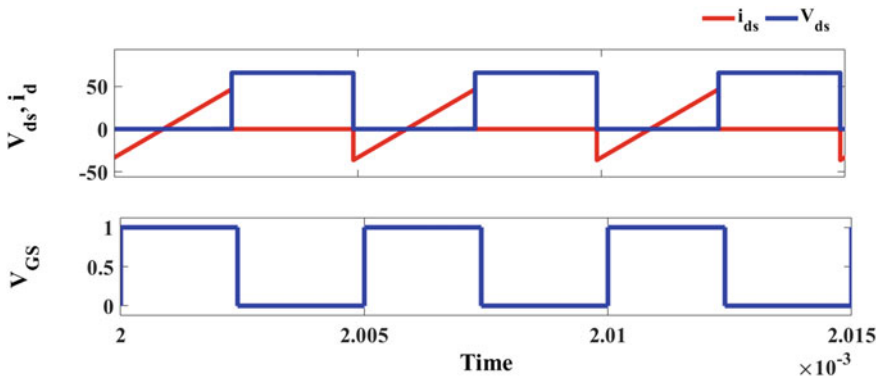

Fig. 8 Switching pulses in soft switched full bridge LED driver

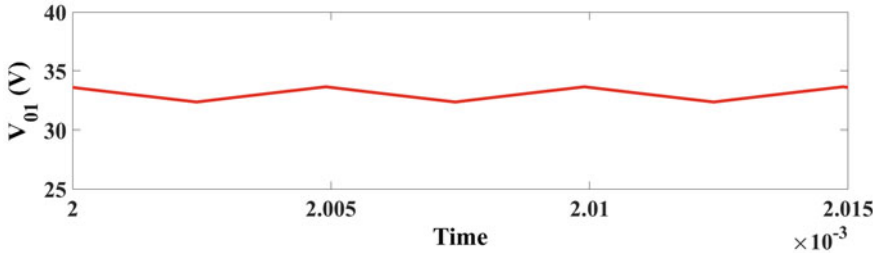

Fig. 9 Voltage across lamp-1 in soft switched full bridge LED driver

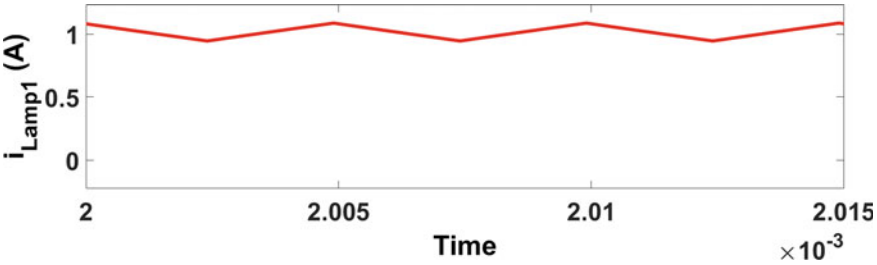

Fig. 10 Current through lamp-1 in soft switched full bridge LED driver

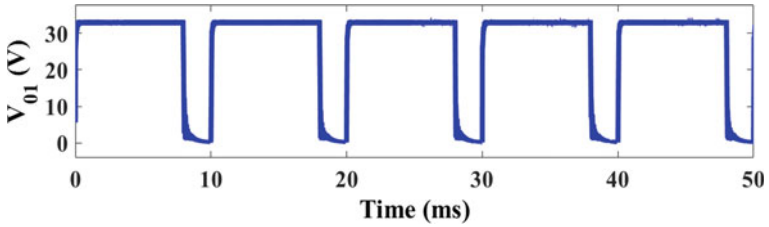

Fig. 11 Voltage across lamp-1 in soft switched full bridge LED driver with 20% dimming

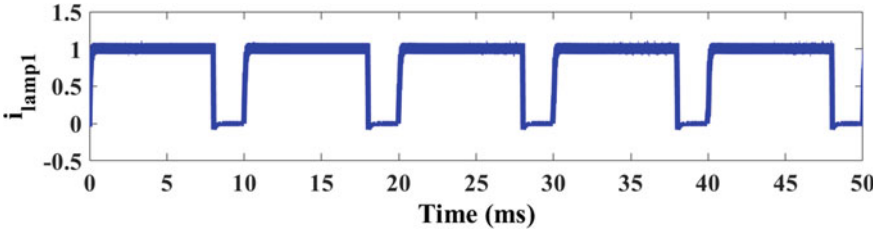

Fig. 12 Current through lamp-1 in soft switched full bridge LED driver with 20% dimming

respectively. Figures 16 and 17 show voltage and current waveforms of ripple-free full bridge LED driver circuit with 20% dimming. The experimental results of this circuit showed high-efficiency dimming in a wide range, i.e., from 0 to 100%. The number of components used per lamp in this topology is more than the soft switched full bridge circuit. The performance comparison of all the topologies is given in Tables 2 and 3 and the components comparison of all the topologies is given in Table 4.

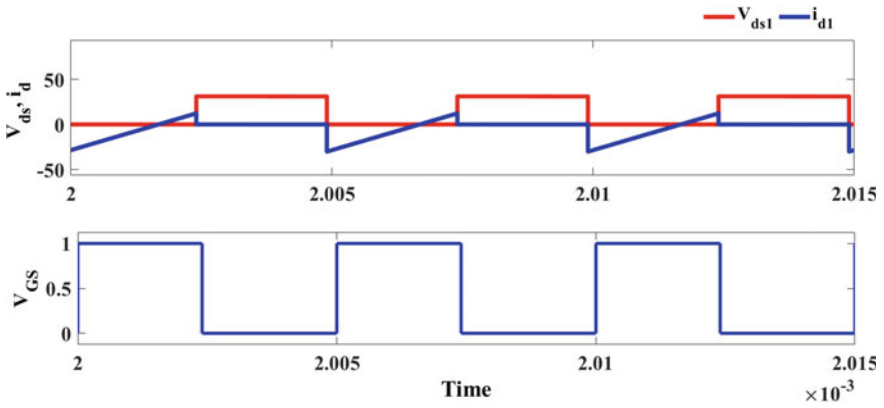

Fig. 13 Switching pulses in ripple-free full bridge LED driver

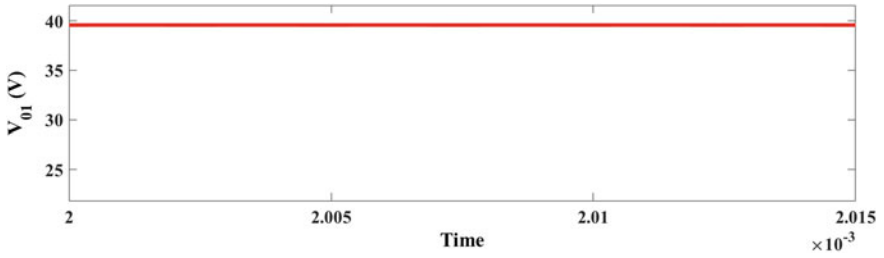

Fig. 14 Voltage across lamp-1 in ripple-free full bridge LED driver

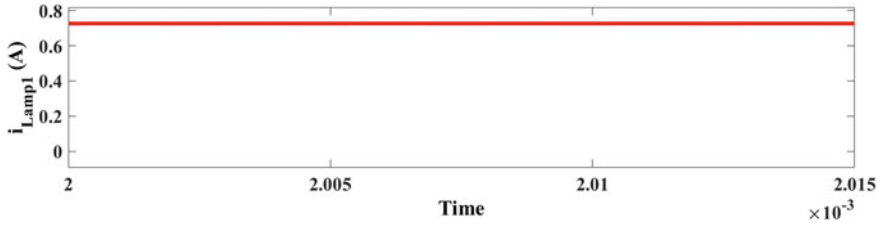

Fig. 15 Current through lamp-1 in ripple-free full bridge LED driver

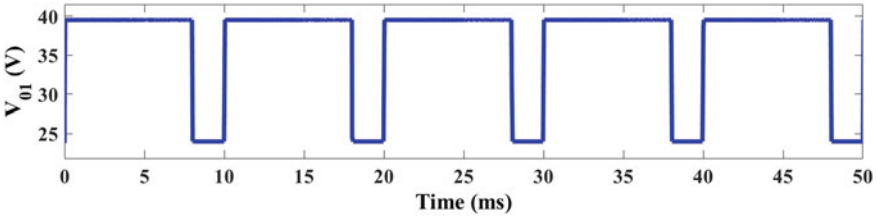

Fig. 16 Voltage across lamp-1 in ripple-free full bridge LED driver with 20% dimming

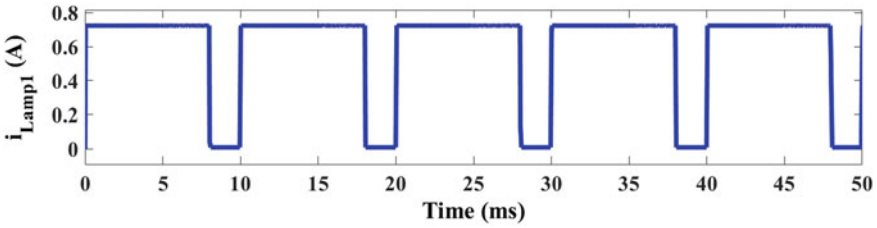

Fig. 17 Current through lamp-1 in ripple-free full bridge LED driver with 20% dimming

Table 2 Performance comparison of all topologies

Topology	Input voltage (V)	Output power (W)	% Efficiency	Dimming	ZVS	ZCS	Number of lamps	Application
[79]	48	126	92.45	Yes	Yes	No	2	Smart lighting
[80]	48	20	93.4	Yes	Yes	No	2	Low-power lighting
[81]	100	15.8	NA	Yes	Yes	Yes	2	Low-power lighting
[82]	18–120	22.77	91.8–94.19	Yes	Yes	No	2	Automotive lighting
[83]	66	36.3	93	Yes	Yes	No	4	Street lighting
[84]	12–24 V	87	94	Yes	Yes	No	2	Street lighting

5 Conclusion

A few resonant topologies presented for multiple load LED lighting applications are discussed in this paper. The performance parameters of all these topologies are given in Tables 2, 3, and 4 for comparison. All the topologies achieved soft switching and are applicable for multiple load LED lighting applications. The soft switched full

Table 3 Performance comparison of all topologies

Topology	Current regulation	Device current stress	Component count per lamp	Independent dimming
[79]	Yes	Low	Moderate	Yes
[80]	Yes	Low	Moderate	Yes
[81]	Yes	Low	Moderate	No
[82]	Yes	Low	Moderate	No
[83]	Yes	Low	Low	No
[84]	Yes	Low	Low	No

Table 4 Comparison of components in all topologies

Components	[79]	[80]	[81]	[82]	[83]	[84]
Switches	6	3	4	4	6	6
Diodes	8	4	2	4	1	1
Capacitors	4	6	3	2	1	1
Inductors	3	1	1	2	5	5
LED lamps	2	2	2	1	4	2
Transformer	0	1	0	0	0	0

bridge topologies presented for street lighting applications are simulated in MATLAB Simulink environment to analyze the advantages and limitations of both topologies.

The three-leg resonant converter topology [79] can be applicable to different power rating LED lamps. The current regulation is achieved by phase modulation and duty ratio control techniques. This topology is suitable for high-power applications. Multi-channel LED driver topology with SCC [80] achieved current regulation through SCC module adjustment. This topology can be used to connect multiple channels as it attains independent current regulation in each unit through a capacitor unit. Two-channel LED driver with automatic current balance [81] achieved ZVS and ZCS in CCM and DCM operation, respectively. The frequency doubling technique reduced the switching losses of the converter. This converter attains automatic current balance by ampere-second balance. Non-isolated wide input series resonant converter topology [82] can be reconfigured into three different topologies by maintaining soft switching. This topology is well suitable for automotive applications. Soft switched full bridge LED driver topology [83] achieves high efficiency by reducing component count by supplying four loads with four inductors, four switches, and one resonant inductor. Ripple-free full bridge LED driver topology [84] obtains zero ripple content in both voltage and current waveforms making it suitable for flicker-free LED lamps. Depending on the application and specifications, any of these driver topologies can be chosen for multiple load LED lighting applications.

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State-of-Charge Estimation in Lithium-Ion Battery for Electric Vehicle Applications: A Comparative Review

Rajbala Purnima Priya, Shivam Mishra, Aryan Priyadarshi, and Sanjay

1 Introduction

Scientists have been alerted of the necessity to reduce pollution and conserve the Earth as the global temperature has risen. Electric Vehicles emit very few pollutants into the atmosphere as compared to vehicles powered by gasoline or diesel. Greenhouse gases (GHG) are a significant issue that harms the environment. Greenhouse gases (GHG) include CO_2, methane, Fluorinated gases (F-gases), and nitrogen oxide, and CO_2 contributes a major percentage of GHG. Therefore, European Union established an intermediate goal of reducing net CO_2 emissions by at least 55% by 2030 to attain climate neutrality by the end of 2050 [1].

Electric Vehicles, which are powered by batteries that are charged with renewable energy, offer a sustainable alternative to existing transportation methods. Electric automobiles are 100% environmentally friendly and run on electric engines. LIBs are the best option for EV applications in terms of energy storage [2–4]. The fastest-growing Energy storage system (ESS) technology is lithium-ion batteries (LIBs). Regardless of this, LIB protection and monitoring are critical areas that need to be improved [5]. Because lithium is a temperature-sensitive and reactive metal, the battery management system in a lithium-ion battery is essential for protecting the

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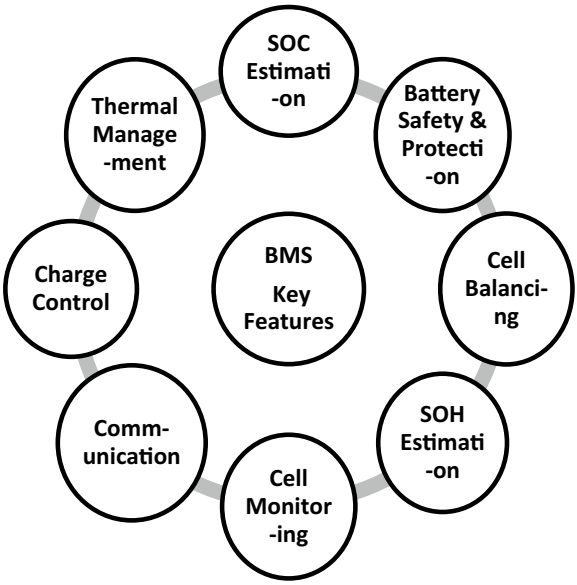

Fig. 1 Key highlights of BMS for EV applications

battery packs from over-voltage, under-voltage, and temperature. Several LIB fires and explosions have occurred in recent past years [6], causing property damage and personal casualties.

As a result, BMS is crucial for powering EVs and has a wide range of features to ensure the optimal operation as highlighted in Fig. 1. A brief assessment of various essential battery management system technologies, including battery charging and state estimation, has been presented in [7]. This paper precisely reviews the battery modeling and methods to estimate the SOC of LIB.

2 Overview on Battery Modeling for SOC Estimation

The models of battery are useful while estimating the model based on the state-of-charge of LIB, there are mainly three models namely an electrochemical model, an equivalent circuit model (ECM), and a data-driven (DD) model surveyed in the literature [8, 9]. Figure 2 describes the three types of models for LIBs.

The electrochemical model is intensively explored in [10] and this model exhibits the best accuracy and high computational cost, electrical equivalent circuit model is described in [11–13] and it has moderate accuracy and moderate computational cost, and DDM [14] has least accuracy and least computational cost.

The electrochemical models are the most accurate representations of LIBs available. The next important battery model to consider is an ECM. The words "gray box models" and "abstract models" are used in the context of ECM. It's a popular battery model for BMS in electric vehicles [15]. The black box model is another

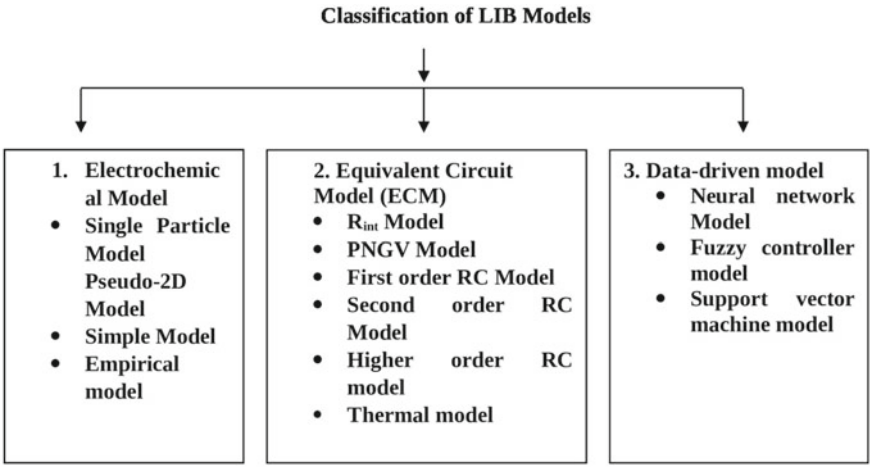

Fig. 2 Methods of battery modeling

name for the DD model. A DD technique is used to increase the accuracy of the SOC estimation. The battery current, voltage, temperature, and state-of-charge (SOC) are analyzed, and a controller is developed based on the system behavior, which does not require an exact system mode. Using battery models to determine the precise SOC of a battery is a tough task. In addition to the three approaches mentioned above, hybrid models are also utilized to estimate the SOC of LIBs [16]. The advantages, disadvantages, and applications of the electrochemical model, EEC model, and DD model are described in Table 1.

Table 1 Application, advantages, and disadvantages of battery modeling

S. No.	Name of the model	Advantages	Disadvantages	Applications
1	Electrochemical models [8, 17]	Laws of physics are required and the most accurate	Complex, not easy to all the types of LIBs, high computational cost, and time consuming	BMS and real-time monitoring
2	ECM models [17– 25]	Mathematical model of battery required, simple, easy to apply, and reliable	Assumptions taken moderate accurate moderate computational cost	BMS, real-time monitoring, and SOC estimation in LIBs for EVs and all ESS
3	DD models [15, 26]	Mathematical model of battery not required, least computational cost, and least time consuming	Least accurate, sensitive to training data, and complex controller is required	SOC estimation in hybrid EVs and EVs

3 Definition of SOC

SOC is the ratio of the amount of charge that can be recovered at a given time to total capacity, and it represents the battery's remaining capacity. In other terms, it may be defined as the amount of energy available at any specified instant with respect to the overall energy of the battery, as indicated by Eq. (1). Because the indication of SOC is comparable to that of a gasoline gauge in an internal combustion engine automobile, precise calculation of SOC is critical for determining the status of the battery and the required charging or discharging time. Because a battery is a chemical energy storage device, its state-of-charge cannot be directly measured; instead, it is calculated indirectly using other parameters of the battery such as voltage, current, and temperature of the battery.

$$SOC_t = SOC_0 - \frac{\int_{t0}^{t} \eta i(t) dt}{C_{\max}} \tag{1}$$

In the above equation, SOC_t signifies current SOC at any time t, SOC_0 denotes the battery's initial SOC, $i(t)$ is the load current (discharging current is taken as positive), η represents Coulombic efficiency (related to the capacity of the battery and is the ratio of discharge capacity to charge capacity after the full charge), and $C_{\max}$ is battery's maximum available capacity when completely charged.

The inverse of SOC is the Depth of Discharge (DOD) [27]; DOD can be used in place of SOC. The link between DOD and SOC of the battery system is depicted in Fig. 3.

The discharge voltage characteristics for different C-ratings of the battery at room temperature (25 °C) are shown in Fig. 4a [28]. The rate at which the battery is discharged or charged relative to the maximum capacity of the battery is called C-rating.

The charging voltage, estimated SOC, and true SOC of the battery are shown in Fig. 4b at 0.2 C at 25 °C [28].

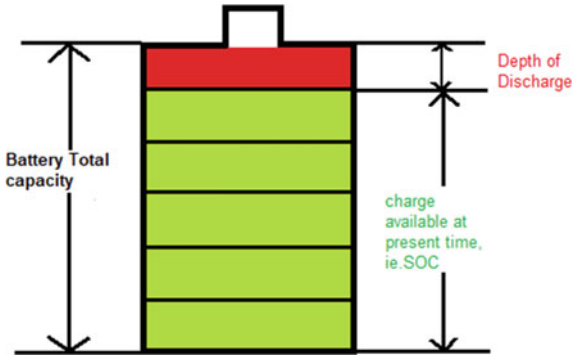

Fig. 3 State-of-charge and depth of discharge relationship

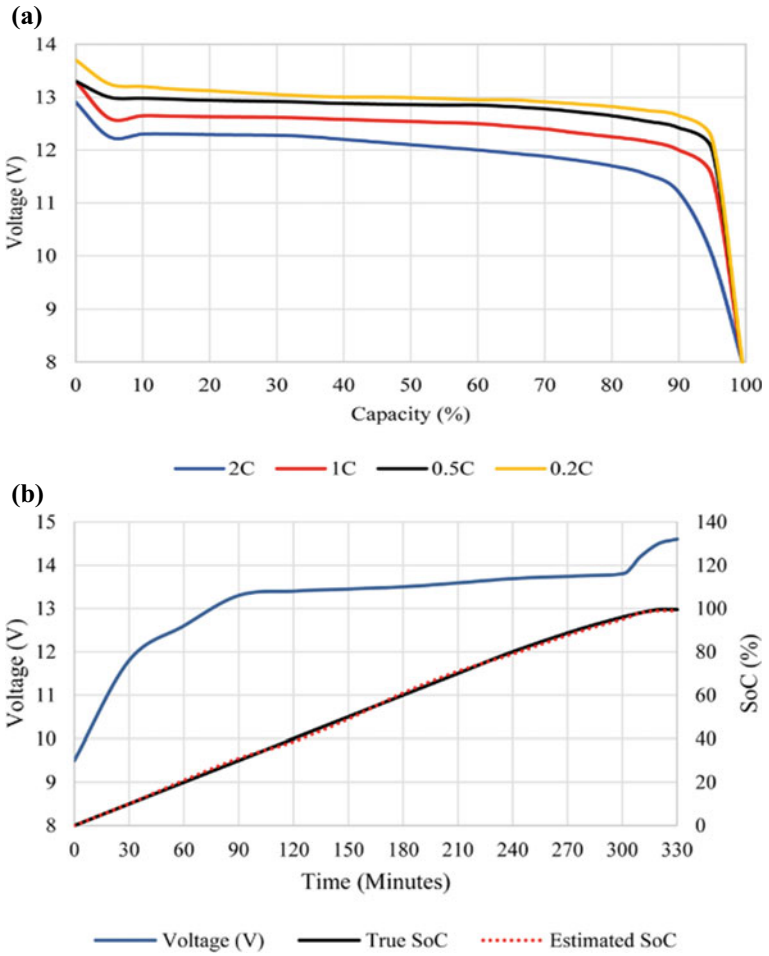

Fig. 4 **a** The discharge voltage characteristics of battery for different C-ratings at 25 °C. **b** Charging voltage at 0.2 C at 25 °C

4 Methods for SOC Estimation

The biggest problem with EV batteries is estimating the SOC. Because the SOC of the battery cannot be directly tested, a particular method is needed to represent the remaining capacity. An accurate SOC estimation plays a critical role in extending battery life and improving performance. This estimating technique continually monitors all of the battery's internal properties and protects it from overcharging and over-discharging. The SOC estimation method can be categorized into four methods [29, 30] as shown in Fig. 5.

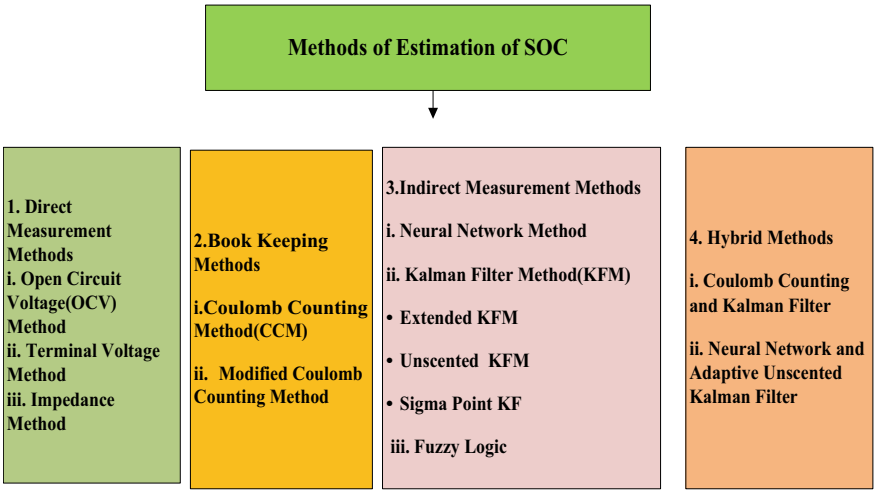

Fig. 5 Methods of SOC estimation in lithium-ion battery

4.1 Direct Measurement Methods

Physical measurements for example the impedance and voltage of the battery are utilized in the direct measurement methods for predicting the SOC of the battery. The open-circuit voltage (OCV) technique, terminal voltage technique, and impedance spectroscopy techniques are all commonly used direct measurement methods. Voltage-based methods such as open-circuit voltage method and terminal voltage method are basically based on lookup table methods. The lookup tables are the tables containing the information of battery voltage, battery current, and temperature of the battery and the subsequent comparison of data with an existing lookup table with experimental data. For each set of information on battery voltage, current, and temperature, there is the corresponding value of SOC.

4.1.1 Open-Circuit Voltage (OCV) Method

For a LIB, open-circuit voltage is the thermodynamic perspective of the battery under no-load conditions and has a nonlinear connection with SOC [30]. Offline OCV tests at certain ambient temperatures and aging phrases are commonly used to acquire the OCV. Despite the accuracy of the open-circuit voltage (OCV) approach, it requires a rest period to estimate the SOC, making it challenging to use in real-world applications so it is not suited for estimation of SOC for EV applications. For a lithium-ion battery, open-circuit voltage (OCV) is the thermodynamic potential of the battery under no-load conditions and has a nonlinear connection with SOC. Offline OCV tests at certain ambient temperatures and aging phrases are commonly

used to acquire the OCV [31]. Although the open-circuit voltage (OCV) approach is quite precise, it does need a rest period.

4.1.2 Terminal Voltage Method

In constant current discharge, the terminal voltage approach (load voltage method) provides a superior estimation impact than the open-circuit voltage method [32]. However, in real applications, the terminal voltage approach cannot be utilized to predict the battery SOC during driving due to substantial fluctuations in demand current. Therefore, only a few studies have been conducted to measure SOC using the terminal voltage approach of LIB [30]. It's generally only used to see if the discharge has been shut off.

According to OCV-SOC curve, the terminal voltage of the battery is matched with SOC. The terminal voltage measurement is done according to Eq. 2 [33].

$$Voltage\,measurement = F(SOC) + G(parameters, Current) \tag{2}$$

where $F(SOC)$ is the function that refers to the open-circuit voltage model, which relates the open-circuit voltage and SOC of the battery. $G(parameters, Current)$ is the function, which relates to voltage drop inside the battery.

4.1.3 Impendence Method

To calculate the impedance of the system, current and voltage measurements of the system should be done at different excitation frequencies, as the impedance also depends on the frequency of the system. However, the effect of change in frequencies is negligible at higher SOC values but should be taken into context at lower SOC values [30].

Electrochemical Impedance Spectroscopy, which provides substantial information about the complicated electrochemical processes taking place inside the battery, is one of the technologies being examined. The theory of electrochemical impedance spectroscopy is employed by Ji'ang Zhang et al. to guide and develop the equivalent circuit model [34].

4.2 Book Keeping Methods

Two types of bookkeeping methods are the coulomb counting method (CCM) and the modified CCM. The input to this technique is the battery charging and discharging current. It enables the calculation of SOC to include many battery internal effects, including capacity loss and self-discharge, as well as battery statistics, such as nominal capacity [30].

4.2.1 Coulomb Counting Method (CCM)

CCM is a common method for calculating the state-of-charge that is considered accurate taking the account of initial SOC and battery capacity are known. This method is also known as the Ampere-Hour method for SOC estimation. The SOC of the LIB is calculated by integrating the load current as discussed in Eq. 1. On the other hand, this method is prone to errors from several causes, and Kiarash Movassagh [33] has investigated the extent of these errors. However, this method is the easiest method to calculate SOC [35], and this method is used to verify the accuracy of the results obtained from other methods.

4.2.2 Modified Coulomb Counting Method

The coulomb counter is an open-loop counter so errors are added continuously. The battery aging, high rate of discharge, and extreme temperature the factors that limit the real-time use of the CCM method. The Modified CCM is capable of dealing with difficult working circumstances, and the SOC estimation accuracy is within 3.6% [36].

$$SOC(t) = SOC(0) + \frac{\eta}{C_{batt}} \int_0^t i(t)dt \tag{3}$$

Here η is the Coulombic efficiency which is defined by Eq. 4

$$\eta = \begin{cases} \eta_c, i(t) \geq 0 \\ \eta_d, i(t) < 0 \end{cases} \tag{4}$$

$i(t)$ is battery current in ampere (A), t is time, $SOC(0)$ denoted the initial SOC, $SOC(t)$ represents the SOC at time interval t, and C_{batt} is the battery capacity in Ampere-Hour (Ah).

4.3 Indirect Measurement Methods

The indirect Measurement method of SOC estimation is also known as a model-based method as this method required an accurate equivalent circuit model (ECM) of the battery [37]. The parameters of an equivalent circuit of LIB play a vital role in the accuracy of the system; parameters are estimated offline as well as online [38] and then fed into the ECM.

4.3.1 Neural Network Method

In recent years, NNM and support vector techniques have attracted considerable attention from the researchers. A neural network uses mathematical models, which is a subfield of artificial intelligence that comprises linked artificial neurons activated by biological neural networks, and uses previous data from that system to anticipate the output of a nonlinear system [30, 39]. NNM methods do not depend on a thermal, chemical, electrical, and physical model of LIB; also, it takes very less amount of time as compared to other methods for estimation of SOC. NN consists of input layer as input variables (voltage, current, temperature), interconnected neurons called hidden layer, and output layer as output variable (SOC). The NNM method estimates the SOC with input variables without using the lookup tables. The steps involved in NNM can be shown in the flowchart in Fig. 6.

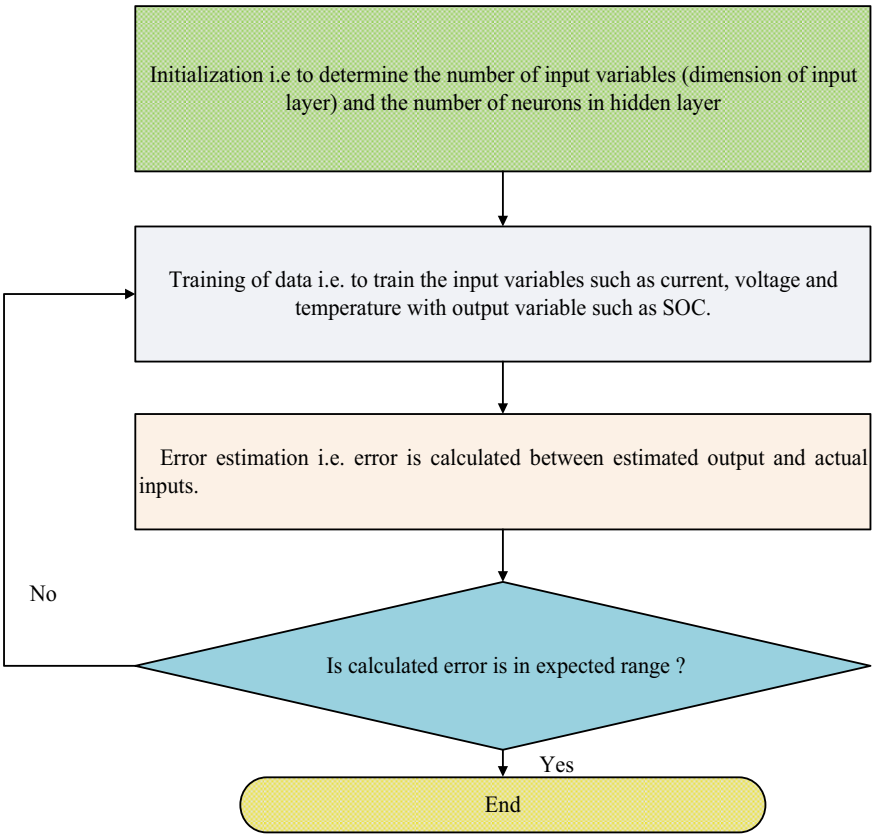

Fig. 6 Flowchart for an algorithm of neural network method for SOC estimation

4.3.2 Kalman Filter Family

As an optimum estimator, the Kalman Filter is a well-known approach for estimating the inner state of dynamic linear systems [40]. KF is a recursive set of equations that is divided into two steps: (i) a prediction step that forecasts the system output, state, and error; (ii) a correction step that adjusts the current state estimate value based on the system output value. Author Prashant Shrivastva examined the family of KF used for SOC prediction [41], and the Kalman filter family is shown in Fig. 7. The dual KF technique, which is a mixture of two KFs in which one KF is used to compute the SOC of the battery and another KF is used to decide the battery parameters online [40], is also a conventional approach. In the face of noise, however, the nonlinear KF technique outperforms the linear KF algorithm in terms of precision. Yang et al. [42] discussed improved Kalman filters, and Qiao Zhu presented the fractional-order AEKF approach in [43]. Hafiz Farhaj Khan proposes a fused online strategy for lithium-ion battery model identification and state-of-charge (SOC) prediction that combines the Lagrange multiplier technique and the sigma point Kalman filter in [44]. Chen et al. present an enhanced unscented Kalman filter technique to improve the online state-of-charge estimation in terms of both robustness and accuracy [45]. Xuan et al. discussed the various advantage of the Square-Root Central Difference Kalman Filter (SRCDEK) technique over EKF and UKF in [46]. Cubature Kalman Filter (CKF) technique discussed in [47] uses a fractional-order model of battery that has better state robustness than EKF, smaller noise covariance, and improved voltage estimation for SOC estimation.

4.4 Hybrid Methods

In recent years, hybrid method techniques have attracted considerable attention from researchers [48, 49]. The linear observer (LO) and the nonlinear observer (NLO) have recently been used to estimate the status of batteries. The fundamental disadvantage of the LO is that it has a higher estimation error than the NLO [50]. The different types of observers: Linear observer, nonlinear observer, sliding-mode observer, proportional-integral observer, and Luenberger observer were discussed for SOC estimation by Ali et al. [51].

The hybrid method uses two methods of SOC estimation, one is taken as a reference for error estimation and another method is used to estimate the SOC. A hybrid strategy combining a gated recurrent unit Neural Network with the adaptive unscented Kalman filter (AUKF) method is suggested in this research by Xu et al. [52].

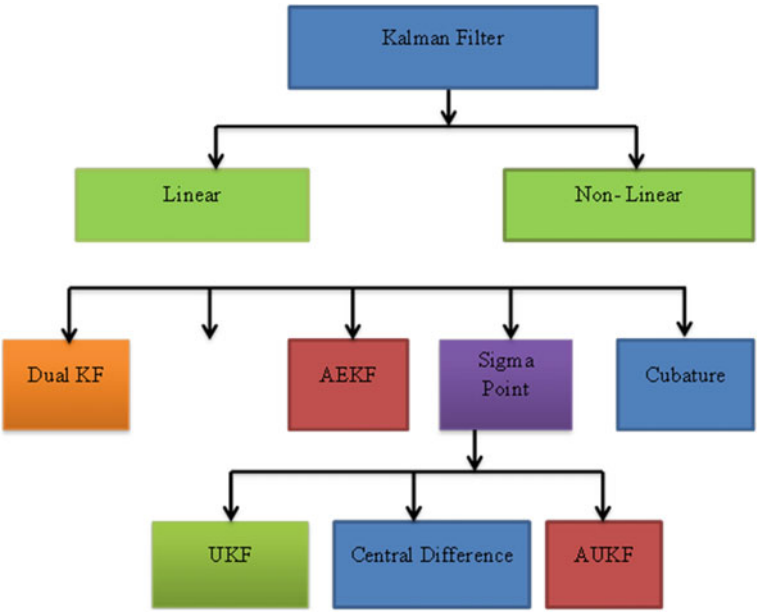

Fig. 7 Family of KF used for SOC estimation in battery for EV application

5 Summary

Electric Vehicles, which are powered by batteries charged with renewable energy, provide a potential alternative to conventional modes of transportation. Electric vehicles run on electric engines and are completely environmentally friendly. As a result, battery management systems are critical for charging electric cars (EVs) and incorporate a variety of functions to ensure optimal operation. SOC is the crucial feature of BMS. This paper precisely reviews the battery modeling and methods to estimate the state-of-charge of LIB. The estimation techniques have been examined and analyzed qualitative as well as quantitative to determine their applicability for dynamic modeling of LIBs for electric vehicle applications. Section 1 of this paper discusses the importance of EVs and Sect. 2 discusses the definition of various terms such as BMS and SOC. The battery models are important for calculating the model-based SOC in the LIB. Section 3 discusses the electrochemical models, equivalent circuit models (ECM), and data-driven (DD) models in detail. Extending battery life and boosting performance both need precise SOC prediction. This estimation method constantly analyzes the battery's internal qualities and protects it from overcharging and over-discharging, and Sect. 4 deals with various methods for SOC estimation. Table 2 summarizes the advantages, limitations, and applicability of EV application of different methods for SOC estimation.

Table 2 Advantages, disadvantages, and usefulness of methods of SOC estimation

S. No.	Methods of SOC estimation	Advantages	Disadvantages	Usefulness in EVs
1	OCV method [30, 31]	Accurate, simple, cost-effective, independent of battery model, and effective method	Time consuming, requires rest period, SOC-OCV relationship varies with batteries	No
2	CCM and modified CCM [30, 33, 35, 36]	Simple, easiest method, cost effective, independent of battery model	Accuracy depends on many factors (battery age, temperature, charge–discharge rate, and sensor precisions), less precision, sensor errors, initial condition problems (initial value of SOC), and cumulative errors problems due to open-loop calculations	Yes
3	Neural network method [30, 38]	Accurate, mathematical modeling is required	Time consuming, high computational cost, and large set of training data required	Yes
4	KF family [30, 40–47]	ECM of battery required, numerical instabilities due to complex matrix operation, easy to apply	High computational cost, high complexity, and accuracy depends on the controller and initial SOC	Yes
5	Fuzzy logic method [30, 53]	Higher accuracy, ECM is not required, easy	High computational cost, high complexity, age of the battery is not considered, rules for fuzzy logic should be clearly defined, depends on statics characteristic of battery	Yes
6	Hybrid method [48–52]	High accuracy	Time consuming, high computational cost, high complexity	Yes

Nomenclatures

S. No.	Abbreviations	Meaning
1	AEKF	Adaptive Extended Kalman Filter
2	AUKF	Adaptive Unscented Kalman Filter
3	BMS	Battery Management System
4	CCM	Coulomb Counting Method
5	DD	Data-driven
6	DOD	Depth of discharge
7	ECM	Equivalent Circuit Model
8	EEC	Electrical Equivalent Circuit
9	EKF	Extended Kalman Filter
10	ESS	Energy Storage System
11	EVs	Electric Vehicles
12	GHG	Green House Gas
13	KF	Kalman Filter
14	LIB	Lithium-Ion Battery
15	LO	Linear Observer
16	NLO	Non-Linear Observer
17	NNM	Neural Network Method
18	OCV	Open-Circuit Voltage
19	SOC	State-Of-Charge
20	SRCDEK	Square-Root Central Difference Kalman Filter
21	UKF	Unscented Kalman Filter

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Novel High Voltage Pulse Generator Structure for Water Treatment Applications

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1 Introduction

Monotonous high voltage pulse generation is widely employed in liquid disinfectant and water disinfection, food processing, etc. Water recirculation or water disinfectant system requires disinfectant to reduce bacteria and viruses. The voltage source or the power required is more than the voltage requirement provided by the standard government norms, so we need different topologies to reduce bacteria and viruses. A high pulse electric field is utilized in water treatment, and the bacteria and germs are killed; hence the water is purified. The high voltage can be produced using a boost converter with the CDVM technique. To avoid electrolyzes of electrodes, PEF Pulse electric field is used. The continuous electric field is employed, and the time duration can be from nanoseconds to microseconds. A DC-DC converter is used for producing Pulsed high voltage output [1]. This high voltage pulse generator was proposed for underwater pulsed streamer corona discharge water treatment applications. This topology of the generator produces modular high voltage and, in this topology, basically as a converter is connected in series with half-bridge-based modules. Multiple analyses were carried out with experimental results, and the converter produces modular voltages for the water treatment plant application. Through the simulation performed, the prototype working was confirmed [2]. In this research, a high voltage generator was designed using the dc-dc converter, and this high voltage pulse generator was used for water treatment application. There were basically many losses found in the generator, which doesn't make it a stabilized design. The simulation was performed

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with stability analysis and found high harmonics and losses. The high voltage generator is proposed with Corona discharge from an underwater pulsed streamer where a regulated voltage supply is objectified. It is effective in killing microorganisms.

The proposed generator is subjected to a comprehensive simulation study for a 10 kV, 400 W pulse generator fed from a 220 V, 50 Hz AC supply. An experimental prototype (1.5 kV, 25 W) is also implemented and tested [3]. In this type of research, a high voltage was basically taken as input. Instead of producing high voltage, we will do it for a short pulse like an overview of high voltage nanosecond pulsar generator technology has been presented. Designs were divided into two storage types which are inductive and capacitive, and they are practically available for a nanosecond and picosecond pulsars. The characteristics of the three primary switches include turn-on time, holdoff voltage, and turnoff. This new research was done on the Marx topology in which were experimented. The conventional topology was modified by using the boost converter in the cascade form and by adding different components [4–6]. Marx generator is the parallel composition of the diode and a capacitor and buck-boost circuits. This circuit is used to give output as high voltage. The experiment is a set of suitable solid-state switches that helps it provide a good HV for the converter's output with a particular number of capacitors. This circuit gives high voltage with fewer components than the topologies in the existing literature [7–15].

2 Quadratic Boost Converter Ringing Circuit (QBCRC)

In the conventional boost converter or quadratic converter, the output is taken across the capacitor, but in QBCRC converter, the output is taken across the input voltage source and the capacitor differentially as illustrated in Fig. 1. It will generate a unipolar discontinuous voltage across the load, which can be used for many water treatment applications. The output is the difference between the input voltage source and the capacitor in the above circuit diagram in the converter presented. The proposed converter consists of a DC voltage source, two inductors, two capacitors, a MOSFET switch, two ideal diodes, and a load resistor. The capacitors are precharged to a voltage equal to the input voltage source.

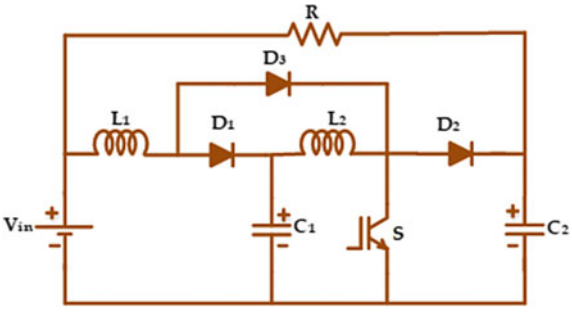


Fig. 1 Quadratic boost converter Ringing circuit

2.1 Operation of QBCRC

The operation of QBCRC is briefly discussed in this section with the circuit, 3 demonstrated in Figs. 2 and 3 in CCM and Fig. 4 in DCM. In the first mode of operation, the switch is conducting, the diode is forward biased, and the output voltage across the load is zero as the capacitor C_2 is precharged to the input voltage and load is connected across the source and capacitor C_2 and measures the difference between the two terminals.

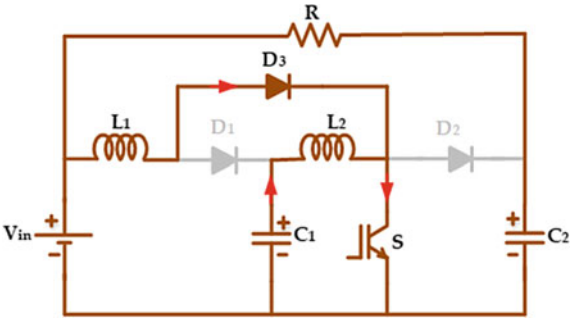


Fig. 2 QBCRC, switch ON CCM operation

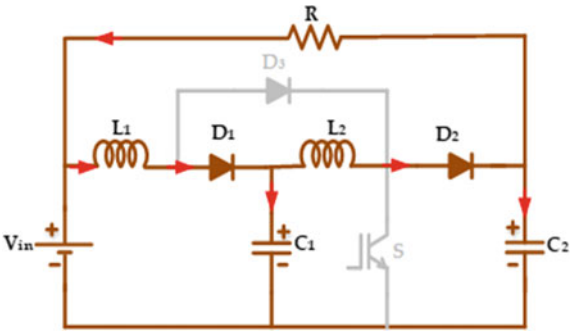


Fig. 3 QBCRC, switch OFF CCM operation

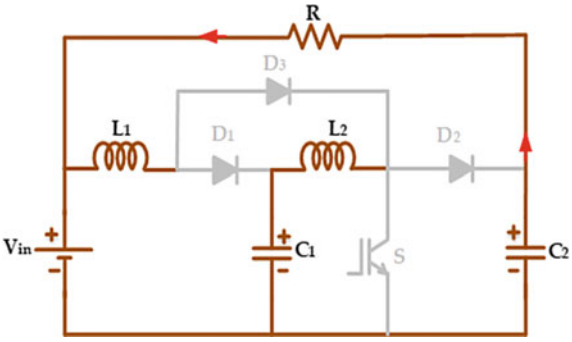


Fig. 4 QBCRC diodes and switches are turned OFF DCM operation

Two diode D_1 and diode D_3 are conducting in mode, and a voltage peak is obtained in this mode. The switch is not conducting in this mode. The output is only obtained in this mode. In this mode, the circuit is a fourth-order passive circuit.

In this state, neither the switch nor the diodes are conducting. When the inductor current approaches zero in mode 2, the diodes are reverse biased and cease conducting. In this mode, the equivalent circuit resembles a primary RC circuit, and the capacitor charges. The voltage output in mode 3 is zero.

2.2 Analysis of QBCRC

In mode 1, only diode D_2 is allowing the current to flow through it, whereas diodes D_1 and D_3 hinder the flow of current and the switch is open. The load resistor is differentially linked across input and C_2. The output voltage is zero in this mode.

$$V_{L1} = V_{in} \tag{1}$$

$$V_R = V_{in} - V_{C2} \tag{2}$$

$$I_{L1} = \frac{V_{in} t_L}{L} \tag{3}$$

The output voltage in Mode 1 is zero as the load is connected differentially across the input voltage source C_2, which is precharged to V_{in}.

$$V_{c1} = V_{in} + V_{L1} \tag{4}$$

$$V_{c2} = V_{c1} + V_{L2} \tag{5}$$

$$V_r = V_{l1} + V_{l2} \tag{6}$$

$$I_{L1} = I_{L2} - I_{C1} \tag{7}$$

$$I_{L2} = I_{C1} + I_R \tag{8}$$

$$I_{C1} = C1 \frac{dV_{c1}}{dt} \tag{9}$$

$$i I_{L1} + C1L1 \frac{d^2 I_{l1}}{dt^2} + C2L1 \frac{d^2 I_{L1}}{dt^2} + C2L2 \frac{d^2 I_{L2}}{dt^2} = \frac{L1 dI_{L1}}{Rdt} + \frac{L2 dI_{L2}}{Rdt} \tag{10}$$

Similarly, the equations are obtained as shown above for other modes of operation. The above fourth-order differential equation has the result in the form given below.

$$y = C_1 y_1 + C_2 y_2 + C_3 y_3 \ldots C_{n-1} y_{n-1} + C_n y_n \tag{11}$$

where $y_1, y_2, \ldots, y_n$ are any n linearly autonomous solutions of equations.

To find the n unknown coefficients C_i, each n-th order equation, n initial conditions are required.

The capacitor discharges and reaches its precharged value in this phase. The output voltage equals zero, during this period the inductor current passes zero, when both the diodes are turned OFF.

$$V_r(t'') = V_{C2}(t'') + V_{in} \tag{12}$$

Accordingly, based on the fundamental principle of first-order circuits, the starting and final values of the capacitor voltage are stated as follows and calculated.

$$V_r(t'') = (V_x - V_{in})e^{-t''/RC} \tag{13}$$

3 Simulation Results of QBCRC

The input voltage is given as 5 V to the proposed QBCRC converter circuit and the output voltage is 85 V, which is 17 times the input voltage. Figure given below shows the load, capacitor voltage in the pulsed form and this has the capability to be extended for higher magnitude for the desired application. These waveforms are shown to match the low power-rated prototype results. The load voltage waveform is shown in Fig. 5.

The capacitor voltage is slightly higher than the load voltage because it stores some voltage during continuous mode. During continuous mode there is no voltage

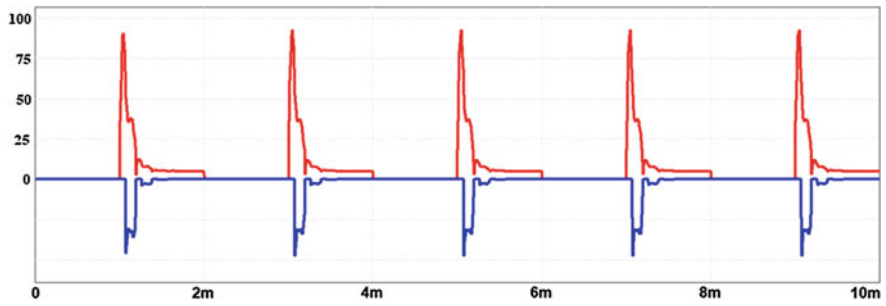


Fig. 5 Load voltage waveform

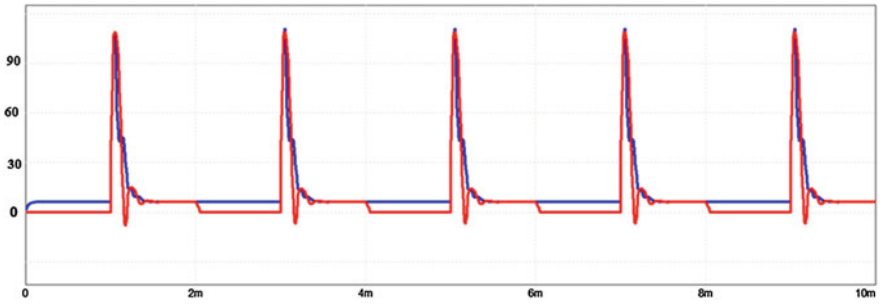


Fig. 6 Capacitor voltage waveform

as it is open circuit and during discontinuous mode there is pulsed output voltage. It is investigated that nearly the same current flows through the inductor and the switches prove the proposed theoretical concept of the converter.

The obtained voltage, inductor current, current, and voltage across the semiconductor switches waveforms shown in Figs. 6, 7, 8 and 9 guarantee successful operation of the converter.

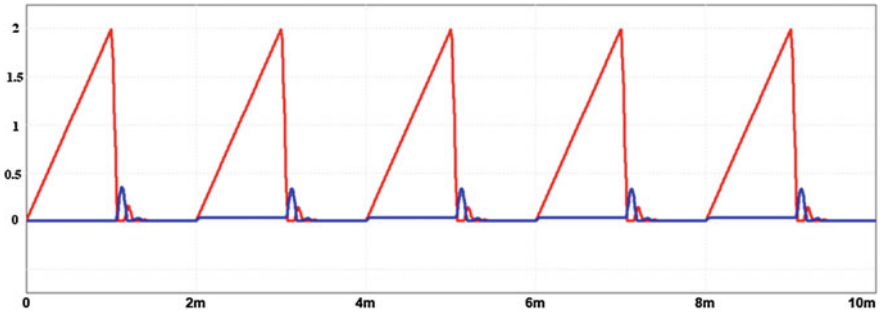


Fig. 7 Inductor current waveform

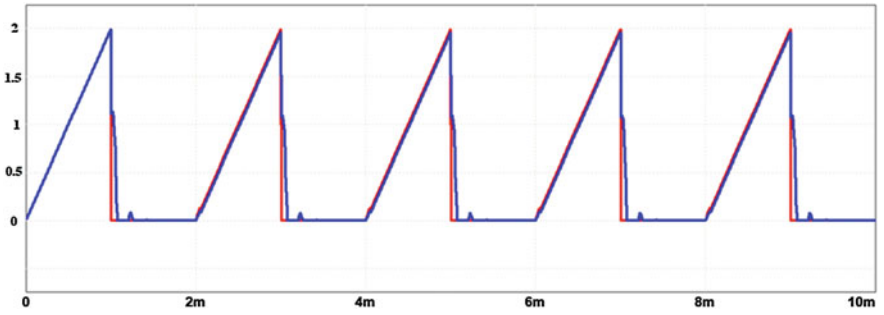


Fig. 8 Current through switches

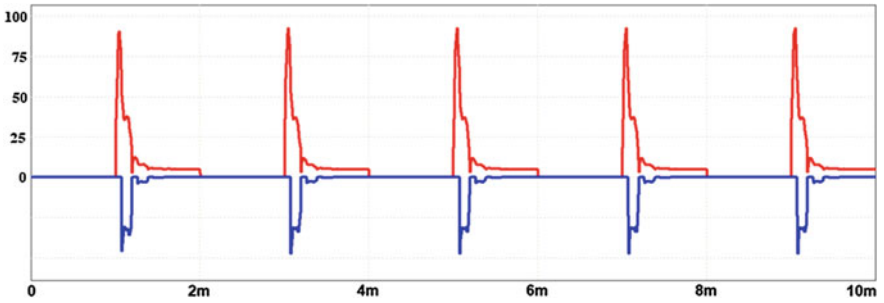


Fig. 9 Voltage across switches

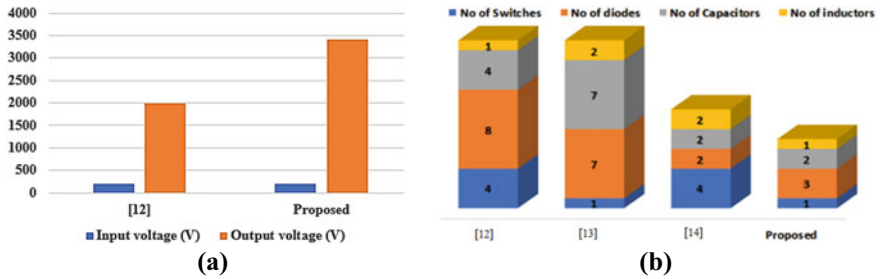


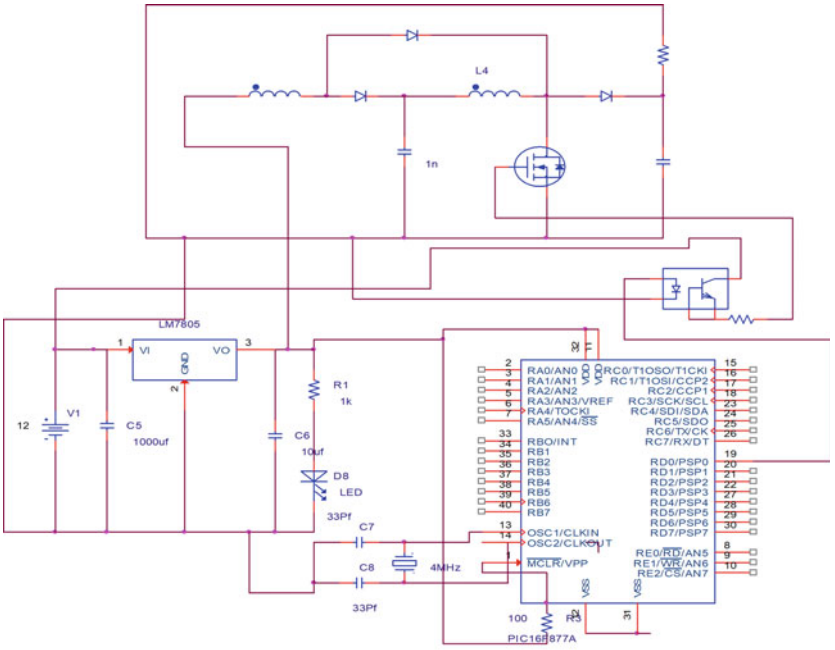
Fig. 10 Comparison of proposed with existing converters

It is examined from the results that the voltage across switch in OFF state is 85 V and it is equal to output voltage. The proposed converter generates chopped output voltage which is 17 times more than the input voltage and results in output pulses with the desired pulse width and repetition rate as illustrated in Fig. 10. This monotonous high voltage pulse generators are generally required for pulsed power wastewater treatment applications [3, 13].

4 Hardware of QBCRC

The hardware internal circuit and prototype are shown in Fig. 11. At first the voltage is supplied through battery. During mode 1, the voltage is zero as the circuit is in discontinuous mode and the diode is reverse biased. During mode 2, the diode is in forward conduction mode and the circuit is in continuous mode and the voltage is peak and it is high.

The predicted output of QBCRC is well matched to the simulation results (Fig. 5) obtained and validated through the measurements in prototype, and the photograph of the hardware in Fig. 11 shows the 17 times gain of the proposed converter.



(a)

(b)

Fig. 11 **a** Hardware internal circuit **b** QBCRC Prototype

5 Conclusion

Quadratic boost converter Ringing circuit is one of the most advanced proposed two-stage boost converters with a single switch topology for this high pulsed electric field applications. The proposed QBCRC circuit is operated in CCM and DCM. QBCRC is structured and operated without a transformer in the circuit or voltage multiplier cells to generate high voltage, proving the converter's superiority. QBCRC produces a high voltage pulsed output of 85 V, around 17 times the input voltage, confirming the theoretical expectations. The low voltage DC is converted to high pulsed output voltage, more appropriate for water treatment applications. Moreover, the converter's performance in simulation and experiment is carried out, and the results are presented. A good match between the designed converter circuit and the experimental results was observed.

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Static and Dynamic Analysis of IGBT Power Modules for Low and High-Power Range Electric Drives

A. Bharathsimha Reddy, S. N. Mahato, and Nilanjan Tewari

1 Introduction

Conduction and switching losses are the most significant losses in IGBT for medium and high-power applications. The life cycle of the power device will also be affected by the junction temperature of the IGBT [1]. This information will aid in the development of gate drive circuits and the prevention of avoidable errors in power electronic applications [2, 3]. The dynamic and static properties of the IGBT have been examined in this study and the important information for designing the gate drive circuit and fabricating power electronic equipment has been given [4–7]. The dynamic behavior of a high-power IGBT module is investigated in this research under various operating situations. In the studies, single pulse tests are utilized to examine the switching way of IGBT and body diodes under a variety of operating situations. A variety of gate-driving approaches for IGBT modules are investigated. Switching transients at different dc-link voltages and junction temperatures are also used to determine the IGBT modules' switching losses. The static and dynamic analysis of the IGBT has been discussed in depth in Sects. 2 and 3, respectively.

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2 Static Analysis

When the IGBT is switched-on, the V_{CE} fluctuates with the I_C, V_{GE}, and T_j. In the ON state, the V_{CE} signifies a collector emitter voltage drop that is used to calculate the IGBT's power dissipation loss. The lower the V_{CE} value, the smaller the power dissipation loss [8, 9]. As a result, the V_{CE} value of the IGBT must be as low as possible. The *V-I* characteristics of the IGBT is shown in Fig. 1.

V_{GE} should be kept at 15 V and collector current should be kept at or below the rated I_C current.

2.1 ON State

There are two distinctive curve sections in the forward on mode "V_{CE}" and +ve "I_C".

The turn-on and turn-off characteristics of the IGBT are discussed in [10].

The forward transconductance (g_{fs}) is a measurement of the transfer behavior seen in Fig. 1a.

$$g_{fS} = \frac{\Delta I_C}{\Delta V_{GE}} = \frac{\text{“}I_C\text{”}}{\text{“}V_{GE}\text{”} - \text{“}V_{GE(th)}\text{”}}$$

From above g_{fs}, α, I_C [$g_{fS} \alpha I_C$] decrease as chip temp rises [10]. The active region is only run through during switch-on and switch-off in the mode of the switching that is only permitted for power module's functioning with numerous IGBT chips linked in parallel. In this region, stationary module operation is not permitted since $V_{GE(th)}$

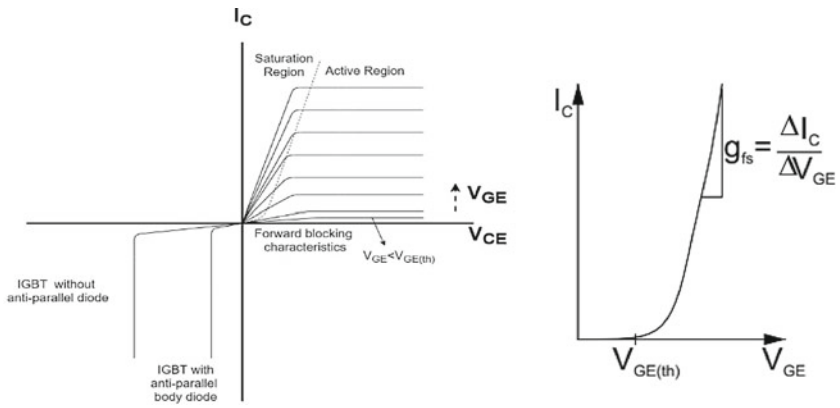


Fig. 1 **a** General static characteristics of the IGBT. **b** Transfer characteristics $I_C = f(V_{GE})$

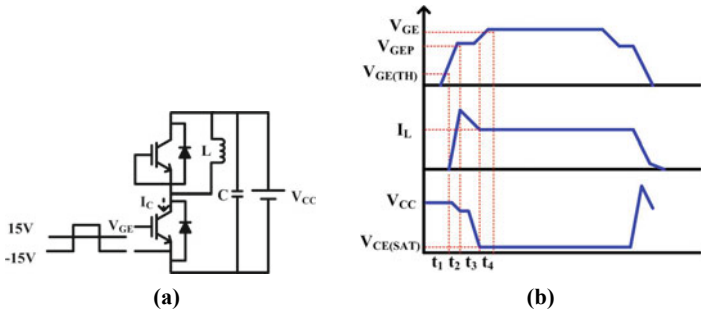


Fig. 2 **a** Switching characteristics measuring circuit. **b** Typical current and voltage waveforms of the IGBT during turn on and turn off

decreases as the temperature rises. This will cause the instability in temperature in each chip.

Saturation region:

The saturation area which corresponds to the ON-state during switching processes has been reached when the I_C is exclusively controlled by the outside circuit. The $V_{CE(sat)}$ of IGBT characterizes the on-state behavior (Fig. 2).

3 Dynamic Analysis of an IGBT Power Module

As the IGBT is so widely used for switching, it's critical to understand both the "turn-on" and "turn-off" switching characteristics in order to calculate "switching-loss". It's also worth remembering that while determining operating conditions, a variety of factors impact these features. The circuit depicted in Fig. 3a has been used to measure the four switching time parameters, *tr*, *ton*, *tf*, and *toff*, as illustrated in Fig. 3b.

The structure, internal capacitances, and internal and external resistances of IGBT power modules impact their switching behavior.

Internal resistances and capacitances influence/effects the IGBT's switching behavior. "C_{GC}" is low and near to "C_{CE}" when the IGBT is off. When V_{GE} surpasses the collector-emitter voltage during the on-state, "C_{GC}" quickly increases. Inversion in the enhancing layer directly under the gate regions causes this quick surge (Table 1).

Since the input and reverse transfer capacitance would grow dramatically in a fully switched transistor, this data can only be used to a limited degree to determine switching behavior.

The charging and discharging rates of the parasitic capacitances are determined by gate resistance. This will affect the IGBT's turn-on and turn-off times.

$$\tau = RC$$

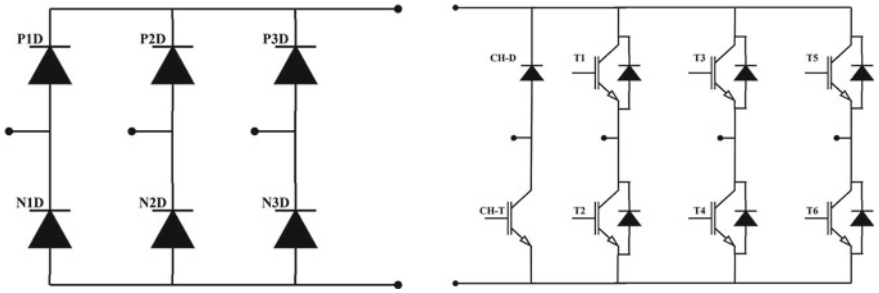


Fig. 3 Power module circuit diagram

Hard switching:

Hard switching occurs when both "I_C" and "V_{CE}" are high for a brief period of time between turn-on and turn-off. This is owing to the fact that a body diode in the load side prevents the current from shutting off as a response of the L_{load}.

IGBTs, unlike any other type of thyristor, can manage these states of operations without the use of passive snubber/filter circuits because of the "dynamic" junction that forms in the drift area during the switching conditions. However, with an IGBT, a significant portion of energy is dissipated during switching states.

$$E_{on,}E_{off} = \int v.idt$$

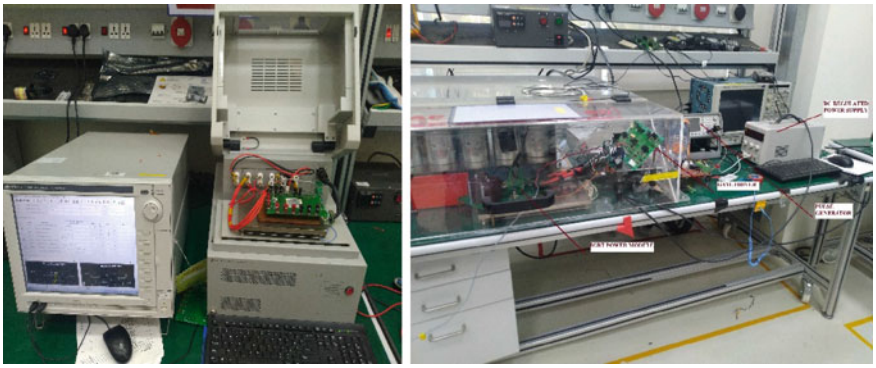
4 Hardware Implementation and Results

Static test is performed on 50 A, 600 V IGBT Power module. In this test, "$V_{CE(SAT)}$", $V_{GE(th)}$, Forward Voltage drop of Diode (V_F), Collector leakage Current I_{CES}, $I_{GES,}$ and diode (I_R) are measured at 25 and 150 °C (Fig. 4).

4.1 Static Analysis

VCE Measurement at 25 and 150 °C: $V_{CE(SAT)}$ measurements for three IGBT Power module samples S_1, $S_{2,}$ and S_3 are shown in Tables 2 and 3 at 25 °C and 150 °C, respectively. Figures 5 and 6 show the graphical representation of VCE measurements at different gate voltages at 25 °C and 150 °C, respectively.

It is seen from the tables and graphs that when junction temperature rises, so does VCE sat, and vice versa. Furthermore, by lowering the gate voltage, $V_{CE(SAT)}$



(a) **(b)**

Fig. 4 **a** Static analysis setup. **b** Dynamic analysis setup

Table 1 Low signal capacitances of IGBT

	IGBT
C_{input}	$C_{ies} = C_{GC} + C_{GE}$
C_{miller}	$C_{res} = C_{GC}$
C_{output}	$C_{oes} = C_{CE} + C_{GC}$

Table 2 V_{CE} measurement at 25 °C

$V_{CE(SAT)}$: $I_{CE} = 50$ A, $V_{GE} = 15$ V, $T_j = 25$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	1.81	1.82	1.85	1.82	1.86	1.88	1.96
S_2	1.95	1.99	1.89	2.05	2.01	2.08	2.02
S_3	1.95	1.95	1.99	1.84	1.99	2.01	2.08
Unit = volt							

Table 3 V_{CE} measurement at 150 °C

$V_{CE(SAT)}$: $I_{CE} = 50$ A, $V_{GE} = 15$ V, $T_j = 150$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	2.14	2.27	2.3	2.39	2.27	2.32	2.46
S_2	2.19	2.19	2.3	2.3	2.21	2.31	2.46
S_3	2.26	2.25	2.33	2.28	2.36	2.26	2.43
Unit = volt							

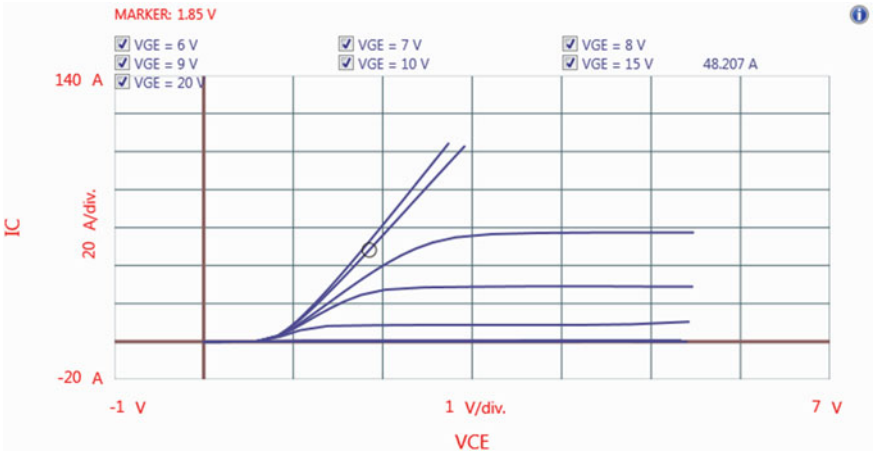


Fig. 5 Graphic plot of $V_{CE(SAT)}$ at 25 °C

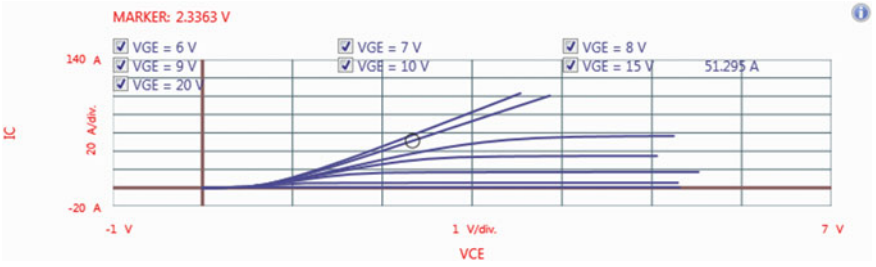


Fig. 6 Graphic plot of $V_{CE(SAT)}$ at 150 °C

will rise. The junction temperature can be managed with the right gate voltage and $V_{CE(SAT)}$. As a result, the power module's life expectancy will be extended.

***$V_{GE(th)}$* measurement at 25 and 150 °C**: Tables 4 and 5 provide $V_{GE(th)}$ measurements for three IGBT Power module samples S_1, S_2, and S_3 at 25 °C and 150 °C, respectively. Figures 7 and 8 exhibit graphical representations of $V_{GE(th)}$ measurements at various gate voltages at 25 °C and 150 °C, respectively.

The gate-emitter threshold voltage will drop as the temperature rises in the IGBT junction, as shown in the tables and figures above. Breakdown at the gate-emitter junction may occur as a result of this.

VF measurement of body diode at 25 and 150 °C: Tables 6 and 7 show V_f measurements of three IGBT Power module samples S_1, S_2, and S_3 at 25 °C and 150 °C, respectively. Figures 9 and 10 exhibit graphical representations of V_f measurements at various gate voltages at 25 °C and 150 °C, respectively.

The V_F drop of the body diode has increased as the junction temperature (T_j) increases.

Table 4 $V_{GE(th)}$ measurement at 25 °C

$V_{GE(th)}$: $I_c = 0.8$ mA, $V_{GE} = V_{CE}$, $T_j = 25$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	5.94	5.91	5.96	5.91	5.91	5.89	5.85
S_2	5.93	5.97	5.95	5.96	5.96	5.96	5.93
S_3	5.92	5.88	5.91	5.91	5.92	5.96	5.88
Unit = volt							

Table 5 $V_{GE(th)}$ measurement at 150 °C

$V_{GE(th)}$: $I_c = 0.8$ mA, $V_{GE} = V_{CE}$, $T_j = 150$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	3.86	3.63	3.72	3.59	3.61	3.56	3.31
S_2	3.17	3.36	3.57	3.31	3.18	3.26	3.28
S_3	3.82	3.7	3.82	3.49	3.88	3.79	3.66
Unit = volt							

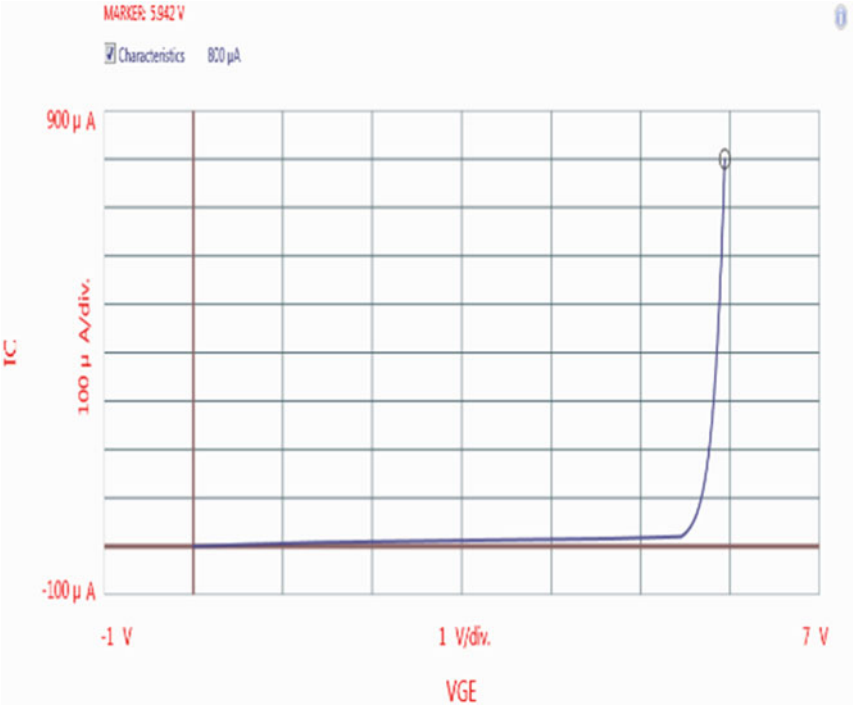


Fig. 7 Graphic plot of $V_{GE(th)}$ at 25 °C

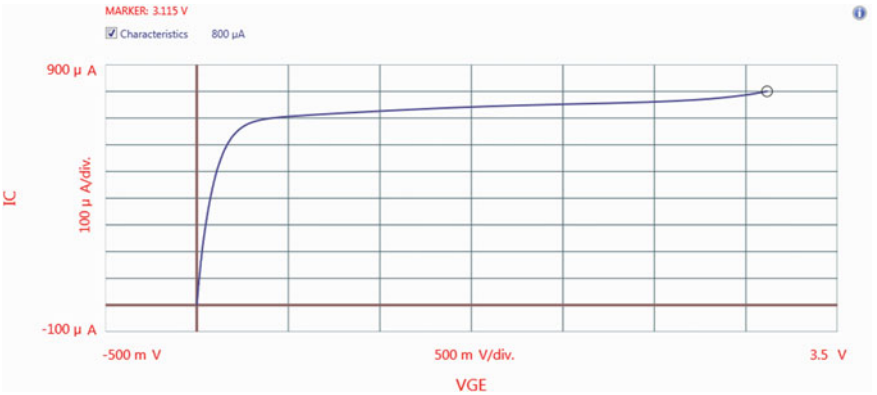


Fig. 8 Graphic plot of $V_{GE(th)}$ at 150 °C

Table 6 V_f measurement at 25 °C

$V_F, I_F = 50$ A for D_1–D_6, $T_j = 25$ °C						
Initial measurements						
Sample	D_1	D_2	D_3	D_4	D_5	D_6
S_1	1.95	1.82	1.85	1.82	1.86	1.88
S_2	2.13	2.16	2.04	2.22	2.17	2.17
S_3	2.12	2.11	2.13	2.26	2.17	2.24
Unit = volt						

Table 7 V_f measurement at 150 °C

$V_F, I_F = 50$ A for D_1–D_6, $T_j = 150$ °C						
Initial measurements						
Sample	D_1	D_2	D_3	D_4	D_5	D_6
S_1	1.89	2.01	2.03	2.12	2.02	2.11
S_2	1.94	1.96	2.03	2.06	1.97	2.12
S_3	2.04	2.02	2.08	2.08	2.14	2.11
Unit = volt						

***I_{CE}* measurement at 25 and 150 °C**: I_{CES} measurements for three IGBT Power module samples S_1, S_2, and S_3 are shown in Tables 8 and 9 at 25 °C and 150 °C, respectively.

***I_{CE}* measurement at 25 and 150 °C**: I_{GES} measurements for three IGBT Power module samples S_1, S_2, and S_3 are shown in Table 10 and Table 11 at 25 °C and 150 °C, respectively.

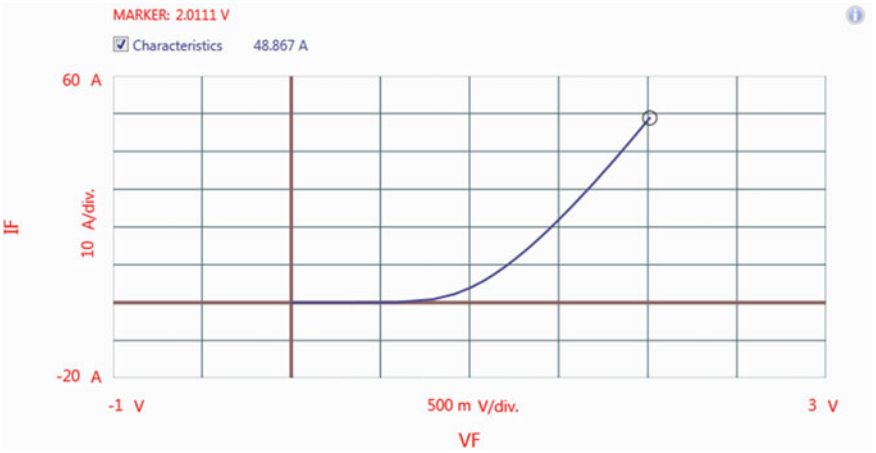


Fig. 9 Graphic plot of V_f at 25 °C

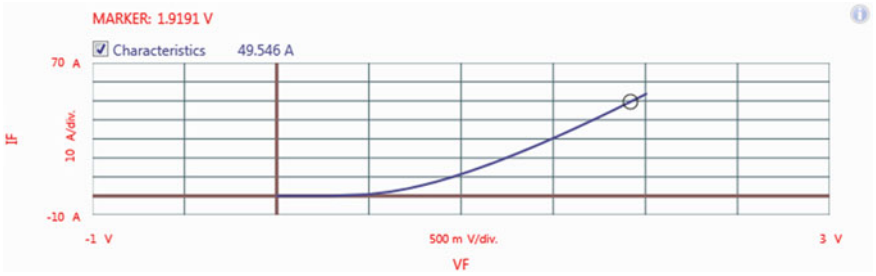


Fig. 10 Graphic plot of V_f at 150 °C

Table 8 I_{CES} measurement at 25 °C

I_{CES}: $V_{CE} = 600$ V, $V_{GE} = 0$, $T_j = 25$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	5.94	5.91	5.96	5.91	5.91	5.89	5.85
S_2	5.93	5.97	5.95	5.96	5.96	5.96	5.93
S_3	5.92	5.88	5.91	5.91	5.92	5.96	5.88
Unit = nA							

According to the static analysis, the gate voltage and junction temperature have an impact on the performance of IGBT. For example, lowering the gate voltage raises the junction temperature, which raises the leakage current and the voltage. The gate's threshold voltage is reduced as the junction temperature rises.

Table 9 I_{CE} measurement at 150 °C

I_{CES}: $V_{CE} = 600$ V, $V_{GE} = 0$, $T_j = 150$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	0.966	1.15	1.14	1.18	1.17	1.2	1.33
S_2	1.344	1.344	1.324	1.367	1.404	1.374	1.566
S_3	0.980	1.0501	0.965	1.281	0.973	1.0254	1.2102
Unit = nA							

Table 10 I_{GES} measurement at 25 °C

I_{GES}: $V_{GE} = \pm 20$ V, $T_j = 25$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	96.1	98	99	96	115	106	160
S_2	105	167	96.5	184	89.5	164	144
S_3	83	109	81.7	124	108	138	101
Unit = pA							

Table 11 I_{GES} measurement at 150 °C

I_{GES}: $V_{GE} = \pm 20$ V, $T_j = 150$ °C							
Initial measurements							
Sample	T_1	T_2	T_3	T_4	T_5	T_6	*CH-T*
S_1	280	303	255	255	908	247	231
S_2	246	338	190	324	203	222	301
S_3	298	395	179	2.67n	4.44n	948	101
Unit = pA							

4.2 Dynamic Analysis

Dynamic analysis was performed in three different gate resistances of 3.5, 12, and 22 Ω, as well as at 25 and 125 °C (Figs. 11, 12, 13 and 14).

From the dynamic analysis, it is seen that the switch-on time, switch-off time, and blanking time are all determined by the R_g of the IGBT. From Tables 12 and 13, it is found that when gate resistance is low, the IGBT's on and off times are shorter. The IGBT takes longer time to switch on and off when the gate resistance is large.

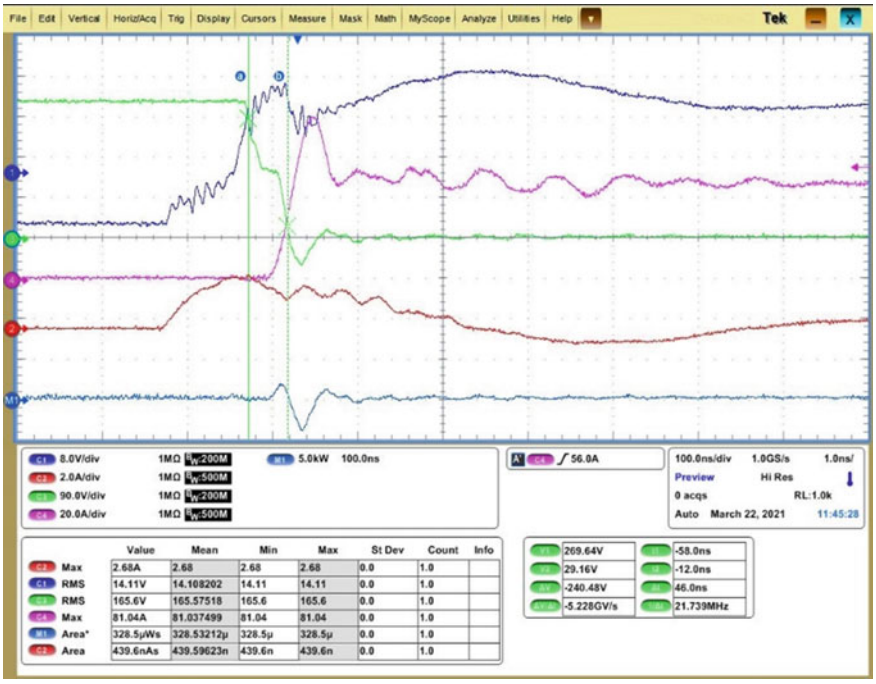


Fig. 11 Turn on wave form with $R_g = 3.5\ \Omega$ at 25 °C

When gate resistance is high, charging and discharging of C_G is slow; when gate resistance is low, charging and discharging of C_G is quick. When gate resistance is low, the voltage and current fluctuations with respect to time are greater, and when gate resistance is more, the voltage and current variations with respect to time are less. From Tables 12 and 13, it is understood that the value of the gate resistance is having impact on peak current, peak voltage, and reverse recovery characteristics of the IGBT.

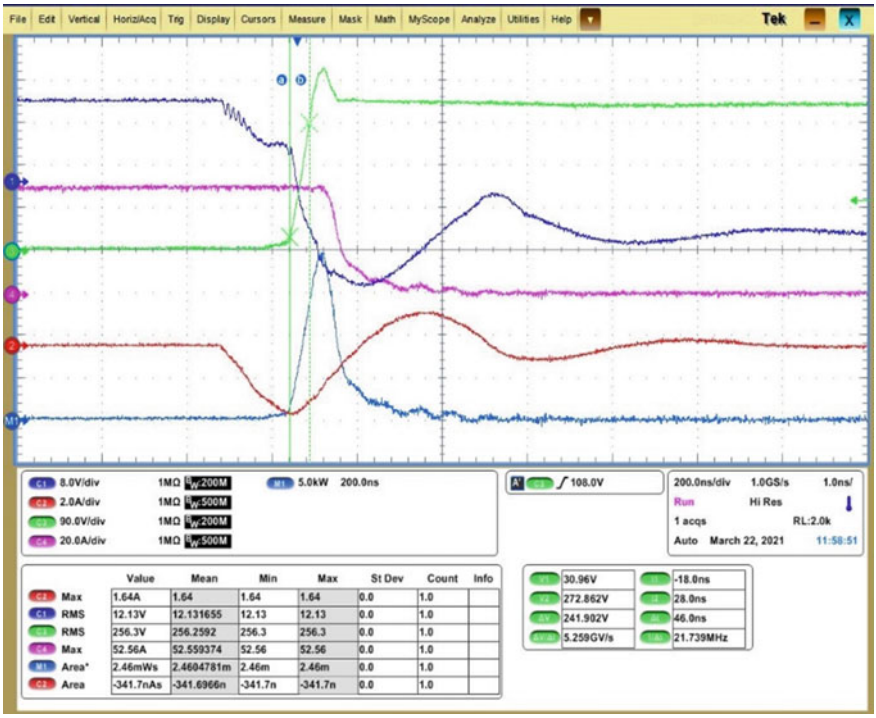


Fig. 12 Turn off wave form with $R_g = 3.5\ \Omega$ at 25 °C

The dynamic test was carried out at two distinct temperatures (25 and 125 °C). The energy loss is greater when the ambient temperature reaches 125 °C according to the test. The reverse recovery time is influenced by the ambient temperature. When the ambient temperature is higher, the reverse recovery period is longer.

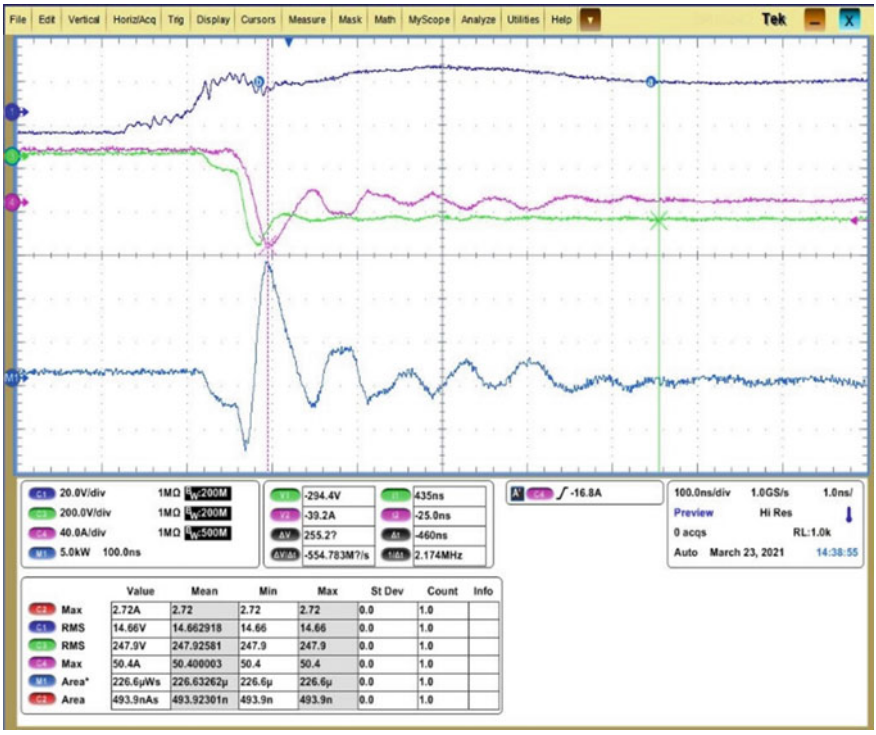


Fig. 13 Turn on wave form with $R_g = 3.5\ \Omega$ at 125 °C

5 Performance Analysis with Respect to Speed

The efficiency of electric drives is entirely dependent on the motor's speed and torque. When the drive operates at low speed and torque, the efficiency is reduced. Table 14 shows a comprehensive study of the drive at various speeds and torques. It is found that raising the speed and torque till the rated values increases the efficiency of the drive.

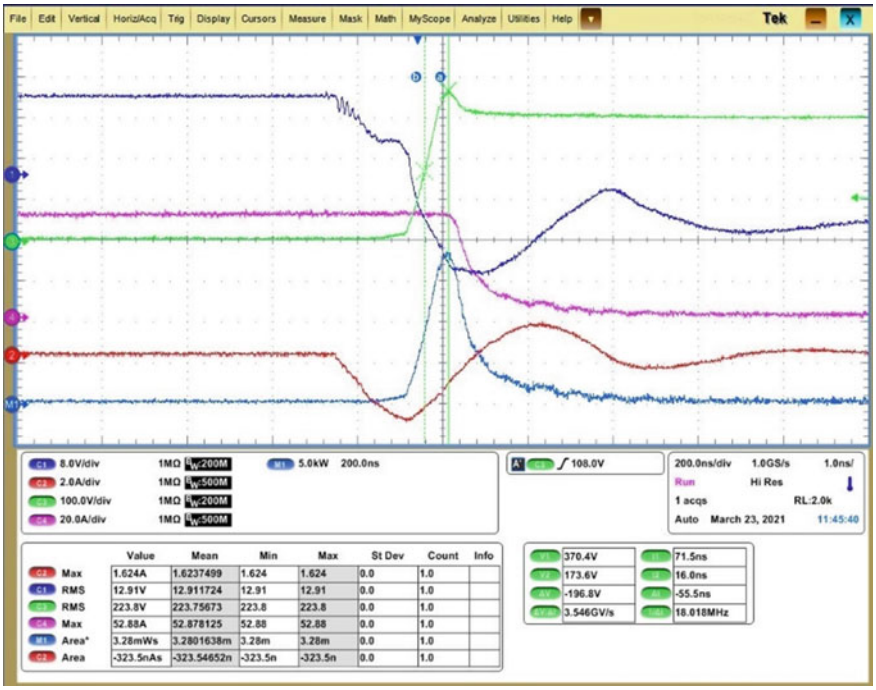


Fig. 14 Turn off wave form with $R_g = 3.5\ \Omega$ at 125 °C

6 Conclusion

The influence of the gate resistance on circuit characteristics is first examined in this study. Based on the discussions, some recommended resistor values have been determined for various applications, which can be used as a starting point for optimization. In any case, the final value is utilized to test the circuit in concern. Simultaneously, an example on how to pick appropriate drive modules for the determined R_g value is shown. Finally, several circuit layout methodologies and concepts have been discussed in brief. Total losses are minimized by maintaining the optimum saturation voltage across the collector and the emitter and the rated gate voltages. This information might be useful to the circuit designers. The junction temperature, gate

Table 12 Dynamic test results at 25 °C

25 °C				
	R ohms	3.5	12	22
Energy loss	*Eon* mJ	0.3285	0.2949	1.288
	Eoff mJ	2.826	2.246	2.335
Gate charge	*Qg* on nC	439.6	340	330.2
	Qg off nC	−338.9	−363.7	−345.3
Reverse recovery	*Err* mJ	0.2266	0.3394	0.093
	Qrr nC	493.9	491.9	585.3
Time	*trr* ns	54	58	132
	tr ns	22.5	31.4	140
	tf ns	99.5	140	189.5
	tdon ns	44	49.1	74
	td off ns	244	296	408.5
	Ip (A)	81.036	76.4	63.44
	Vp (V)	389.52	377.6	405.6
	Irp (A)	−44.128	−30.8	−15.77
	di/*dt* on	1.826 GA/s	1.25 GA/s	0.78 GA/s
	di/*dt* off	−393 MA/s	−290 MA/s	−0.4 GA/s
	dv/*dt* on	−5.2 GV/s	−3.97 GV/s	−1.3 GV/s
	dv/*dt* off	−5.26 GV/s	5.02 GV/s	3.3 GV/s
	dv/*dtr*	−5.64 GV/s	−5.6 GV/s	−1.7 GV/s

voltage, and gate resistance should all be kept within a certain range for improved IGBT performance, as stated in this work.

Table 13 Dynamic test results at 125 °C

125 °C				
	R ohms	3.5 Ω	12 Ω	22 Ω
Energy loss	*Eon* mJ	0.362	0.432	1.492
	Eoff mJ	3.28	2.248	2.836
Gate charge	*Qg* on nC	416.7	331	326.8
	Qg off nC	−323.5	−368.98	−353.4
Reverse recovery	*Err* mJ	1.34	1.15	0.939
	Qrr nC	493.2	500	344.9
Time	*trr* ns	162	164.5	318.5
	tr ns	24	31.2	57.5
	tf ns	167	171	169.5
	tdon ns	45	53.2	74.5
	td off ns	272	329.5	442.5
	Ip (A)	93.6	94	74
	Vp (V)	370	374.4	383.18
	Irp (A)	−59.4	−49.56	−31.8
	di/*dt* on	1.655 GA/s	1.295 GA/s	699 MA/s
	di/*dt* off	−240 MA/s	−233 MA/s	−241 MA/s
	dv/*dt* on	−3.9 GV/s	−3.1 GV/s	−1.1 GV/s
	dv/*dt* off	3.87 GV/s	3.94 GV/s	2.81 GV/s
	dv/*dtr*	−4.29 GV/s	−4.19 GV/s	−1.44 GV/s

Table 14 Performance of electric drive at various speeds and loads

Test no.	Line voltage (V RMS)	Motor frequency (% of nom. freq)	Load/torque (% of NO)	Output current (A)	Motor speed (RPM)	Input power (kW)	Output power (kW)	Loss (W)	Efficiency (%)
1	400	20	25	16.4	306	1.2	1.056	0.144	88.00
2		20	50	19.6	312	2.24	2.058	0.182	91.88
3		20	75	24	316	3.26	3.018	0.242	92.58
4		20	100	29.3	320	4.3	4	0.3	93.02
5		50	25	16.6	735	2.75	2.58	0.17	93.82
6		50	50	20.5	742	5.13	4.91	0.22	95.71
7		50	75	26.2	747	7.62	7.31	0.31	95.93
8		50	100	31.7	752	9.87	9.47	0.4	95.95
9		100	25	16.6	1466	5.05	4.88	0.17	96.63
10		100	50	21	1471	9.92	9.69	0.23	97.68
11		100	75	27	1478	14.7	14.38	0.32	97.82
12		100	100	33.1	1485	19.9	18.76	1.14	94.27

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Implementation of Multilevel Inverter with Reduced Switching Components

Albert Alexander Stonier and M. Yazhini

1 Introduction

Multilevel inverters are used to synthesize near-sinusoidal voltage from several levels of DC voltage. Multiple levels are used to reduce THD (total harmonic distortion). In [1], fewer switches are employed, resulting in decreased voltage stress across them. In this configuration, there are eight switches and three voltage sources. SHEPWM (selective harmonic elimination pulse width modulation technique) is used to enhance voltage by reducing lower order harmonics by using a smaller number of DC voltage sources. The paper [2] proposes a 15-level multilevel inverter with fewer power electronic components and a standard boost converter to achieve greater DC-link voltage. Eight BJT, three DC source and staircase PWM technique is implemented. Higher efficiency and less THD are obtained from its output. It suits for grid connected and FACTS applications. The method elucidated in [3] is to reduce the cost and inverter size uses lower switch count and obtain 21-level MLI. P&O-algorithm-based MPPTs are used for getting more power and then stable output is achieved irrespective of partial shaded condition. THD is 3.49%, efficiency = 94.21%, and alpha = 3.14. From the value of alpha, it shows the cost of inverter is very less compared with various topologies. In paper [4], four voltage source, ten switches

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are used for generating 17 level. With the help of three cascading approaches the efficiency is 98.8% and the cost of the inverter is also reduced.

In [5], the work presents a single-phase multilevel inverter. Cascading of modular structure is used for reducing the components. Advantage of this paper is without using H-bridge inverter, it generates positive and negative voltages. 31 level is obtained from ten switch and five voltage source. In [6], new multilevel inverter is invented with the name of envelope type (E type). With the help of this inverter, 13-level output is generated. It is used in high-voltage, high-power application with unequal DC source. Without H-bridge this MLI generates both positive and negative output levels. THD is 3.46 which satisfies the standard (IEEE519). In [7], topology termed as packed U cell multilevel inverter is used to restrict maximum output voltage, high-voltage stress on switch, and limited performance to low-voltage application. Each cascade module uses 2 DC sources and 30 switches are used in each U cell.

In [8], the paper presents modular multilevel inverter with the aim of reducing switch count and the number of DC voltage source. Selective harmonic elimination technique is used to produce the pulse for multilevel inverter. In this paper 71 levels are obtained by combining two basic units. One basic unit provides 11 levels. Basic unit contains eight switches with three DC voltage sources. In [9], the paper generate 25 levels of output voltage with the help of two dc sources and ten power switches. This paper gives an idea about multilevel inverter which will help to reduce the number of switching components and the number of DC source, standing voltage across the switches. In [10], the paper presents the improving of the voltage quality and reducing the inverter size for the symmetric and asymmetric multilevel inverter. For asymmetric MLI, selective harmonic elimination and flower pollination algorithm were used. Ten power switches and two DC sources were used. By using this method we can easily eliminate the 3rd- to 11th-order harmonics easily. In [11], the paper deals with reduced harmonic distortion and low-voltage rating of the switches, small filter size but it contains some fewer drawbacks. They are using more number of switching component and control strategy is difficult. The major advantage is reduced cost and complexity. With the help of 8 switches this paper produces 11 levels as output voltage. Efficiency of proposed methodology is 97.5% and output power is 1 kW. In [12], paper deals with the switched-diode dual source single switch multilevel inverter. It requires lower switch count compared to other multilevel inverters. Fish swarm optimization technique is used for eliminating the harmonics from the output voltage. In [13], the topology offers a made-stride cascaded multilevel inverter based on a profoundly productive and stable setup for spilled current mitigation. The suggested architecture, when combined with the provided PWM approach, reduces high-frequency voltage changes inside the terminal and common-mode voltages. Keeping a strategic distance from high-frequency voltage movements reduces leakage current and keeps it within the range of EMI filters. Furthermore, the suggested CMLI is expanded along with the PWM method for $2m + 1$ levels, where m represents the number of photovoltaic sources. For all $2m + 1$ levels of operation, the suggested PWM process necessitates the use of a single carrier wave. When coupled in solar control frameworks, the quasi-Z-source cascade multilevel inverter

exhibits several advantages over conventional CMI, according to [14]. The qZS-CMI (quasi-z source cascade multilevel inverter), for example, provides the adjusted DC-link voltage and voltage boost capacity, saves one-third of the modules, and so on. In any scenario, the qZS-CMI is still unable to overcome the lattice's discontinuous and stochastic fluctuation due to sun-based control. This research presents a PV control generation system based on qZS-CMI that stores energy. The framework integrates the qZS-CMI and vitality capacity by including an energy storage battery in each module to correct the stochastic models of PV control. This research also presents a control plan for a qZS-CMI-based PV (photovoltaic) system that stores energy. The suggested architecture may achieve the most extreme power point track for PV in a scattered manner. In [15], it looks at a single-phase cascading multilevel inverter made up of complete NPC (neutral point clamp) bridges for renewable energy frameworks. The advancement of the control procedure is predicated on the use of the show prescient control procedure to assemble the needed determinations of the individual voltage level control of each partitioned DC source and the unbiased point potential adjustment under unity power calculation. Two partitioned PV strings are regulated while being subjected to temporal variations linked to deviating string circumstances in terms of solar radiation and reference voltage variation, demonstrating the feasibility of the constructed controller. The ideal consonant ventured waveform approach is suggested in [16] to dispose of the specific consonant orders available at the yield of a cascaded multilayer inverter driven by solar energy. This approach is used to decipher the consonant elimination equations using experimental waveform analysis in order to find the best exchanging places and so reduce whole consonant mutilation. In each half cycle, the SHEPWM method treats the yield voltage waveform as four equal symmetries. A sun-powered, 15-level cascaded multilevel is examined as part of the suggested method, with the size of six consonant orders being lowered. A programmed switching pulse generator is designed to deliver the exchanging points to the semiconductor switches obtained as a result of the semiconductor switches.

In [17], an inverter topology is detailed that is competent to function palatably with wide variety in DC interface voltage, whereas nourishing control to the ac network. A topological building piece is to begin with presented that has one full bridge inverter associated in arrangement with a level multiplying arrange. Taking after this, the interconnection of such building pieces is endeavored to extend the number of levels at the yield voltage waveform. The examination uncovers that for a three-phase framework, a converter setup with two such building blocks is competent to create a ostensible asymmetry of 14:7:2:1 utilizing as it were four voltage sources. In sun-based PV applications, one primary source may be encouraged by PV cluster and the other three assistant sources may be encouraged through isolated DC/DC converters, each having control rating of 3.2% of the top control rating of PV arrays. The proposed converter can create 3097 space vectors. Hilter kilter hexagonal deterioration is adjusted (to guarantee palatable operation of LDN and to dispense with any DC component within the stage voltage waveform) to control such converter. The converter is broadly mimicked in MATLAB/Simulink. A sun-powered PV system of 9.4 kWp accessible within the research facility is utilized to bolster control to the lattice at distinctive irradiance. Recreation comes about coordinating well with

the model tests affirming the convenience of the proposed topological elective for sun-oriented PV applications.

In [18], it gives a hypothetical dialog and comparison in vitally adjusting between a measured multilevel cascade inverter based on single-star bridge cells and that on single-delta bridge cells. Consideration is paid to applications including hilter kilter active-power era in utility-scale grid-tied photovoltaic frameworks. Both qualitative and quantitative assessment measurements to evaluate the energy-balancing capability are presented and connected to both SSBC and SDBC inverters. As for the SSBC inverter, six zero-sequence voltage waveforms with diverse consonant substance empowering enhanced energy-balancing capability are analyzed and compared regarding their adequacy. This paper too emphasizes on the SDBC as an elective to the SSBC, and highlights its predominant operating characteristics beneath hilter kilter active-power era.

2 Proposed Method

2.1 Block Diagram of Proposed Methodology

In proposed methodology, solar panel acts as input. Output of solar panel is given as input for reduced switch multilevel inverter. Multilevel inverter is controlled with the help of control circuit. Then, finally, the output of inverter is fed back to the load (Fig. 1).

3 Reduced Switch Multilevel Inverter

Switching sequence (Fig. 2):

Level 1—Switches 2, 3, 5, 7
Level 2—Switches 2, 3, 5, 8
Level 3—Switches 1, 3, 7, 5
Level 4— Switches 1, 3, 5, 8
Level 5—Switches 2, 3, 6, 7

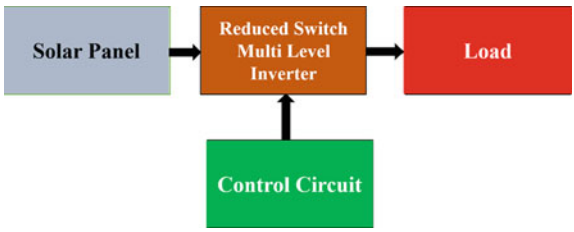

Fig. 1 Block diagram of proposed method

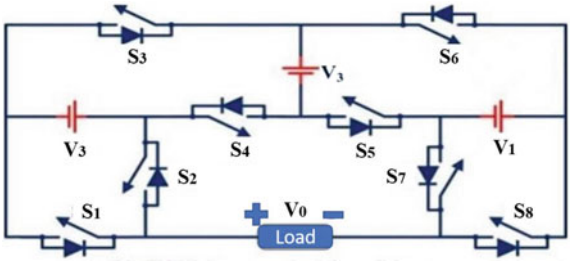

Fig. 2 Circuit diagram of reduced switch multilevel inverter

Level 6—Switches 2, 3, 6, 8
Level 7—Switches 1, 3, 6, 7
Level 8—Switches 2, 4, 5, 7
Level 9—Switches 2, 4, 5, 8
Level 10—Switches 1, 4, 5, 7
Level 11—Switches 1, 4, 5, 8
Level 12—Switches 2, 4, 6, 7
Level 13—Switches 2, 4, 6, 8
Level 14—Switches 1, 4, 6, 7
Level 15—Switches 1, 4, 6, 8.

3.1 Modes of Operation

3.1.1 Mode 1

During this mode, switches 3, 2, 5, 7 are turned ON, across the load, voltage sources V2, V3 are added and give the output voltage as 200 V. The current path is indicated in red lines (Fig. 3).

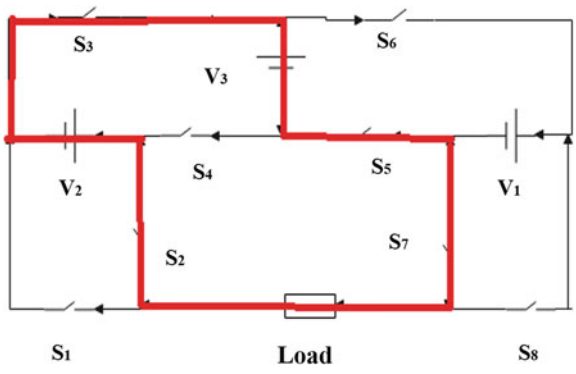

Fig. 3 Mode 1

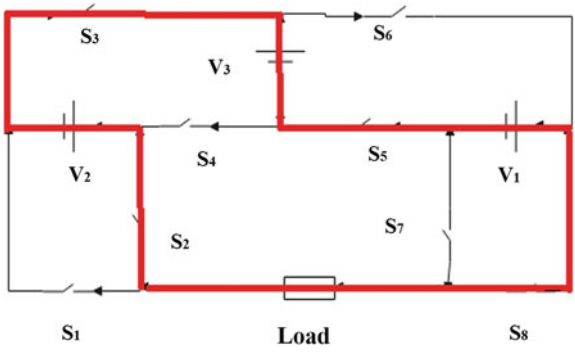

Fig. 4 Mode 2

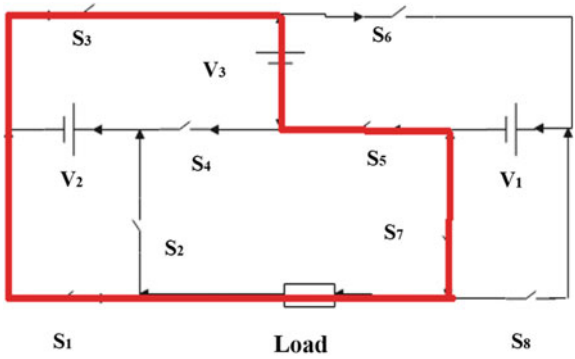

Fig. 5 Mode 3

3.1.2 Mode 2

During this mode, switches 3, 2, 5, 8 are turned ON, across the load, voltage sources—V1, V2, V3 are added and give the output voltage as 175 V. The current path is indicated in red lines (Fig. 4).

3.1.3 Mode 3

During this mode, switches 3, 1, 5, 7 are turned ON, across the load, voltage source V3 is added and gives the output voltage as 150 V. The current path is indicated in red lines (Fig. 5).

3.1.4 Mode 4

During this mode, switches 3, 1, 5, 8 are turned ON, across the load, voltage sources −V1, V3 are added and give the output voltage as 125 V. The current path is indicated in red lines (Fig. 6).

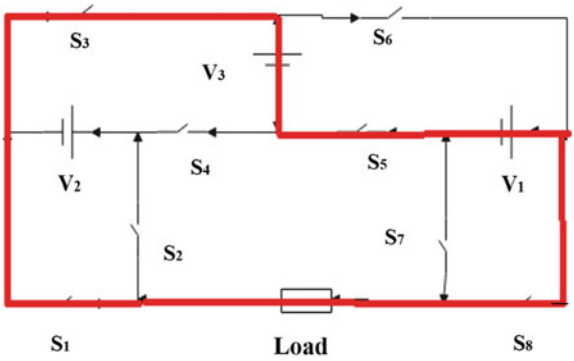

Fig. 6 Mode 4

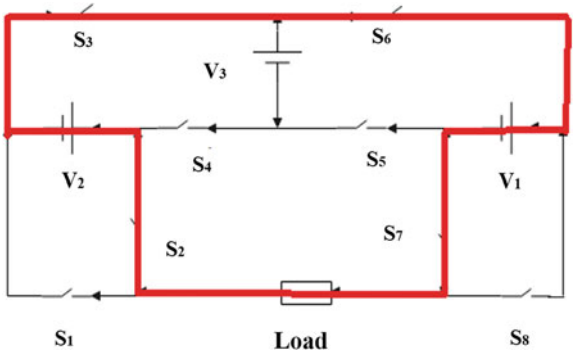

Fig. 7 Mode 5

3.1.5 Mode 5

During this mode, switches 3, 2, 6, 7 are turned ON, across the load, voltage sources V1, V2 are added and give the output voltage as 75 V. The current path is indicated in red lines (Fig. 7).

3.1.6 Mode 6

During this mode, switches 3, 2, 6, 8 are turned ON, across the load, voltage source V2 is added and gives the output voltage as 50 V. The current path is indicated in red lines (Fig. 8).

3.1.7 Mode 7

During this mode, switches 3, 1, 6, 7 are turned ON, across the load, voltage source V1 is added and gives the output voltage as 25 V. The current path is indicated in red lines (Fig. 9).

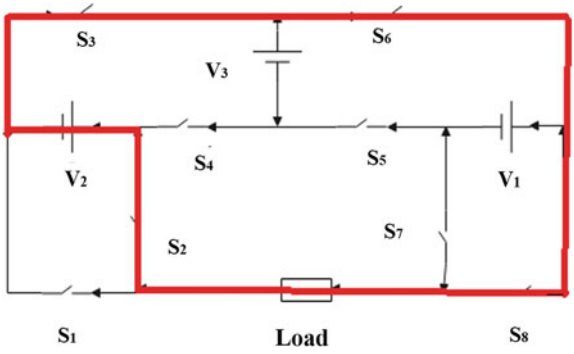

Fig. 8 Mode 6

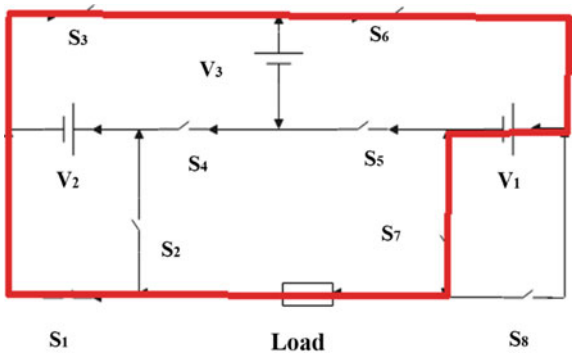

Fig. 9 Mode 7

3.1.8 Mode 8

During this mode, switches 4, 2, 5, 7 are turned ON, across the load, no voltage source is connected so it gives the output voltage as 0 V. The current path is indicated in red lines (Fig. 10).

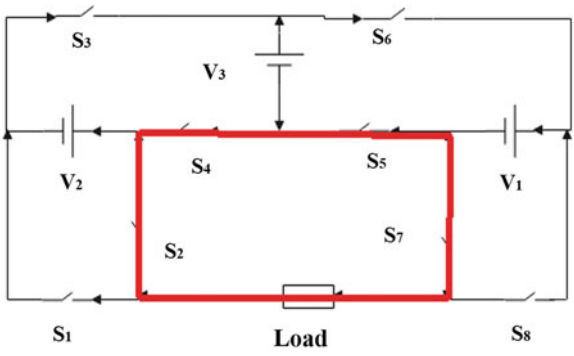

Fig. 10 Mode 8

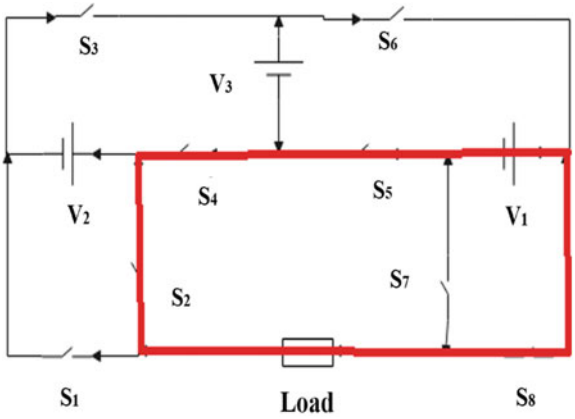

Fig. 11 Mode 9

3.1.9 Mode 9

During this mode, switches 4, 2, 5, 8 are turned ON, across the load, voltage source −V1 is added and gives the output voltage as −25 V. The current path is indicated in red lines (Fig. 11).

3.1.10 Mode 10

During this mode, switches 1, 4, 5, 7 are turned ON, across the load, voltage source –V2 is added and gives the output voltage as −50 V. The current path is indicated in red lines (Fig. 12).

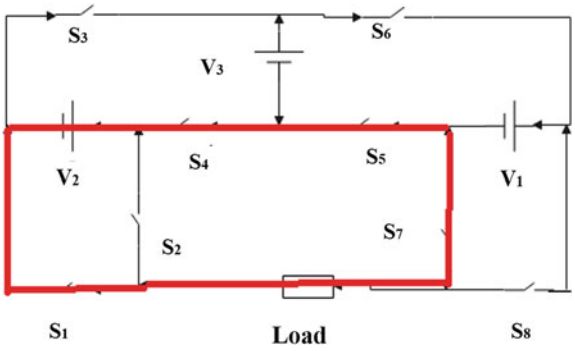

Fig. 12 Mode 10

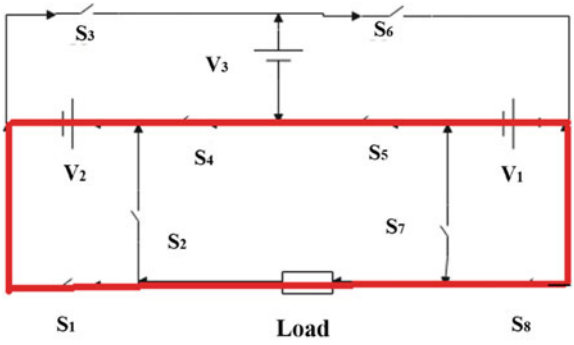

Fig. 13 Mode 11

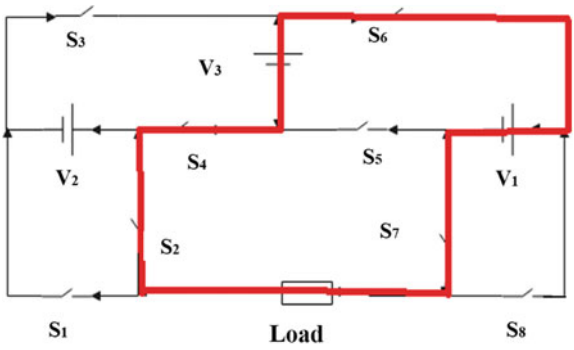

Fig. 14 Mode 12

3.1.11 Mode 11

During this mode, switches 4, 1, 5, 8 are turned ON, across the load, voltage sources –(V1, V2) are added and give the output voltage as −75 V. The current path is indicated in red lines (Fig. 13).

3.1.12 Mode 12

During this mode, switches 4, 2, 6, 7 are turned ON, across the load, voltage sources −(V1, V3) are added and give the output voltage as −125 V. The current path is indicated in red lines (Fig. 14).

3.1.13 Mode 13

During this mode, switches 4, 2, 6, 8 are turned ON, across the load, voltage source –V3 is added and gives the output voltage as −150 V. The current path is indicated in red lines (Fig. 15).

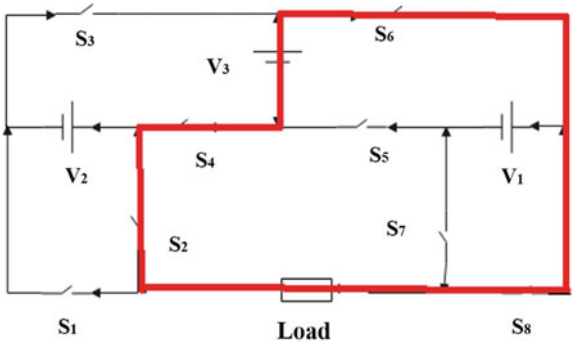

Fig. 15 Mode 13

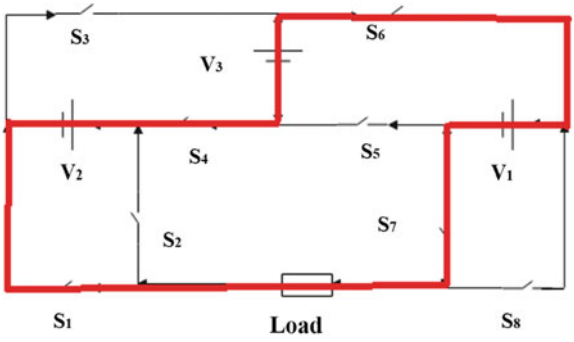

Fig. 16 Mode 14

3.1.14 Mode 14

During this mode, switches 1, 4, 6, 7 are turned ON, across the load, voltage sources −(V1, V2, V3) are added and give the output voltage as −175 V. The current path is indicated in red lines (Fig. 16).

3.1.15 Mode 15

During this mode, switches 1, 4, 6, 8 are turned ON, across the load, voltage sources –(V2, V3) are added and give the output voltage as −200 V. The current path is indicated in red lines (Fig. 17).

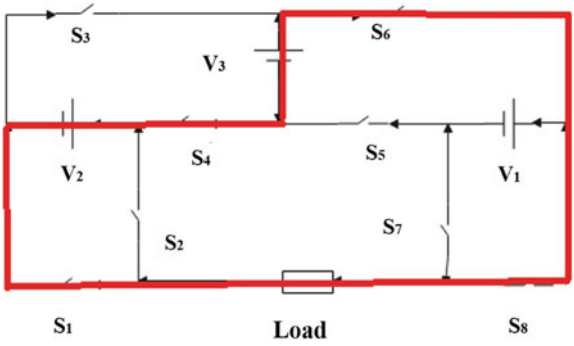

Fig. 17 Mode 15

3.2 MATLAB Simulation of Reduced Switch Multilevel Inverter

For MATLAB simulation, eight unidirectional switches were used. These switches are controlled with the help of repeating sequence stair and three DC voltage sources were used. The load is taken as 100 Ω. Across the load, the output voltage is measured with the help of voltage measurement. By using scope we can see the waveform (Figs. 18, 19 and 20).

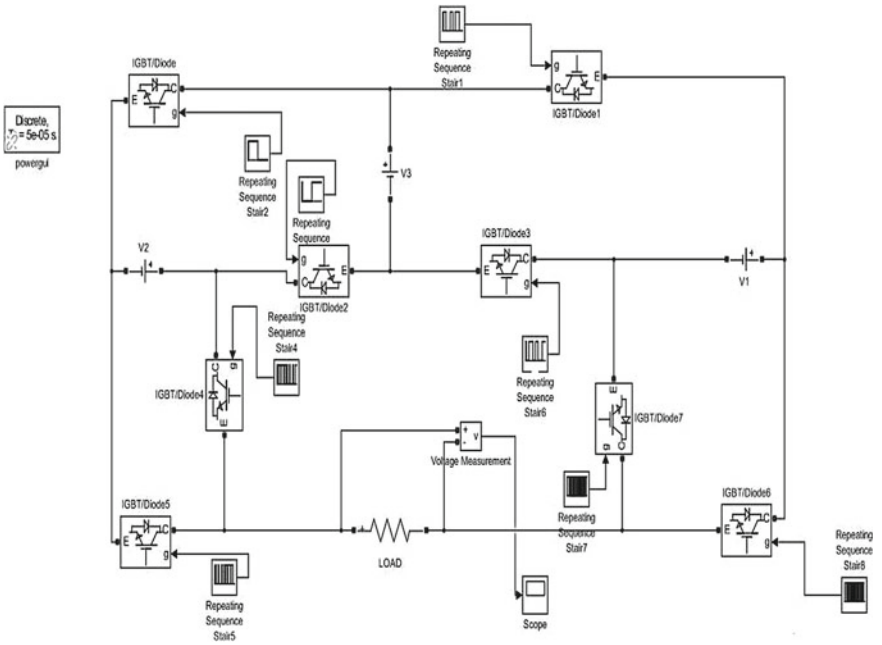

Fig. 18 Simulation of reduced switch multilevel inverter

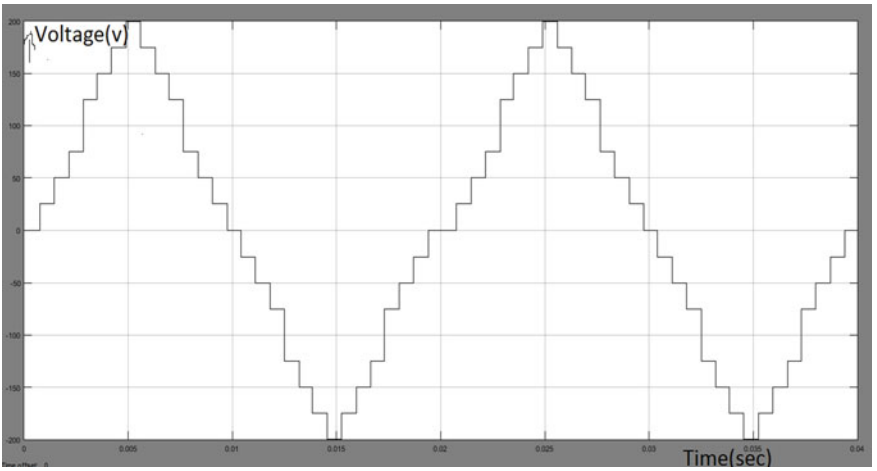

Fig. 19 Output waveform for reduced switch multilevel inverter

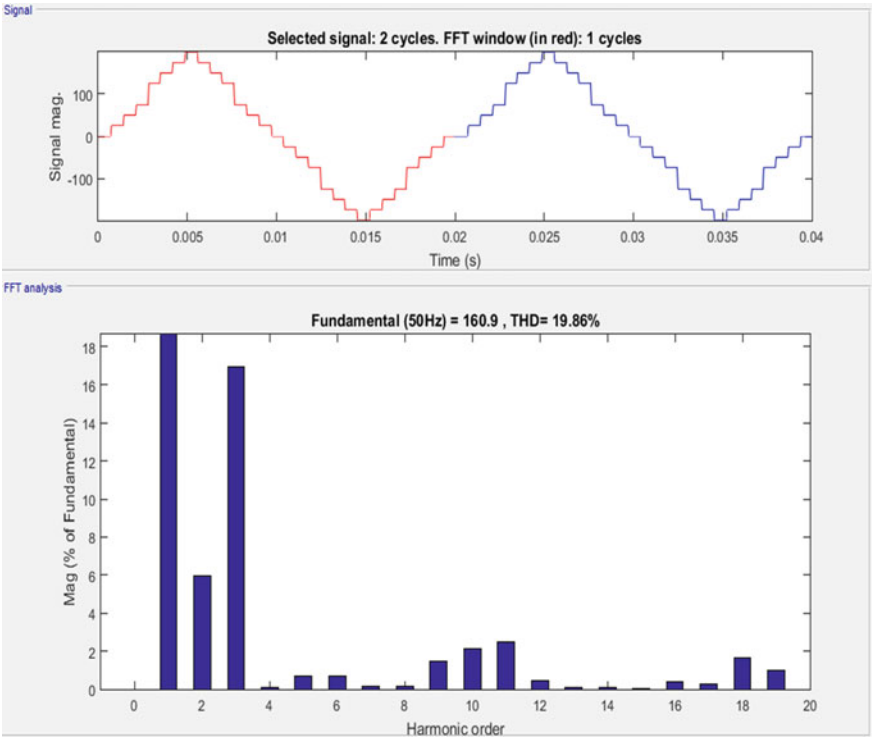

Fig. 20 THD waveform

3.3 Conventional Cascade Multilevel Inverter

See Figs. 21, 22 and 23.

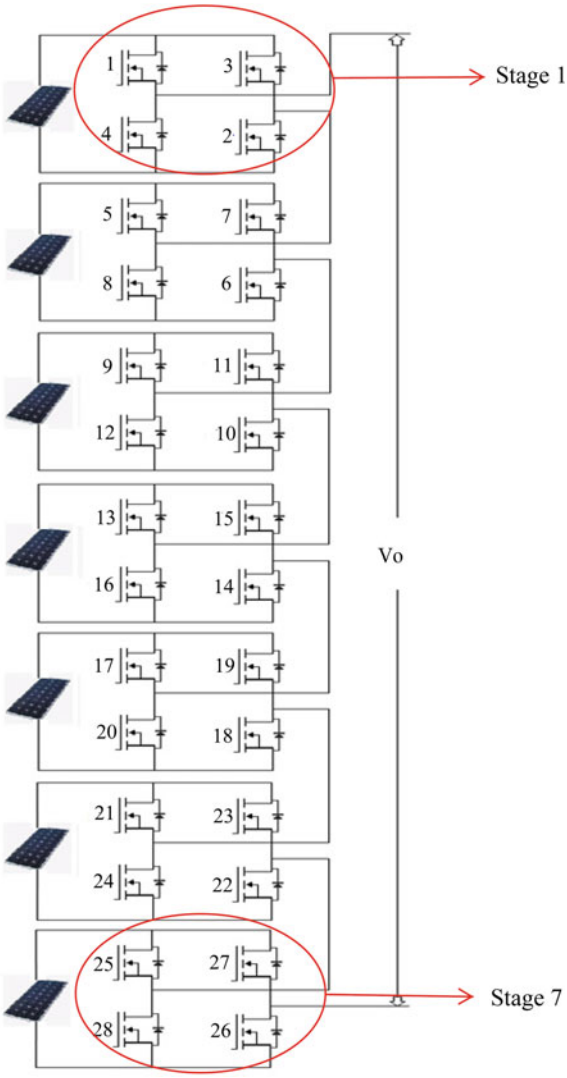

Fig. 21 Cascade MLI

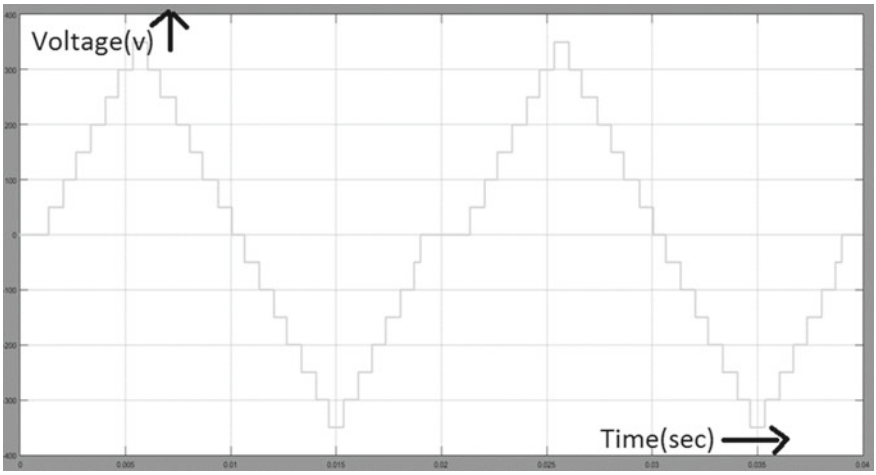

Fig. 22 Output waveform for cascade MLI

3.4 Comparison Between Cascade Inverter and Modified Inverter

Modified inverter	Cascade H-bridge inverter
Number of switches used: 8	Number of switches used: 28
No. of DC source used: 3	No. of DC source used: 7
Specification of voltage source used: V1 = 25 V2 = 50 V3 = 150	Each voltage source rating as 100 V
Output voltage of inverter: 200 V	Output voltage of inverter: 350 V
THD is 17.42%	THD is 22.46%

4 Conclusion

A decreased switch multilayer inverter has been presented in this proposed work with the comparison of conventional multilevel inverter. MATLAB simulation is used to measure the output voltage and THD. The proposed inverter is explained in different modes of operation and its voltage level and current paths are mentioned in each levels. The suggested converter's output voltage, THD, number of elements, and other specifications were then compared to conventional inverters, and the proposed inverter's advantage was validated using the above given table.

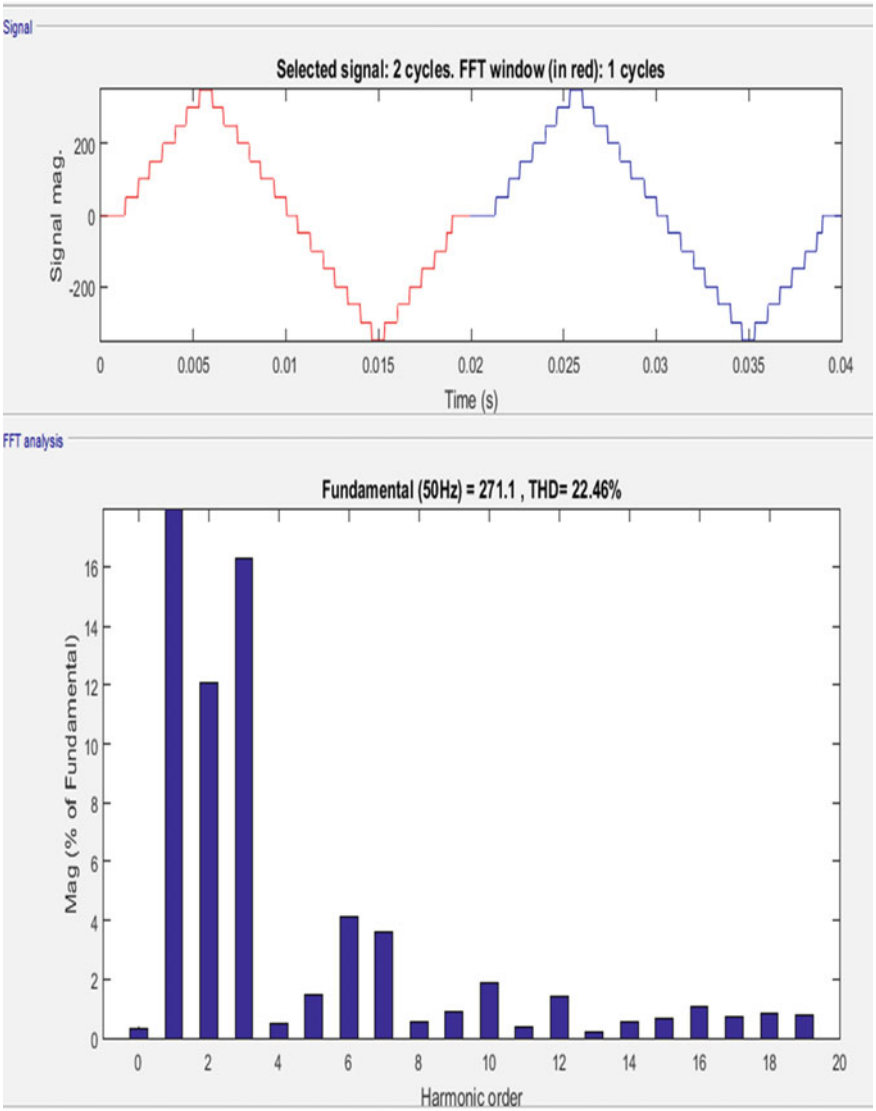

Fig. 23 THD waveform

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Design and Implementation of Resonant WPT for Electric Vehicle Battery Charging

Amit Sharma and Navdeep Singh

1 Introduction

The electric vehicle is a good solution for reducing the pollution and the energy shortage. Electric vehicle has two charging techniques: one is contact charging and the other is wireless charging. WPT technique can accelerate the market of EVs. There are certain drawbacks like fast charging, weight of batteries and high prices that cannot be solved using current battery research technology. Electric vehicles are becoming the need due to their eco-friendly behaviour and the incentives provided by the government. Cabled charging system can be totally replaced by the WPT technique, as driver has to park his electric vehicle on the transmitting coil T_X that is already installed in the parking area. The vehicle body has the receiving coil R_X that is already installed, due to which vehicle starts charging. There are various advantages for WPT as there is no direct contact between the plates, hence the overall charging process is safe. There are no moving parts and hence the overall life of the mechanism increases. WPT allows frequent recharging of the electric vehicle, and this helps to increases the battery life and declines the initial cost.

Nicola Tesla conducted various experiments for the exchange of the power wirelessly [1]. Kurs et al. [2] discussed the magnetic resonance phenomenon in WPT.

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Various works were done to transfer power wirelessly for electric vehicle. Mahadavifard et al. [3] discussed the various studies, advantages and drawbacks of WPT.

Prasanth et al. [4] discussed the novel approach for the WPT when the electric vehicle is in motion. Zaheer et al. [5] in their paper have discussed the various wireless power transfer advancement techniques, which are necessary for the roadway power electric vehicles. Dia J et al. [6] proposed a wireless power transfer technique, which uses the concept of magnetic resonance. In this, the resonating coils were coupled and were able to transfer 60 W of power.

Moon et al. [7] discussed the analysis of life cycle of both plug-in electric vehicle and wireless charging electric vehicle. He also discussed on how to increase the efficiency of the battery and phase energy consumption. Khaligh et al. [8] proposed a method to extend the charging limits of a wireless charging system by enhancing the capacitors of the coils. Vaka et al. [9] discussed the various challenges in the design of a wireless battery charger. In this AC to DC, rectification and boost converter are discussed to develop the proposed model.

Hui et al. [10] described the apparatus and method of mid-range application of WPT. It discusses the activities based on magneto-inductive research. It also covers two coils, four coils system with relay resonators. Mi et al. [11] proposed the various models for WPT for roadside powered electric vehicles. This paper shows that good efficiency can be achieved through their proposed model. Ning et al. [12] discussed flow of power through wireless transfer, it provides selection of primary frequency and the tuning of secondary with reactive power voltage control.

Ladas et al. [13] proposed a particle swarm optimization algorithm for wireless power transfer. This method opens the new approach to increase the efficiency.

Figure 1 shows the layout of WPT system. There are three modes of charging in electric vehicle. In stationary wireless charging as shown in Fig. 2 [14], the EVs are standstill and batteries are charged with the help of mutual induction but due to certain limitations of the battery capacity the number of charging cycles has to be increased so that they can travel longer distance. Dynamic wireless charging (DWC) is solving the issue by placing the small transmitting pads on roads. This type of charging is expensive but will provide dynamic charging to the electric vehicles when they are in motion. The disadvantage of DWC can be removed by QWC, which is quasi-dynamic charging system in which the EVs are charged when they are not moving or while they are in slow speed. These are widely used in public transportation, bus stops, taxi stands and traffic lights. Table 1 depicts the various types of WPT for electric vehicle charging system.

Fig. 1 Layout of WPT system

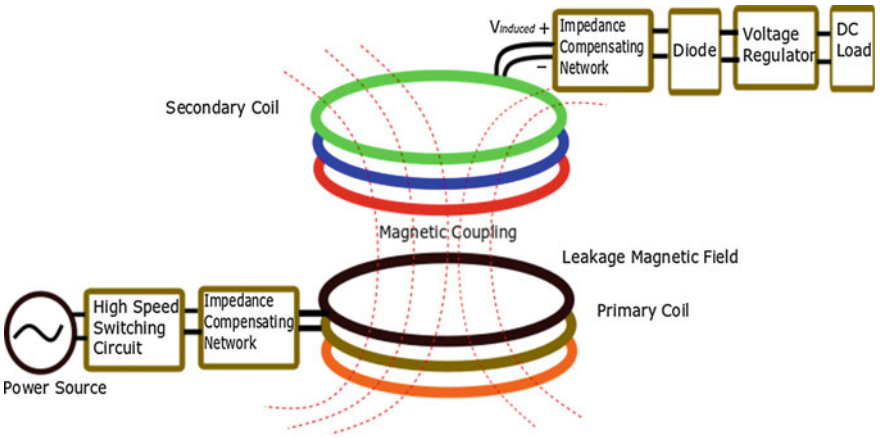

Fig. 2 Mechanism of inductive power transfer

Table 1 Different types of WPT system

Energy carrying medium	Method		Power	Range	Effectiveness	Comments
Electromagnetic field	Near field	IPT	High	Low	High	Implementation shows good result
	Far field	Coupled magnetic resonance	High	Medium	High	
		Laser, microwaves	Big	High	High	Direct line of transmission is required
		Radio waves	High	High	Low	Efficiency is less and tracking is difficult
Electric field		Capacitive power transfer	Low	Low	High	Distance is small and power level is small
Mechanical force		Magnetic gear	High	Medium	High	Good for EVs

2 Design of a System

In Fig. 3, wireless transfer of inductive power is shown. Different AC to DC and DC to AC stages are added in this figure. In order to charge a battery, the power is required to flow from DC link to the battery.

Two magnetically coupled coils are transferring the inductive power. Consider two coils L_1 and L_2 and mutual inductance M. L_1 and L_2 are representing the primary

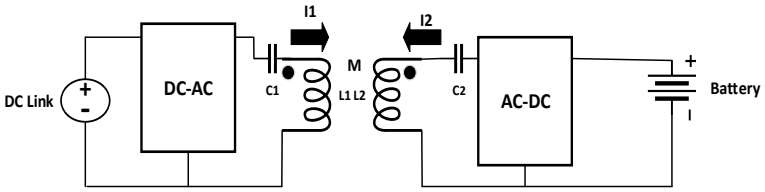

Fig. 3 Diagram of IPT system

and the secondary coils. The battery to be charged is represented on the secondary side of the coil. The primary side of a coil is having DC voltage, which is connected to the grid. The transfer of power between coupled coils is done in AC and hence two circuits are needed which are AC–DC converter on primary side and DC–AC converter on secondary side.

The coupling of coils is loose, so a reactive circuit is required to get the maximum power and the maximum efficiency if the system is at resonance [15]. Compensation networks are called as reactive networks, which are added to both primary and secondary coils. In this model, two capacitors C_1 and C_2 in series are used on each side. Some of the main parts of the IPT system are as follows.

2.1 Rectifier Circuit

Figure 4 represents the circuit, which is connected to the grid, which provides AC voltage to the circuit. This AC source is connected to the full wave rectifier circuit. The full wave rectifier circuit consists of four diodes as shown. The AC voltage is converted into DC voltage. The capacitor C is connected in parallel in order to filter the waveform. The input AC voltage is 230 V.

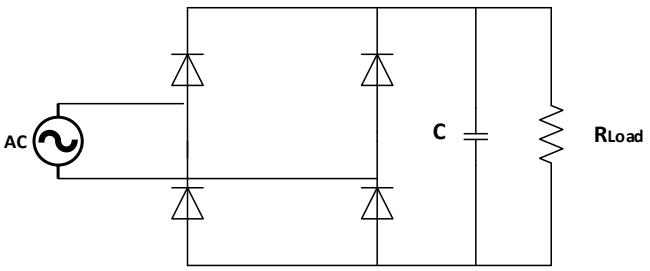

Fig. 4 Rectifier circuit

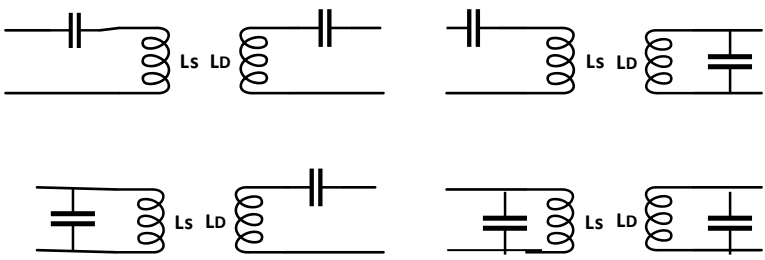

Fig. 5 Four types of compensated networks

2.2 Compensation Network

In order to transfer more power towards the load, reactive networks are used. Since coupled inductive elements are to be compensated, capacitors are used as compensating elements in the network. Two capacitors C_1 and C_2 are connected in series with primary and secondary coils.

There are four different types of compensating topologies [16], which depend on the connection between coil and a capacitor, which is shown in Fig. 5. The possible types are series–series compensation (SS), series–parallel compensation (SP), parallel–series compensation (PS) and parallel–parallel compensation (PP). In this model, series–series compensation is chosen with an appropriate value capacitor depending only on the self-inductances. With the change in load and misalignments of the coils, the value of SS capacitor will remain same. This is the main reason for the adoption of SS compensating technique for the convenient electric vehicle battery charging.

2.3 Primary and Secondary Circuits

Figure 6 is the primary and the secondary circuits of the model. The nature of the inductive coupling across the primary and the secondary is AC. The source of power is electrical grid and the secondary side of coupling is connected to a battery as shown in Fig. 7, which is acting as a load. Hence, two power converters are required in order to change the nature of supply. In the secondary circuit, DC to AC converter is applied and it is double stage. The double stage is added to increase the power frequency from 50 Hz to higher frequency level, which is in kHz of the IPT [17]. In order to supply the DC voltage to battery, the secondary side of coupling AC voltage is converted to DC voltage with the help of rectifier circuit. The higher frequency gate pulse is given to operate the inverter circuit.

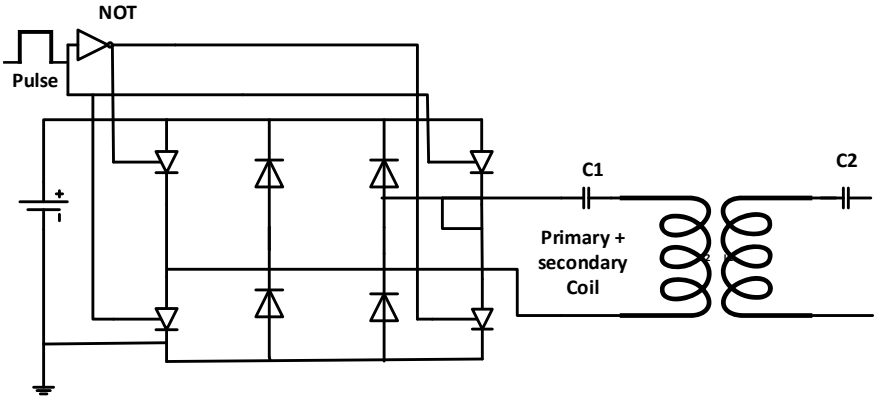

Fig. 6 High-frequency AC generation from DC source

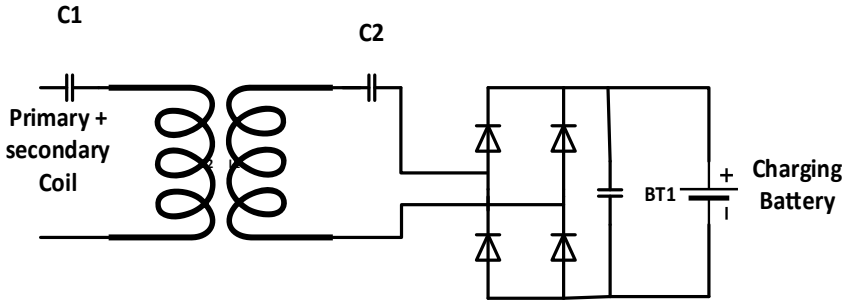

Fig. 7 WPT to battery

3 Mathematical Modelling

In this section, system modelling is discussed. This is helpful for finding the system parameters. These parameters are thus required by the system to get the maximum efficiency. Inductor, capacitor, resistor and resonant frequency values are required to get the system output [18].

The primary and the secondary coil inductances L_1 and L_2 can be found from the relationship, which is shown by Eqs. 1 and 2:

$$L_1 = N_1^2 R_1 \mu_O \mu_r \left[\ln\left(\frac{16R_1}{d} - 2 \right) \right] \tag{1}$$

$$L_2 = N_2^2 R_2 \mu_O \mu_r \left[\ln\left(\frac{16R_2}{d} - 2 \right) \right] \tag{2}$$

where μ_O is the vacuum permeability, μ_r is the relative permeability, N_1 and N_2 are the number of turns of the coil, R_1 and R_2 are the radius of the inner turn and d corresponds to the equivalent diameter of the coils

The value of d can be found by the following expression in Eq. 3. Here N is the number of turns in coils and S is the cross section of the cable.

$$d = 2 * \sqrt{\frac{N * S}{\pi}} \tag{3}$$

The coil has a mutual inductance that can be found by Eq. 4 shown below, k is the coefficient of mutual coupling.

$$L_M = k\sqrt{L_1 L_2} \tag{4}$$

The resonance frequency f_r can be found with the help of Eq. 5 shown below:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{5}$$

The modified model system efficiency is given by Eq. 6 shown below:

$$\eta = \frac{\omega^2 M^2 R_L}{\left[Z_2\{Z_1 Z_2 + (\omega M)^2\}\right]} * 100 \tag{6}$$

For *S–S* configuration at resonance frequency, capacitive reactance is equal to inductive reactance and hence cancel out the effect. Hence, the impedances Z_1 and Z_2 shown in Eqs. 7 and 8 can be found from Fig. 8 as

$$Z_1 = R_1 + R_S \tag{7}$$

$$Z_2 = R_l + R_2 \tag{8}$$

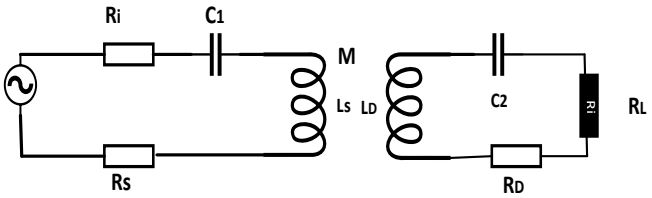

Fig. 8 Circuit diagram for primary and secondary coils

4 Results and Discussion

In this section, MATLAB model for the modified system has been discussed. It consists of circuit diagram of rectifier circuit as shown in Fig. 9. MATLAB circuit diagram for generation of high-frequency gate signal is shown in Fig. 10 and MATLAB circuit diagram for primary and secondary coil is shown in Fig. 11.

Table 2 shows the parameters that are designed as per the need. Various simulations are performed in order to meet the requirements. The various graphs are plotted below.

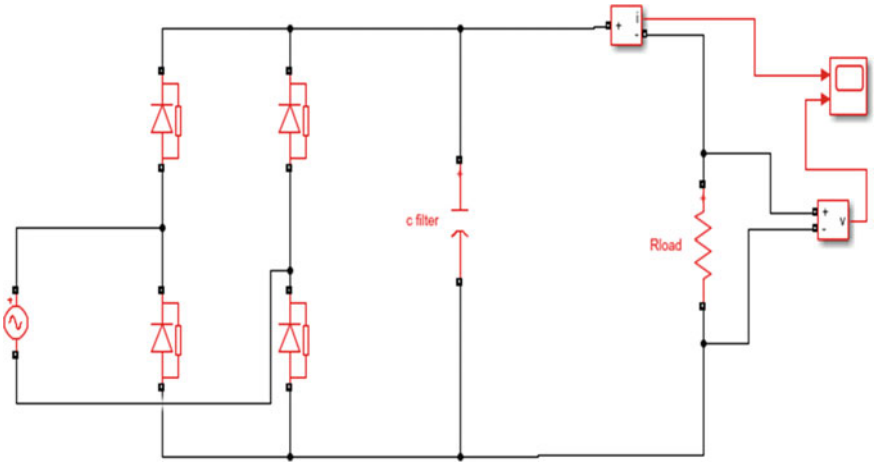

Fig. 9 MATLAB model of rectifier circuit

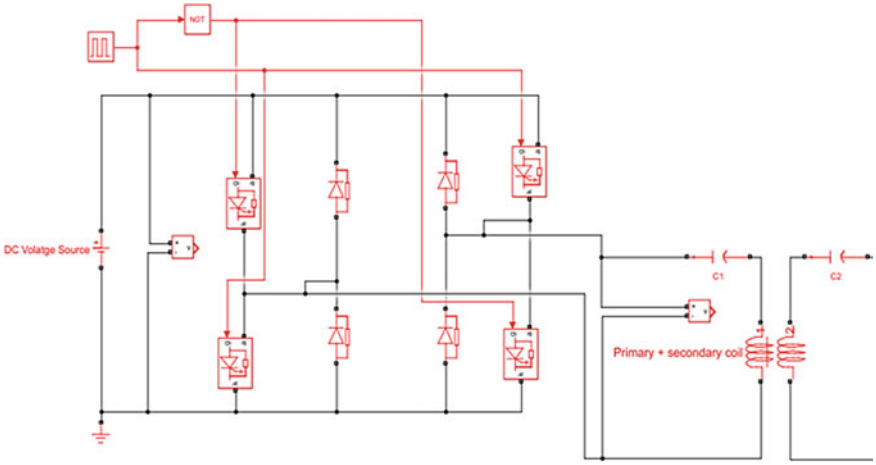

Fig. 10 MATLAB model of high-frequency AC generation from DC source

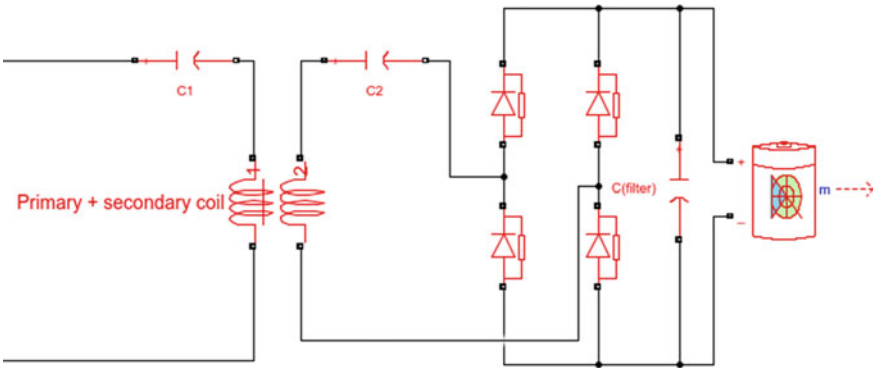

Fig. 11 MATLAB model of circuit diagram for primary and secondary coils

Table 2 Element and their specific value for the model

Sr. no.	Element	Value
1	V_{peak}	230 V
2	R_1 and R_2	0.0714 Ω
3	L_1 and L_2	73.43 μH
4	C_1 and C_2	0.2 μF
5	R_M	0.142 Ω
	L_M	$1.46 * 10^{-5}$ H
7	R_L	100 Ω
8	f	50 Hz
9	f_r	41.5 kHz
10	K	0.2

Figure 12 depicts the waveform from a rectifier circuit. The output shown are DC current and DC voltage for 1 Ω resistor. This output is given to the secondary circuit. Figure 13 depicts the high-frequency gate pulses, which are provided to trigger the inverter circuit. The triggering is done at $2.409 * 10^{-5}$ s. The inverter circuit is converting DC into AC. The scope attached shows three waveforms in Fig. 14, which are (a) DC voltage, which is given to the inverter; (b) AC current output, which has got the maximum value of 3.6 A and (c) AC voltage which has got the maximum value of 226 V.

The AC output voltage is given to the primary coil, which is mutually coupled with the secondary coil. There is a generation of voltage and current in the secondary coil. The peak magnitudes of AC voltage and current are 12 V and 0.31 A which are shown in Fig. 15. In order to charge the battery, AC is again changed to DC with the help of rectifier circuit. This DC current is available to the battery to charge the battery, which is the part of electric vehicle. Figures 16 and 17 are showing the current, voltage, and the SOC of a battery. As shown in Fig. 17, the battery is charging

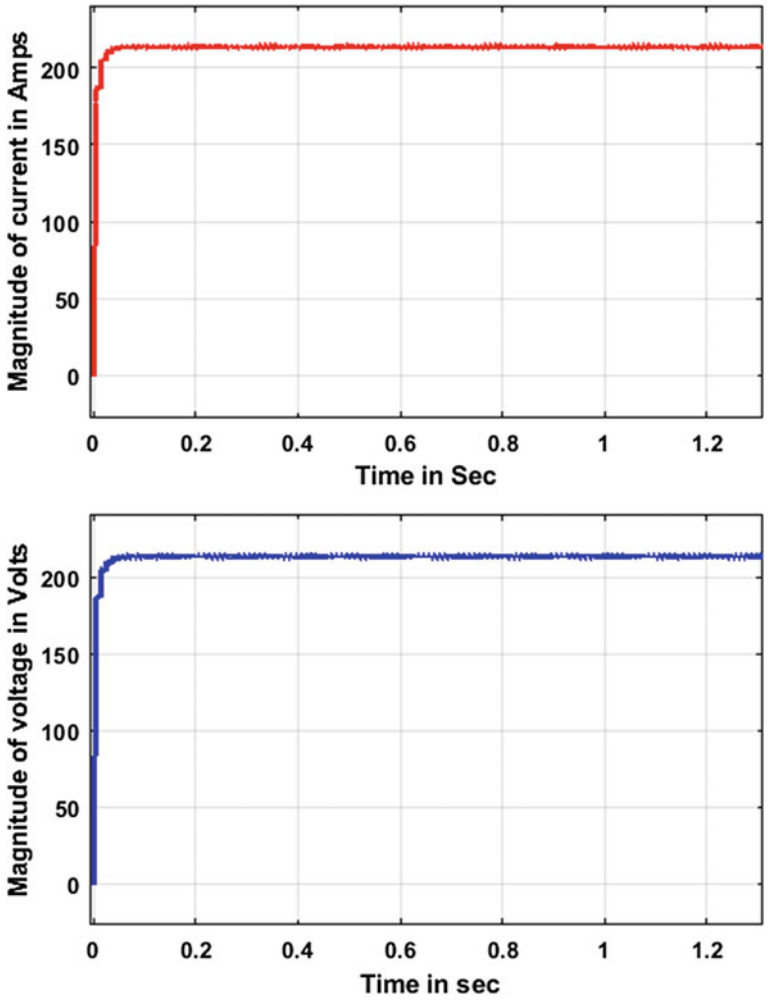

Fig. 12 Current and voltage generation in rectifier circuit

as per the voltage and the current available. Table 3 shows the various output for the model.

5 Conclusion and Future Scope

This research work concludes that the battery of the electric vehicle can be charged using the modified technique, which is resonant wireless power transfer. Proper designing and the implementation of the parameters have been taken care to get

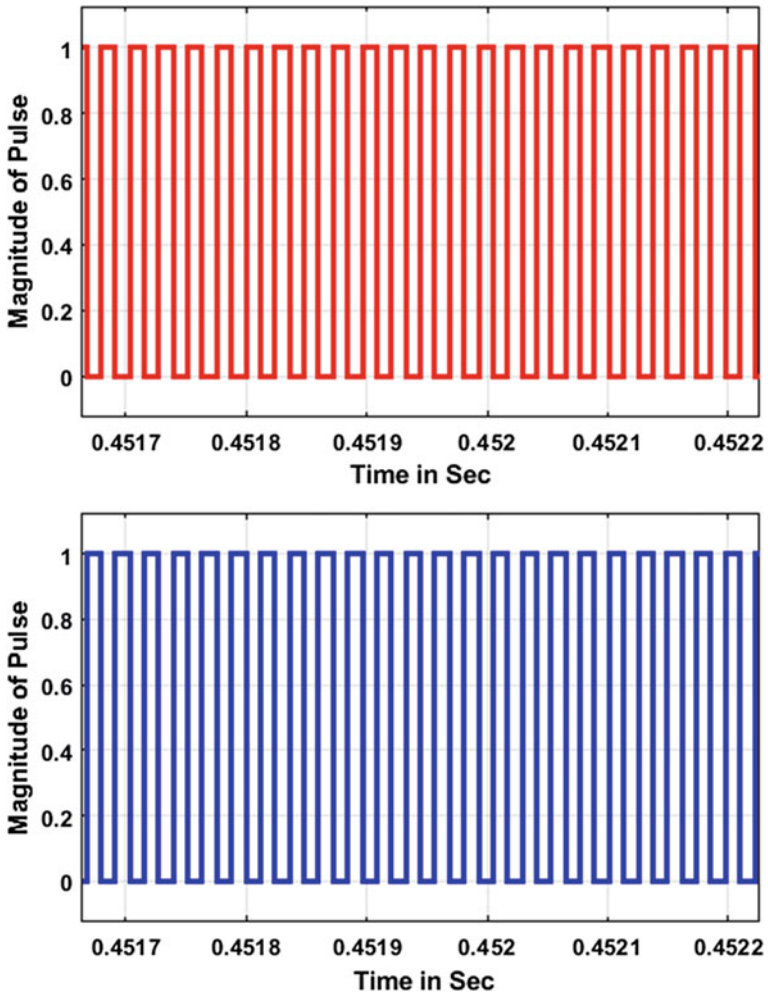

Fig. 13 High-frequency gate pulse

the good results. As compared with other works, the modified technique uses less components and is cheap. The efficiency of the system is around 68% and it uses SS compensated system. Most of the energy is lost during the primary and secondary coupling. This is the major drawback of the system, which has to be improved. Thus, the future work can be done on designing and implementation of a shielding mechanism to the WPT coils, which will improve the system efficiency and the voltage output.

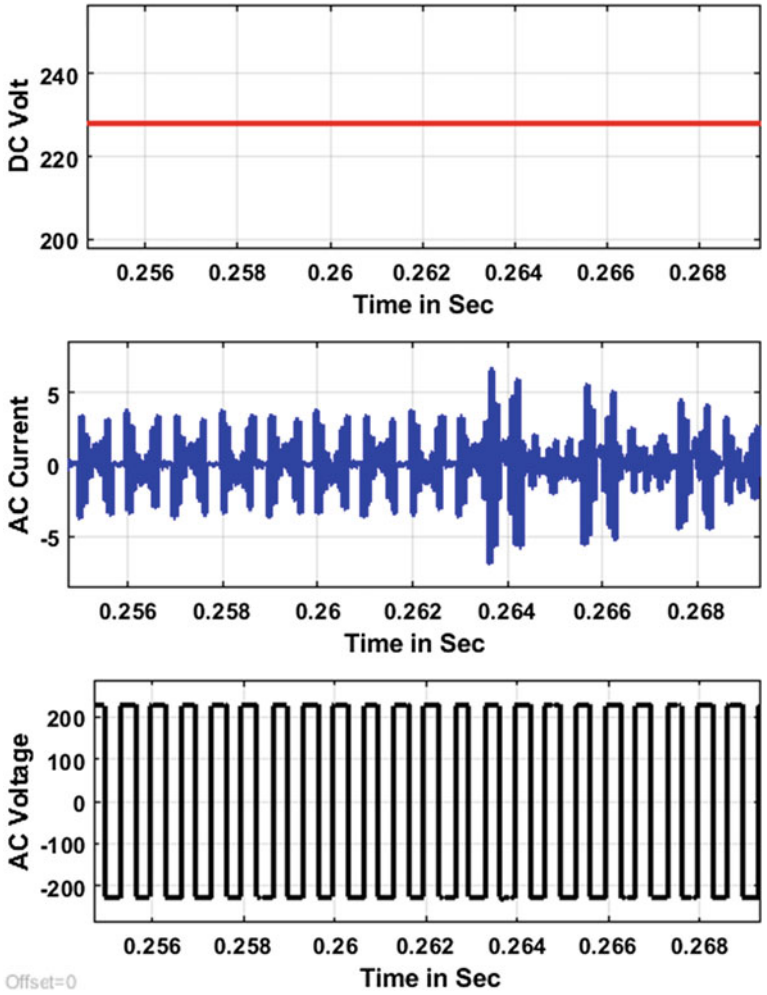

Fig. 14 Generation of **a** DC voltage **b** AC current **c** high-frequency AC voltage in primary side of secondary circuit

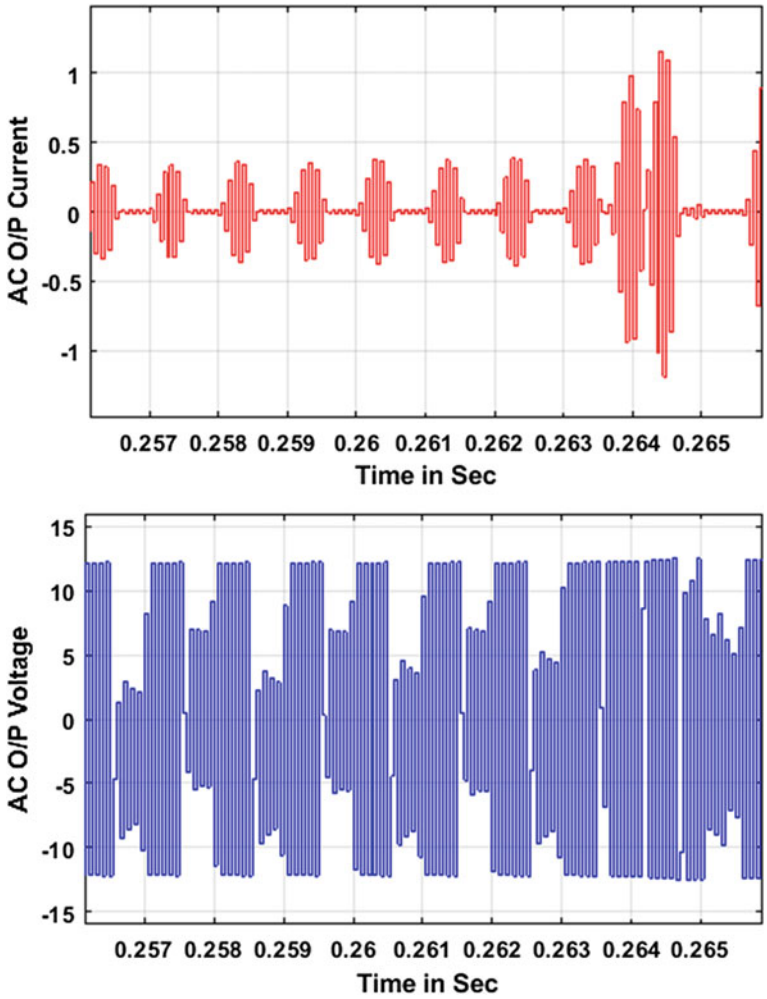

Fig. 15 Waveform for AC output signal and AC output voltage at secondary side of secondary circuit

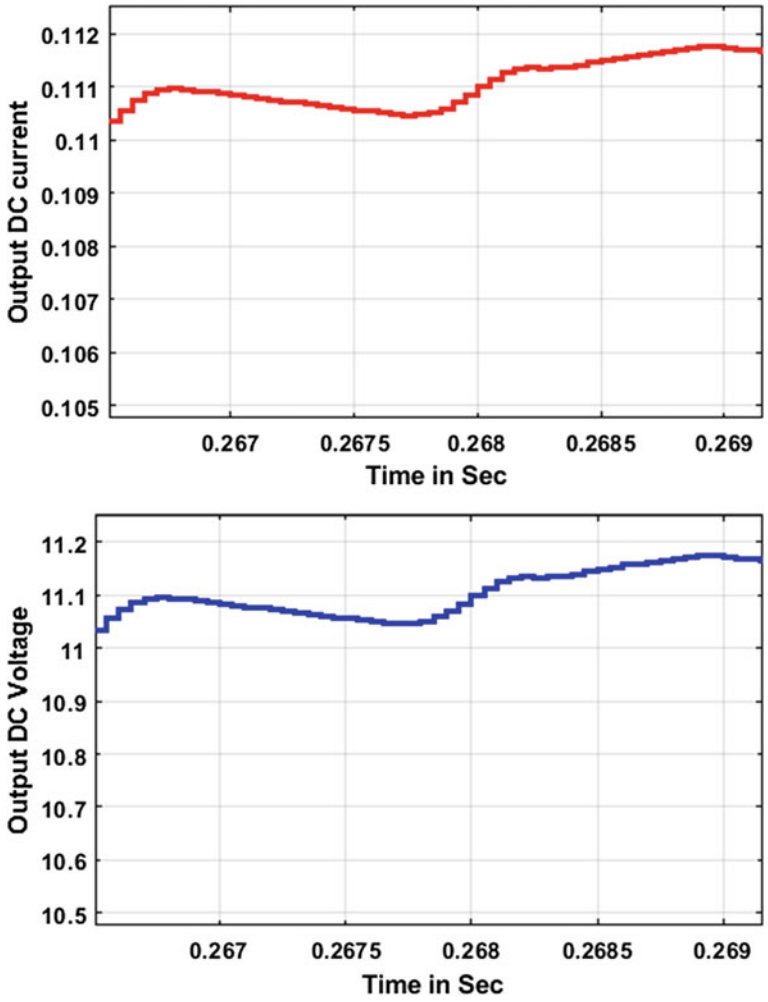

Fig. 16 Waveform showing the output current and voltage to charge the battery

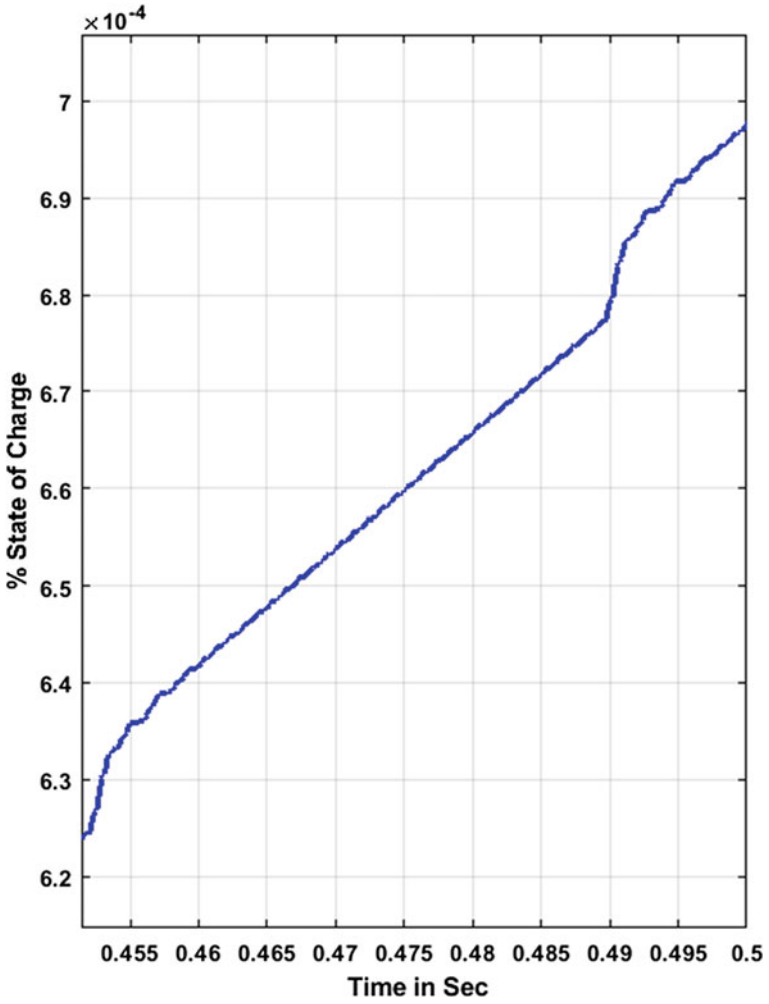

Fig. 17 Battery state of charge

Table 3 Output of secondary coil of secondary circuit

Sr. no.	Parameter	Value
1	V_{ac} (Peak)	226 V
2	I_{ac} (Peak)	3.6 A
3	V_{dc}	12 V
4	I_{dc}	0.31 A
5	Efficiency of system	68%

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A Comparative Simulation Study Between ZSI and BB-ZSI Based Distribution Static Compensator for Power Quality Improvement in Power Distribution Network

Mrutyunjaya Mangaraj, Jogeswara Sabat, and Ashok Kumar Chahattaray

1 Introduction

In recent years, development in power electronic devices provides feasible solutions for PQ issues meeting critical customer requirements [1]. Over the last two decades, a number of custom power device (CPD) based inverters have been proposed for active power filtering (APF) of low and medium voltage PDN [2, 3]. The voltage source inverter (VSI) and current source inverters (CSI) are two well known inverters widely used in various applications like electric vehicles, distributed energy resources, adjustable speed drives and microgrid integration. But the inherent demerits of VSI and CSI, which makes them less efficient like; CSI is unfit for buck operation while VSI is not suitable for voltage boost inversions [4]. Hence, for this particular application, an additional converter is required. The additional converter requires extra semiconductor switches which increase the switching losses and cost of the system. It also decreases the efficiency and system reliability. Since VSI can reduce the voltage level, CSI can only increase the voltage and both have a limit in compensation capability.

The limitations of conventional inverters are overcome in the ZSI topology [4, 5]. It is a special form of inverter that provides voltage boost capability. Now a day, energy resources require two stages of power conversion (dc–dc conversion and dc–ac conversion) and ZSI has the ability to perform [6]. In between the bridge inverter and dc link of ZSI, two inductors and two capacitors are cascaded. Generally, the

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ZSI operates in two states, state-1 the shoot-through state and state-2 the non-shoot-through state. During state-1 operation, the capacitors are supplied energy to charge the inductors and during state-2 operation, the energy in charged inductors and input are supplied to the dc link [7]. Hence, it boosts the voltage gain of the ZSI in one stage without an additional converter. Also, it increases the reliability and abolishes the dead time [6–8]. The traditional VSI can replace with ZSI due to the inherent shoot-through and open-circuit protection offered by ZSI. Among all inverters, ZSI become the most reliable and permissible power inverter for operation of power conversion [4–8].

The authors attempted to design a unique model BB-ZSI supported by DSTATCOM as a strategy to strengthen its shunt compensation capability. Because the ZSI has some drawbacks like low voltage boost gain and weak active power filtering. The direction of inverter current depends upon the topology configuration and its application. Besides the various advantages of ZSI, some demerits are also noticed such as discontinuous primary current, more capacitor stress and boost factor limit. Different topologies are developed to bridge the demerits of ZSI. In recent years, back to back connections of inverters have mostly been used in medium voltage drives, electric frequency changers and power electronics transformers [9–13]. This article proposed a unique topology BB-ZSI based DSTATCOM for enhanced shunt compensation capability motivated from the previous research work based on back to back connected inverters by different authors in different platforms [10–13]. The proposed topology can successfully reduce source current THD value to less than conventional ZSI. A DSTATCOM is required for PDN to meet the IEEE standard grid code [14, 15]. The BB-ZSI is shown as a promising and developing topology for DSTATCOM. It uses the neural network based ALMS control technique to achieve the goals such as harmonic elimination with filtering performance, improvement in PQ, p.f correction and better voltage balancing at PCC [16–18]. Taking into consideration of the above benefits, the BB-ZSI supported DSTATCOM is selected for the efficient operation of PDN.

This paper is organized as follows. Later in the introduction, the proposed model is briefly presented with a detailed operation of BB-ZSI in Sect. 2. After that, in Sect. 3, the ALMS control method for a ZSI and BB-ZSI supported DSTATCOM with shunt compensation are presented and discussed. Then, both the topologies are presented and verified as per IEEE standard grid code using ALMS technique in Sect. 4. Finally, conclusions are summarized in Sect. 5.

2 Topology Descriptions

The recommended PDN in which the proposed BB-ZSI integrated at the point of common coupling (PCC) is shown in Fig. 1. The circuit topology of ZSI is depicted in Fig. 2. The formation of the designed topology is verified in order to prove the shunt compensation capability. The BB-ZSI is connected to the 3-phase balanced source through distribution line impedance (Z_S). The three phase source supplies

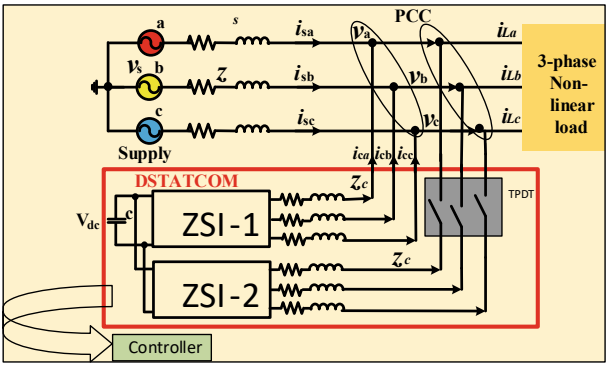

Fig. 1 Proposed PDN with BB-ZSI based DSTATCOM

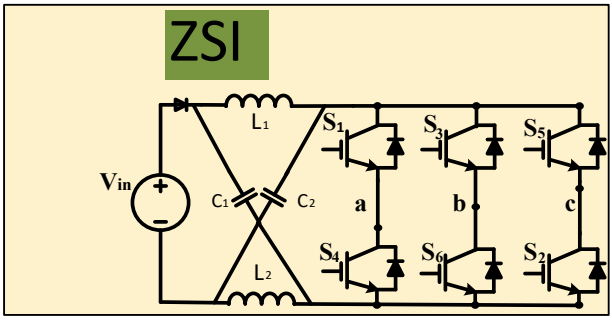

Fig. 2 ZSI configurations

source currents (i_{sa}, i_{sb} and i_{sc}) to the 3P3W load (uncontrolled rectifier with resistive and inductive load) and it draws the load currents (i_{la}, i_{lb} and i_{lc}). A self capacitor supported BB-ZSI based DSTATCOM is utilised as shunt compensator to compensate for the PQ and its associated issues. The optimised operation of BB-ZSI is to highlight the meticulous topology for proper dynamic operation and reduces the complexity of the entire conversion in the field of PDN.

3 Proposed ALMS Control Algorithm

In this section, the ALMS technique is discussed by considering the different weighting parameters like learning rate, step size, unit input weights and bias etc. The main purpose is to provide an individual phase tuned weight equivalent to the system frequency active component of the three phase load current [16, 17]. The learning mechanism of the ALMS algorithm is shown in Fig. 3 and expressed as per the following iteration:

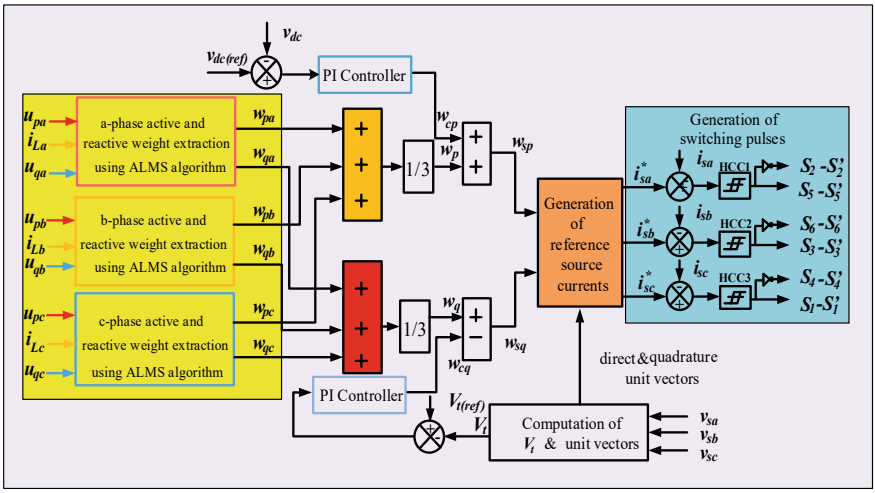

Fig. 3 Switching signal generation using ALMS principle

The updating weights (w_{pa}, w_{pb}, w_{pc}) of active part of the load current are calculated as

$$w_{pa}(n) = \alpha\gamma\left\{i_{la}(n) - w_{pa}(n-1)u_{pa}(n)\right\}u_{pa}(n) + w_{pa}(n-1) \tag{1}$$

$$w_{pb}(n) = \alpha\gamma\left\{i_{lb}(n) - w_{pb}(n-1)u_{pb}(n)\right\}u_{pb}(n) + w_{pb}(n-1) \tag{2}$$

$$w_{pc}(n) = \alpha\gamma\left\{i_{lc}(n) - w_{pc}(n-1)u_{pc}(n)\right\}u_{pc}(n) + w_{pc}(n-1) \tag{3}$$

The updating weights (w_{qa}, w_{qb}, w_{qc}) of reactive part of the load current are calculated as

$$w_{qa}(n) = \alpha\gamma\left\{i_{la}(n) - w_{qa}(n-1)u_{qa}(n)\right\}u_{qa}(n) + w_{qa}(n-1) \tag{4}$$

$$w_{qb}(n) = \alpha\gamma\left\{i_{lb}(n) - w_{qb}(n-1)u_{qb}(n)\right\}u_{qb}(n) + w_{qb}(n-1) \tag{5}$$

$$w_{qc}(n) = \alpha\gamma\left\{i_{lc}(n) - w_{qc}(n-1)u_{qc}(n)\right\}u_{qc}(n) + w_{qc}(n-1) \tag{6}$$

The three phase average active component weight (w_a) is given as:

$$w_a = \frac{w_{pa} + w_{pb} + w_{pc}}{3} \tag{7}$$

Similarly, the three phase average reactive component weight (w_r) is given as:

$$w_r = \frac{w_{qa} + w_{qb} + w_{qc}}{3} \tag{8}$$

Active unit voltage templates (u_{pa}, u_{pb}, u_{pc}) are estimated as:

$$u_{pa} = \frac{v_{sa}}{v_t}, u_{pb} = \frac{v_{sb}}{v_t}, u_{pc} = \frac{v_{sc}}{v_t} \tag{9}$$

Similarly, the reactive unit voltage templates (u_{qa}, u_{qb}, u_{qc}) are estimated as:

$$u_{qa} = \frac{u_{pb} + u_{pc}}{\sqrt{3}}, u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \tag{10}$$

where v_t can be expressed as

$$v_t = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \tag{11}$$

The difference between reference dc voltage and sensed dc voltage is the error in dc voltage (v_{de}) can be expressed as

$$v_{de} = v_{dc(ref)} - v_{dc} \tag{12}$$

$$w_{cp} = k_{pa} v_{de} + k_{ia} \int v_{de} dt \tag{13}$$

$$w_{sp} = w_a + w_{cp} \tag{14}$$

The ac voltage error (v_{te}) is determined by subtracting sensed amplitude of PCC from reference ac voltage is calculated as

$$v_{te} = v_{t(ref)} - v_t \tag{15}$$

The output of PI controller can be expressed as [16–18]:

$$w_{cq} = k_{pr} v_{te} + k_{ir} \int v_{te} dt \tag{16}$$

The reference source current is obtained by subtracting the average magnitude of reactive component of load current from the output of AC side PI controller as;

$$w_{sq} = w_r - w_{cq} \tag{17}$$

Three phase instantaneous reference source active components are estimated as

$$i_{aa} = w_{sp}u_{pa}, i_{ab} = w_{sp}u_{pb}, i_{ac} = w_{sp}u_{pc} \tag{18}$$

Similarly, three phase instantaneous reference source reactive components are estimated as

$$i_{ra} = w_{sq}u_{qa}, i_{rb} = w_{sq}u_{qb}, i_{rc} = w_{sq}u_{qc} \tag{19}$$

$$i^*_{sa} = i_{aa} + i_{ra}, i^*_{sb} = i_{ab} + i_{rb}, i^*_{sc} = i_{ac} + i_{rc} \tag{20}$$

The reference source currents ($i^*_{sa}, i^*_{sb}, i^*_{sc}$) and the real supply currents (i_{sa}, i_{sb}, i_{sc}) of 3-phase are evaluated, after that the error in signals are fed to the hysteresis current controller.

4 Simulation Results

The proposed BB-ZSI is tested under PQ issue over ZSI. The different parameters and their magnitudes utilised to make the models are arranged in Table 1. At first, PDN is operated without connecting the DSTATCOM at PCC. It is observed from the simulation results that the source current is similar to the load current distortion. Next, the DSTATCOM is performed under both steady state and transient state loading to verify its effectiveness. The BB-ZSI for PQ improvement and reliable operation in the field of PDN, compared with traditional single ZSI to justify the effectiveness through the simulation results, which are detailed below in the subsequent section:

Table 1 Proposed system parameters

Parameters	Magnitude
f_s (fundamental frequency)	50 Hz
v_{dc} (DC link voltage)	600 V
C_{dc} (capacitor)	2000 μF
K_{pa} (proportional controller gain)	0.01
v_s (system voltage)	230 V/phase
R_c (compensator resistance)	0.25 Ω
R_s (source resistance)	0.5 Ω
L_c (compensator inductance)	1.5 mH
L_s (source inductance)	2 mH
K_{pr} (source inductance)	0.2 mH
K_{ir} (AC integral controller)	1.1
K_{ia} (integral controller gain)	0.05

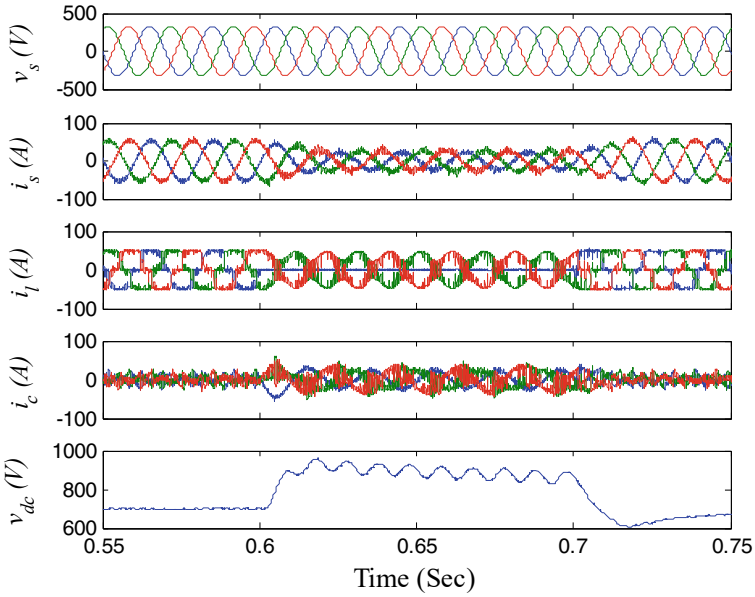

Fig. 4 Compensation performance using ZSI based DSTATCOM

4.1 Shunt Compensation Analysis of ZSI

The simulation model consists of ZSI, an uncontrolled bridge rectifier with $R = 10$ Ω and $L = 20$ mH for non-linear load, 230 V (rms)/phase balanced source voltage, system frequency 50 Hz and 600 V dc link reference voltage. The other details of the parameters used to construct the model are presented in Table 1.

The load varying performance of ZSI is shown in Fig. 4. The impact of distortion in the PDN is testified at (0.55–0.6 s and 0.7–0.75 s) for steady state condition and (0.6–0.7 s) for dynamic state condition. ZSI is tested in time in varying responses of dc link voltage v_{dc} (ref) from 700 to 870 V. Figures 5 and 6 shows the harmonic content and THD factor of supply current 4.01%, 53.8 A and load current 26.08%, 52.09 A correspondingly.

4.2 Shunt Compensation Analysis of BB-ZSI

The load varying performance of BB-ZSI is shown in Fig. 7. The impact of distortion in the PDN is testified, at (0.55–0.6 s and 0.7–0.75 s) for steady state condition and (0.6–0.7 s) for dynamic state condition. Proposed model is tested in time in varying response of dc link voltage v_{dc} (ref) from 600 to 780 V. Figures 8 and 9 shows the harmonic content and THD factor of supply current 3.85%, 53.89 A and load

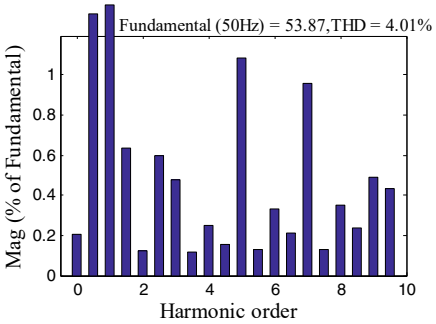

Fig. 5 ZSI source current THD after compensation

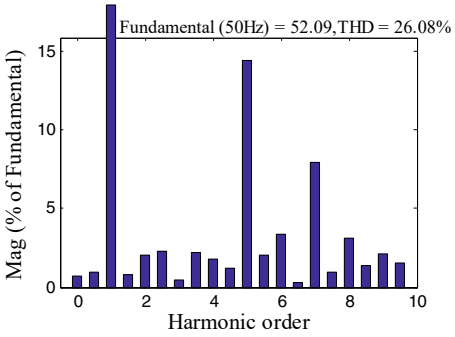

Fig. 6 ZSI load current THD after compensation

current 26.06%, 52.08 A correspondingly. The source side harmonic reduction of PDN shows superior shunt compensation. Apart from this, reliability and flexible operation of the PDN are achieved. The comparison analysis of ZSI and BB-ZSI are arranged in Table 2. The source current and load current THD analysis of ZSI and BB-ZSI are presented in Fig. 10.

5 Conclusion

This paper proposed BB-ZSI based DSTATCOM for three phase three wire PDN. It enhanced the PQ of PDN and compared it with traditional ZSI. The shunt compensation capability and buck-boost ability of the ZSI provided PQ enhancement with better reliability and flexibility of PDN. It is noticed that the BB-ZSI performs better over ZSI like distortion reduction in the supply side, balanced voltage at PCC, decreased switching losses, better voltage regulation and p.f correction. Moreover, this paper showed the BB-ZSI based DSTATCOM for the low and medium voltage PDN. Furthermore, the proposed topology can be expected to provide better compensation capability with other improvements as per the system requirements in the different applications.

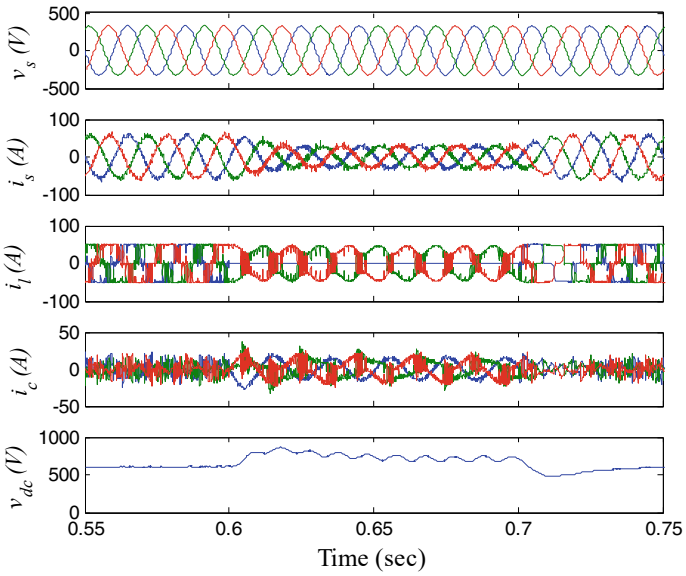

Fig. 7 Compensation performance using BB-ZSI based DSTATCOM

Fig. 8 BB-ZSI source current THD after compensation

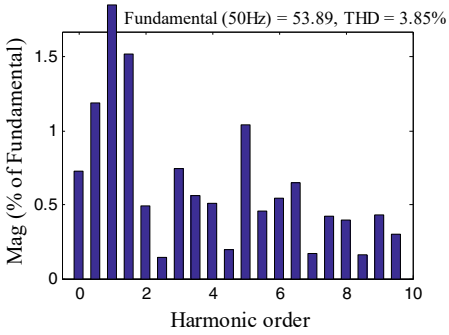

Fig. 9 BB-ZSI load current THD after compensation

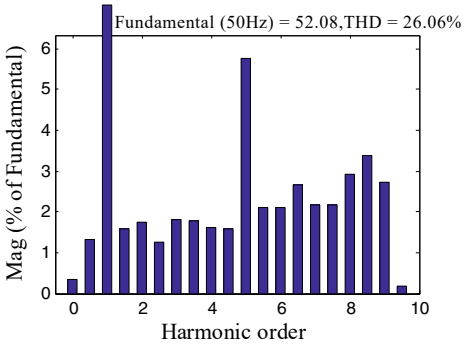

Table 2 Different parameters compensation analysis of both topologies

Topology	Supply current (THD%, A)	Load current (THD%, A)	p.f	System voltage (V, THD%)
ZSI	53.87, 4.01	52.09, 26.08	0.968	299.8, 1.31
BB-ZSI	53.89, 3.85	52.08, 26.06	0.985	299, 1.02

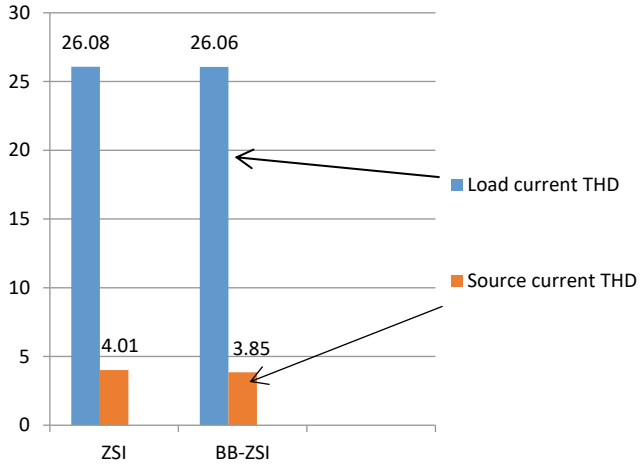

Fig. 10 After compensation supply current and non-linear load current THD factor of both topologies

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A Novel EDS Fed Trans-ZSI Based DSTATCOM for PQ Improvement

Mrutyunjaya Mangaraj, Jogeswara Sabat, and Ashok Kumar Chahattaray

1 Introduction

Power Electronics devices play a major role in transferring electrical power from energy sources to electrical distribution systems (EDS). This movement is predictable to continue and would therefore mandate the design of improved inverters. Contemporary power electronic device (conventional inverters) applications in EDS or grid integration usually require equal output voltage to match with PCC voltage. In traditional power inverters, most inverters can either be considered as a voltage source inverter (VSI) or a current source inverter (CSI) with each having some merits and demerits. In specific, VSI is referred to as voltage buck inverter and CSI is referred to as current buck inverter. Conversion using VSI and CSI, in different applications such as EDS, hybrid electric vehicles and photovoltaic systems suffer from some severe drawbacks [1]. The most straightforward method to add boost ability is to integrate a dc-dc converter at the front of the inverter [2–5]. But this process is not efficient and reliable because of more than one stage of power conversion and usage of more switches. The THD in VSI increases due to the dead time but it is required to avoid short circuits. Similarly, overlap time in CSI black out the semiconductor switches but it is required to avoid the open circuits [6].

First time in 2003, the ZSI is developed to overcome the demerits of conventional inverters like dead time issue. It also increases the importance of power electronics devices because it has the capability to transfer electrical power in a single stage with buck-boost voltage as per the system requirement [7]. The voltage boost gain of

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ZSI is inversely proportional to modulation index (M.I) and the small change in M.I produces high voltage stress on ZSI. But in theory the ZSI has infinite voltage boost gain [8–11]. The ZSI also has some negative aspects, such as large voltage stresses, discontinues input source current, high current at starting, high component count, and high THD at the output voltage waveform. To overcome the above drawbacks of ZSI, a quasi Z-source inverter (QZSI) was introduced in [12]. But it also suffers from higher component stress and found more distortion in output waveform. The increase in shoot-through duty ratio of QZSI decreases the M.I which reduces the output fundamental components and increases the distortion. To diminish these complications, a motivating approach is to use inductor coupled or transformer integrated to achieve both the required M.I and gain by reducing the component requirements [13–15].

At present, the inductor coupled and transformer integration inverters have made great progress in many fields of applications for gain boosting [15–17]. In this paper, a neural network based adaptive least mean square (ALMS) control technique is recommended for DSTATCOM operation to achieve the goals such as harmonic elimination with filtering performance, improvement in PQ, p.f correction and better voltage balancing at PCC [18–20]. The significant contributions of this research work are presented below:

i. In Trans-ZSI, the transformer is integrated with ZSI for high voltage boosting and the voltage of the primary inductor is transferred to the secondary inductor via magnetic coupling. Also the gain is increased by decreasing the turn ratio of integrated transformers instead of increasing the turn ratio.
ii. It achieves higher M.I with a small value of duty cycle, hence it reduces switching stress and supplies distortion free waveforms. This merit of Trans-ZSI based DSTATCOM has overcome the drawbacks of ZSI.
iii. In the traditional EDS, due to variation of non-linear loading and fault disturbance occurs which reduces the natural life of the DC link capacitor. Here, a transformer is connected with ZSI, and the electrical power from DSTATCOM to EDS is transferred only magnetically, a transformer provides isolation from the EDS. Thus the proposed system increases the natural life of the DC link capacitor.
iv. The THD of the source current and power factor are 4.01% and 0.968 respectively under ZSI based DSTATCOM. Whereas, the THD of the source current and power factor are 3.76% and 0.987 respectively obtained from Trans-ZSI based DSTATCOM.

To ensure stability, robustness, and increase the system performance of EDS, in Sect. 1, introduction and capability of the Trans-ZSI based DSTATCOM is presented. Section 2 shows the power circuit design of the Trans-ZSI and conventional ZSI, in sub-section Trans-ZSI operation is derived. The ALMS control scheme and its design are shown in Sect. 3. Simulation results used for comparison between the inverters are provided in Sect. 4. Finally, the conclusion is drawn in Sect. 5.

2 Circuit Configuration and Operation of Trans-ZSI Based DSTATCOM

A typical 3P3W EDS, in which a three phase non-linear load (uncontrolled rectifier with resistive and inductive load) is supplied by a three phase balanced source is depicted in Fig. 1. Figure 2 show the basic structure of a ZSI configuration. Compare to ZSI, in Trans-ZSI the capacitor C_2 is removed from the Z-network because the voltage of the primary inductor L_1 is transferred to the secondary inductor L_2 via magnetic coupling. In Fig. 3, Trans-ZSI configuration is illustrated. Pulses for switches of the Trans-ZSI are generated by using the ALMS control technique. Performance of both Trans-ZSI and conventional ZSI are maintained by similar types of loading for the PQ analysis.

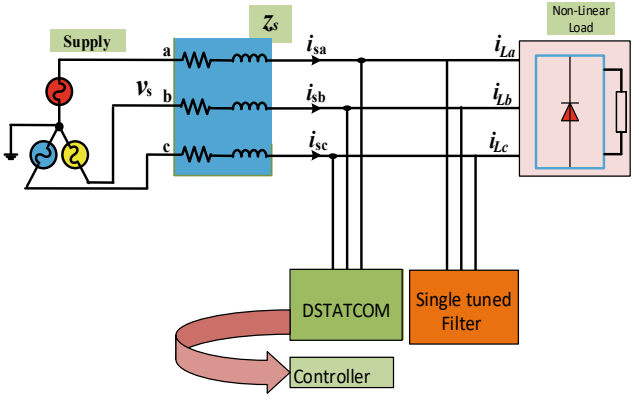

Fig. 1 EDS with trans-ZSI based DSTATCOM

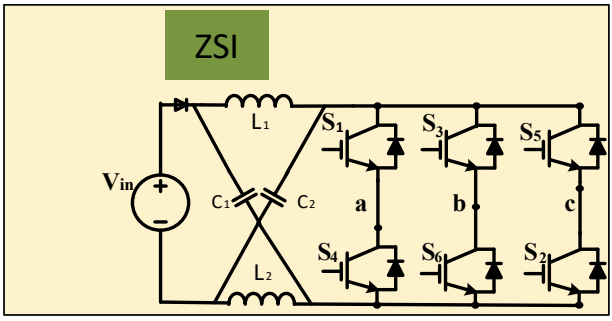

Fig. 2 ZSI configurations

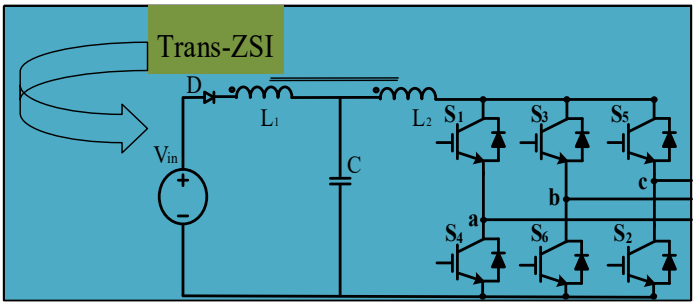

Fig. 3 Trans-ZSI configurations

2.1 Trans-ZSI Operations

The structural diagram of Trans-ZSI is depicted in Fig. 3. Two inductors L_1 and L_2 connected at the impedance network of Trans-ZSI as per the circuit diagram. The Trans-ZSI 'B' (boost factor) is calculated as

$$B = \frac{V_{pn}}{V_{in}} = \frac{1}{(1-(1+n)D)}$$

V_{pn} = dc link voltage
V_{pn} = input voltage
n = Transformer turns ratio

The process of switching signals generation for Trans-ZSI based DSTATCOM using ALMS control technique is derived in the next section.

3 Proposed ALMS Control Algorithm

In this section, the ALMS technique is discussed by considering the different weighting parameters like learning rate, step size, unit input weights and bias etc. The main purpose is to provide an individual phase tuned weight equivalent to the system frequency active component of the three phase load current. The learning mechanism of the ALMS algorithm is shown in Fig. 4 and expressed as per the following iteration.

The updating weights (w_{pa}, w_{pb}, w_{pc}) of active part of the load current are calculated as

$$w_{pa}(n) = \alpha\gamma\left\{i_{la}(n) - w_{pa}(n-1)u_{pa}(n)\right\}u_{pa}(n) + w_{pa}(n-1) \quad (1)$$

$$w_{pb}(n) = \alpha\gamma\left\{i_{lb}(n) - w_{pb}(n-1)u_{pb}(n)\right\}u_{pb}(n) + w_{pb}(n-1) \quad (2)$$

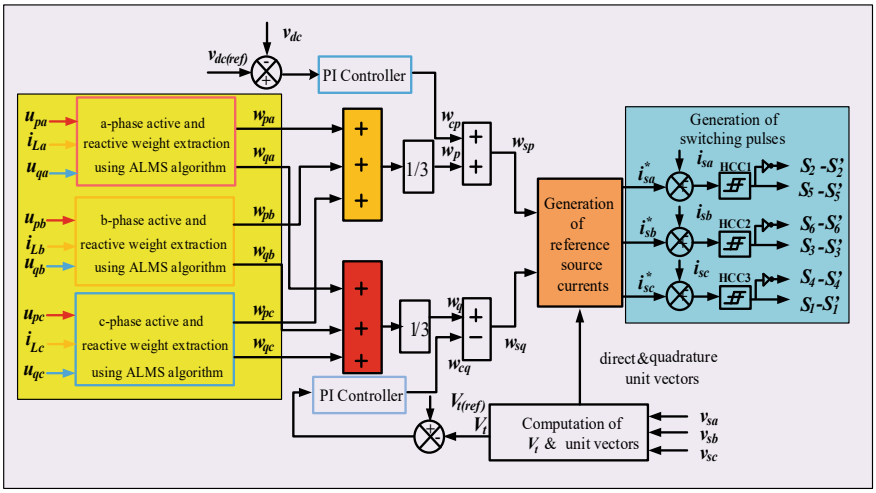

Fig. 4 Switching signal generation using ALMS principle

$$w_{pc}(n) = \alpha\gamma\left\{i_{lc}(n) - w_{pc}(n-1)u_{pc}(n)\right\}u_{pc}(n) + w_{pc}(n-1) \tag{3}$$

The updating weights (w_{qa}, w_{qb}, w_{qc}) of reactive part of the load current are calculated as

$$w_{qa}(n) = \alpha\gamma\left\{i_{la}(n) - w_{qa}(n-1)u_{qa}(n)\right\}u_{qa}(n) + w_{qa}(n-1) \tag{4}$$

$$w_{qb}(n) = \alpha\gamma\left\{i_{lb}(n) - w_{qb}(n-1)u_{qb}(n)\right\}u_{qb}(n) + w_{qb}(n-1) \tag{5}$$

$$w_{qc}(n) = \alpha\gamma\left\{i_{lc}(n) - w_{qc}(n-1)u_{qc}(n)\right\}u_{qc}(n) + w_{qc}(n-1) \tag{6}$$

The three phase average active component weight (w_a) is given as:

$$w_a = \frac{w_{pa} + w_{pb} + w_{pc}}{3} \tag{7}$$

Similarly, the three phase average reactive component weight (w_r) is given as:

$$w_r = \frac{w_{qa} + w_{qb} + w_{qc}}{3} \tag{8}$$

Active unit voltage templates (u_{pa}, u_{pb}, u_{pc}) are estimated as:

$$u_{pa} = \frac{v_{sa}}{v_t}, u_{pb} = \frac{v_{sb}}{v_t}, u_{pc} = \frac{v_{sc}}{v_t} \tag{9}$$

Similarly, the reactive unit voltage templates (u_{qa}, u_{qb}, u_{qc}) are estimated as:

$$u_{qa} = \frac{u_{pb} + u_{pc}}{\sqrt{3}}, u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \quad (10)$$

where v_t can be expressed as

$$v_t = \sqrt{\frac{2\left(v_{sa}^2 + v_{sb}^2 + v_{sc}^2\right)}{3}} \quad (11)$$

The difference between reference dc voltage and sensed dc voltage is the error in dc voltage (v_{de}) can be expressed as

$$v_{de} = v_{dc(ref)} - v_{dc} \quad (12)$$

$$w_{cp} = k_{pa} v_{de} + k_{ia} \int v_{de} dt \quad (13)$$

$$w_{sp} = w_a + w_{cp} \quad (14)$$

The ac voltage error (v_{te}) is determined by subtracting sensed amplitude of PCC from reference ac voltage is calculated as

$$v_{te} = v_{t(ref)} - v_t \quad (15)$$

The output of PI controller can be expressed as [16–18]:

$$w_{cq} = k_{pr} v_{te} + k_{ir} \int v_{te} dt \quad (16)$$

The reference source current is obtained by subtracting the average magnitude of reactive component of load current from the output of AC side PI controller as

$$w_{sq} = w_r - w_{cq} \quad (17)$$

Three phase instantaneous reference source active components are estimated as

$$i_{aa} = w_{sp} u_{pa}, i_{ab} = w_{sp} u_{pb}, i_{ac} = w_{sp} u_{pc} \quad (18)$$

Similarly, three phase instantaneous reference source reactive components are estimated as

$$i_{ra} = w_{sq} u_{qa}, i_{rb} = w_{sq} u_{qb}, i_{rc} = w_{sq} u_{qc} \quad (19)$$

$$i_{sa}^{*} = i_{aa} + i_{ra}, i_{sb}^{*} = i_{ab} + i_{rb}, i_{sc}^{*} = i_{ac} + i_{rc} \tag{20}$$

The reference source currents ($i_{sa}^{*}, i_{sb}^{*}, i_{sc}^{*}$) and the real supply currents (i_{sa}, i_{sb}, i_{sc}) of 3-phase are evaluated, and after that the error in signals are fed to the hysteresis current controller.

4 Simulation Results

The proposed Trans-ZSI is tested under PQ issue over ZSI. The different parameters and their magnitudes utilised to make the models are arranged in Table 1. At first, EDS is operated without connecting the DSTATCOM at PCC. It is observed from the simulation results that the source current is similar to the load current distortion. Next, the DSTATCOM is performed under both steady state and transient state loading to verify its effectiveness. The Trans-ZSI for PQ improvement and reliable operation in the field of EDS, compared with traditional single ZSI to justify the effectiveness through the simulation results, which are detailed below in the subsequent section.

4.1 Shunt Compensation Analysis of ZSI

The simulation model consists of ZSI, an uncontrolled bridge rectifier with $R = 10$ Ω and $L = 20$ mH for non-linear load, 230 V (rms)/phase balanced source voltage, system frequency 50 Hz and 600 V dc link reference voltage. The other details of the parameters used to construct the model are presented in Table 1. The load varying

Table 1 Proposed system parameters

Parameters	Magnitude
f_s (fundamental frequency)	50 Hz
v_{dc} (DC link voltage)	600 V
C_{dc} (capacitor)	2000 μF
K_{pa} (proportional controller gain)	0.01
v_s (system voltage)	230 V/phase
R_c (compensator resistance)	0.25 Ω
R_s (source resistance)	0.5 Ω
L_c (compensator inductance)	1.5 mH
L_s (source inductance)	2 mH
K_{pr} (source inductance)	0.2 mH
K_{ir} (AC Integral controller)	1.1
K_{ia} (integral controller gain)	0.05

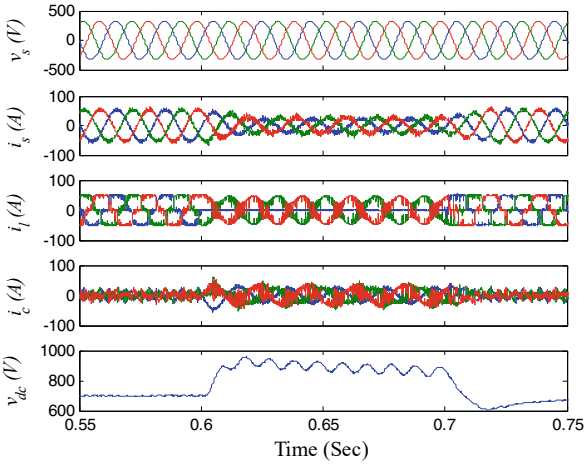

Fig. 5 System performance using ZSI based DSTATCOM

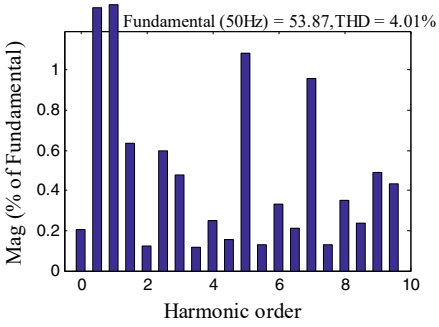

Fig. 6 ZSI source current THD after compensation

performance of ZSI are shown in Fig. 5. The impact of distortion in the PDN is testified at (0.55–0.6 s and 0.7–0.75 s) for steady state condition and (0.6–0.7 s) for dynamic state condition. ZSI is tested in time in varying responses of dc link voltage v_{dc} (ref) from 700 to 870 V. Figures 6 and 7 shows the harmonic content and THD factor of supply current 4.01%, 53.8 A and load current 26.08%, 52.09 A correspondingly.

4.2 Shunt Compensation Analysis of Trans-ZSI

The load varying performance of Trans-ZSI is shown in Fig. 8. The impact of distortion in the EDS is testified, at (0.55–0.6 s and 0.7–0.75 s) for steady state condition and (0.6–0.7 s) for dynamic state condition.

Proposed model is tested in time in varying responses of dc link voltage v_{dc} (ref) from 540 to 620 V. Figures 9 and 10 shows the harmonic content and THD factor of

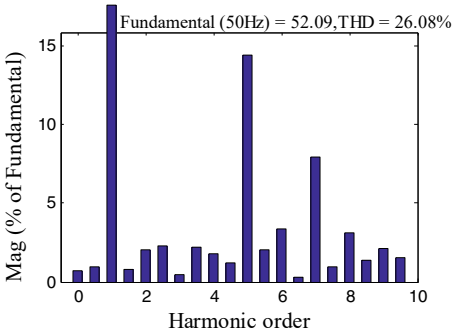

Fig. 7 ZSI load current THD after compensation

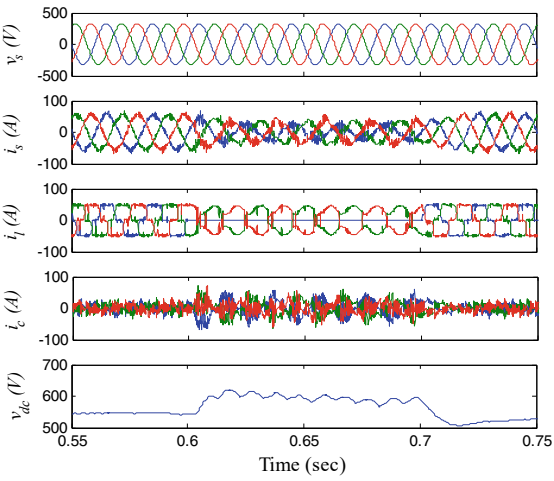

Fig. 8 System performance using Trans-ZSI based DSTATCOM

supply current 3.76%, 53.88 A and load current 26.10%, 52.01 A correspondingly. The source side harmonic reduction of EDS shows superior shunt compensation. Apart from this, reliability and flexible operation of the EDS are achieved. The comparison analysis of ZSI and Trans-ZSI are arranged in Table 2. The source current and load current THD analysis of ZSI and Trans-ZSI are presented in Fig. 11.

5 Conclusion

In this paper, the performance of Trans-ZSI based DSTATCOM under PQ issues is verified. Compared to the ZSI, the Trans-ZSI inherits some merits which are presented below:

- The suggested Trans-ZSI has higher buck-boost capabilities by dropping the components simultaneously.

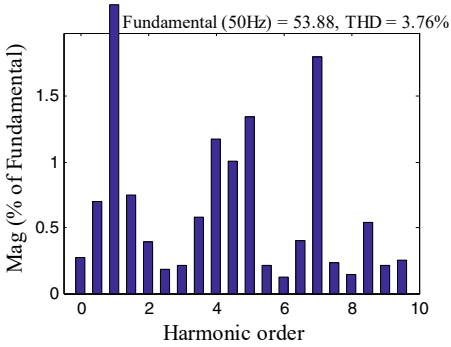

Fig. 9 Trans-ZSI source current THD after compensation

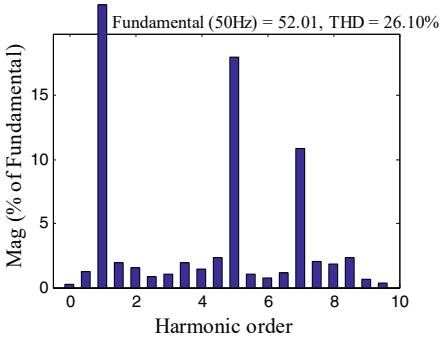

Fig. 10 Trans-ZSI load current THD after compensation

Table 2 Different parameters compensation analysis of both topologies

Topology	Supply current (THD%, A)	Load current (THD%, A)	p.f	System voltage (V, THD%)
ZSI	53.87, 4.01	52.09, 26.08	0.968	299.8, 1.31
Trans-ZSI	53.88, 3.76	52.01, 26.10	0.987	300, 1.12

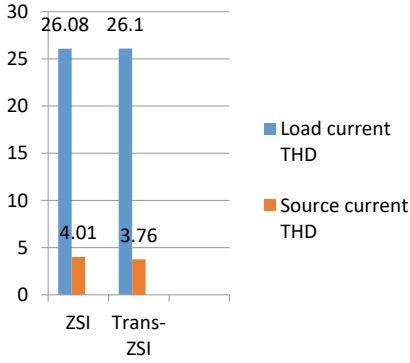

Fig. 11 After compensation supply current and non-linear load current THD factor

- It has low shoot-through duty ratio.
- The high quality and low distortion are found in output waveform of Trans-ZSI.

Further, it has been found that the Trans-ZSI suppresses the PQ issues and enhances the shunt compensation such as, efficiently abolishing the source side harmonic, minimizing switching losses, voltage balancing at PCC, p.f improvement, and reasonable voltage regulation at PCC. The future work will focus on renewable energy integration with present EDS considering both reactive power compensation and active power injection using the Trans-ZSI topology.

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PFC Isolated Cuk Converter Based Sensored BLDC Motor for the Application of Ceiling Fan

Tanya Agarwal and Prakash Chittora

1 Introduction

The BLDC motor is broadly used in applications where low and medium power is required comprising automotive, automated industrial equipment, aerospace, medical, consumer, transportation, robotics, renewable energy applications and instrumentation [1].

The Brush-less DC motor is a motor that works by a DC source with the help of an inverter and this inverter uses switching power supply which generates an electric pulse to run the motor and driving algorithm is used to drive the circuit.

The main advantage of this motor is its long-term use over a period of time. In BLDC motor [2] commutation is done electrically by switches instead of commutator and brushes which are used in DC motors. Comparing with an induction motor or DC motor, the BLDC motor has following advantages: (1) Lighter in weight, (2) More efficient, (3) Better controllability, (4) Higher speed range, (5) Stable performance even with unstable voltage conditions, (6) Good dynamic response, (7) Lower acoustic noise, (8) Better speed versus torque characteristics, (9) Longer life.

To run a BLDC motor [1], a power converter is required. In this arrangement, a rectifier and DC-DC converter are used, which give the required input to a VSI (Voltage Source Inverter) to run the BLDC motor for the application of fan. The switches of Inverter are switched according to the position of the rotor which is sensed using a set (usually 3) of position Hall-Effect sensors or using BEMF signals. The switching logic of 3 phase inverter is produced by the controller of the motor and

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according to the BLDC motor speed, the reference voltage is generated to regulate the voltage at the DC link.

The paper [1] deals with the pfc based cuk converter fed BLDCM fan and performance has been analyzed in four different modes of operation in CCM and DCM. The study shows that cuk converter with output inductor current operating in DICM is the best working mode.

Paper [3] presents the working of unity PF bridgeless isolated cuk converter based BLDC which eliminated the use of DBR hence, the conduction losses. There is another control strategy for BLDCM is considered that consists of current modulation [4].

The AC-DC pfcc brush-less motor fan using SEPIC is presented in DCM mode [2] with high-frequency transformer with improved power quality. This topology provides low harmonic distortion and lesser losses with reduced fan cost due sensorless technique.

The paper [5] analyses the behavior of ceiling fan using a bridgeless isolated pfc SEPIC converter in DCIM mode. This also uses an HFT which provides isolation in the system. The isolated sepic [6] based power supply gives excellent power quality at both input and output sides. This also provides a fast dynamic response, small size and less no. of components with a high degree of reliability and efficiency.

The system based on single switch boost-flyback converter [7] reduces the voltage sensor so reduces the cost of fan. The isolated converter HFT provided simple control, lower component count and isolation [6]. One more topology of flyback converter that is single stage bridgeless flyback (SSBL-Flyback) has been analyzed. This can reduce conduction losses [8].

Some research has also been done on pfc buck-boost converter [9, 10] for ceiling fan. This topology has less no. of components so it is a cost-effective solution for the system having low power.

Publication [11] analyses the performance of ceiling fan circuits using pfc zeta converter in DCM mode. This power supply uses high-side switch and gives protection from inrush currents, overload and short-circuits. These power supplies are also used in high power applications. Zeta converter also exhibits the continuous current on both input and output sides.

The paper [12] represents the close loop for the speed control of BLDC Motor as well as the dynamic modeling of BLDCM.

There are various other converter topologies investigated such as a BL-CSC converter (Bridgeless canonical switching cell) [13] for low power applications. Another is Bridgeless Luo converter [14] which works in DICM that performs as an inherent PF pre-regulator and the other one is Bridgeless Landsman converter [15] that works well for adjustable speed applications.

2 Converters Topology and PFCC Design

Various DC-DC Converters topologies have been used for controlling the speed of fan. Here, an isolated cuk converter is taken into consideration for the purpose of supplying DC voltage to the motor.

2.1 Overview of Isolated Cuk Converter

The single-phase AC-DC buck–boost converters are generally preferred and these are suitable for low power applications, which is less than 500 W.

Cuk converters are the also derived from the buck-boost converter and they also provide the almost same characteristics as buck-boost.

Here, the transformer helps to provide multiple outputs as well as the isolated converter with high-frequency transformer enables isolation, better control and electrical safety. The isolated cuk converter also shows excellent power quality at both the input and output sides.

Generally, the energy is transferred through inductors but in this topology, the energy is moved through capacitors. Hence both the current (input and output side) are continuous and the ripple in both input and output currents is lower than the other converters. This design provides a wide range of input and output voltage, very low switching current ripple, small size, high overall conversion efficiency and natural protection against inrush current so, this design is a popular choice for use [6]. Figure 1 demonstrates the complete working of Isolated Cuk PFC converter based sensored BLDC motor fan.

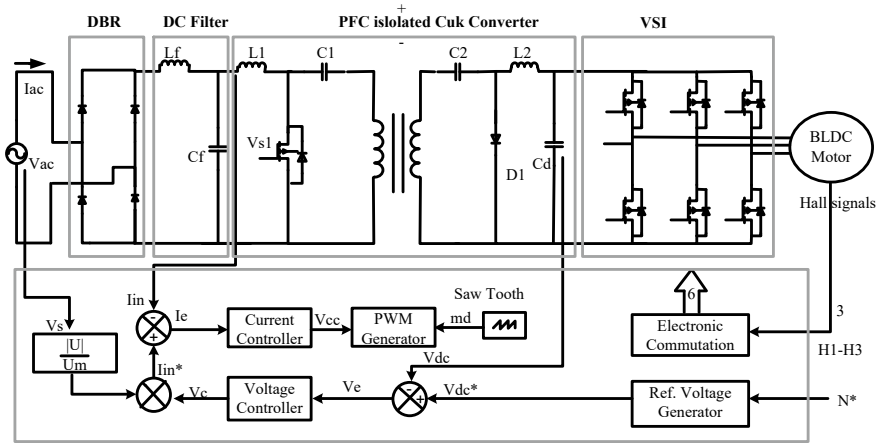

Fig. 1 A BLDCM drive fed by an isolated cuk PFC converter in CCM (with a current multiplier approach)

2.2 PFCC Design

This PFC converter is designed for an output voltage of 48 V and an input power of 30 W specifications. Here, the switching is taken as 200 kHz so that it reduces the inductor size. This converter works in CCM (continuous current mode) so a current controller is also used in close loop. This PFCC improves the power factor as well as the THD. With the change in output voltage of this converter, the speed of the BLDC motor changes so the fan speed can be controlled.

According to the variation in domestic power supply, the voltage variations are considered (or taken) as 85 V ($V_{\min}$) to 270 V ($V_{\max}$) and the DC link voltage from 10 V (VDC(min)) to 48 (VDC(max)) respectively.

2.3 Calculation

The values for the PFC converter can be taken according to design equations. The supply voltage for the DBR is

$$V_{in} = V_m.\sin(\omega t) \tag{1}$$

where, V_m is peak of supply voltage.

The average voltage of the DBR is

$$V_{in} = \frac{2\sqrt{2}.V_m}{\pi}\sin(\omega t) = 198.07\,\text{V} \tag{2}$$

The peak (or max) voltage is

$$V_m = \sqrt{2}.V_{in} = 311\,\text{V} \tag{3}$$

The peak voltage according to 85 V ($V_{\min}$) and 270 V ($V_{\max}$) will be 120.21 V and 381.83 V respectively.

The DC link voltage (V_{dc}) is taken 48 V according to motor requirement.

Hence, the output voltage can be calculated by,

$$V_{dc} = \frac{D}{(1-D)} \times \frac{N_2}{N_1} \times V_m$$

Here, N_2/N_1 is the Transformer (HFT) turns ratio which is taken as 0.5 for the calculation. Hence, the duty ratio required for the system is,

$$D_{\min} = \frac{V_{dc}}{V_{dc} + (V_m)_{\max}\left(\frac{N_2}{N_1}\right)}$$

$$D_{\min} = \frac{48}{48 + \sqrt{2} \times 270 \times 0.5} = 0.2009$$

$$D_{nom} = \frac{V_{dc}}{V_{dc} + (V_m)_{nom}\left(\frac{N_2}{N_1}\right)}$$

$$D_{nom} = \frac{48}{48 + \sqrt{2} \times 220 \times 0.5} = 0.2358$$

$$D_{\max} = \frac{V_{dc}}{V_{dc} + (V_m)_{\min}\left(\frac{N_2}{N_1}\right)}$$

$$D_{\max} = \frac{48}{48 + \sqrt{2} \times 85 \times 0.5} = 0.4440 \tag{4}$$

The minimum, nominal and maximum duty ratio are 0.2009, 0.2358 and 0.4440 respectively. The converter is designed to operate in CCM, so the value for inductor (input side) can be calculated by considering 40% ripple in current as

$$L_1 = \frac{V_s D_{\max} T_s}{\Delta i_{L1}} = \frac{V_s^2 V_{dc} T_s}{\Delta i_{L1} \times P_{in} \times (n(V_m)_{\min} + V_{dc})} \tag{5}$$

$$L_1 = \frac{85^2 \times 48 \times 5 \times 10^{-6}}{0.4 \times 30 \times (0.5 \times \sqrt{2} \times 85 + 48)} = 1.33\,\text{mH}$$

Considering switching frequency as 200 kHz, the designed value of inductor is selected as 1.4 mH so that it will work in CCM.

The load resistance and input side capacitance of the converter are

$$R_{dc} = \frac{V_{dc}^2}{P_{in}} = \frac{48^2}{30} = 76.8\,\Omega \tag{6}$$

$$C_1 = \frac{V_m n^2 D_{\min}^2}{\Delta V_{c1} f_s R_{dc}(1 - D_{\min})}$$

$$= \frac{220 \times \sqrt{2} \times 0.2009 \times 0.5^2}{0.1 \times (\sqrt{2} \times 220 \times 0.5 + 48) 200{,}000 \times 76.8 \times (1 - 0.2009)}$$

$$C_1 = 12.55\,\text{nF} \tag{7}$$

The designed value of C_1 is selected as 15 nF and the voltage ripple is considered as 10%.

The magnetizing inductance of HFT can be calculated by the following equation

$$L_m = \frac{(1 - D_{\max})^2 R_{dc}}{2n^2 f_s D_{\max}} \tag{8}$$

$$L_m = \frac{(1-0.4440)^2 \times 76.8}{2 \times 0.5^2 \times 0.4440 \times 200{,}000} = 534.72\,\mu\text{F}$$

The magnetizing inductance of HFT was chosen as 390 μF.

The capacitor C_2 can be calculated as

$$C_2 = \frac{P_i}{\Delta V_{dc} f_s (n.\sqrt{2} V_{in} + V_{dc})} \tag{9}$$

$$C_2 = \frac{30}{0.1 \times 48 \times 200{,}000(0.5 \times \sqrt{2} \times 220 + 48)} = 0.15\,\mu\text{F}$$

The designed value of C_1 is selected as 0.15 μF and the voltage ripple is considered as 10%. The inductor L_2 can be calculated as

$$L_2 = \frac{(V^2_{in(\min)}/P_{\max}) \times V_{dc(\max)}}{\Delta i_{L2} f_s \sqrt{2} V_{in(\min)}} \left(\frac{V_{dc(\max)}}{V_{dc(\max)} + \sqrt{2} V_{in(\min)}} \right) \tag{10}$$

$$L_2 = \frac{\left(\frac{85^2}{30}\right) \times 48}{0.4 \times 200{,}000 \times \sqrt{2} \times 85} \left(\frac{48}{48 + \sqrt{2} \times 85} \right)$$

$$L_2 = 0.34\,\text{mH}$$

The output capacitor of converter can be calculated as

$$C_{dc} = \frac{\left(\frac{P_{out}}{V_{dc}}\right)}{2\pi f \Delta V_{dc}} \tag{11}$$

$$C_{dc} = \frac{\left(\frac{30}{48}\right)}{2\pi \times 50 \times 48 \times 0.02} = 1036.7\,\mu\text{F}$$

Here, the ripple in the capacitor voltage is considered as 2%.

The designed value of capacitor can be chosen as 1200 μF.

2.4 Filter Design Calculation

The electromagnetic interference (EMI) filter is designed to remove the harmonics at the input current. The values for the same can be taken as

$$C_{fmax} = \frac{I_{pk}}{\omega . V_m} \tan\theta \tag{12}$$

$$C_{fmax} = \frac{\sqrt{2} \times \frac{30}{220}}{2 \times 3.14 \times 50 \times 311} \tan 1^\circ = 34.4\,\text{nF}$$

As, $C_f \ll C_{fmax}$, C_f is taken as 25 nF for design and according to the value of capacitor L_f is,

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} \tag{13}$$

$$L_f = \frac{1}{4\pi^2 \times 100{,}000^2 \times 25 \times 10^{-9}} = 101.42\,\mu\text{F}$$

f_c is chosen as, $f_1 << f_c << f_s$. Hence, f_c is taken as 100 kHz. Where f_1 is line frequency and f_c is cut-off frequency. The designed value is selected as 150 μF.

3 Dynamic Modeling of BLDC Motor

Modeling for BLDCM can be done as 3-ph induction motor. The stator winding of BLDCM can be represented as [12]

$$V_{an} = R_s + L.\frac{di_a}{dt} + M.\frac{di_b}{dt} + M.\frac{di_c}{dt} + E_a \tag{14}$$

$$V_{bn} = R_s + L.\frac{di_a}{dt} + M.\frac{di_b}{dt} + M.\frac{di_c}{dt} + E_b \tag{15}$$

$$V_{cn} = R_s + L.\frac{di_a}{dt} + M.\frac{di_b}{dt} + M.\frac{di_c}{dt} + E_c \tag{16}$$

where,

L is armature self-inductance [H],
R is armature resistance [Ω],
M is armature mutual inductance [H],
i_a, i_b, i_c are motor input current [A],
E_a, E_b, E_c are motor back-EMF [V],
V_{an}, V_{bn}, V_{cn} are terminal phase voltage [V].
In matrix form,

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} Rs & 0 & 0 \\ 0 & Rs & 0 \\ 0 & 0 & Rs \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} L & M & M \\ M & L & M \\ M & M & L \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix}$$

$$V_{an} = R_s + L.\frac{di_a}{dt} + M.\frac{d(i_b + i_c)}{dt} + E_a \tag{17}$$

$$V_{an} = R_s + L.\frac{di_a}{dt} - M.\frac{di_a}{dt} + E_a \tag{18}$$

$$V_{an} = R_s + (L - M).\frac{di_a}{dt} + E_a \tag{19}$$

$$V_{an} = R_s + L_s.\frac{di_a}{dt} + E_a \tag{20}$$

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} Rs & 0 & 0 \\ 0 & Rs & 0 \\ 0 & 0 & Rs \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + Ls \begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} + \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} \tag{21}$$

$$\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} = \frac{1}{L_s} \left\{ \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} - \begin{bmatrix} Rs & 0 & 0 \\ 0 & Rs & 0 \\ 0 & 0 & Rs \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} E_a \\ E_b \\ E_c \end{bmatrix} \right\} \tag{22}$$

The output power can be calculated as,

$$P_m = E_a.i_a + E_b.i_b + E_c.i_c \tag{23}$$

$$T_e = \frac{P_m}{\omega_{rm}} \tag{24}$$

$$T_e = \frac{E_a.i_a + E_b.i_b + E_c.i_c}{\omega_r}.\frac{P}{2} \tag{25}$$

$$T_e = \frac{(K_a.i_a + K_b.i_b + K_c.i_c)Wr}{\omega_r}.\frac{P}{2} \tag{26}$$

$$T_e = \frac{(K_a.i_a + K_b.i_b + K_c.i_c)}{2}P \tag{27}$$

The equation of mechanical part is represented as

$$T_e - T_L = J.\frac{d\omega_{rm}}{dt} + B\omega_{rm} \tag{28}$$

$$T_e = T_L + J.\frac{d\omega_r}{\frac{P}{2}dt} + \frac{B\omega_r}{\frac{P}{2}} \tag{29}$$

$$\frac{d\omega_r}{dt} = \frac{P}{2J}\left(T_e - T_L - \frac{2B.\omega_r}{P}\right) \tag{30}$$

Table 1 Motor parameters

Motor parameters	Rated values
Rated voltage	48 V
Rated torque	0.5 N m
Winding resistance	4 Ω
Winding inductance	10.75 mH
Rotor poles	16
Speed	350 rpm
V_k	127 V_{pk}/krpm

4 BLDC Motor Parameters

See Table 1.

5 Simulation and Results

Here, the performance of BLDCM fan can be seen using MATLAB results. The operation is performed under steady state and dynamic state conditions. In this, the power factor and THD have been measured for different supply voltages and corresponding RMS current. And different speed according to different dc link voltage of the motor for the fan application has also been measured.

5.1 Steady-State Operation

Figure 2 shows the low harmonic distortion in input current supply as per the IEC standard 61000-3-2 at 220 V input voltage. In steady state operation, Fig. 3a shows the waveforms of input supply Voltage, input current, DC link voltage and voltage across filter capacitor and Fig. 3b shows the waveform of current in inductor L_1, voltage across mosfet (switch), current in magnetizing winding (L_m), voltage across diode of converter. Figure 3c depicts the waveform of torque, hall sensor (A), back-EMF (E_a), current in stator winding (I_a) and speed of BLDCM (rpm). Figure 4 shows the low harmonic distortion in input current supply as per the IEC standard 61000-3-2 at 270 V input voltage.

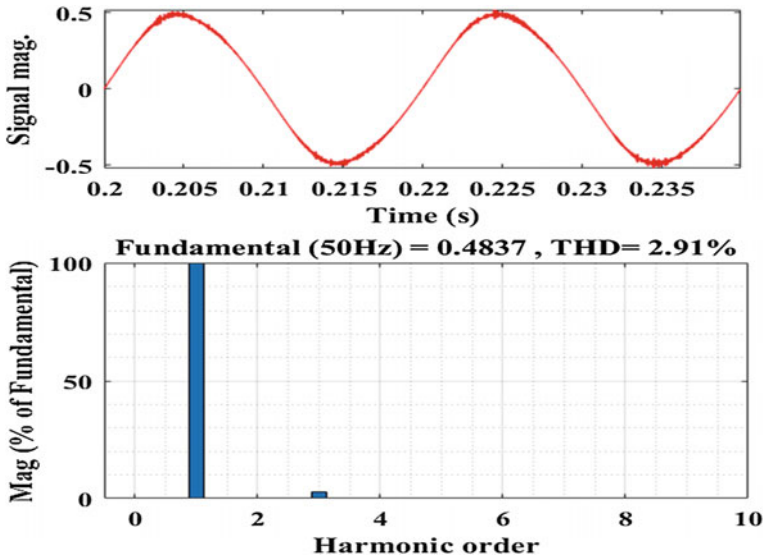

Fig. 2 THD in supply current (RMS) at a supply voltage of 220 V

5.2 Dynamic Operation

Figure 4 shows the dynamic behavior of BLDCM. In this input, supply has been changed from 220 to 270 V. Figure 3a shows the waveforms of input supply Voltage, input current, DC link voltage, voltage across filter capacitor and Fig. 3b depicts the waveform of torque, back-EMF (E_a), current in stator winding (I_a), speed of BLDCM (rpm).

5.3 Modes of a Ceiling Fan

The ceiling fan has different modes. Hence, speed varies according to the dc voltages of BLDCM. The Table 3 depicts the performance of fan under different modes.

6 Power Loss Analysis

The power loss analysis for the converter is

The power input for the converter is = 32 W.

The power output for the converter is = 28 W.

Hence, the power loss in converter is 4 W for BLDC motor fan.

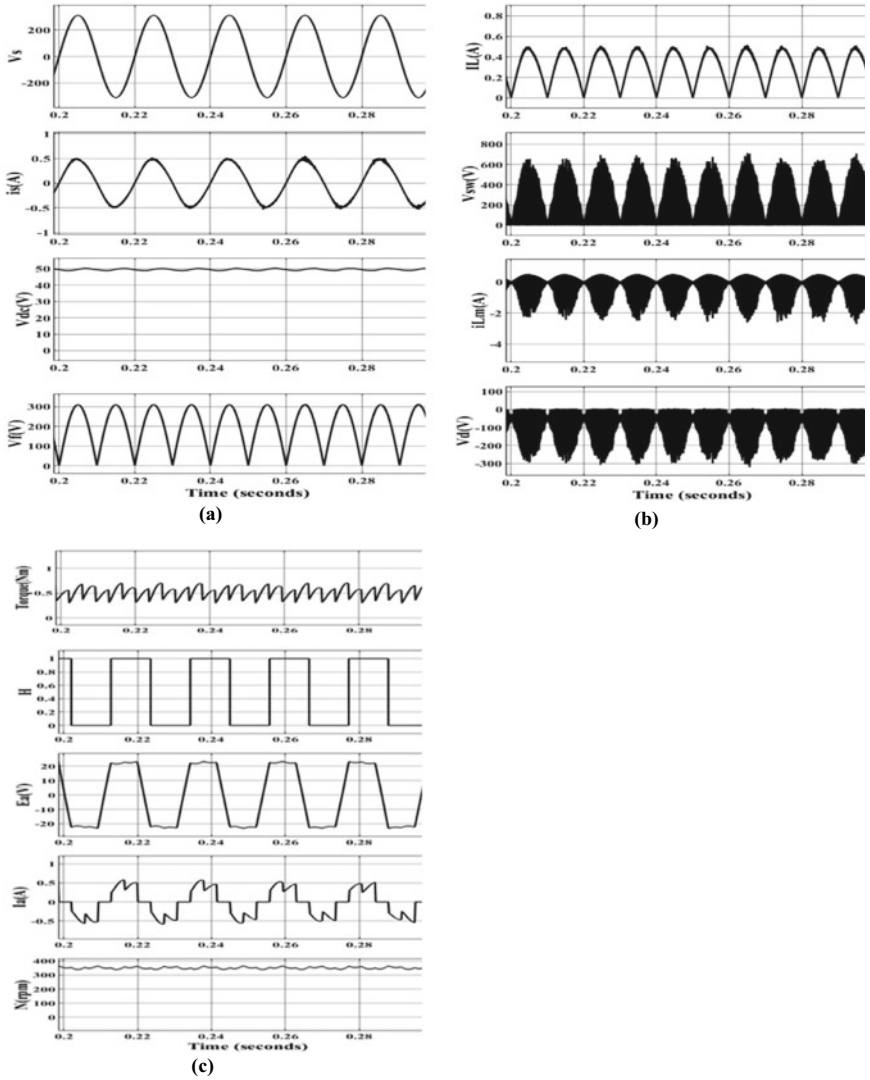

Fig. 3 (**a**), (**b**) and (**c**) performance of ceiling fan under the steady state condition at input supply voltage of 220 V and converter output voltage of 48 V

7 Conclusion

The Brush-less DC motor is driven using hall sensors under different voltage conditions and using MATLAB. It is found that the results satisfy the IEC standard 61000-3-2. Tables 2 and 3 shows the performance and power quality of BLDCM ceiling fan under different input supply and different DC voltage respectively. Figure 2 and

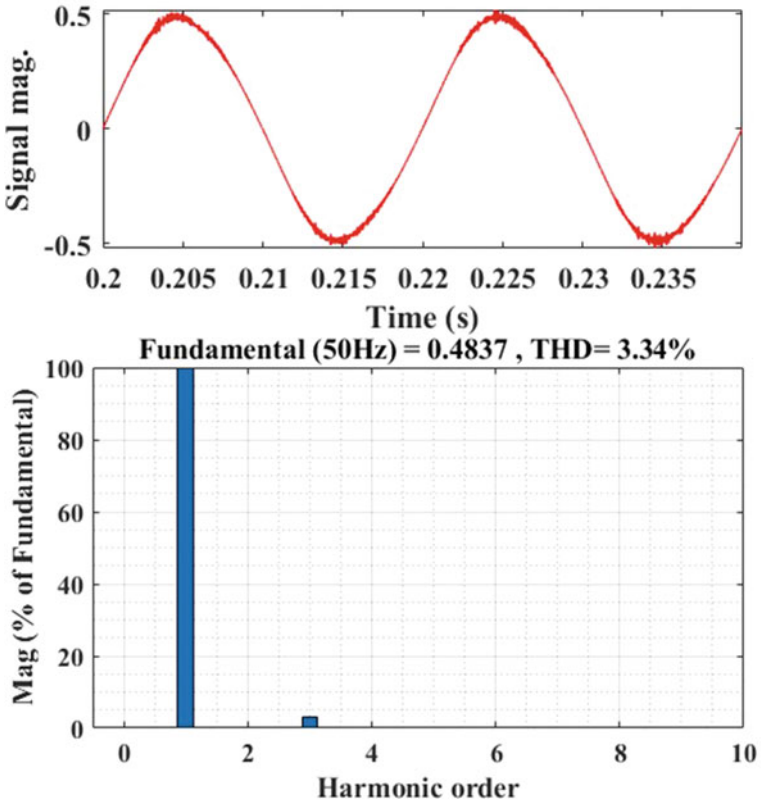

Fig. 4 THD in supply current (RMS) at a supply voltage of 270 V

Table 2 BLDCM performance for different value of supply voltage

V_s (V)	I_s (mA)	PF	THD (%)
85	598.7	0.999	1.52
110	527.1	0.999	1.94
160	424.8	0.999	2.53
220	371.2	0.999	2.92
270	335.8	0.999	3.34

Fig. 4 shows the THD in input current at 220 V and 270 V respectively and Fig. 3 shows the steady state operation at 220 V and Fig. 5 shows the dynamic operation from 220 to 270 V. Hence BLDC motor fan performs better when there is an unstable power supply. This design provides wide range of input and output voltage, very low switching current ripple, small size and high overall conversion efficiency.

Table 3 BLDCM performance for different converter output voltage

V_{dc} (V)	Speed (rpm)	I_s (mA)	PF	THD (%)
12	80	119.5	0.988	16.03
24	160	203.0	0.995	10.03
36	260	294.4	0.998	4.69
48	350	371.2	0.999	2.92

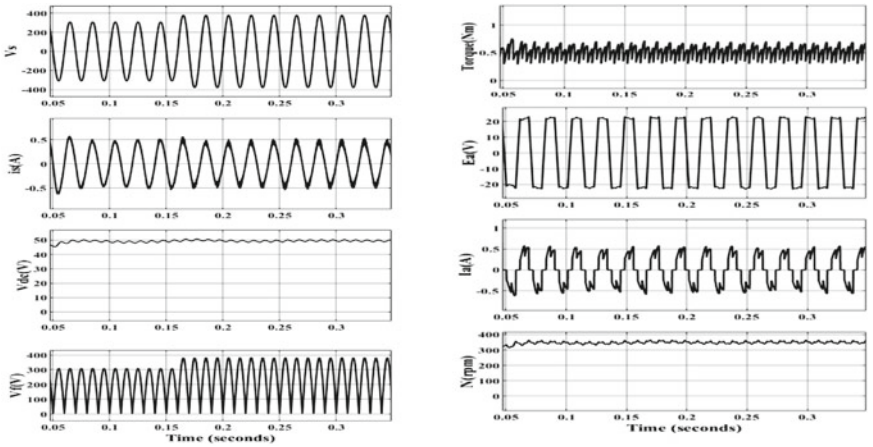

Fig. 5 (**a**) and (**b**) performance of ceiling fan under the dynamic condition varies input supply voltage from 220 V to 270 V at converter output voltage of 48 V

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Performance Analysis of Multi-level DC–AC Inverter for Solar Power Application

Richa Chaurasia and Shashi Bhushan Singh

1 Introduction

Increased energy demand has resulted in massive fossil fuel usage, which has a detrimental impact on the environment due to large greenhouse gas emissions. As a result, the necessity to transition to renewable energy resources has become unavoidable, resulting in growing awareness and popularity of renewable energy resources as a source of efficient electric power with virtually no pollution. Solar energy, wind energy, geothermal energy, hydropower, and many more are some of the renewable energy resources.

For the efficient conversion of various forms of energy to electrical energy, multiple power tracking systems, various power converter topologies, and several control approaches [1] have been developed. Still, additional study is being done on how to efficiently incorporate renewable energy sources into the electric grid. Power converters and their controls are receiving more attention as a result of their major role in power converters. In [2], different MLI topologies and their pros and cons are discussed, which helped in finding the best topology for solar.

MLI is commonly utilized in grid-connected, high-power, medium- and large-scale renewable energy systems [3]. MLI is required in PV Array for integration of PV into the power grid, for use in power applications, and also to have high voltage operation capability, high efficiency, high reliability, low switching losses, and good power quality performance [4–6].

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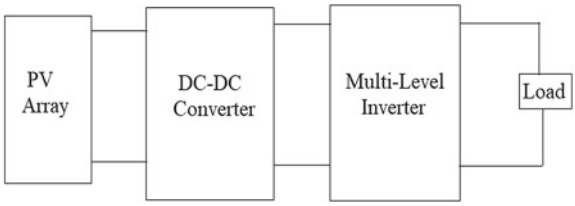

Fig. 1 Block diagram

Many topologies have been developed [7–9] which have only one advantage, either reduced count or lower THD. But in [10], both the advantage is found, which is reduced switch count and reduced THD.

Currently, the trends are the integration of MLI with renewable energy resources, having lower number of switches, lesser THD, new modulation technique, attenuation of leakage current [11], and application in medium and high voltage, application of MLI in PV having varying irradiance [12].

In this paper, Performance analysis of a Solar PV-based Multi-level Inverter for different load is proposed. The paper includes advantages of paper [10] and extends its application to solar PV array, since the use of renewable energy resources has become inevitable in absence of grid failure and to reduce the greenhouse effect, moving towards reducing carbon footprint. In this paper, Sect. 2 contains the circuit configuration; its basic block diagram is shown in Fig. 1. Section 3 contains simulation of the paper and also its results are discussed. The outcome of the paper i.e. conclusion is given in Sect. 4.

2 Circuit Configuration

In this paper, the main components include—PV array, DC-DC Converter, Seven Level Multi-level Inverter, and R-L load. Figure 1 depicts the block diagram of the circuit configuration used in this paper. The Solar PV Array generates dc power, which is supplied to a boost converter, which maintains a constant voltage regardless of the Photovoltaic array's irradiance or temperature. The dc voltage is then fed to Seven Level inverter for converting dc voltage into ac voltage and which is used to run R-L Load.

2.1 Photovoltaic System

PV-based power generation has received considerable attention because of its numerous benefits which include- ease of allocation, shorter installation time, long life, component portability, high mobility, and the ability to generate output power which can meet the peak load requirements. Solar PV arrays are used in a wide range

Table 1 Parameter values of solar PV

Parameter	Values
No. of parallel strings	2
No. of series strings	5
Open circuit voltage of solar PV	64.2 V
Short circuit current of Solar PV	5.96 A

of industrial applications including solar-powered water pump, battery charging system, solar hybrid electric vehicle, satellite power system, and many more.

MPPT tracks the maximum power using Perturb and Observe (P&O) Technique. MPPT compares the solar PV output power with the preceding perturbation cycle. The perturbation would keep on increasing in the very same direction if the power increases in the following cycle; if it does not, it will reverse. Hence, in this algorithm, the perturbation is provided to array terminal voltage for each cycle. As a result, after achieving the Maximum power, the P&O algorithm will fluctuate around it. The parameters used for PV are shown in Table 1.

2.2 DC-DC Converter

Because the PV output voltage is often insufficient to meet the load requirement in solar PV-fed system, the boost converter is required [13]. Boost converter increases input dc voltage, and produces increased dc voltage as an output. Figure 2 shows a boost circuit. It mainly consists of an IGBT (as a switch), an inductor, a diode, and a capacitor. The values of inductor and capacitor used here are 10 mH and 1000 μF respectively.

The IGBT (switch) is turned on and off by the duty cycle provided by the P&O algorithm. The boost circuit's output capacitor can help to reduce output voltage ripple.

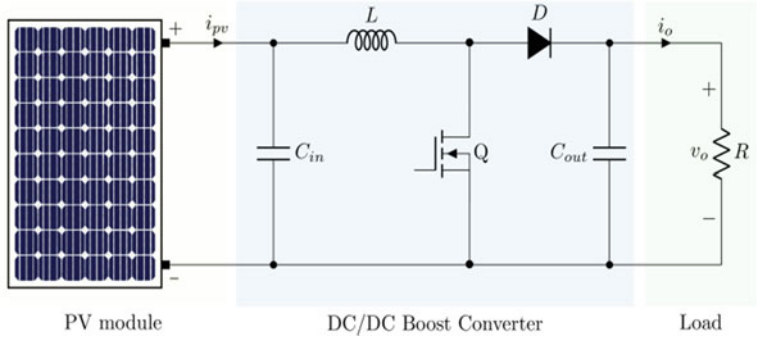

Fig. 2 PV-fed DC-DC converter

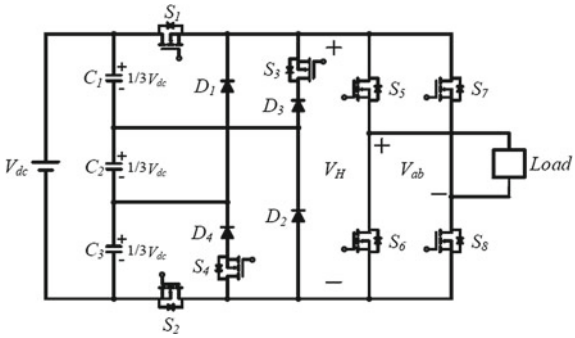

Fig. 3 Circuit of seven level MLI [10]

2.3 Multi-level Inverter

It is known that MLI is being preferred by everyone in every industrial and domestic application. Though it holds many attractive features, it also holds certain limitations. So, a new topology with a lower switch count and lower THD is employed to overcome these restrictions and to increase the beneficial effect of MLI [10].

Figure 3 depicts the 7-level inverter's power circuit, which includes C_1, C_2, and C_3 as dc-link capacitors across the applied dc source. The voltages are combined using S_1, S_2, S_3, and S_4 power semiconductor switches and D_1, D_2, D_3, and D_4 freewheeling diodes. It also has a standard two-level VSI circuit with power switches S_5, S_6, S_7, and S_8 for generating positive and negative half-cycles [10].

In this paper, the Phase disposition Level Shifted Multicarrier SPWM technique is used for providing gate pulse to switches. Here 3 carriers and 1 reference signal are used to generate a sinusoidal PWM signal.

Since voltage across each capacitor i.e. C_1, C_2, C_3, cannot be the same so a voltage balancing circuit i.e. Resonant Switching Capacitor Converter [14] is used to balance voltage across each capacitor, and hence reduces harmonic distortion in the output ac voltage of multi-level inverter. Figure 4 depicts the voltage balancing circuit used in the paper. Every switch has a duty cycle of 50%.

3 Results and Discussion

Figure 5 shows the Solar PV-based Multi-Level inverter for R-L Load. In this figure, the Solar PV is used to produce constant DC Voltage for MLI irrespective of temperature and irradiance, and then MLI subsequently transforms DC voltage to AC output Voltage. The R-L Load is fed by MLI, and results are obtained from simulation of MATLAB.

The dc voltage is constant irrespective of irradiance and temp. Figure 6 shows the varying irradiance from 1000 to 675 W/m^2 and temperature from 26 to 31.5 °C [12]. The irradiance is decreased from 1000 to 675 W/m^2 at instant $t = 0.6$ s and increases

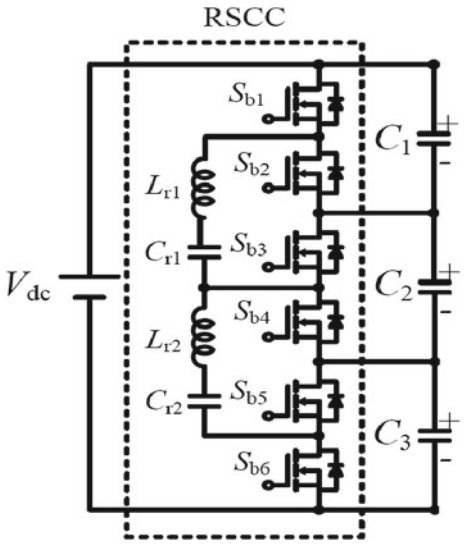

Fig. 4 Voltage balancing circuit [14]

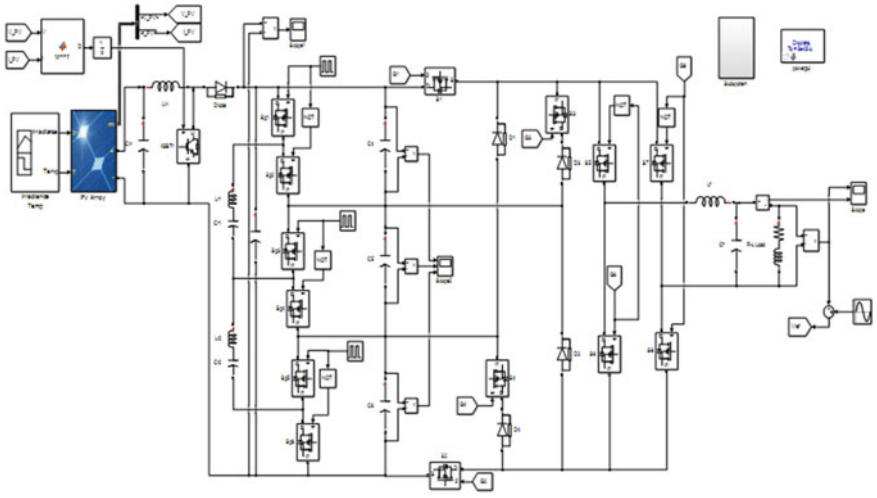

Fig. 5 Simulation of multi-level DC-AC inverter for solar application

from 675 to 1000 W/m^2 at instant $t = 1.2$ s and remains constant at 1000 W/m^2 from time $t = 1.6$ s. The temperature of the solar panel increases from 26 to 31.5 °C at time $t = 2$ s. The solar PV array's dc output can be seen in Fig. 7, which indicates that the PV array output is approximately 320 V and has very few ripples regardless of irradiance and temperature. The parameters used in this paper for solar PV is presented in Table 1.

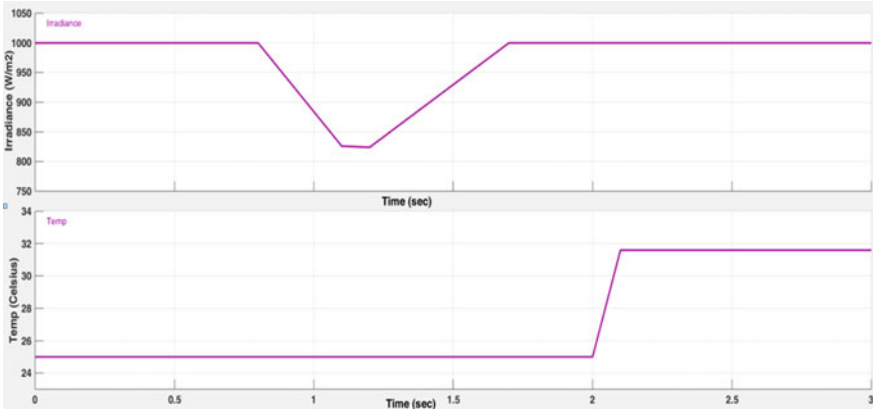

Fig. 6 Varying irradiance and temp

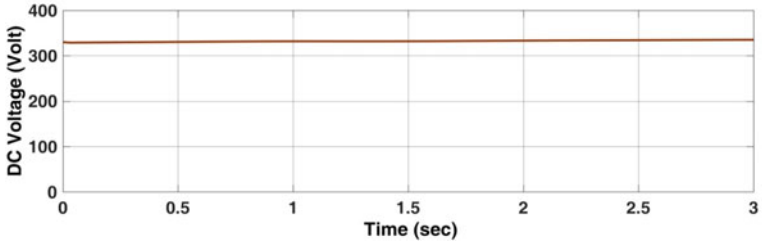

Fig. 7 DC voltage of solar PV array

Figure 8 shows the desired seven level output of the MLI. The figure shows seven level which are 106.67, 213.33, 320, 0, −106.67, −213.33, −320 V.

Figure 9 shows the capacitor voltage of C_1, C_2 and C_3 of MLI, in which voltage is equally distributed among them. The equal voltage across the three capacitors acts as

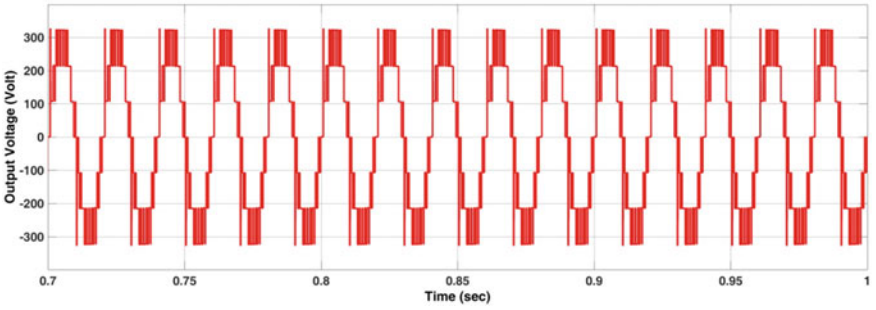

Fig. 8 Seven level AC

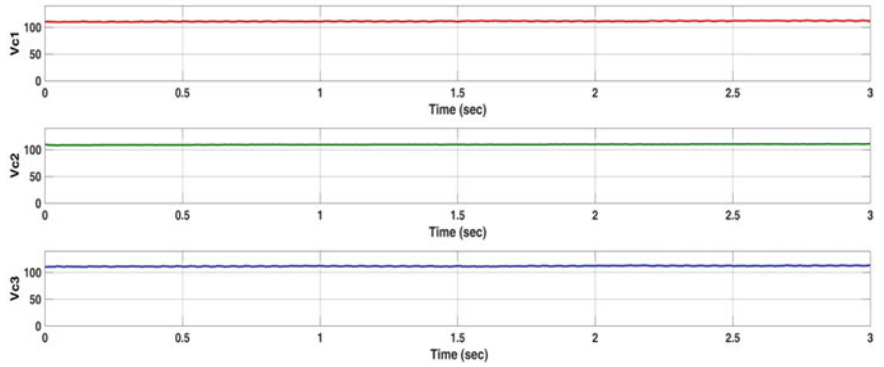

Fig. 9 Input capacitor voltage of MLI

three dc source and helps in generating seven level output. The voltage across each capacitor is approximately 106 V. The voltage balancing circuit helps in achieving balanced voltage [14].

Case 1: Full load

At full load and 0.95 pf, the rms voltage obtained is 220 V which can be seen in Figs. 10 and 11, the full load current is approx. 16.15 A. The generated AC output voltage and AC output current are extremely close to sinusoidal, with very little harmonic content, as seen in Figs. 10 and 11. Figure 12 depicts the THD of output voltage at full load. The THD obtained is 2.46%.

Case 2: Half Load

The rms voltage measured at half load and 0.95 pf is approximately 230 V, as shown in Fig. 13, and the half load current is around 8.99 A, which falls from the full load value as depicted in Fig. 14. Generated AC output voltage and AC output current are extremely close to sinusoidal, with very little harmonic content, as seen in Figs. 13

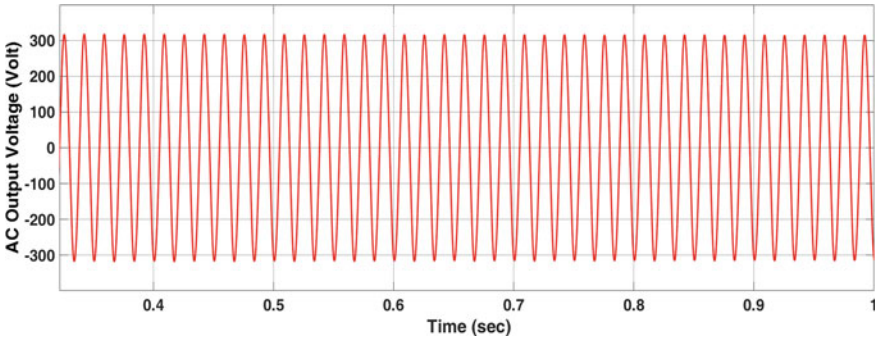

Fig. 10 AC output voltage of MLI at full load

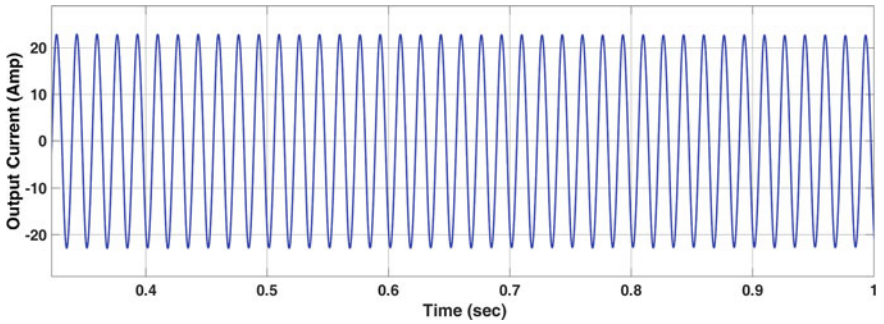

Fig. 11 AC output current of MLI

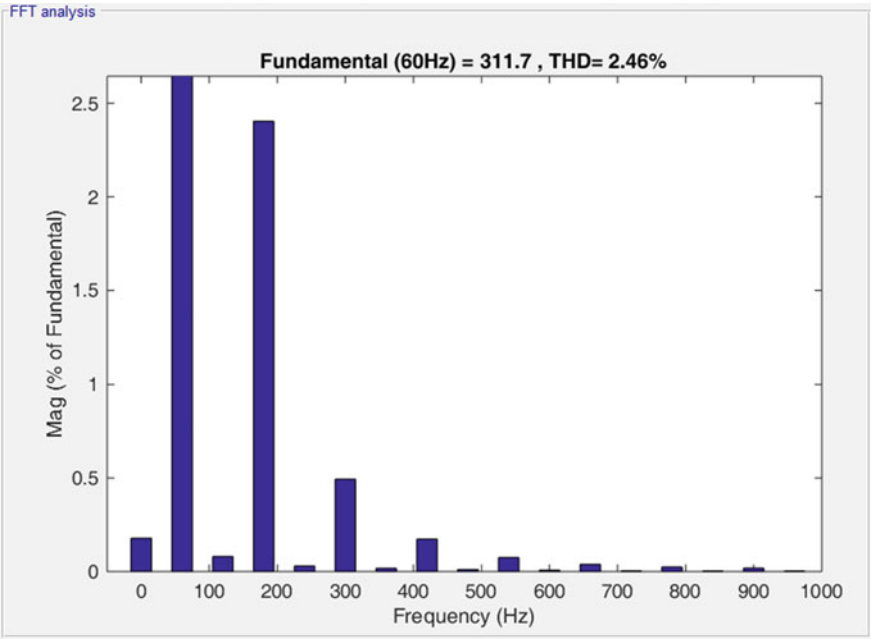

Fig. 12 THD of AC output voltage at full load

and 14. Figure 15 depicts the THD of AC output voltage at full load. The THD obtained is 2.19%.

The specifications of the MLI are:

DC Voltage $V_{dc} = 325$ V.
Output AC Voltage $= 220\ V_{rms}$.
Rated Power Output, $P_o = 3500$ W.
Switching frequency, $f_s = 20$ kHz.

Table 1 shows the various parameter values used in this paper.

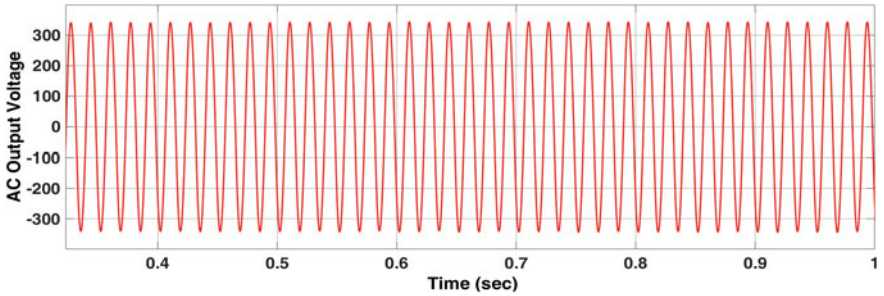

Fig. 13 AC output voltage of MLI at half load

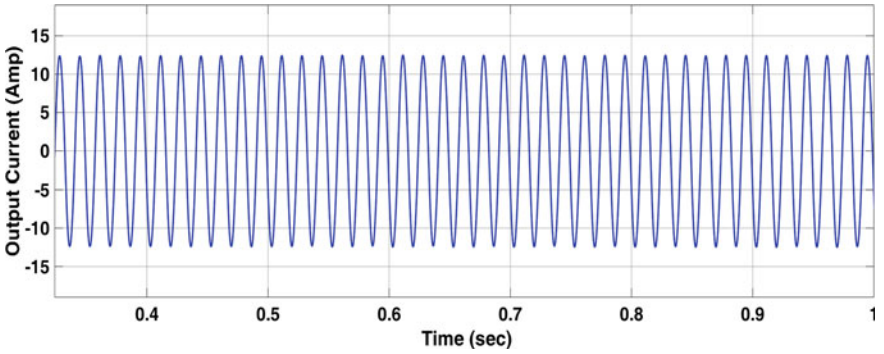

Fig. 14 AC output current of MLI at half load

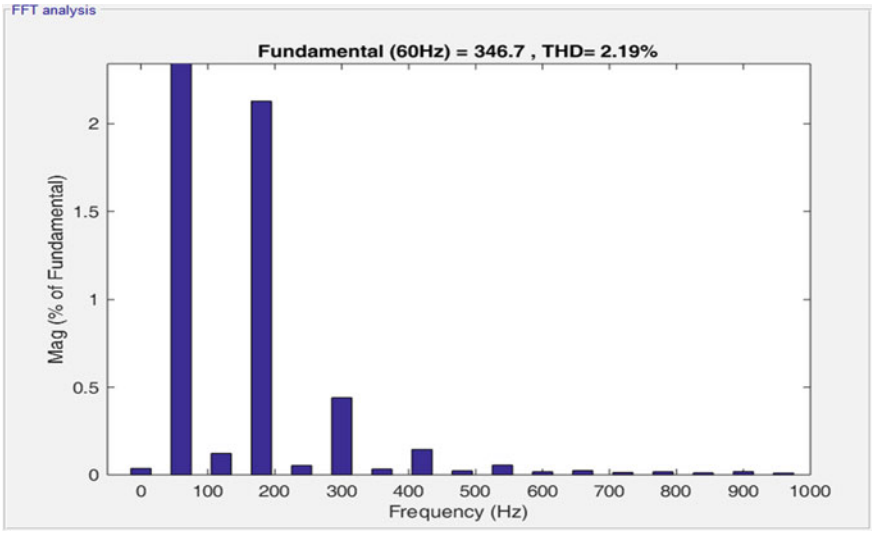

Fig. 15 THD of output voltage at half load

4 Conclusion

In this paper, analysis of MLI fed by PV Array for R-L Load with 320 V dc input and 220 V rms output with variable irradiance and temperature is proposed. The idea of this paper is to integrate MLI with PV array with varying irradiance and temperature while having reduced output voltage THD. MLI's gate pulses are controlled using the phase disposition SPWM approach. Analysis has been done at full load and half load at 0.95pf lag and the results are shown in the form of case 1 and case 2 respectively. The THD of output voltage has been found as 2.46% for full load and 2.19% for half load condition. For inductive loads like a motor, the overall system performance is determined to be satisfactory for different loading conditions.

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Development of a Smart Wind Monitoring System Using Arduino Technology

Papia Ray, Surender Reddy Salkuti, K. R. Satyajit, Abhilash Asit Kumar Majhi, and Chinmay Singh

1 Introduction

Today's world needs safe and clean energy. The energy is pollution-free, renewable, and easy to harness [1]. Political and environmental concern for sustainable development has encouraged electricity production growth from renewable sources. One of the most practical options is wind energy; furthermore, energy production from this type is more cost-effective [2]. Consumers of this energy need not require to invest in motor-generator units (Diesel) in distant locations where connection to a public electrical grid is not possible. The cost of operation rises in tandem with the price of petroleum. Academics and corporations all around the globe are currently attempting to minimize petroleum usage by incorporating the hybrid system into their varied presentations (thermal-wind, wind-diesel, etc.) [3]. Other sources of generation power, such as hydro, nuclear, and fossil fuels, currently provide a minor fraction of total power demand. An integrated electrical system for wind production covers just a small portion of the overall power demand [4].

Wind behavior research is essential for determining the practicality of wind power. Humans have not yet commercially exploited this unconventional source of energy. Wind power is a technically and economically viable solution for meeting energy needs in places with suitable climatic conditions [5]. As the world progresses, we need to incorporate the use of renewable energy to replace conventional sources. Wind energy being the most dominant source of renewable energy, needs equipment

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to measure wind speed and direction to harness wind energy [6] properly. This extremely feasible and cost-effective design can be used anywhere to determine wind speed and direction. This wind element data is beneficial to know the climatology of an area so that humans can utilize the wind conditions according to their needs. Wind data can also reduce or even avoid the risk of stormy wind. An automatic wind system is an electronic device that measures and records wind parameters with the help of sensors. This sensor serves as a measuring tool to measure any changes in the wind [7]. The output data from the sensor will be processed in the data logger and then sent to the webserver so that it can be accessed by users or people who need wind station data [8].

The paper is divided into five sections. The section gives an overview of the wind monitoring system and its need. Section 2 provides details about various apparatus used like NodeMCU and IR sensors and the thingspeak website. Section 3 describes how the designed device is connected and tested. Section 4 shows the results obtained through the proposed device. Section 5 gives a conclusion about the work.

1.1 Literature Review

This paper discusses the design techniques of wind direction and speed monitoring systems. With the facility access to the internet network, the occurrence of long-distance communication to send the results of sensor readings to the webserver is allowed. The operator can easily access the data collected by the wind monitoring system on the webserver to create and analyze or store data [9]. One of the main advantages of using a web server is that data is very secure.

The wind being a vector quantity, monitoring its speed and direction is crucial for wind power generation [10]. Wind power generation systems provide one of the most acceptable cost-effective percentages for renewable energy applications in houses, reducing bills for electricity by 50–90%. It is worth pointing out that commercial wind turbines for homes require a speed of at least 3 m/s to start up and a maximum average wind speed of 10 m/s to achieve maximum efficiency [11]. In general, energy production and savings are calculated primarily using the classical methods of energy generated, usable energy and useful energy dissipated. Wind speed and direction are independent variables that must be adequately modeled to accurately predict the performance of the wind power system [12]. The most suitable places for wind turbines are where the annual average wind speed is at least 14 km/h for small turbines and 21 km/h for more giant turbines. Speed and direction of the wind vary hourly and seasonally throughout India. This further pushes the need to design such a monitoring system that can measure and store the change in wind parameters. Wind energy makes up nearly 10% of India's total installed power production capacity [13]. To achieve the vision of net-zero carbon emission and clean energy production, non-conventional renewable sources need to be heavily exploited and commercialized [14]. Wind is the best energy source that is easy to use and harness energy provided we conduct a proper study on its parameters.

1.2 Objective

The primary goal of this work is to monitor the wind speed and direction of our locality and send it to the webserver. A proper setup consisting of an anemometer and a wind vane is built to achieve it. This setup is then attached with various sensors and microcontrollers to record, store and upload data to the webserver.

2 Proposed Mythology

This work starts with making an anemometer and a wind vane, which are then connected with the sensors. These sensors are then combined with the microcontroller and coding is done. The Thingspeak website is set up according to our specifications and the results are uploaded. We use 2 types of IR sensors to measure both speed and direction separately.

2.1 IoT and Things Speak Website

The Internet of things (IoT) describes real-time objects (or groups of such entities) connected with sensors, processors, software, and other technologies that exchange data with other devices and systems over the Internet or other communications networks. Thingspeak is a cloud-based IoT analytics platform that allows you to collect, visualize, and analyze real-time data streams. From the gadgets, we can submit data to Thingspeak to do preprocessing, analysis and visualization by writing and executing MATLAB code. Scientists and engineers can use Thingspeak to design and prototype IoT-based systems without servers or web software [15].

2.2 NodeMCU and Sensors

NodeMCU stands for Node Microcontroller Unit. The module named ESP-12E, which contains the ESP8266 chip with Tensilica Xtensa 32-bit LX106 RISC CPU, is included with the NodeMCU ESP8266 development board. The NodeMCU microprocessor supports RTOS and runs at a variable clock frequency of 80–160 MHz. It features 128 KB of RAM and 4 MB of Flash memory for data and applications. Its high processing power, built-in Wi-Fi/Bluetooth, and Deep Sleep Operating capabilities make it perfect for IoT projects. A Micro USB jack and Vin pin can be used to power NodeMCU (External Supply Pin) [16]. UART, SPI, and 12C interfaces are all supported. 8 IR sensors are used for 8 directions and 1 IR speed sensor is used

for measuring the speed. With the help of Arduino IDE software, code is written and uploaded to the NodeMCU [17].

3 Implementation

The overall block diagram in Fig. 1 illustrates creating an Arduino Based Wind Monitoring System using Cellular Networks or Wi-fi starting from the study literature, hardware design, software design, and testing processes. In the system block diagram (Fig. 1), the design process is carried out with the hardware design for each circuit block. At this stage, a series of microcontrollers and sensors are designed and users with desktops or smartphones can access the design of sensor data on the web. The following process is to assemble each circuit block and proceed with the software design process for several blocks of the circuit, including designing software for sensor components used and developing software for ESP8266 on Arduino-based microcontroller circuits.

Testing of each block consists of several stages:

- Testing of Arduino-based microcontroller circuits and wind direction and speed sensors.
- Testing data transmission systems with wi-fi and cellular on 3G/4G networks.
- Testing devices and results on web servers.

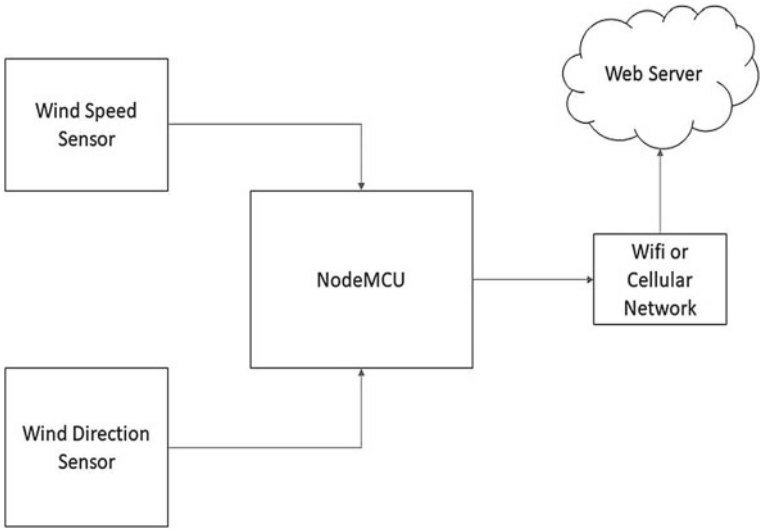

Fig. 1 Wind speed sensor and wind direction sensor built with IR speed sensor sending the data to NodeMCU

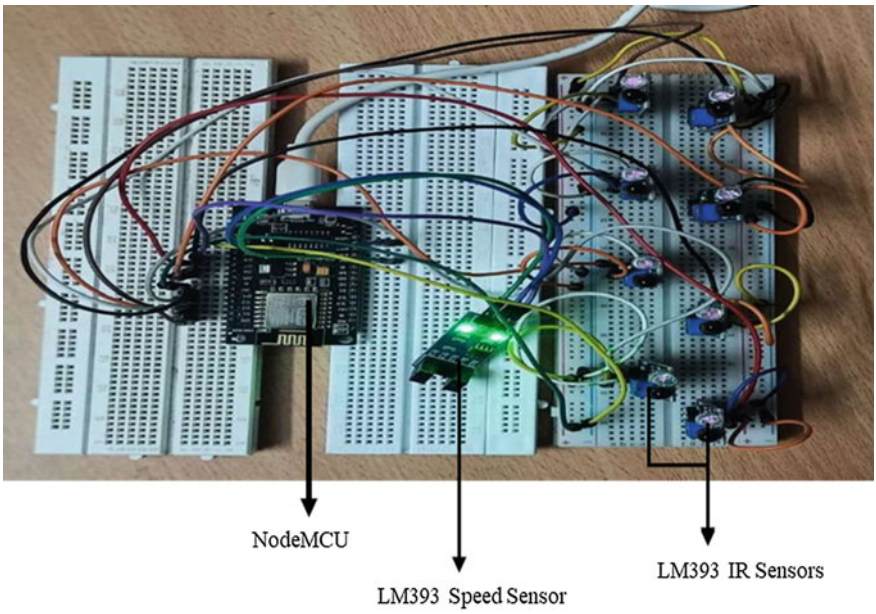

Fig. 2 Setup, coding, and testing of NodeMCU and IR sensors

The Arduino-based Wind Monitoring System uses 2 types of sensors, namely the LM393 speed sensor as a wind speed sensor and the LM393 IR sensor as a wind direction sensor. Data received by the sensor will be sent via the Cellular network or Wi-fi using a 3G/4G network. The software used in this design is the Arduino IDE Software with a sensor library that is already available.

3.1 Designing Devices with Sensors

The sensors used in this automatic wind monitoring system have their respective functions, LM393 speed sensor for measuring wind speed and LM393 IR sensor for measuring wind direction. All sensors get the same voltage from NodeMcu (Fig. 2).

3.2 Display Design Sensor Output on the Web

To display the results of the sensors used in the tool on the web, it is necessary to configure several items. The web used in this research is thingspeak which supports Arduino-based sensor systems. After registering on the web, thingspeak.com continues by creating a field or table containing sensor data. The number

of fields used is 2 fields according to the number of parameters measured through the device. Use the API keys in Arduino to indicate that the device is registered on the Thingspeak web.

4 Results and Discussion

Testing the wind monitoring system includes testing sensors, which run simultaneously. This test is done to observe the results of sensors on the Thingspeak web on 3G/4G cellular networks or Wifi. This test also aims to determine that each block diagram of the device has been successfully executed.

A. Sensor Testing

Testing the sensors as a whole can be seen on the serial monitor in the Arduino IDE program. The test includes data on wind speed and direction (Fig. 3).

B. Test results on the webserver

The data from the sensors are displayed on the graph at the Thingspeak.com website's public view.

Figure 4 shows the change in wind direction in a small interval of time. The directions are assigned with numbers as per the below table. The corresponding numbers are plotted on the chart. For example, at 20:21, it is planned 1 and the direction is North (Table 1).

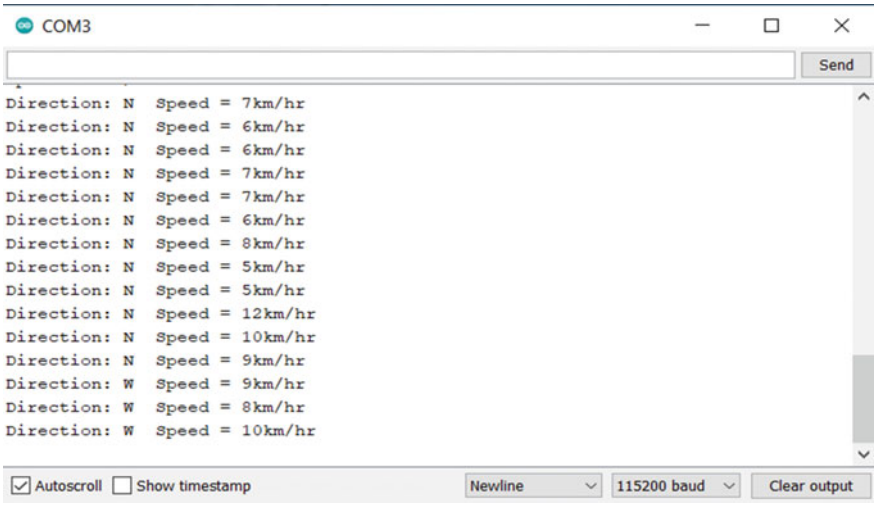

Fig. 3 Results obtained about wind speed and direction on the serial monitor

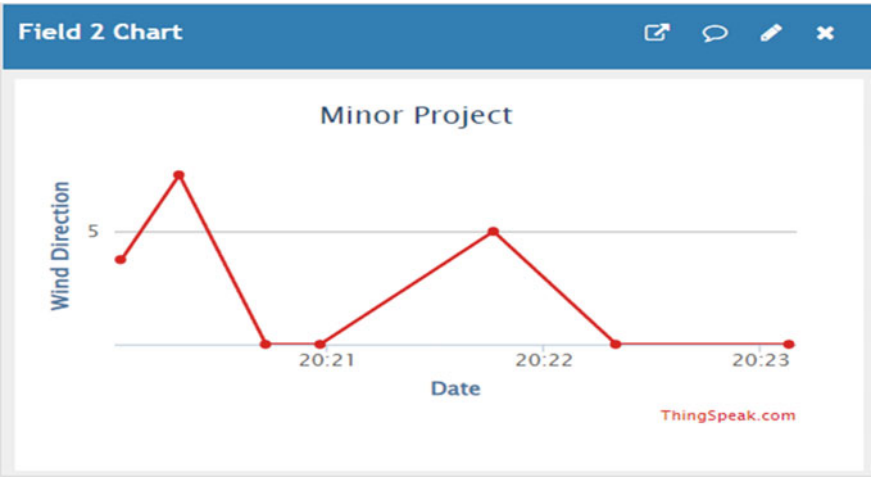

Fig. 4 Data about wind direction plotted on the Thingspeak website

Table 1 The symbology used for wind direction

Direction	Symbol	Associated no. on Thingspeak graph
North	N	1
North East	NE	2
East	E	3
South East	SE	4
South	S	5
South West	SW	6
West	W	7
North West	NW	8

Figure 5 shows the change in wind speed recorded by the IR speed sensor, sent and plotted on the website. It shows that wind speed is mostly around 7–9 km/h, corresponding to a gentle breeze.

5 Conclusions

Like many novel concepts, wind power energy generation requires incremental research to improve its application and better comprehend its future dynamics, problems, and potential. It has become necessary to predict or rather anticipate future wind speeds and directions in recent years. This enables planning and scheduling, the placement of appropriate wind farms, the estimation of total future energies generated from new wind projects, and the forecasting of energy needs. The proposed device

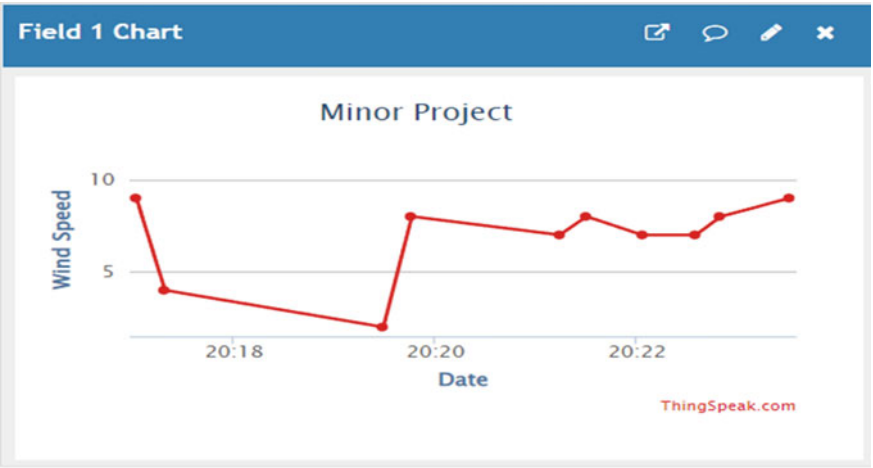

Fig. 5 Data about wind speed plotted on the Thingspeak website

in this paper consists of an anemometer and wind vane assisted with various sensors and a microcontroller that sends data to the Thingspeak website for visualization. It can be deployed in multiple locations and this Arduino-based Automatic Wind Monitoring System can work on 3G/4G Cellular Networks or over a Wi-fi network. Users need not personally visit and monitor where the gadget is located because the Thingspeak.com website can be used to monitor sensor data output remotely.

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Development of a Power Quality Analyzer Using Arduino Technology

Papia Ray, Nirlipta Parida, Suparna Biswal, and Arvind R. Singh

1 Introduction

A set of electrical boundaries that permits a piece of equipment to function in its intended manner without considerable loss of performance or life expectancy is referred to as "power quality." The two most significant power quality components are supply continuity and voltage quality [1]. The power system's economic operation requires that the power quality be maintained. It entails dealing with the negative impacts of over-voltages, under-voltage losses, and non-linear loads that inject harmonics into the system and reduce power factors.

A power quality analysis is performed to verify that all loads operate correctly. Improper wiring, inadequate grounding, and unbalanced loads are all circumstances that can cause electrical noise, harmonic distortion, and other power quality issues in an electrical system. Poor power quality manifests itself in service outages, device malfunction, and excessive power usage. Various power quality analysis approaches are currently in use. One is extracting fundamental and harmonic components from a voltage or current signals using the Fast Fourier Transform (FFT) in MATLAB for graphical analysis.

The primary goal of this paper is to create a smart power quality analyzer. Design of a low-cost and portable Power Quality Analyzer, calculation of parameters for monitoring power quality such as the power factor and THD, and validation of

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results using MATLAB/ SIMULINK are considered the essential sub-objectives to accomplish the main objective.

1.1 Literature Review

A power quality analysis is performed to verify that all loads operate correctly. Improper wiring, inadequate grounding, and unbalanced loads are all circumstances that can cause electrical noise, harmonic distortion, and other power quality issues in an electrical system. Poor power quality manifests itself in service outages, device malfunction, and excessive power usage. Various power quality analysis approaches are currently in use. One is extracting fundamental and harmonic components in voltage/current signals using the Fast Fourier Transform (FFT) in MATLAB and graphical analysis. J. Driesen et al. presented the development of an experimental flexible energy measurement system including a DSP, sensor, and communication components. This system is intended for modern electricity distribution networks with several suppliers in a deregulated market, bidirectional energy flows from distributed generation, and a wide range of power delivery quality demands. S. A. Deokar et al. attempted to investigate twelve forms of power quality disturbances, including seven basic and five combinations that were very near to real-world circumstances and were taken into account for classification by parametric equations [2]. Further, four more situations were investigated by adding noise to the four basic disturbances of sag, swell, harmonics, and flicker. M. J. B. Reddy et al. presented a Stockwell transform-based multipurpose real-time (hardware) PQ monitoring system (S-transform). In research on "Harmonic Analysis," Rajesh Ingale et al. proposed that the FFT spectrum differentiates the odd and even harmonic components and other waveform distortion components such as DC offset, inter harmonic notching, noise, and so on. In a study of low-cost power quality measurement devices, M. Szmajda et al. identified possible values for basic parameters used in digital signal processing to calculate time and frequency power quality parameters. Using the IEC technique, Javier Valenzuela et al. proposed research on windowing effects in inter harmonics identification. Because of its computational efficiency, the FFT was utilized for signal processing. Real-time platforms were used for simulations and experiments. Sawsan Sayed et al. proposed designing and deploying an open-source and modular smart meter with bidirectional communication capabilities that would substantially influence energy management and control systems that would benefit both the utility and the customers. Vicky T. Kullakar et al. investigated power quality with nonlinear loads. They estimated THD under these conditions using the FFT method, concluding that power quality in the power system is lowered only due to the nonlinear load. Bonar Harahap et al. proposed utilizing an Arduino to measure harmonic content, thereafter simulated using proteus software. This meter harmonic circuit is employed with resistor, capacitor, LCD, and Atmega 328P microcontroller. The microcontroller's software reads the voltage, and the current sent to the microcontroller. Lubis et al. attempted harmonic detection using Arduino and proposed

the critical benefits of the optimization method, namely, easier harmonic detection and accurate harmonic and THD measurement. Nonlinear loads are also thought to cause harmonic distortions in the power system. In a study, Jeremias Leda et al. used the FFT and Wavelets to detect power quality issues even when there was noise in the MATLAB environment. Difficulties arise when signals, even periodic signals of different fundamental frequencies, such as power system harmonics signals, are contaminated by noise. When a noisy time-domain signal is used to discover such frequency components, Fast Fourier transformations are used. According to the study, prominent peaks on the graph created by the FFT function ($y = fft(x)$) were used to extract the 3rd and 5th harmonics accurately. S. Thirunavukkarasu et al. used the FFT method to calculate the value of THD. The THD and power factor values are calculated or measured using a mathematical operation carried out by the programme downloaded to the Arduino UNO microcontroller. The THD and power factor values are calculated for single-phase and three-phase equipment used in enterprises and homes. P. Kumar et al. gave an overview of power quality difficulties, issues, world-wide standards, and remedy strategies. L. S. Pinto et al. developed a compression method to perform data storage more efficiently due to the vast volume of data created during power quality analysis. P. Suryawanshi and colleagues conceived and constructed a harmonic analyzer to investigate power systems' harmonic content.

1.2 Objective

The main objective of this work is to develop a smart power quality analyzer. The proposed design of a low-cost and portable Power Quality Analyzer necessitates the calculation of specific metrics for monitoring the various power quality parameters such as the power factor and THD and validating the obtained results using suitable software like MATLAB/SIMULINK.

The organization of the rest of the contents in this paper is in the following manner:

Section 2 presents the Power Quality concepts and various methodologies like FFT, harmonic analysis, an Arduino nano. Section 3 describes the implementation of the methods and the development of a smart power quality analyzer with Arduino, including the hardware setup and the software validation. The analysis of THD and error have been done and also the validation of the apparent result with the DSO (digital storage oscilloscope) has been shown in Sect. 4. Finally, Sect. 5 concludes the total work, and the results are discussed.

2 Power Quality Concepts

2.1 Fast Fourier Transform

Fourier analysis converts the waveform in the time domain into its frequency components and vice versa. The magnitudes and phases of the fundamental and harmonic components can be computed when the waveform is periodic [3].

Only one peak is produced when FFT is applied to a noise-free sinusoidal signal. This makes sense because a sinusoidal signal can be recreated with only one sinusoidal signal. The FFT uses some smart algorithms to do the same task as the DFT but a fraction of the time. A complex vector with n elements' finite, or discrete, Fourier transform is another complex vector y with n elements is given by:

$$Y_k = \sum_{j=0}^{n-1} \omega^{jk} \cdot y_j \tag{1}$$

where, ω is a complex nth root of unity:

$$\omega = e^{j2\pi/n} \tag{2}$$

2.2 Harmonic Analysis

Harmonic analysis is a technique for determining a linear structure's steady-state response to loads that vary concurrently in time. In harmonic response analysis, the transient that occurs at the initial state of excitation is not considered [4]. The periodic function $f(t)$'s trigonometric series is as follows:

$$f(t) = \sum_{n=1}^{\infty} \left(a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right) + a_0 \right) \tag{3}$$

where a_0 is the average value of the function $f(t)$ while a_n and b_n are the square components of the nth harmonic and the time interval is from 0 to T.

$$a_0 = \int_0^T f(t)dt \tag{4}$$

$$a_n = \frac{2}{T} \int_0^T f(t) \cos(n\omega t)dt \tag{5}$$

$$b_n = \frac{2}{T} \int_0^T f(t) \sin(n\omega t) dt \tag{6}$$

2.3 Total Harmonic Distortion (THD)

The ratio of the sum of the powers of all apparent harmonic components to the power of the fundamental frequency is known as THD. Lower THD in motors in power systems means lesser peak currents, less overheating, lower electromagnetic emission, and lower core loss. The Fast Fourier transform method is used in the experiment to determine the THD value. Among other things, the Fourier transform aids in the separation of odd/even and inter harmonics [5, 6]. More material is added at multiples of the original frequency when a sinusoidal frequency signal travels through a non-ideal, non-linear device. THD (Total Harmonic Distortion) is a metric that measures signal content that isn't present in the input signal. When the original sine wave's "purity" is the most critical performance criterion (in other words, the contribution of the actual frequency concerning its harmonics) [7]. The RMS amplitude of a sequence of higher harmonic frequencies divided by the RMS amplitude of the first harmonic frequency is the most frequent definition of THD.

$$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \cdots}}{V_1} \tag{7}$$

where V_n denotes the RMS value of the nth harmonic voltage and V_1 represents the RMS value of the fundamental component.

2.4 Arduino Nano

In the experiment, the Arduino Nano, a development board similar to the Arduino Uno but has a smaller form factor, was employed. It's an ATmega328P-based board that's compact, comprehensive, and easy to use on a breadboard. It features 30 male I/O headers structured in a DIP30-like style [7, 8].

2.4.1 Specifications

The maximum current rating of the Arduino Nano is 40mA, so any load connected to its pins must not exceed this number. The tasks assigned to these Digital and Analog Pins are varied, but their primary job is to be programmed as Input/Output.

Fig. 1 Arduino FFT library

When Arduino pins communicate with sensors, they act as input pins; when a load is powered, however, they act as output pins. Digital pin functions are controlled by PinMode() and digitalWrite(), while analogue pin operations are controlled by analogRead(). The analogue pins have a 10-bit full resolution and can sense values between 0 and 5 V [9].

2.4.2 Arduino FFT Library

Arduino FFT is a package that allows to perform floating-point FFT calculations on the Arduino platform. A block in this library calculates the frequency of a sampled signal. The technique for opening and installing the FFT library is depicted in the diagram shown in Fig. 1.

Figure 1 is a block diagram that shows the procedure to open and install the FFT library.

3 Implementation

3.1 Circuit Diagram

Figure 2 shows the circuit diagram of the proposed hardware setup done using Proteus.

3.2 Hardware Setup

An ACS712 20 A current sensor and a ZMPT101B AC single-phase voltage sensor were utilized in the suggested approach to detect the current and voltage at the given load. The current sensor was linked in series with the load, while the load was connected in parallel with the voltage sensor. The entire functional unit was interfaced using an Arduino Nano microcontroller. The data pins of both sensors were linked to one of the microcontroller's analogue pins. In contrast, the Vcc pins received a 5 V DC supply from the microcontroller and the ground connections were connected to the microcontroller's ground pins. The output values were also displayed in the

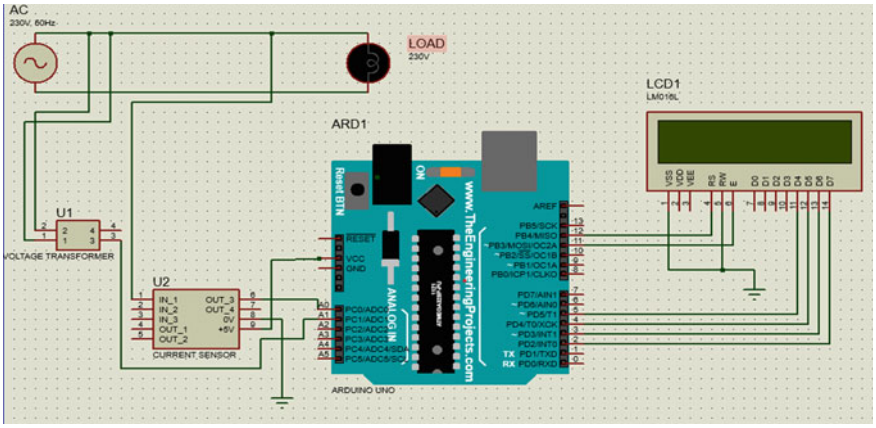

Fig. 2 Proteus circuit design

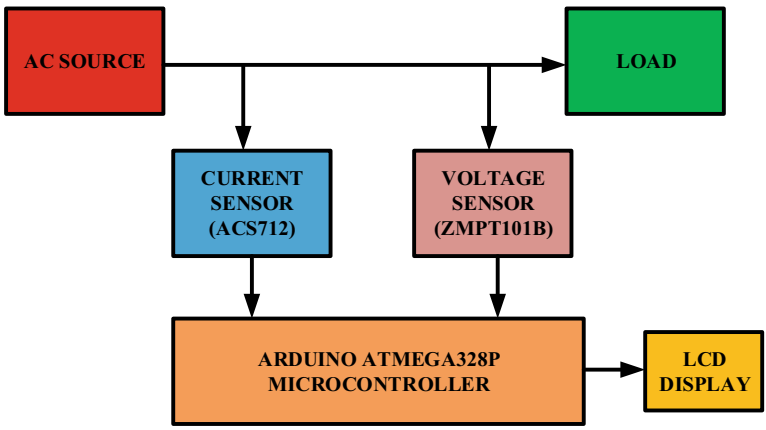

Fig. 3 Diagram of the proposed hardware setup

LCD using the Arduino microcontroller. Figure 3 shows the block diagram, which indicates how the hardware setup was done and Fig. 4 shows the hardware prototype for analysis of power quality parameters.

3.3 Working and Simulation

Figure 5 shows the proposed SIMULINK model, which can be done practically and various parameters such as power factor THD can be found. Also, the FFT analysis can be found using MATLAB/SIMULINK.

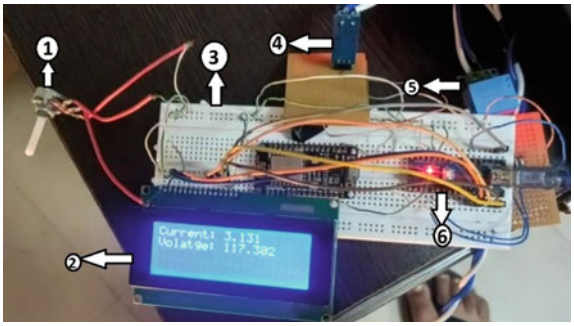

Fig. 4 Hardware setup. Legends: **1**. Potentiometer, **2**. 16*2 LCD display, **3**. Breadboard, **4**. ACS712current sensor, **5**. ZMPT101B voltage sensor, **6**. Arduino Nano

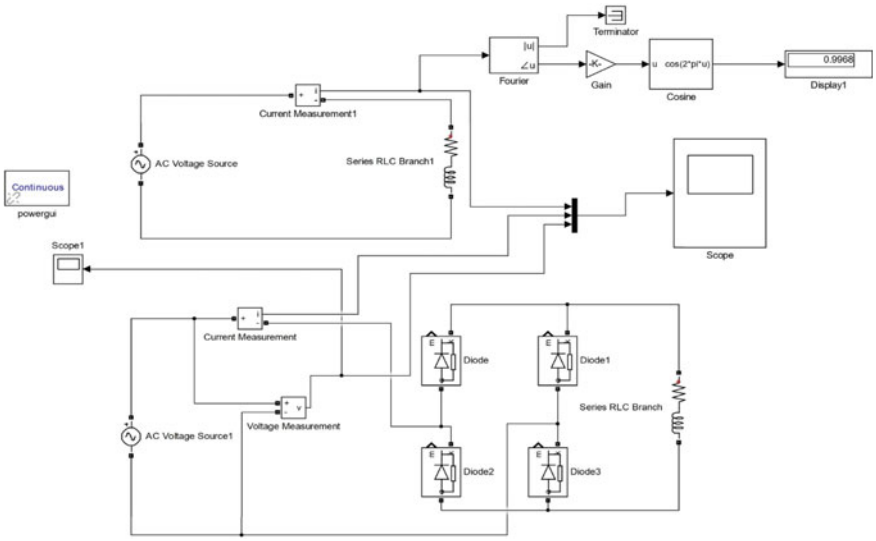

Fig. 5 Proposed Simulink model

3.4 Calculations

Table 1 shows the Voltage, Current, Power Factor, and THD%. The instantaneous values of Power Factor and THD% are calculated as shown in the table below. Table 1, shows the average voltage, current, power factor and THD measured using the power quality analyzer.

Figure 6 shows the graph between Frequency (on X-axis) in Hz and amplitude (on Y-axis) in decibels obtained while performing in hardware setup.

Table 1 Different parameters acquired from the power quality analyzer

Sr. No.	Voltage (V)	Current (A)	Power factor	THD (%)
1	201.48	2.131	0.89	30.131
2	211.98	2.054	0.94	28.072
3	221.52	1.9	0.969	25.506
4	222.74	1.9	0.957	29.919
5	217.36	1.823	0.949	26.336
6	206.36	1.823	0.9387	27.092
Average	213.573333	1.9385	0.940616667	27.842667

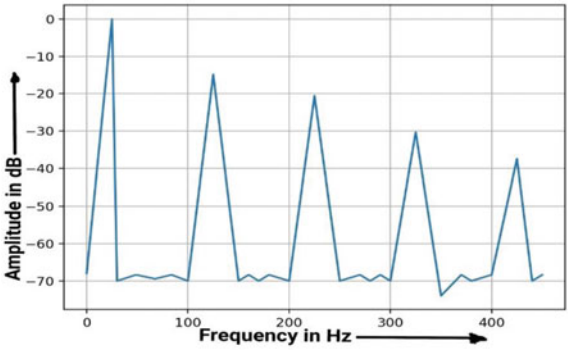

Fig. 6 Frequency versus amplitude

4 Results and Discussion

4.1 THD Analysis

The current waveform in Fig. 7 is compared to a reference value to determine whether the power signal has any frequency variations. If the frequency changes, harmonic distortion in the power stream may occur, reducing the equipment's lifespan. The current waveform is compared with the voltage waveform, which gives a reasonable estimate of the THD [10]. The application already uploaded in the Arduino compares the voltage value with the current waveform. This process shows the frequency change by comparing the current and voltage waveform with the fundamental frequency.

The voltage waveform is shown in Fig. 8 which results from the connections established in the circuit. The Arduino software compares the current and voltage waveforms and displays the frequency change as a THD value and a waveform. The frequency change is expressed as a THD value when the voltage and current waveforms are compared [11].

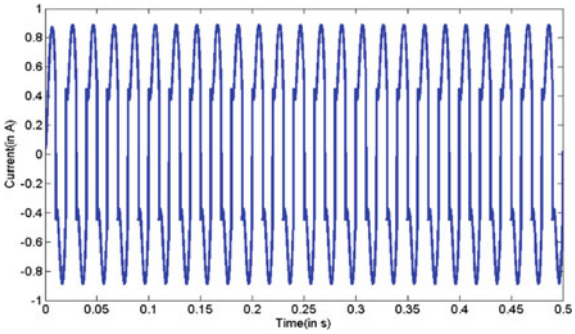

Fig. 7 Current waveform

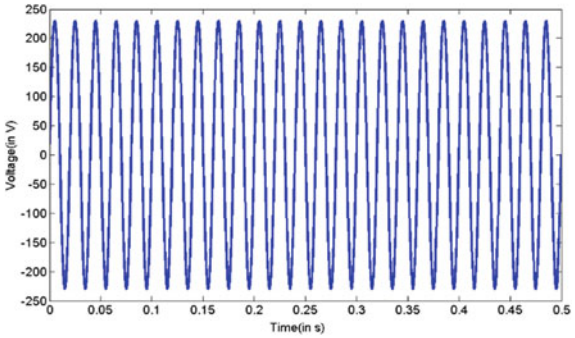

Fig. 8 Voltage waveform

The FFT analysis [12] for current and voltage is shown in Figs. 9 and 10. The harmonic order is determined by comparing the voltage/current value to the fundamental frequency [13, 14]. We can't verify the complete power signal. Therefore, we check the frequency variation in the first 5–8 cycles.

4.2 Validation Using Digital Storage Oscilloscope (DSO)

Figure 11 shows the graph between the Voltage versus Time and Current versus Time plotted simultaneously on DSO. The graph can be analyzed and the power factor of the connected R-L Load is calculated manually. The value of the Power Factor is found to be 0.96.

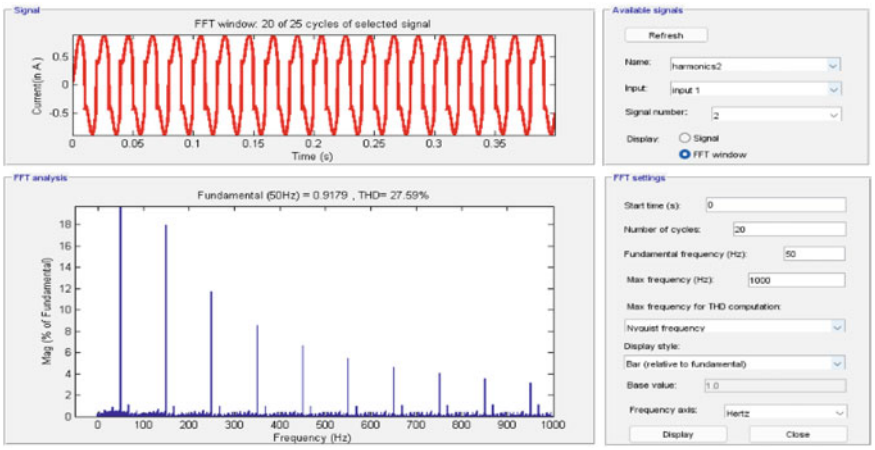

Fig. 9 THD analysis for current

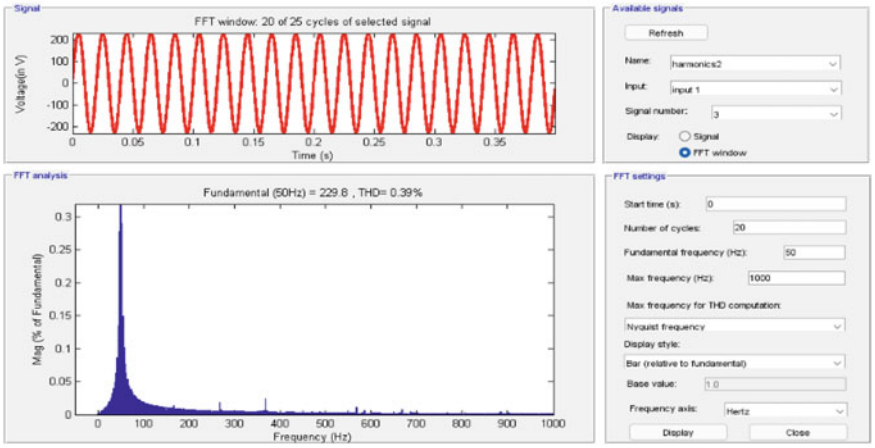

Fig. 10 THD analysis for voltage

4.3 Error Analysis

The percentage error can be calculated as the absolute difference between the expected value (E_0) and the measured value (E_m) to the expected value. i.e.

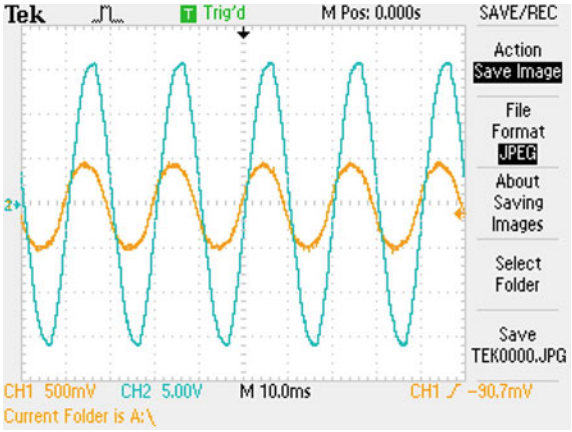

Fig. 11 Output voltage and current waveform using DSO

$$\%\text{error} = \left| \frac{E_0 - E_m}{E_m} \right| \times 100 \tag{8}$$

$$\%\text{THD Error}|(26.76 - 27.84)/26.76| \times 100 = 4.035\% \tag{9}$$

The error obtained was around 4.035%. This error comes from the result being obtained from a low-cost power quality analyzer prototype compared to the conventional FFT analysis in SIMULINK.

5 Conclusions

Power Quality Analysis was carried out in this study using an Arduino Nano and a low-cost, user-friendly power quality analyzer. Some power quality analysis approaches were implemented. The analyzer was used to do the FFT analysis. Harmonics analysis was used to determine the order of harmonics based on FFT analysis. The findings of the FFT analysis were used to determine the Total Harmonic Distortion (THD). The voltage and current from the sensor were computed using an Arduino Nano as a microcontroller, and the data was stored using storage devices. The hardware setup revealed voltage, current, power factor, and THD parameters. A Simulink model was used to validate the FFT analysis performed using the Arduino library. The THD of the current waveform was determined to be 26.76% and that of the voltage waveform was found to be 0.89% using the Simulink model. The current waveform's THD was 27.84% in the hardware setup. The DSO was used to verify the power factor. The error analysis of THD was then performed, with a result of roughly 4.035%. This inaccuracy is because the result was acquired from a low-cost prototype of a power quality analyzer rather than a high-end Power Quality Analyzer.

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Power Quality Improvement in PMBLDC Motor Drive Using Front End Converter with Reduced Power Stages

Akash D. Sarode, Shailendra Kumar, and Sanjeev Singh

1 Introduction

India is the third largest carbon emitter in all over the world since the economic growth of the country demands more energy from the utility grid. Most of the electricity is generated from the coal-based power plants and to reduce this carbon emission, this one has to generate the electricity from renewable energy sources and induction machines must be replaced by the energy efficient machines [1, 2]. The permanent magnet brushless (PMBL) DC motor drives are used in many low and medium power applications in place of conventional electric machines. The PMBLDC machines have several advantages such as high energy density, low electric losses, ruggedness, high torque to weight ratio, which leads the suitability of this machine for light electric vehicles, ceiling fans etc. The absence of brushes leads to less maintenance requirement along with less severity of the sparking. Moreover, if the BLDC motor drives are compared with the permanent magnet synchronous machine (PMSM) drives, the PMSM drives require an instantaneous position sensing of the rotor for switching of the converter. However, in case of the PMBLDC drive, it requires only six position signals [3]. The PMBLDC drives exhibit flat torque characteristics. Therefore, the speed control of the PMBLDC drive is easier as compared to other conventional machines and due to these attributes, it is suggested for light electric vehicles. The station construction of this machine is similar to the three phase asynchronous machine, except it has a permanent magnet on the rotor which makes the machine dynamic response faster as compared to other machines. In conventional DC machines, the commutation is achieved by using the mechanical commutator ring.

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However, in PMBLDC machines, the brushes are absent and hence the commutation is achieved electronically. For commutation, the PMBLDC machines are fed through a three phase voltage source inverter (VSI), hence they are known as electronically commutated machines. However, for proper commutation, there is need of information related to the position of the rotor and this task is achieved by using the three Hall Effect sensors. The position sensors are decoded to determine which winding of the PMBLDC motor has to be excited. The decoded signals are used to generate the pulse width modulation (PWM) gate pulses for the VSI fed PMBLDC machine [4–11]. This scheme draws the nonlinear current from the utility, which deteriorates the power quality of the grid. As per the IEC standard 61000-3-2, there is need of improved power quality, which suggests the improved power factor and low THD for low power applications. Hence, there is requirement of the power factor corrections converter at the front end side [5]. In the literature, it is reported that the speed of the PMBLDC drive is regulated by controlling the DC link voltage [6–10]. Therefore, the DC link voltage is regulated to achieve the unity power factor and THD within the limits. The power factor correction converters consist of the energy storage elements like the inductor and capacitor, operated in the Discontinuous mode (DCM) of conduction according to the requirements. Therefore, there is a need for two voltage sensors and the one current sensor. If a bridgeless power factor correction converter is used in the voltage follower mode it needs only one voltage sensor and current sensor [6–9]. However, in the voltage follower mode, the switch stress is more as compared to the current multiplier approach.

In the literature, the number of the bridgeless topologies have been presented for power factor correction. A bridgeless Landsman converter is used in the DCM mode of conduction for maintaining the supply power factor at unity while speed-controlling BLDC motors [6]. The CUK converter is operated in the DCM mode of conduction in the inductor current mode to control the DC link voltage by maintaining unity power factor at supply. It not only reduces the switching losses optimistically but also provides the wide range speed variations [7–10]. To maintain the supply power factor at unity, the DC link voltage is varied through the DCM inductor current mode of bridgeless Luo converter (BLLC) to allow low-frequency switching [11]. It is suggested that apply the DCM inductor current mode to the Bridgeless canonical switching cell to obtain unity power factor it utilizes only in one voltage sensor [12, 13]. The isolated zeta converter operates in the DCM mode; BLDC motor speed and power factor are adjusted by regulating the DC-link voltage and it also permits the reduction of switching losses [14, 15]. The BLDC motor speed is controlled with a Buck-Boost converter, and in order to achieve low-frequency switching with unity power factor, the buck-boost converter is functioned in the DCM mode [16]. Rectifier followed by the flyback converter is employed for power quality improvement, Here the flyback converter is operated in the DCM mode to attain the UPF turns ratio of the transformer that is selected in such a way that there is minimum stress on the switch [17]. In Ref. [18], the performance comparison of the SEPIC, CUK and Zeta converter fed BLDC drive for mitigation of power quality issues, is utilized in the voltage follower mode. The bridgeless flyback converter (BLFBC) is operated in the DCM conduction for maintaining the UPF at ac mains, and this is mainly dedicated

to reduce the stress on the switches and reduction of the voltage sensors [19]. To correct the power factor of the ac mains, combinations of zeta and boost converter are utilized, and voltage follower control is used to control the converter in the DCM conduction mode [20].

2 System Description

This paper presents the current multiplier approach to control the power quality improvement (PQI) converter and it is one of the cost effective and efficient topology to drive the PMBLDC motor for low power application with the following features:

1. It maintains the grid side power factor at unity.
2. It reduces the THD at the grid side.
3. The switching losses are reduced and hence the efficiency is enhanced.
4. Reduced one power stage as compared to conventional topologies.

In Fig. 1, a front end converter followed by a VSI feeds the PMBLDC motor of the PFC converter fed motor. Here, the actual speed of the PMBLDC motor is compared with the reference speed and error generated processed via the PI controller in order to regulate the speed of the PMBLDC motor. In order to generate the signal of the reference current, the output signal of the PI controller is multiplied by the unit vector of the input voltage. A comparison of the reference current with the line current is made, and the resulting error is used by the hysteresis controller for getting gate pulses for the single-phase AC-DC converter that is supplied by the AC-DC rectifier and gate pulses for the three phase VSI is generated by using Hall Effect signal. Actual location of the rotor is traced by the Hall effect sensor. According to this hall effect, the sensor's signal can be decoded to get the information about which stator winding is to be excited and this information is in the form of EMF signal. Gate pulses are generated by using this back EMF signal.

3 Mathematical Modeling and Control

This section briefs about the modeling of the BLDC motor, and modeling of the grid side front end converter control and electronic commutation logic for the VSI.

3.1 Modelling of the PMBLDC Drive

PMBLDC motors are modeled with some assumptions, like ignoring constant losses, ignoring the field due to the integral components of the fundamental, ignoring the

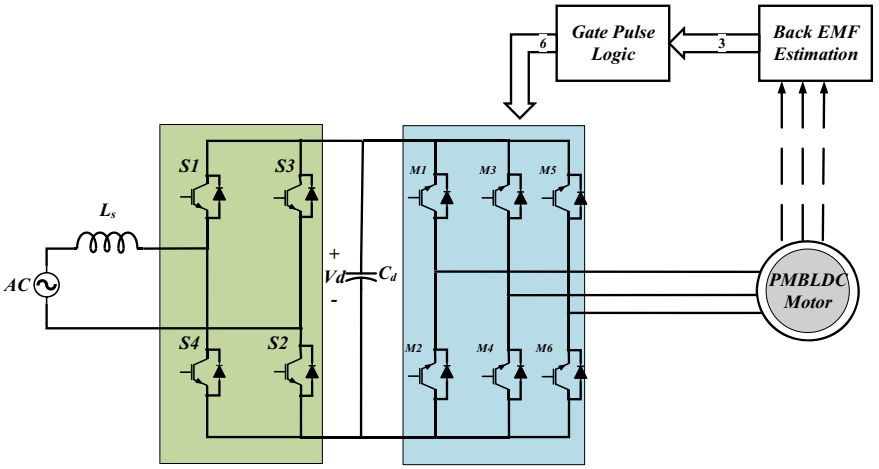

Fig. 1 System configuration

damper winding, and assuming the motor is three-phase. The modelling of stator winding is given as 4.

$$\begin{bmatrix} V_{us} \\ V_{vs} \\ V_{ws} \end{bmatrix} = \begin{bmatrix} R_{st} & 0 & 0 \\ 0 & R_{st} & 0 \\ 0 & 0 & R_{st} \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + p \begin{bmatrix} L_{uu} & L_{uv} & L_{uw} \\ L_{vu} & L_{vv} & L_{vw} \\ L_{wu} & L_{wv} & L_{ww} \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + \begin{bmatrix} e_{us} \\ e_{vs} \\ e_{ws} \end{bmatrix} \quad (1)$$

where,

R_{st} = Per phase stator winding resistance
e_{us}, e_{vs}, e_{ws} = trapezoidal induced EMFs
i_u, i_v, i_w = per phase stator currents
The per phase induced EMF equation is given as,

$$Eph = (Blv)N = N(Blr\omega_m) = N\Phi_a\omega_m = \omega_m\lambda_p \quad (2)$$

where N = number of series conductors per phase
v = speed
l = Length of the conductor
r = rotor bore radius
ω_m = angular speed
B = Flux density of the field in which conductors are placed

$$\Phi_a = Blr \quad (3)$$

$$\Phi_a = Blr = \frac{1}{\Pi}B\Pi lr = \frac{1}{\Pi}\Phi_g \quad (4)$$

Assuming a cylindrical rotor, with 3 phases, there will be no change in the rotor reluctance along with the angle hence, self-inductances of stator winding conductors are equal to L_{st}, and mutual inductances are equal to M_{st}

The PMBLDC model is modified as,

$$\begin{bmatrix} V_{us} \\ V_{vs} \\ V_{ws} \end{bmatrix} = \begin{bmatrix} R_{st} & 0 & 0 \\ 0 & R_{st} & 0 \\ 0 & 0 & R_{st} \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + p \begin{bmatrix} L_{st} & L_s & L_s \\ L_s & L_s & L_s \\ L_s & L_s & L_s \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + \begin{bmatrix} e_{us} \\ e_{vs} \\ e_{ws} \end{bmatrix} \tag{5}$$

The stator currents are balanced, i.e. $i_u + i_v + i_w = 0$

Moreover, the modeling equation is modified as,

$$\begin{bmatrix} V_{us} \\ V_{vs} \\ V_{ws} \end{bmatrix} = \begin{bmatrix} R_{st} & 0 & 0 \\ 0 & R_{st} & 0 \\ 0 & 0 & R_{st} \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + p \begin{bmatrix} (L_{st} - M_{st}) & 0 & 0 \\ 0 & (L_s - M_{st}) & 0 \\ 0 & 0 & (L_{st} - M_{st})) \end{bmatrix} \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + \begin{bmatrix} e_{us} \\ e_{vs} \\ e_{ws} \end{bmatrix} \tag{6}$$

The electromagnetic torque is given as,

$$T_{em} = [e_{us} i_u + e_{vs} i_v + e_{ws} i_w] \frac{1}{\omega_m} \tag{7}$$

The instantaneous induced emfs are given as,

$$\begin{aligned} e_{us} &= f_{us}(\theta_r)\omega_m \lambda_p \\ e_{vs} &= f_{vs}(\theta_r)\omega_m \lambda_p \\ e_{ws} &= f_{ws}(\theta_r)\omega_m \lambda_p \end{aligned} \tag{8}$$

The electromagnetic torque equation is given as,

$$T_{em} = [f_{us}(\theta_r) i_u + f_{vs}(\theta_r) i_v + f_{ws}(\theta_r) i_w] \tag{9}$$

Dynamic equation of the motor is given as below

$$J \frac{d\omega_m}{dt} + B\omega_m = (T_e - T_l) \tag{10}$$

And the electrical rotor speed and position are related as,

$$\frac{d\theta_r}{dt} = \frac{p}{2} \omega_m \tag{11}$$

State space representation is given as,

$$X' = AX + BU$$

where $X = \begin{bmatrix} i_u & i_v & i_w & \omega_m & \theta_r \end{bmatrix}$

$$A = \begin{bmatrix} -\frac{R_{st}}{L_1} & 0 & 0 & -\frac{\lambda_p}{L_1} f_{us}(\theta_r) & 0 \\ 0 & -\frac{R_{st}}{L_1} & 0 & -\frac{\lambda_p}{L_1} f_{bs}(\theta_r) & 0 \\ 0 & 0 & -\frac{R_{st}}{L_1} & -\frac{\lambda_p}{L_1} f_{ws}(\theta_r) & 0 \\ \frac{\lambda_p}{J} f_{us}(\theta_r) & \frac{\lambda_p}{J} f_{vs}(\theta_r)) & \frac{\lambda_p}{J} f_{ws}(\theta_r) & -\frac{B}{J} & 0 \\ 0 & 0 & 0 & \frac{p}{2} & 0 \end{bmatrix} \tag{12}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{1}{L_1} & 0 \\ 0 & 0 & 0 & -\frac{1}{J} \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{13}$$

$$L_1 = L_s - M_s$$

$$u = \begin{bmatrix} v_{us} & v_{vs} & v_{ws} & T_l \end{bmatrix}^T$$

Therefore, the modeling of the PMBLDC motor has been done by using these equations.

3.2 *Grid Side Front End Converter Control*

Figure 2 shows the schematic diagram of the current multiplier control for the front end converter. Here, a PI-based control is used to maintain the DC link voltage and it further generates the reference current control signal for the gating signals in the front end converter. The error between the DC link voltage $V_D{}^*(k)$ and actual DC voltage $V_D(k)$ at any instant of time is give as,

The PI voltage controller output $I_p(k-1)$ at $(k-1)$th instant is given as,

$$V_e(k) = V_D{}^*(k) - V_D(m) \tag{14}$$

$$I_p(m-1) = K_{pu} V_e(m-1) + K_{iu} \sum V_e(m-1) \tag{15}$$

The PI voltage controller at the Kth instant is given as,

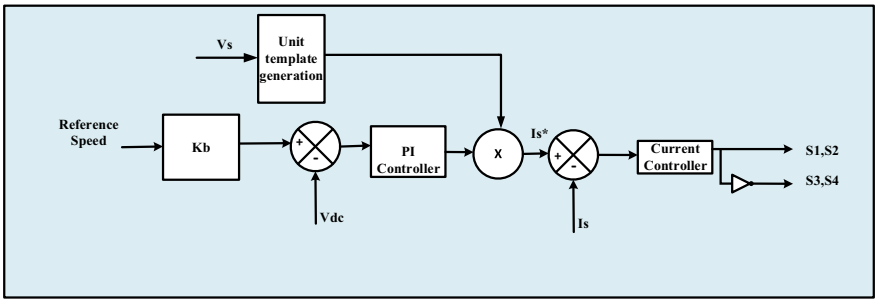

Fig. 2 Current multiplier control scheme for front end converter

$$I_p(m) = K_{pu}V_e(m-1) + K_{iu}\left\{V_e(m) + \sum V_e(m-1)\right\} \tag{16}$$

Subtract (15) from (16).

The final control signal is derived as,

$$I_p(m) = I_c(\mathrm{m}-1) + K_{pu}\{V_e(m) - V_e(m-1)\} + K_{iu}V_e(m) \tag{17}$$

Now, the reference current signals have to be generated. For this purpose, the unit template of the utility voltage is required, which is calculated as follows,

$$V_t = \sqrt{V_\alpha^2 + V_\beta^2} \tag{18}$$

$$U_v = \frac{V_s}{V_t} \tag{19}$$

where V_α and V_β are the components of the source voltage V_s.

Then, reference current signals are derived as,

$$I_s^* = U_v * I_p(m) \tag{20}$$

$$I_e = I_s - I_s^* \tag{21}$$

This error is fed to the current controller, where the current controller is basically a hysteresis controller and logic gate. By comparing the reference current signal and actual current signal the relay gives 0 and 1 according to the error generated. This relay has a switch ON and switch OFF point. The relay gives 1 when the error signal exceeds the switching point and 0 otherwise. These pulses are provided to the controlled bridge converter.

Table 1 Switching of the VSI for electronic commutation

H_U	H_V	H_W	$M1$	$M2$	$M3$	$M4$	$M5$	$M6$
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	1	1
0	1	0	0	0	1	1	0	0
0	1	1	0	0	0	1	1	0
1	0	0	1	1	0	0	0	0
1	0	1	1	0	0	0	0	1
1	1	0	0	1	1	0	0	0
1	1	1	0	0	0	0	0	0

3.3 PMBLDC Motor Side Converter Control

For electronic commutation, here, VSI is used, gate pulses for the VSI are generated according to the signal of the Hall Effect sensor's signal. With respect to the location of the rotor is detected by Hall Effect sensor excite the stator winding correctly. The transition of switches of the VSI is done as per Table 1.

4 Results and Discussion

This section is brief about the simulated results and discussion of the PMBLDC drive under the static, dynamic and starting condition of the drive.

4.1 Analysis of the PMBLDC Drive Under Steady State Conditions

Figure 3 shows utility voltage (V_s), input current, DC link voltage, speed, torque, stator current and back EMF characteristics of the PMBLDC drive under the steady state conditions. It is observed that the grid current and grid voltage are exactly in-phase i.e. it maintains the UPF at the supply side. The DC link voltage settles at its rated value (486 V) and hence the motor runs at a rated speed (3000 RPM).

4.2 Starting Response of PMBLDC Motor Drive

Figure 4 shows that the starting performance of the PMBLDC drive is observed as the response of the controller is very fast, and the speed of the machine reaches its

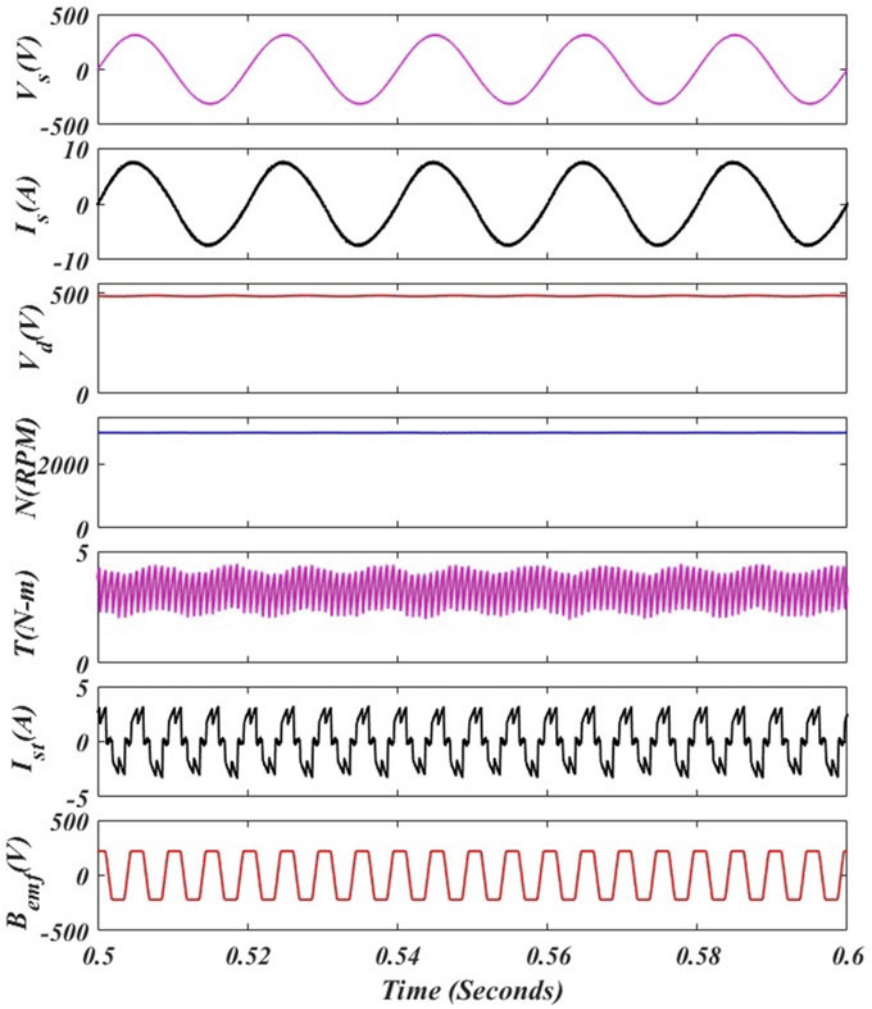

Fig. 3 Steady state performance of PFC front end converter fed PMBLDC drive

rated value within 0.08 s. Moreover, the smooth starting of the PMBL drive is also achieved by using this approach.

4.3 Dynamic Performance of PMBLDC Motor Drive

Figure 5 shows that the response of the drive under dynamic conditions. Here, response of the controller is simulated under step change in speed. The speed of the PMBLDC drive is regulated by changing appropriate DC link voltage of the VSI,

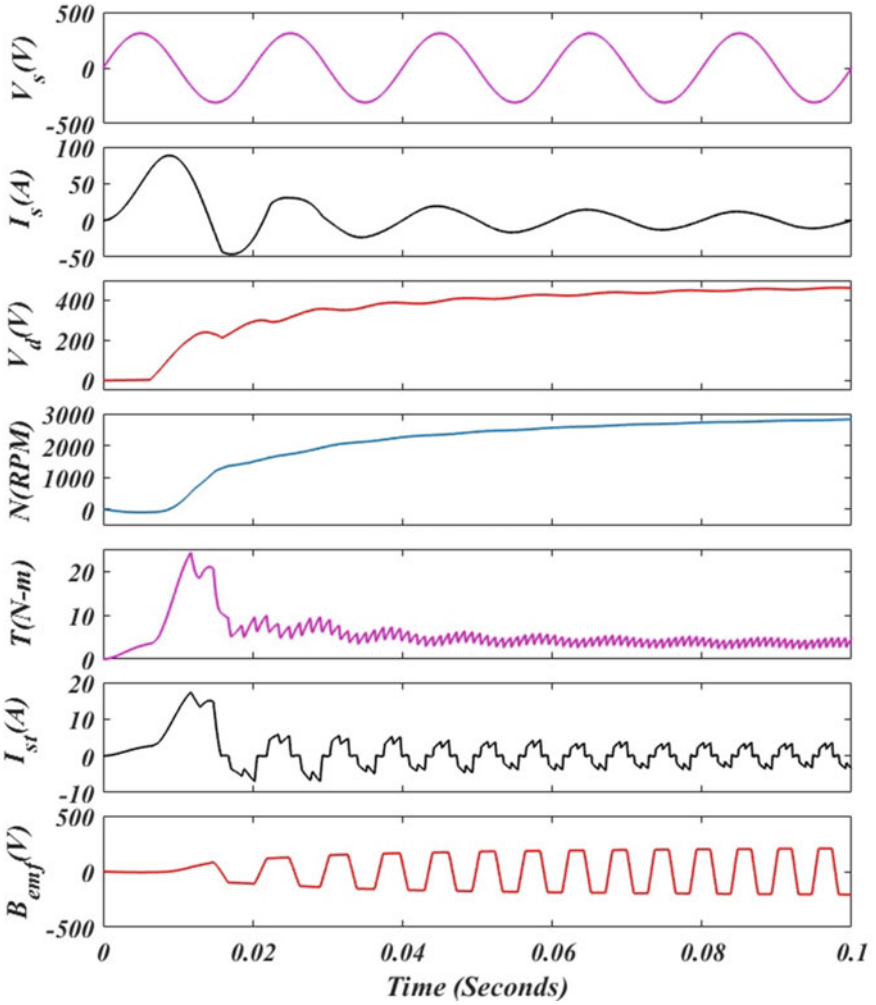

Fig. 4 Starting performance of PFC front end converter fed PMBLDC drive

where it leads to low switching losses. Here, it is observed that the actual speed follows the reference speed, and within few milliseconds the motor regains its reference speed. It shows that this control approach maintains the stability of the drive. Figure 5 shows the THD profile of the source current, where the waveform is purely sine wave and as per IEEE standard 519 THD is less than 5% (2.35%), as shown in Fig. 6.

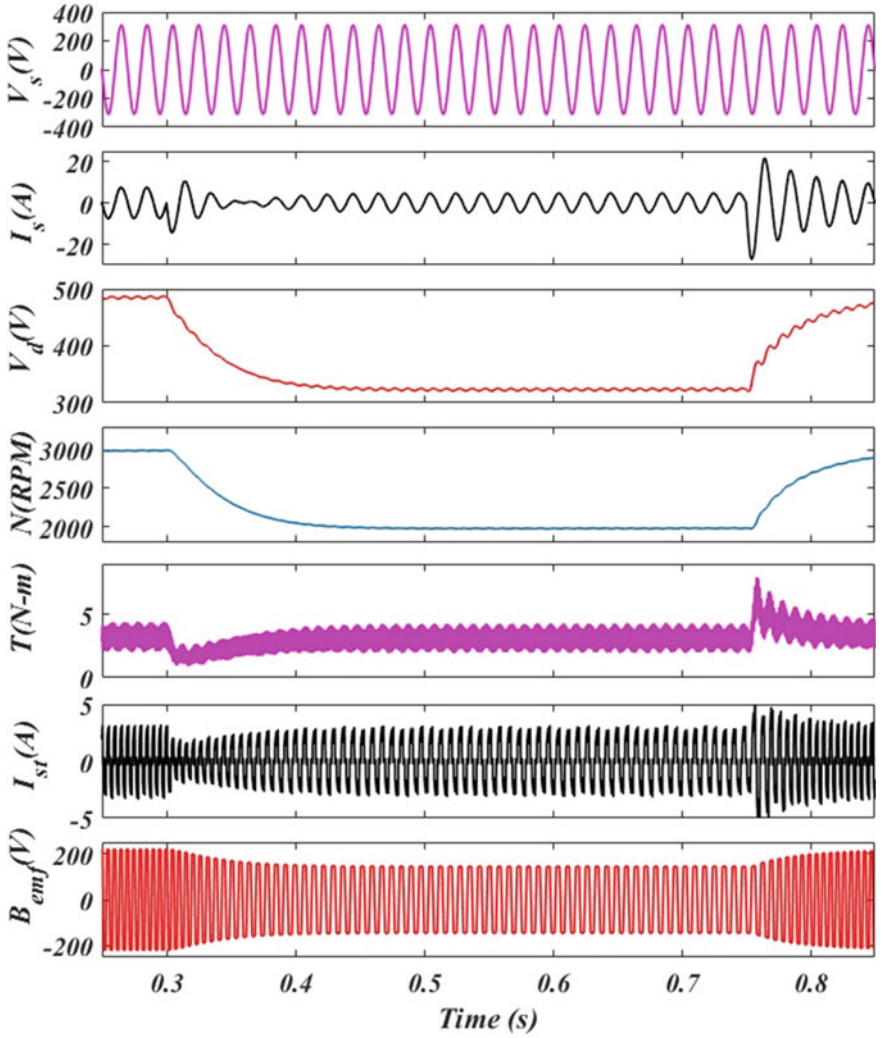

Fig. 5 Dynamic performance of PFC front end converter fed PMBLDC drive

5 Conclusion

The response of the system has been carried out in the MATLAB/SIMULINK-based platform and satisfactory performance has been achieved, which shows that it is economical, and improves the power quality of the PMBLDC motor drive. By proper controlling the DC link voltage for speed regulation, the switching losses in the

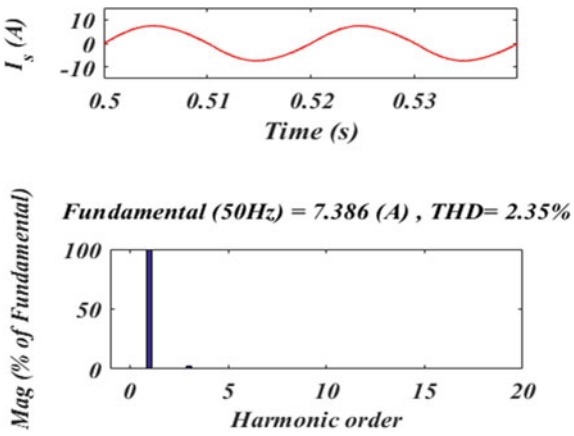

Fig. 6 FFT Analysis of supply current

system, have been reduced. This control strategy has given harmonics distortion of about 2.35% and has improved the power factor near to unity thereby improving the voltage regulation and efficiency. This proposed scheme has given satisfactory results in various conditions.

Appendix

Specification of PMBLDC motor

Sr. No.	Specification	Values
1	Poles (P)	4 poles
2	Power rating (P_{rated})	942 W
3	DC link voltage (V_d)	485
4	Torque (T_{rated})	3 Nm
5	Speed (ω_{rated})	3000 rpm
6	Back emf constant (K_t)	162 V/krpm
7	Phase resistance (R_{st})	2.8750 Ω
8	Phase inductance (L_{st})	8.5 mH
9	Moment of inertia	0.8e-3 J(kg m^2)

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Power Quality Analysis of Grid Connected Solar Powered EV Charging Station: A Review

Kunal Parashar, Khushboo Verma, and Suresh Kumar Gawre

1 Introduction

Electric vehicles are very energy efficient since they consume less fuel and emit less pollution than fossil fuels. They also offer 60% greater mileage than gasoline vehicles [1–4]. The enhancement of EVs may optimize energy structure, reduce energy consumption, and reduce emissions. EVs are on the rise, so there is a requirement to increase the count of the charging stations. Nowadays, the EVCS are generally grid-connected [5, 6]. To encounter the real objective of Electric Vehicles (like decrease in pollution caused by air, reduction of fossil fuel reliance, and an upsurge in energy reliability), electrical energy should be obtained from renewable sources for charging the vehicles [7]. Among the numerous exhaustible energy sources, the charging stations based on solar energy are an easily available and practical solution. PV systems that are grid-interactive and EV systems are the hottest technologies at the moment [8–12]. The block diagram of the solar PV scheme connected with the grid has been illustrated in Fig. 1.

Due to the existence of nonlinear components, huge amounts of harmonics are produced when the EVs are charged [13–15]. If the harmonics are not handled appropriately, it might even cause great harm to the utility grid. Harmonic currents may cause a great deal of damage to power networks. Excessive harmonics can cause line losses, aggravate the problem of electric equipment heating, cause the malfunction of control equipment, and catastrophic impairment in the performance of your power system.

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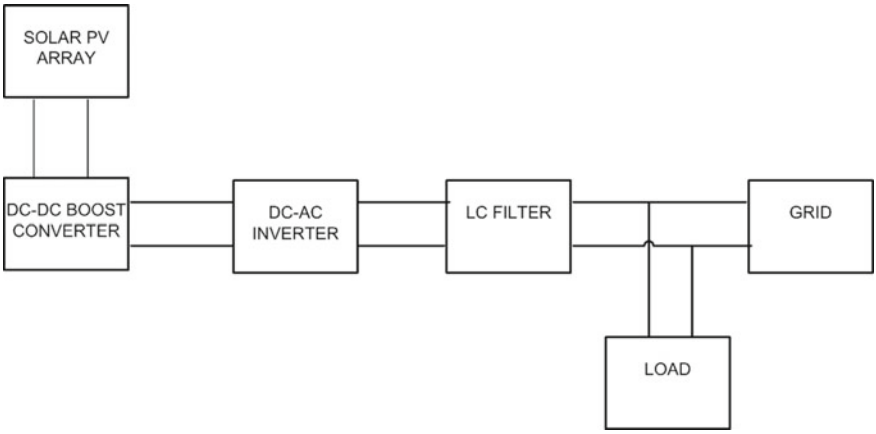

Fig. 1 Block diagram of PV scheme connected with grid

2 Grid-Connected PV System

Solar cells or photovoltaic cells convert the light energy (i.e. photons) of the sun directly to electricity by converting it into voltage. PV cells were named after the action of converting light energy (photons) into electricity via the PV effect. The main components of the whole PV scheme are depicted below.

2.1 PV Arrays

PV cells are photovoltaics units that generate electricity by converting sunlight into electric power. In general, one PV cell typically produces between one and two watts of power. PV cells are interconnected into strings of a bigger unit known as a module or panel to enhance the output power [16]. The arrays of PV panels have to be connected to construct a system, and then several such arrays are attached to the power grid to develop a grid tied-PV system. Due to this flexibility in modularity, solar PV arrangements can be extended to cater nearly any electric power requirement, large or small.

2.2 DC-DC Boost Converter

The voltage of PV panels varies throughout the day because of different temperatures and the radiation. Boost type DC to DC converters are required to sustain a uniform DC link voltage [17]. In order to control the functioning of DC to DC step up

converter (boost), maximum power point tracking is employed. This method directs the converter to haul out the maximum amount of power from the PV unit.

2.3 DC-AC Inverter

An inverter is the heart of a PV system since it links it to the utility grid. It serves two functions primarily. In the first place, it converts the DC generated from the solar panels into AC in synchrony with the grid where the electrical appliances are powered. Secondly, it prioritizes the use of solar energy over grid power.

3 Issues of Power Quality in Grid-Integrated System

During the incorporation of a PV system along with the grid, the quality of power is the most significant factor. It is described as the utility's ability to deliver a stable and noiseless power source to its customers. Inadequate quality of power would start to damage the electrical equipment and the components of power allocation as variations in frequency would cause processes in unwanted sections [18, 19]. The incorporation of the PV system with the already occurring power system causes major issues associated with the quality of power. The various issues associated with the quality of power have been concisely stated below.

3.1 Harmonics

Distortions caused by harmonics are recognized among the primary effects in PV systems connected with the grid. A dissimilarity from non-harmonic sinusoidal waves is a harmonic fluctuation in voltage and currents. Harmonic frequency is a multiple of fundamental frequency [20–22]. Harmonics are present because of various power electronic mechanisms in the system.

3.2 Voltage Variation

Solar PV system has intermitted nature which leads to voltage variations in the grid-connected PV system. There are many factors to be considered when determining solar irradiance, including transitory clouds, PV installation location, and certain points of reflection. By virtue of these factors, PV systems are prone to unsteadiness [23].

Variations in voltage are responsible for:

- Voltage Sag and Voltage Swell*:* Voltage sags are voltage drops that occur temporarily (voltage drop between 10 and 90% compared to the standard RMS voltage). The swell in voltage occurs when the RMS voltage reaches 110% of its nominal voltage in less than a minute.
- Short and Long Interruptions*:* It is called voltage interruption when the RMS voltage falls below a little percentage in perceptible voltage or when the entire voltage is lost. Short interruptions have a duration of less than one minute and long interruptions have a duration of more than one minute. The word "interruption" is usually used to describe short-interruptions, while the latter is known as a long-interruption or long-duration interruption due to the use of the word "sustained".
- Overvoltage and Undervoltage: An overvoltage condition can last up to one minute where the voltage exceeds 180% of the rated value. In order to be considered undervoltage, at least one minute's voltage must be less than 0.9 pu of the rated voltage.

3.3 Reactive Power

The huge amount of energy from solar PV is typically utilized by PV systems that work close to the unity power factor (UPF). By using this method, a PV system will provide real power to the electrical grid that will compensate for the outpouring of reactive power in the photovoltaic (PV) system. Due to inadequate reactive power, the voltage of close by buses will be improved [24]. A deficient VAR may lead to undesirable results due to system power outflow throughout the course of action. Deficient transmission may cause the power to be reduced [25, 26].

3.4 Frequency Variation

Variations (fluctuations) of the power system frequency (usually 50 Hz or 60 Hz) are called frequency variation. Frequent frequency variations above the tolerance level (±5%) are problematic for PV systems and may lead to system failure [27]. Depending on climatic conditions, weather, and topography, PV system's frequency can differ greatly, resulting in severe difficulties (Table 1).

4 Literature Survey

Paper [1] examines the impact of photovoltaic systems connected to the grid on electrical power quality. Paper [2] explains the multimode power supply system

Table 1 IEC and IEEE standards linked with power quality

S. No.	Power quality issues	Standards
1	Harmonics	IEEE-519-1992/2014, IEEE 1346, IEC SC 77A
2	Voltage sag or swell	IEEE P1564, IEC 61000-2-8, IEC 61000-4-11
3	Voltage flicker	IEEE P1453, IEC 61000-2-2, IEC 61000-4-15
4	Interruptions in voltage	IEEE 1159-95

utilizing the PV array, battery, grid and DG (Diesel Generator) set-based charger station (CS) to enable uninterrupted supply and charging to household loads. As the major energy resource for the charging station, photovoltaic arrays (PV) and wind energy conversion systems (WECS) are used in paper [3]. Solar PV arrays, battery energy storage (BES), and a DG set are used in paper [4] to provide continuous charging for island-based, grid-integrated, and Diesel Generator set-coupled electric cars. The impact of numerous equal single-phase devices linked at the same location in a network, such as some of the small-sized inverters in a solar farm, is explained in paper [5].

In paper [6], a new methodology is described, which comprises of seven steps. An integration of a PV based charging station design and charge controller driven by a battery charging strategy with a grid to vehicle strategy driven by a unidirectional PWM approach in a Smart Grid is suggested in paper [7]. Paper [8] presents a charging station (CS) integrated with a solar PV array, the grid, a BES, and a DG to allow nonstop charging of EVs. Nevertheless, these sources of energy are used in such a manner that the CS's operating costs are minimized. The challenges of fast-charging of EVs on highways are discussed in Paper [9], which is based on the power network needs. The sequence in which EVs arrive at CSs, the power rating of the chargers which are installed, the number of charging slots per station, the distance between CSs, and the state of charge (SoC) of the EVs involved in the charging process are all factors considered in the study. In Paper [10], a user-defined model (UDM) for analysis of power flow based on electric car loads in the Power System Analysis Toolbox (PSAT) is described, which was created utilizing the User Define Models (UDMs). Figure 2 depicts a grid-integrated photovoltaic EV charging station.

The state-of-the-art approach, fast charging specifications, power quality concerns and IEC and IEEE PQ standards are all comprehensively discussed in the paper [11]. Reference [12] offers an exact approach for simulating plug-in electric vehicles and charging stations in a steady-state shared power-flow analysis. The aim of paper [13] is to draw attention to the potential for harmonic disturbances as a result of installation charging stations for EVs in Medium Voltage/Low Voltage distribution zones. Reference [14] illustrates a switched shunt capacitor (SSC) in SGs in connection with nonlinear loads and an ideal load tap changer (LTC) and photovoltaic EV charging at consumers' homes and CSs. In [15], we learn about the functions of transportation systems and about the Bergamo "San Vigilio" cable car, which now has a new drive. A new method of bidirectional regulation of power flow for battery storage systems (BSS) combined with DG is presented in [28] to offset the negative impacts

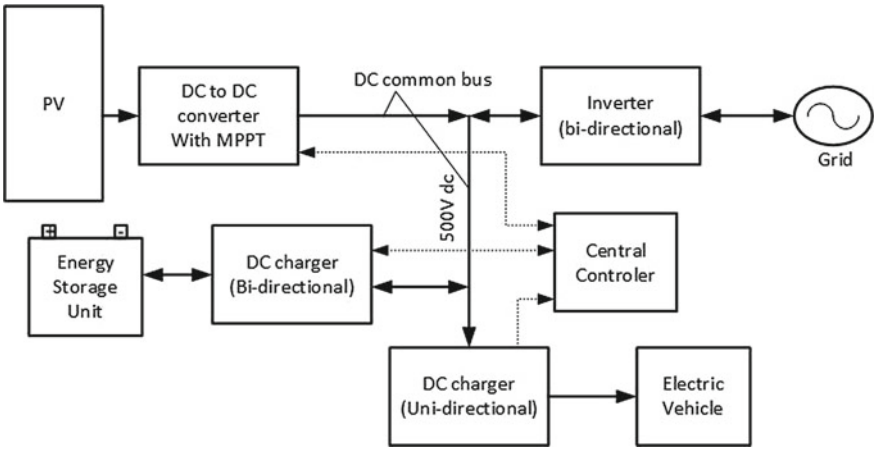

Fig. 2 Grid-integrated PVEV charging station

on power quality. The charging station based on the combination of solar power and grid is presented in [29]. The system works in an incorporated way to optimize the energy which is being used from the grid. A charging station for electric vehicles which uses the solar power and a battery is designed for the current situation in paper [30]. Figure 3 shows the schematic diagram for EV the Charging Station model with controllers.

Reference [16] discusses the main influence that solar power would have on autos and locomotives. Reference [17] presents the development of a solar-powered CS for EVs, which avoids the extra pressure on the grid due to charging EVs directly and thereby benefits the ecosystem. Paper [18] shows a computer prototype of an EV charging station and analyses the harmonics produced during the charging process. The goal of paper [19] is to create a CS that is linked with our houses and the grid, allowing all of our EV charging, grid, and supply needs to be met in a single system.

Fig. 3 Schematic diagram of EV charging station model with controllers

A photovoltaic array, energy storage battery, and the grid are used to operate and implement a charging station for electric vehicles (EVCS) in paper [20]. Reference [21] proposes the implementation and control of a CS for EVs based on a PV array and a wind energy conversion technology. Reference [22] presents a smart compactable integration of EVs with the distribution system that enhances power quality. A second-order universal integrator based on adaptive frequency, which is capable of rejecting the dc offset, is used to control a CS using PV arrays for charging EVs and improving the output quality for the grid. EVs can be charged with AC and DC supply using a three-phase CS that consists of a solar PV array and a BES integrated CS. A three-phase grid interfaced CS for an EV is presented in paper [25]. To adjust for reactive power, it communicates with the grid.

The major goal of paper [26] is to create an EV charging station based on a single phase voltage that may be put at home to meet the EV demand. The goal of [27] is to alleviate the grid load by designing a basic hybrid power system setup for fast charging EVs using MATLAB Simulink. Reference [31] shows a three-phase solar photovoltaic array and storage battery-based EVCS that use a convex combination affine projection sign algorithm (APSA) to improve the grid's output power quality. Reference [32] proposes a charging station based on a dual active bridge (DAB) converter for charging several electric vehicles.

In [33], the author designed a charging system that is single-phase which uses a PV array and a wind energy conversion system mounted on a house's roof and can work in both grid-linked and standalone modes. Reference [34] provides a power quality up-gradation for a solar PV array-powered EV charging station. Paper [35] demonstrates a grid-interlinked and solar photovoltaic charger capable of providing electricity to electric vehicles (EVs), residential loads, and the electricity grid. The experimental validation of a newly proposed real-time control approach for an EV's control system is presented in [36]. This approach operates on a sub-second time scale and aids the CS in responding to changing conditions brought on by variable energy resources like photovoltaic plants.

The goal of [37] is to assess the grid consequences of three potential bus charging techniques—each station-based, end-station-based, and overnight-based—on a typical metropolitan European distribution grid. Modeling the charging behavior of an electric bus line and linking it to a big grid simulation was done with a one-second time precision. Reference [38] presents EV charging stations that can provide grid regulation services like frequency management and control in voltage, balancing of load and peak shaving. The paper [39] proposes a microgrid connected with the grid that includes a logistical allotment system that enables electric vehicles (EVs) to leave a depot, transport goods to various consumers, and then return to the depot. On this foundation, the research seeks to investigate how to optimize EV transmit algorithms in order to smooth out renewable energy and load changes while maintaining logistical quality. In [40], an electric vehicle (EV) charging station for grid-connected photovoltaic energy is shown, which provides EVs and non-linear home loads with uninterrupted power supply.

A hierarchical microgrid operational architecture, according to [41], consists of energy management systems for EV charging lots and smart home energy management systems. Reference [42] seeks to maintain frequency quality by using electricity usage as a technique of improving the system's inertial responsiveness. The study looks at three forms of utilization: charging electric vehicles, heating by using direct electricity, and refrigerator utilization, all of which having diverse features in provisions of how they respond to weather variations in the electrical power grid. Reference [43] created a charging station integrated with the micro-grid for electric vehicles (EVs) in rural areas and hilly locations using a hydro generator and a PV array with unfavorable conditions of the grid.

Paper [44] promotes the application of electric vehicles (EVs) as a power backup solution for software firms, as well as a way to enable Dynamic Voltage Restoration (DVR) to prevent distribution system breakdowns. Reference [45] investigates the influence of random access via LTE-Advanced on grid communication using a large number of linked EVs as a starting point. Our second solution is to use LTE-random Advanced's access channels to avoid congested channels for huge communications between EV-2s and EVSEs. According to [46], a commercial charging station based on PV with ten electric car chargers will perform ideally. Because the EVCS is connected with the key distribution system, electricity can be purchased and sold from it to the grid.

The architecture of a PV-powered EVCS with a smart energy management system is described in [47]. The strategy of energy management maximizes the utilization of solar and grid power at the charging stations by using weather data and load demand information. Reference [48] shows an instant power supply (IPS) system that combines a solar photovoltaic module with a load distribution prioritizing system. Reference [49] proposes a novel approach for examining EV charging stations based on solar PV and management of frequency of load. A cost-effective and intelligent controller is used in [50] to connect PV systems based on solar energy with instant power supply (IPS) modules to provide grid access electricity and maintain uninterrupted electrical power flow. Reference [51] shows a e-bike charging station powered by solar energy that can charge e-bikes in a variety of modes, including AC, DC, and contactless charging. The summary table of the literature review has been presented in Table 2.

5 Research Gap

Although few solar charging station is established in India, however, at cloudy, foggy and night time, solar energy is absent. Thus, the charging station should be based on hybrid renewable resources. The load variation during the integration of the grid with renewable energy sources should be minimized. As we know that harmonics and other power quality issues generated during the charging process of electric vehicles cannot be eliminated entirely but it should be minimized by using various newly advanced mitigation techniques.

Table 2 Summary table for literature survey

S. No.	Techniques	Advantages	Disadvantages
1	Multimode operation of charging station [2]	Power management, voltage and frequency regulation, harmonics current compensation, reactive power compensation	Smooth transition between the islanded mode and grid connected mode
2	7-Step methodology [6]	Reduction in losses, voltage sag and overvoltage in transformers	Low penetration of photovoltaic generation and station chargers
3	Smart solar charge station [7]	Increase the smart grid system and storage alternating renewable energy from solar	Per unit electricity generation cost is higher than the conventional energy sources
4	Bidirectional power flow control for DG-coupled battery energy storage system [28]	Improves fluctuation in voltage and power quality	Grid injected power variation from PV plant is not removed
5	Renewable energy-based smart charging station [19]	Voltage THD is less than 5%, active power filtering	Unable to achieve exact unity power factor
6	Renewable energy-based grid interactive charging station [21]	Grid current THD is less than 5%, voltage synchronizing strategy	Current drawn by home loads are non-sinusoidal
7	Single phase EV charging station for homes [26]	Reactive power support, vehicle to grid, harmonics mitigation, vehicle to home	Load variation affects the power injected into the grid
8	PV-based grid interfaced three phase charging station [34]	Control of charging or discharging of EV battery, harmonics current compensation	Variations in PV insolation, voltage unbalances in the grid
9	Optimal control of charging of PV-based EV charging station [46]	Reduces the operational charging cost, reduction in power loss	Harmonics generated during charging are nor mitigated
10	Grid tied solar power controller [50]	Continuous power supply, supply surplus energy to the grid	Losses during the conversion of power is very high

6 Conclusion

A major concern has always been power quality, as disruptions have caused significant damage to the power grid. This paper defines power quality and the numerous power quality issues that can arise when PV systems are connected to the grid. Overheating, inefficiency, and device service life degradation have all been observed as a result of power quality issues, as well as process interruptions, insulation breakdowns and data loss are witnessed. Despite the fact that the causes cannot be eliminated

entirely, power quality issues can be reduced by taking the right steps. There is a need to improve the quality of power supply and to decrease the persisting outcome of the supply.

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Improved Non-isolated DC-DC Boost Converter with High Gain Capability for Renewable Energy Microgrids

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1 Introduction

Due to the emergence of the industrial revolution and rapid population growth, the ease of energy consumption was increased to a greater extent. So there is a need to increase the production of energy by using renewable energy sources such as solar panels, fuel cells etc. But the magnitude of output voltage that is obtained from these solar panels is considerably less, which is not required to produce sufficient energy from microgrids. Here comes the importance of high gain DC-DC boost converters. These high gain converters will boost the magnitude of voltage to desired levels to produce a sufficient amount of energy.

1.1 Problem Statement

The conventional boost converter configuration as shown in Fig. 1 is able to scale up the voltage level 2 times more than that of the input voltage. It comprises a MOSFET, diode, inductor and capacitor. The MOSFET will act like a switch that requires controlled gating pulses for its operation.

The working of the conventional boost converter is as follows,

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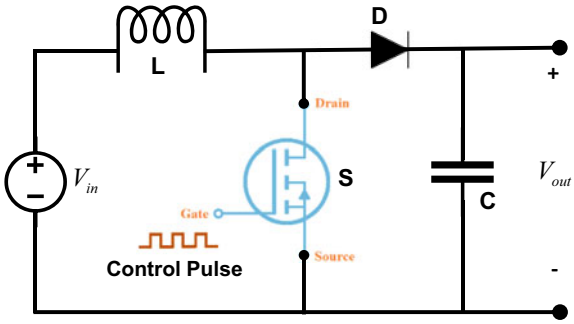

Fig. 1 Basic DC-DC boost converter circuit

– When the switch is on, the inductor gets charged up with the help of supply voltage. Here the voltage across the inductor (V_L) and supply voltage (V_{in}) will be the same as they are in parallel.
– When the switch is off, the current flow path will flow through the inductor, diode and capacitor. So according to basic network rules, the voltage measured across the inductor is shown by Eq. 1.

$$V_C = V_{out} = V_{in} + V_L \tag{1}$$

As the voltage across the inductor (V_L) and supplied voltage (V_{in}) are equal, Eq. 1 can also be represented as shown in Eq. 2.

$$V_{out} = V_{in} + V_{in} = 2V_{in} \tag{2}$$

So as per the input–output relation, the conventional boost converter can scale up 2 times that of the input voltage. The gain of the traditional boost converter is only 2, which is not suitable for renewable energy applications.

1.2 Literature Survey

Several kinds of high gain boost converter topologies already existed in literature [1]. But, there are a few drawbacks associated with them like a higher number of components, high switching frequency and voltage gain for the existed topologies in the literature.

The topology that is demonstrated in [2] has less no of components, but it has a high switching frequency of 40 kHz. It requires a high amount of cost for the topologies having a higher switching frequency. A topology that was shown in [3] has the disadvantage of having a greater number of components and a high switching frequency used in its configuration. Besides, it has a greater advantage of producing

a higher voltage magnitude of around 20 times that of input voltage. A topology which is described in [4] has a greater benefit because of having a higher gain of 25, But it also shows its disadvantages of having a high switching frequency of 118 kHz and more components used. The topology which is demonstrated in [5] has the advantage of having a gain of 20 in producing voltage levels. Despite having a higher gain, this topology requires more no of components and a higher switching frequency of 46 kHz for its operation. There exists one topology as depicted in [6] that is not suitable for renewable energy applications, as it takes a greater no of components of about 22 and a higher switching frequency of 100 kHz.

A topology which was shown in [7] will have a weak point of having less gain value of only 2 and a higher switching frequency of 100, Besides, it shows its advantage in having less no of components. The topology which is shown in [8] has the advantage of having less no of components used for its construction and less switching frequency of about 10 kHz. Besides, it can only produce output voltage levels of 2 times more than the input voltage. The topology which is described in [9] can produce an output voltage magnitude which is 30 times more than the input voltage. Although it is having a minimal number of components needed to build switching frequency. A topology which is shown in [10] was chosen as the worst topology because of having a number of components required of almost 33, But it requires less amount switching frequency of 10 kHz. The topology which was demonstrated in [11] has a higher amount of switching frequency of about 200 kHz, which is not advisable for any application. This topology is having a considerable gain value of 10. The topology shown in [12] has the disadvantage of having more number of components and a considerable voltage gain value of 10. The topology shown in [13] has the disadvantage of having less gain of about 9 and more no of components required for its construction.

1.3 Paper Contribution and Organization

The topologies which are having less number of component count have more switching frequency. Subsequently, the topologies which are having more gain value require more no of components to build. So there is a tradeoff between the number of components, gain values and switching frequency. The objective of the proposed work is to develop one unique boost converter topology, which produces a high gain compared with conventional topologies. Further, the proposed topology is best suitable for renewable energy applications. Additionally, the proposed topology was compared with some considerable conventional topologies in terms of total no of components, voltage gain and performance indices.

2 Description of the Proposed Topology

The proposed topology had designed and simulated in Simulink as shown in Fig. 2. The proposed topology consists of five energy storing elements, i.e., two inductors and three capacitors, it also consists of one MOSFET and one resistor used for switching and load purposes respectively. The specifications of the circuit are, the input voltage $V_{in} = 10$ V; switching frequency $f_s = 10$ kHz; the values of passive elements are tabulated below in Table 1.

By simulating the circuit, it is observed that the output voltage $V_{out} = 181.8$ V, from that it is determined that the gain of the circuit is 18.19 which means the output is approximately 18 times that of the input value.

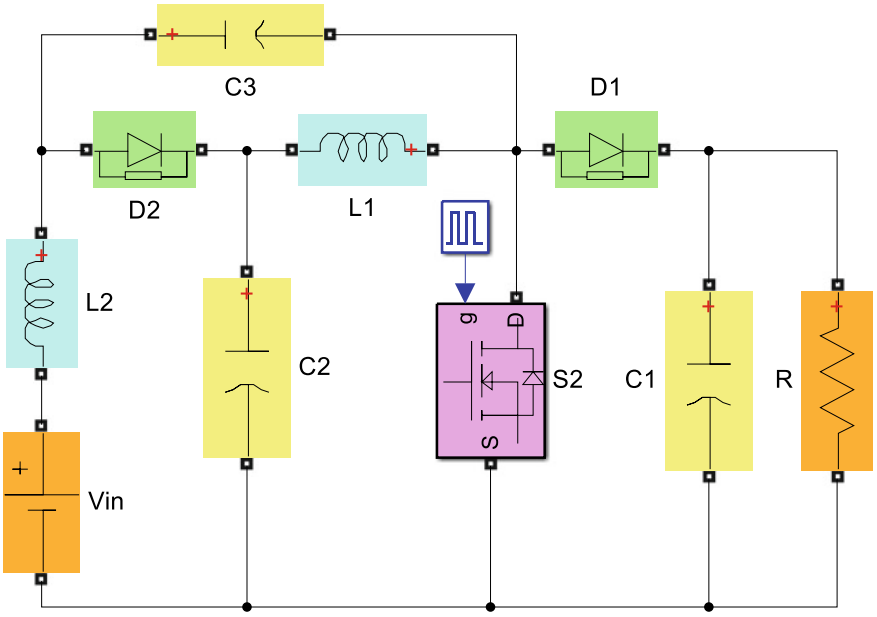

Fig. 2 Proposed DC-DC boost converter circuit

Table 1 Component specifications

Specification	Conventional topologies		Proposed topology
	Topology-1 [12]	Topology-2 [13]	
Resistance (Ω)	58	1000	58
Capacitance (μF)	$C_0, C_1, C_2 = 25$	$C_1, C_2, C_3, C_4, C_5 = 25$	$C_1, C_2, C_3 = 25$
Inductance (mH)	$L_1 = 0.5, L_2 = 0.1$	$L_1 = 1.2$	$L_1 = 0.2$, L2 $= 0.2$

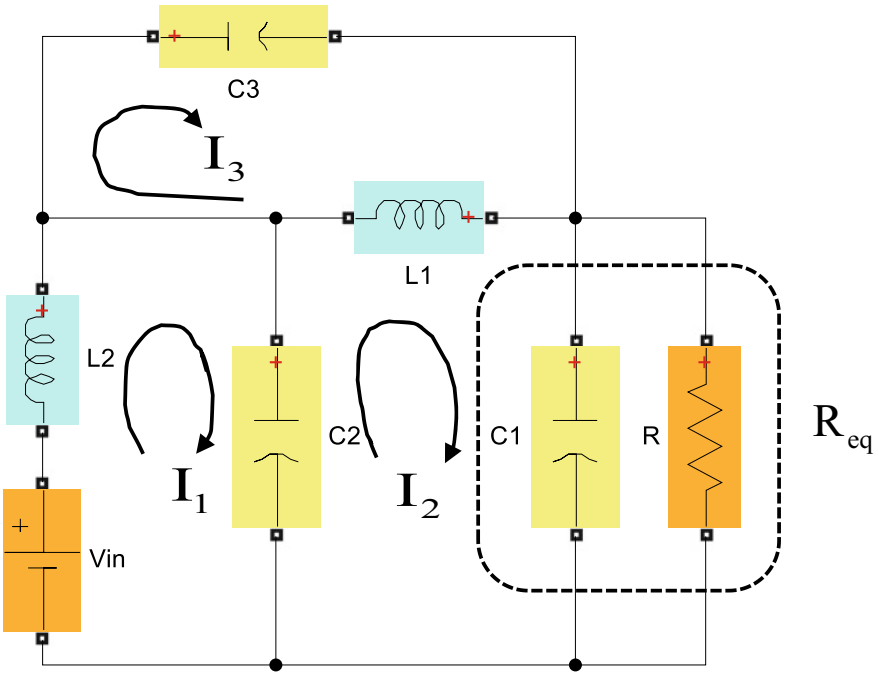

Fig. 3 Simplified circuit of the proposed topology when the switch is in the ON state

The output equation of the proposed topology has been derived by linearizing the circuit. When the switch is turned on, the equivalent circuit is shown in Fig. 3. Applying Kirchhoff's voltage law for the 3 loops, we get,

The KVL equation for loop 1 is given by Eq. 3.

$$V_{in} = I_1 L_2 s + \frac{1}{C_2 s}(I_1 - I_2) \tag{3}$$

The KVL equation for loop 2 is given by Eq. 4.

$$\frac{1}{C_2 s}(I_2 - I_1) + L_1 s(I_2 - I_3) + I_2 R_{eq} = 0 \tag{4}$$

The KVL equation for loop 3 is given by Eq. 5.

$$\frac{1}{C_3 s} I_3 + L_1 s(I_3 - I_2) = 0 \tag{5}$$

By rearranging Eqs. (3)–(5) with respect to current I_1, I_2, I_3 the following equations are obtained as shown in Eqs. 6–8.

$$V_{in} = \left(L_2 s + \frac{1}{C_2 s}\right) I_1 - \left(\frac{1}{C_2 s}\right) I_2 \tag{6}$$

$$-\left(\frac{1}{C_2 s}\right) I_1 + \left(\frac{1}{C_2 s} + L_1 s + R_{eq}\right) I_2 - (L_1 s) I_3 = 0 \tag{7}$$

$$-(L_1 s) I_2 + \left(\frac{1}{C_3 s} + L_1 s\right) I_3 = 0 \tag{8}$$

The matrix representation of Eqs. (6)–(8) is shown in Eq. 9.

$$V_{in} = \begin{bmatrix} \left(L_2 s + \frac{1}{C_2 s}\right) & -\frac{1}{C_2 s} & 0 \\ -\frac{1}{C_2 s} & \frac{1}{C_2 s} + L_1 s + R_{eq} & -L_1 s \\ 0 & -L_1 s & \frac{1}{C_3 s} + L_1 s \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{9}$$

The resultant product $I_2 \times R_{eq}$ will give the output equation of the proposed topology. Here I_2 can be found by using the crammers rule as mentioned in Eq. 10.

$$I_2 = \frac{\Delta_2}{\Delta} \tag{10}$$

Here Δ represents the determinant of the matrix. As per the crammers rule, the value Δ_2 can be found as Eq. 11. Similarly, Δ can be found as Eq. 12.

$$\left.\begin{aligned} \Delta_2 &= \begin{vmatrix} \left(L_2 s + \frac{1}{C_2 s}\right) & V_{in} & 0 \\ -\frac{1}{C_2 s} & 0 & -L_1 s \\ 0 & 0 & \frac{1}{C_3 s} + L_1 s \end{vmatrix} \\ \Rightarrow \Delta_2 &= V_{in}\left[-\frac{1}{C_2 C_3 s^2} \quad \frac{-L_1 s}{C_2 s}\right] = V_{in}\frac{[-1 - L_1 C_3]s}{C_2 C_3 s^2} \end{aligned}\right\} \tag{11}$$

$$\left.\begin{aligned} \Delta &= \begin{vmatrix} L_2 s + \frac{1}{C_2 s} & -\frac{1}{C_2 s} & 0 \\ -\frac{1}{C_2 s} & \frac{1}{C_2 s} + L_1 s + R_{eq} & -L_1 s \\ 0 & -L_1 s & \frac{1}{C_3 s} + L_1 s \end{vmatrix} \\ \Rightarrow \Delta &= \frac{(R_{eq} L_1 L_2 C_2 C_3)s^4 + [L_1 L_2 (C_2 + C_3)]s^3 + (L_2 C_2 + L_1 C_3) R_{eq} s^2 + (L_1 + L_2)s + R_{eq}}{C_2 C_3 s^2} \end{aligned}\right\} \tag{12}$$

So, I_2 can be found by dividing Δ_2 and Δ. The resultant I_2 is as Eq. 13.

$$I_2 = \frac{V_{in}(-s[1 + L_1 C_3])}{(R_{eq} L_1 L_2 C_2 C_3)s^4 + [L_1 L_2 (C_2 + C_3)]s^3 + (L_2 C_2 + L_1 C_3) R_{eq} s^2 + (L_1 + L_2)s + R_{eq}} \tag{13}$$

Thus, the final output voltage equation of the proposed topology is given as Eq. 14.

$$V_{out} = \frac{V_{in}(-s[1 + L_1C_3])R_{eq}}{(R_{eq}L_1L_2C_2C_3)s^4 + [L_1L_2(C_2 + C_3)]s^3 + (L_2C_2 + L_1C_3)R_{eq}s^2 + (L_1 + L_2)s + R_{eq}} \tag{14}$$

Table 1 comprises values of the passive components of conventional topologies and proposed topology. Here for the comparison purpose, all the capacitor ratings are taken the same. Inductor ratings of the proposed topology are less compared to ratings of conventional topologies. All three ratings of the proposed topology don't exceed the ratings of conventional topologies. The design equations for the calculation of inductance and capacitance are given in Eqs. 15 and 16.

$$L = \frac{D(1 - D)R}{2f} \tag{15}$$

$$C = \frac{D}{2fR} \tag{16}$$

3 Simulation Results and Discussion

From Fig. 4, it is found that the settling time is 30 ms and the output voltage is 181.9 V. In the zoom-in graph, it is observed that the change of voltage is slow because of capacitors. It is known that the capacitor doesn't allow the sudden change in voltage because that saw tooth graph had occurred in the output graph. The voltage of the saw-tooth is fluctuating between 168.7 and 181.8 V. Here maximum voltage is considered as the output of the circuit.

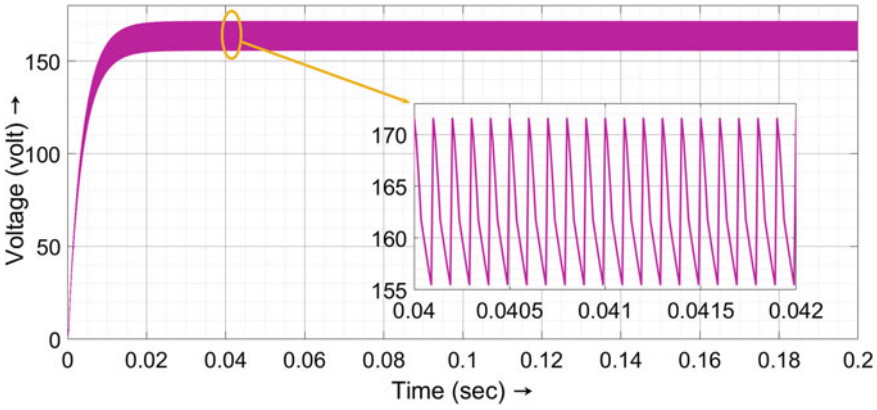

Fig. 4 Output of the proposed topology

3.1 Conventional Versus Proposed Topology Analysis

The simulation models of conventional topologies are shown in Figs. 5 and 6. From Table 2, it is found that the total number of components of the proposed topology is less than conventional topologies. Here, the majority number of switches is one and the number of diodes is very less compared to conventional topologies which leads to a decrease in the cost of the circuit.

Tables 2 and 3 comprise the input voltage (V_{in}), output voltage (V_{out}), number of components, duty cycle, switching frequency, and the gain of circuits. Here proposed topology is compared with conventional topologies. The input voltage, switching frequency, and duty cycle are considered the same for all three topologies so that comparison will be good. It is observed that gain is high for the proposed topology compared to the other two topologies, and almost the sum of gains of two conventional topologies is equal to the proposed topology's gain.

From Table 4, it is summarized that conventional topology—2 has peak-overshoot at 104 V. So, it is not preferred. There is no peak-overshoot in the output response of conventional topology-1 as shown in Fig. 7 and the proposed topology. Settling

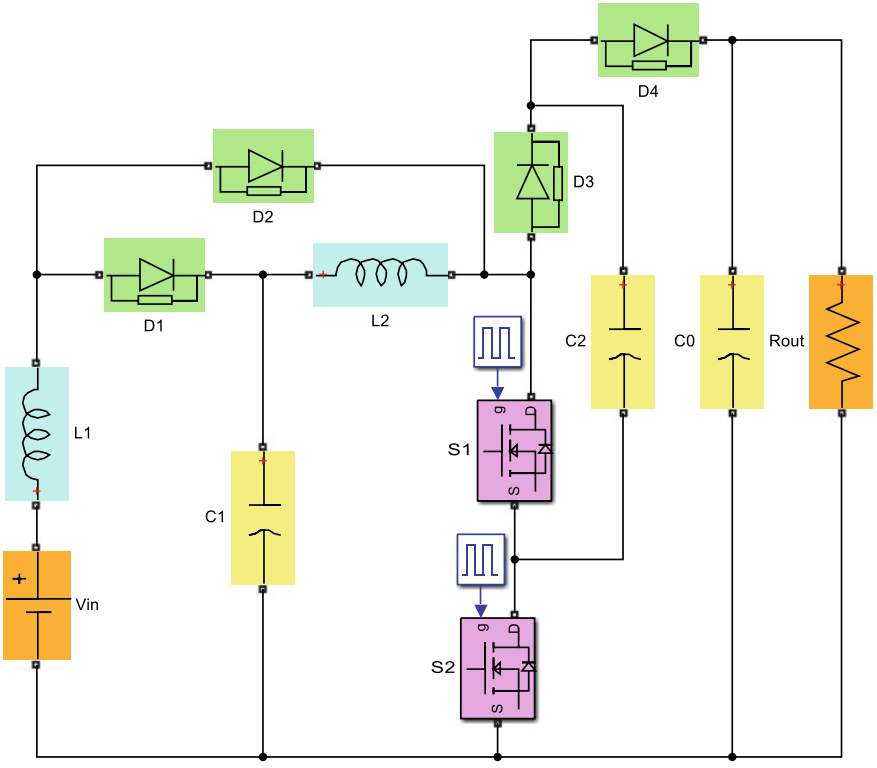

Fig. 5 Conventional topology-1 [12]

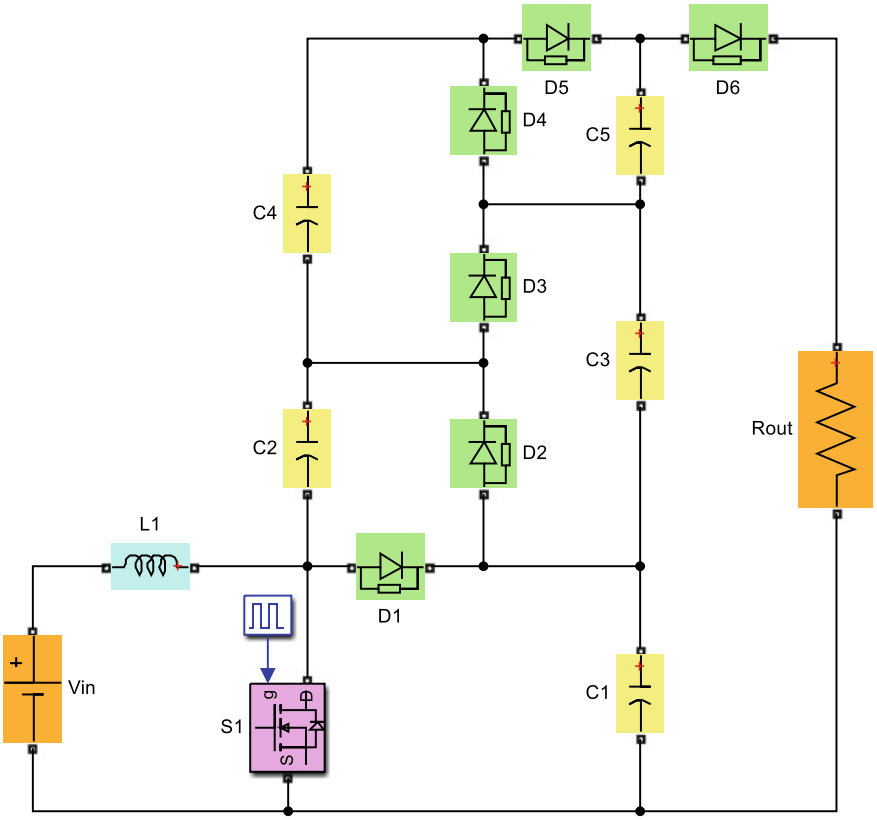

Fig. 6 Conventional topology-2 [13]

Table 2 Comparison of number of components used in conventional and proposed topologies

Topology	Number of sources	Number of switches	Number of capacitors	Number of inductors	Number of diodes	Total
Conventional topology-1 [12]	3	2	3	2	4	14
Conventional topology-2 [13]	2	1	5	1	6	15
Proposed topology	2	1	3	2	2	10

Table 3 Analysis of output responses of conventional and proposed topologies

Topology	V_{in} (V)	V_{out} (V)	Switching frequency (kHz)	Duty cycle	Gain
Conventional topology-1 [12]	10	105.3	10	0.6	10.53
Conventional topology-2 [13]	10	70.02	10	0.6	7
Proposed topology	10	181.8	10	0.6	18.18

time is less for proposed topology, so it is good compared to conventional topologies. Delay time and rise time are high for the proposed topology and low for conventional topology-2 as shown in Fig. 8. The comparative response of conventional, as well as proposed topologies, is given in Fig. 9 for better visualization.

Table 4 Analysis of the transient performance of conventional and proposed topologies

Topology	Delay time (ms)	Rise time (ms)	Peak overshoot (%)	Peak-time (ms)	Settling time (ms)
Conventional topology-1 [12]	1.46	6.89	0	0	25
Conventional topology-2 [13]	5.03	2.01	48.8	3.5	40
Proposed topology	3.02	8.61	0	0	30

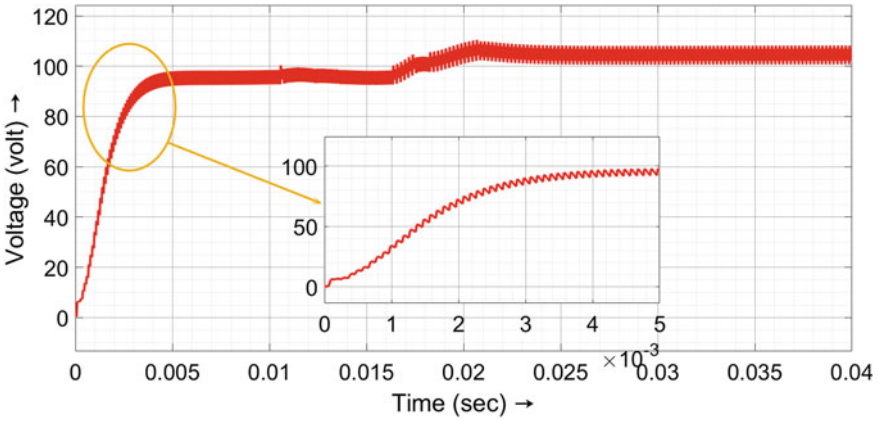

Fig. 7 Output of conventional topology-1

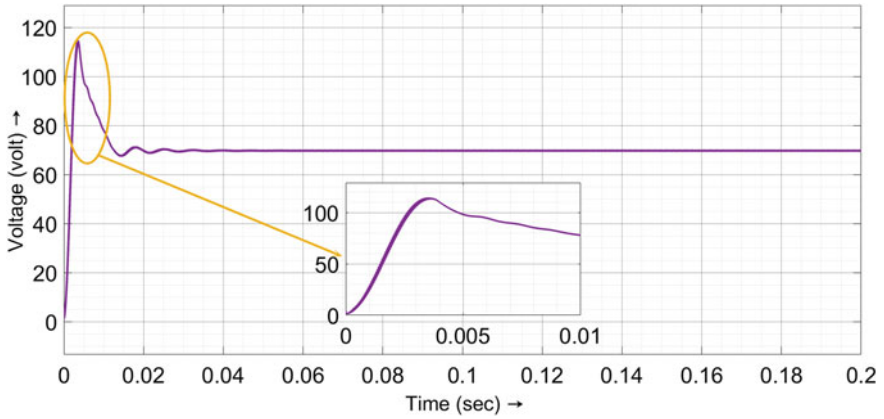

Fig. 8 Output of conventional topology-2

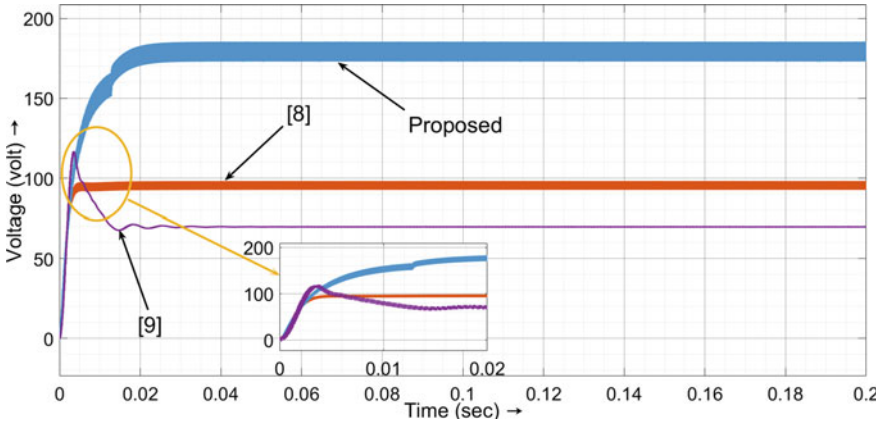

Fig. 9 Comparison of responses produced by conventional and proposed topologies

4 Conclusion

Thus, this paper considers the following factors to look at the best circuit, those are gain, number of components, switching frequency, duty cycle, and number of sources. For the desired circuit following criteria should be followed, the gain should be high, the number of components should be less, and switching frequency should be less. From the summary of Tables 2, 3 and 4, it is observed that the proposed topology satisfies the maximum criteria that are given as follows.

– High gain
– Less number of components
– Less switching frequency

– Less settling time
– No peak-overshoot
– Low cost.

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A Unified Rounding Control Scheme for T-type Packed U-Cell Switched Capacitor-Based Multilevel Inverter Topology

Aratipamula Bhanuchandar and Bhagwan K. Murthy

1 Introduction

Conventional Multilevel Inverters (MLIs) like Neutral Point Clamped (NPC)/DCMLI were proposed by Akira Nabae in 1981, Cascaded H-Bridge (CHB) and Flying Capacitor (FC) topologies have been extensively used in industrial and grid connected applications in the past years [1, 2]. Nevertheless these traditional topologies faces some practical challenges like control complexity, DC link capacitor balancing issues, efficiency and cost whenever going to the higher number of levels [3, 4]. Therefore, to overcome the above problems, some Reduced Device Count (RDC) MLIs have been proposed with reduced cost [5]. To generate or produce nine level output, symmetric H bridge inverters take 8 switches and 4 DC sources [6]. Similarly 2 DC sources and 12 switches are required in [7]. With asymmetric configuration, H-Bridge topology requires unequal number of DC sources [8, 9]. To synthesize nine level wave form 4 equal DC sources and 10 switches have been used in [10]. In the similar way, for producing nine level output Packed U-Cell (PUC) topology 8 switches and 3 DC sources in the ratio of 1:1:2 have been used [11–14]. So far, in most of RDC MLI topologies more number of switches and higher number of isolated DC sources are required. To reduce the higher number of DC source count, a single stage switched capacitor (S^3CM) module has been proposed in [15]. In [15], the nine level output is obtained with the use of 2 capacitors, 12 switches and 1 DC source and is also capable to produce both subtractive and additive combination of DC input levels. In [16], a 9-level T-type PUC topology has been presented. But with that given switching table and hybrid modulation scheme, as equal or unequal number of DC source, it always produces

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nine level output only. And also because of hybrid modulation, fewer switches operate at a fundamental frequency and remaining switches are operated with a high frequency mode. Here, High Switching Frequency (HSF) means, switching losses are drastically increased and thereby efficiency will decrease.

Conventionally there are different modulation schemes available both in low switching frequency (LSF) (like SHE, NLC) and HSF methods [17]. Generally, the Selective Harmonic Elimination (SHE) method can extensively concentrate on to eliminate lower order harmonics but this technique fails to apply in closed loop system operations like grid connected applications. And Nearest Level Control (NLC) scheme also operates at a fundamental switching frequency, thereby switching losses are greatly reduced as compared with conventional high switching frequency methods [18]. In [19], there is a unified switching logic that was developed for any seven inverter topologies and for this a separate lookup table was required. A universal control scheme was developed for any MLI topology but it should require more number of carriers and a new look up table [20]. Because of carriers, the control complexity increases and burden on the processor also increases. Based on [18, 21], in this paper a new Unified Rounding Control Scheme (URCS) or Unified Low Switching Frequency Control Scheme (ULSFCS) is proposed for the T-type PUC Switched Capacitor (T-PUCSC) based MLI. And in this MLI topology, the proposed control technique is applied to both symmetric (9-level with 1:1) and asymmetric source (11-level with 3:2) configurations with the same switching Table 1. The proposed control scheme is the modified version of the NLC method. And it is well suitable for any level inverter topology so that's why it can be names as "unified" with the use of rounding function.

Rest of the work is summarized as follows: Description of the topology and proposed control scheme for the T-PUCSC-based inverter is discussed in Sect. 2, a comparative analysis/comparison of topologies is discussed in Sect. 3, the final simulation results are presented in Sect. 4 and conclusion part is presented in Sect. 5.

2 Description of Topology and Proposed Control Scheme

A. *Topology and Operating Principle of T-PUCSC based Inverter*

The T-PUCSC inverter topology consists of 8 switches, 2 DC sources (Vdc1 and Vdc2) and 2 capacitors as depicted in Fig. 1. In this, the top portion looks like the T-shape neutral point clamped leg and the bottom portion is the half bridge circuit-PUC model and the joint connection with two switches named as "T-PUCSC". Here, the capacitors are automatically self-balanced with the proposed control scheme as depicted in Fig. 2. From Table 1 with symmetric sources (1:1 that is Vdc1 = Vdc2 = Vdc), the output can be synthesized as 9-level in terms of 0, ± 0.5Vdc, ± 1Vdc, ± 1.5Vdc and ± 2Vdc and similarly with asymmetric sources (3:2 that is Vdc1 = 3Vdc and Vdc2 = 2Vdc), the output can be synthesized as 11-level in terms of 0, ±1 Vdc, ± 2Vdc, ± 3Vdc, ± 4Vdc and ± 5Vdc on the basis of the same switching

Table 1 Valid switching state for the T-PUCSC based inverter topology

Switching Table [S1 to S8]	Load Voltage - V_{AB}	
	For 1:1 Source Configuration (Vdc1=Vdc2=Vdc)	For 3:2 Source Configuration (Vdc1=3Vdc; Vdc2=2Vdc)
[1 0 1 0 0 0 1 1]	$0.5V_{dc}$	$1V_{dc}$
[1 0 1 0 0 1 0 0]	$1V_{dc}$	$2V_{dc}$
[0 1 1 0 1 0 0 0]	$1V_{dc}$	$3V_{dc}$
[0 1 1 0 0 0 1 1]	$1.5V_{dc}$	$4V_{dc}$
[0 1 1 0 1 0 0 0]	$2V_{dc}$	$5V_{dc}$
[1 0 1 0 1 0 0 0]	0	0
[0 1 0 1 0 1 0 0]	0	0
[0 1 0 1 0 0 1 1]	$-0.5V_{dc}$	$-1V_{dc}$
[0 1 0 1 1 0 0 0]	$-1V_{dc}$	$-2V_{dc}$
[1 0 0 1 0 1 0 0]	$-1V_{dc}$	$-3V_{dc}$
[1 0 0 1 0 0 1 1]	$-1.5V_{dc}$	$-4V_{dc}$
[1 0 0 1 1 0 0 0]	$-2V_{dc}$	$-5V_{dc}$

action. With the 1:1 source configuration case, the peak value of the output voltage is 2Vdc and similarly in the 3:2 source configuration case, the peak value of the output voltage is 5Vdc. In 1:1 and 3:2 source configurations, redundant switching states are presented and highlighted in Table 1. In the positive half cycle from zero to a positive peak value, the switch S3 is always in the conducting state. Similarly in the negative half cycle from zero to a negative peak value, the switch S4 is always in the conducting state.

Based on uneven switching (charged and discharged in series and parallel configuration) in the each state it is possible to obtain a self-balancing property with the proposed control scheme. Here another important point to note is how to choose the DC source values for getting the peak value of 400 V (assume) in both 1:1 and 3:2 configurations. For example, in the 1:1 configuration case, the peak value is to be 2Vdc that is 2Vdc = 400 then Vdc = 200 V is given for generating the desired nine level output. Similarly, in the 3:2 source configuration case, 5Vdc = 400 V then Vdc = 80 V is given for generating a 11-level output. By the longest discharging period method, it is possible to get the formula for capacitor values with better voltage ripple but it cannot give exact values of the capacitors that are required and so for better solution always try to make trial and error values using simulink to check the good voltage ripple across the capacitors and finally decide the capacitor desired values.

B. *Proposed Control Scheme-URCS or ULSFCS*

Figure 2 shows the conventional NLC scheme that was reported in [18]. Figure 3 shows URCS and it is the modified version of NLC technique. In this unified control

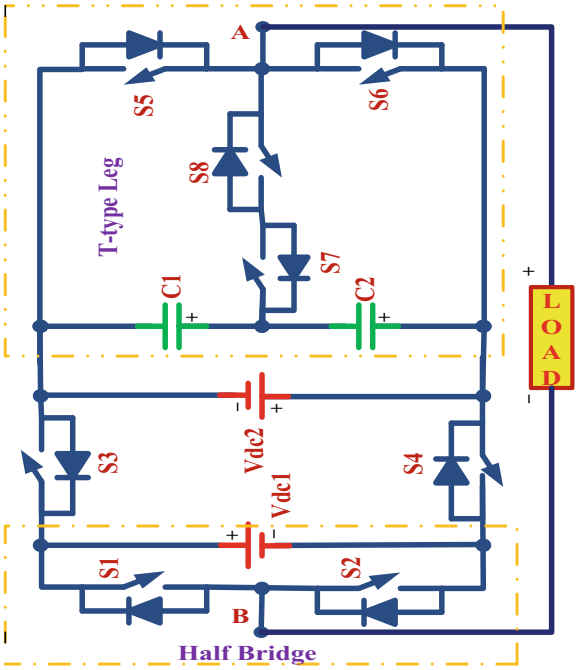


Fig. 1 T-type PUCSC based MLI topology

scheme case, all switches are operated at the fundamental frequency only thereby greatly reducing switching losses as compared with the conventional carrier based control schemes. The proposed control scheme takes less computational time as compared with the NLC technique and there by the design control complexity further reduces.

The proposed control scheme consists totally of four blocks for generating switching pulses to the inverter. Here, in this scheme there is no need of high frequency carriers. The first block is called as the reference signal or sine wave or modulating signal and in this the amplitude value can be selected generally according to the level count, that is, amplitude = (level-1)/2. But here in this proposed topology case, if the targeted peak value is 400 V [Assume: 2Vdc (peak value)-1:1 and 5Vdc (peak value)-3:2] then in both symmetric and asymmetric source configuration cases for generating the required level number we have to choose the amplitude of the modulating signal as value four and five respectively for the same switching Table 1. The second block that is Accumulated Signal Generation/Aggregated Signal Generation (ASG) using rounding function can be operated and it rounds each element of the input signal to the nearest integer automatically. Then the output signal acts like a control signal. The third block: Switching Table Generation (STG) is contributed from Table 1 and it will act as the data signal. Both control and data signals when given to the fourth block leads to its truncation accordingly as each level basis. And

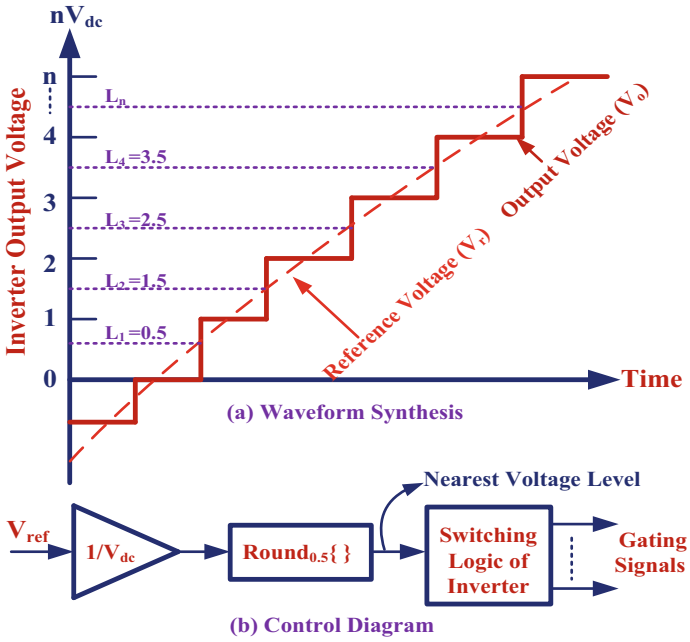
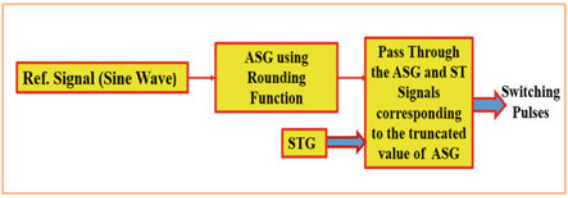


Fig. 2 Conventional NLC scheme [18]

Fig. 3 Proposed Unified Rounding Control Scheme (URCS)



it is finally generates the required switching pulses for the inverter. The main advantages of the proposed unified control scheme are it operates only with a fundamental switching frequency (50 Hz) there by switching losses are greatly reduced, will be applicable to any MLI topology even in switched capacitor based topologies also, is a simple control scheme there by control complexity greatly reduces thus reducing the burden on the processor (no carriers are required), no need to use any separate switching logic gate arrangement, no need of look up table arrangement and is well suitable for closed loop grid connected systems also. By using the PLECS software, it is possible to calculate switching losses directly and suppose the devices are made up with silicon carbide MOSFETs then switching losses are drastically decreased.

3 Comparative Analysis

In this section, the comparison in terms of the number of DC sources, number of output levels, number of IGBTs, number of capacitors, number of main diodes, number of gate drivers, voltage gain and TSV (p.u) with respect to Refs. [15, 22] are shown in Table 2. The following formulae are to be used for calculation of the Total Standing Voltage (TSV) or Total Blocking Voltage (TBV) in per unit basis and voltage gain (G).

$$\mathrm{TSV_{pu}} = \frac{\mathrm{TSV}}{\mathrm{V_{0,peak}}} \tag{1}$$

$$\mathrm{G} = \frac{\mathrm{V_{0,peak}}}{\mathrm{V_{step}}} \tag{2}$$

The blocking/standing voltage of each power switch of the proposed T-PUCSC topology can be summarized as Vdc, Vdc, 2Vdc, 2Vdc, Vdc, Vdc, 0.5Vdc and 0.5Vdc from S1 to S8 respectively then totally it becomes 9Vdc. Finally, from Table 2, it is concluded that the proposed topology gives better results as compared with the traditional topologies. In RDC MLI topologies, even if one switch reduces the requirement of the gate driver circuit, heat sink and protection circuit also reduce there by drastically decreasing the cost also as compared with the conventional control schemes available in [16, 19, 20]; the proposed control scheme has more advantages in terms of design of control complexity.

Table 2 Comparison of conventional and proposed topologies

	Proposed topology (1:1 and 3:2)	Reference [15]	Reference [22]-(1:1)	CHB-(1:3)
Number of output levels (N_{Level})	9 (1:1) and 11 (3:2)	9	9	9
Number of DC sources (N_{DC})	2	1	4	2
Number of capacitors (N_C)	2	2	–	–
Number of IGBTs (N_{IGBT})	8	12	16	8
Number of anti parallel diodes (N_D)	8	12	16	8
Number of gate drivers (N_{GD})	7	12	16	8
Voltage gain (G)	1	2	1	1
TSV	9	11	8	8

4 Simulation Results

The proposed control scheme is applied to the T-PUCSC based inverter topology and simulation was done using the MATLAB platform. Table 3 shows the simulation parameters of the proposed topology. Figure 4 shows ASG, switching pulses from S1 to S8, capacitor voltages, load voltage (V) and load current (A) waveforms for the 3:2 source configuration. From Fig. 4 it is concluded that capacitors are self-balanced at 80 V with very less ripple and finally 11-level output is obtained with THD of 7.59%. And also the proposed control method increases DC bus utilization from 400 to 403.9 V with modulation index = 1.

Similarly, Fig. 5 shows ASG, switching pulses from S1 to S8, capacitor voltages, load voltage (V) and load current (A) waveforms for the 1:1 source configuration. From Fig. 5 it is concluded that capacitors are self-balanced at 100 V with very less ripple and finally the 9-level output is obtained with THD of 9.36%. And also

Table 3 Simulation parameters

S. No.	3:2 Source configuration	1:1 Source configuration
1	$V_{o,peak}$ = 400 V (assume)	$V_{o,peak}$ = 400 V (assume)
2	Vdc = 80 V	Vdc = 200 V
3	C1 = C2 = 2200 μF	C1 = C2 = 2200 μF
4	R = 160 Ω, L = 30 mH	R = 160 Ω, L = 30 mH
5	Switching frequency = 50 Hz	Switching frequency = 50 Hz
6	Modulation index = 1.0	Modulation index = 1.0

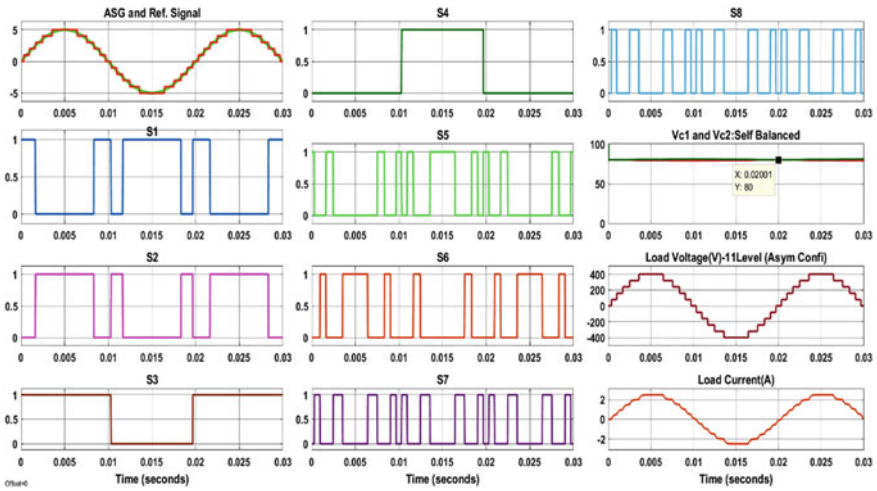


Fig. 4 Asymmetric source configuration (3:2)-ASG, switching pulses, capacitor voltages, load voltage (eleven level) and load current wave forms

the proposed control method increases DC bus utilization from 400 to 405.4 V with modulation index = 1. The output of the load current waveform is completely dependent on load values. Figures 6 and 7 show harmonic spectrums of the 11-level output voltage and the 9-level output voltage.

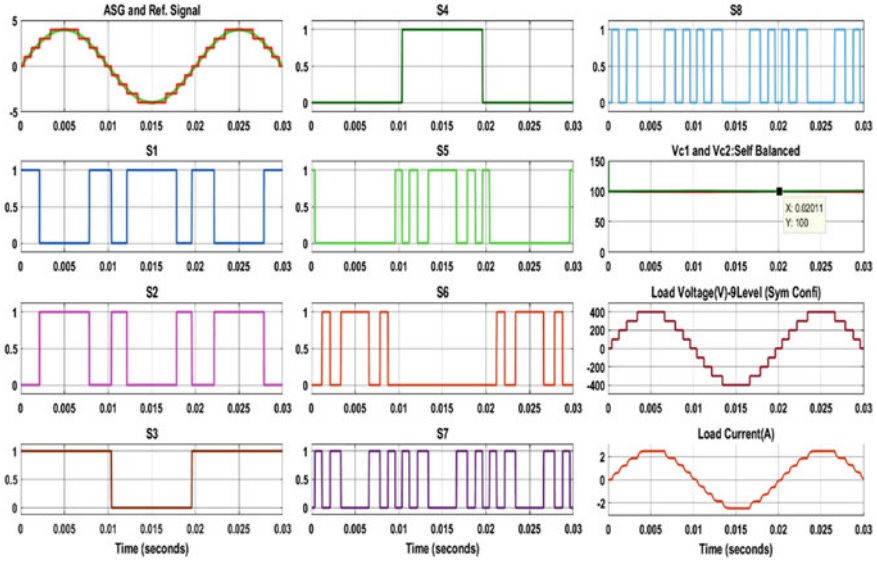


Fig. 5 Symmetric source configuration (1:1)-ASG, switching pulses, capacitor voltages, load voltage (nine level) and current wave forms

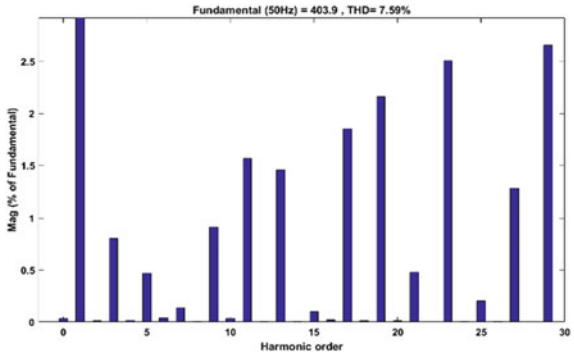


Fig. 6 Harmonic spectrum-eleven level output voltage

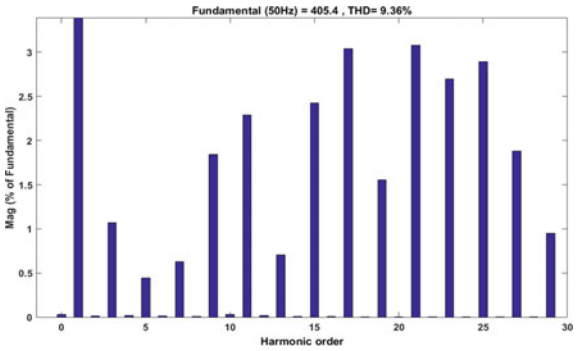


Fig. 7 Harmonic spectrum-nine level output voltage

5 Conclusion

Compared with other conventional nine/eleven level inverter topologies, the T-PUCSC-based topology has less number of IGBTs thereby is a gate drive circuit, protection circuit and the heat sink greatly reduces then overall volume of the system drastically decreases. This topology uses only two DC sources and two capacitors. For better operation, a new URCS has been proposed. The proposed control scheme takes less computational time as compared with the NLC technique and thereby the design control complexity further reduces. By using this control scheme, the self-balancing of the capacitors is possible without using any additional auxiliary circuits. The switching losses are greatly reduced because all switches are operated with fundamental frequency only and this scheme is applicable for any RDC MLI topology. It has the advantages like simplicity, does not require any separate switching logic gates and it is well suitable for grid connected applications.

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