Lecture Notes in Electrical Engineering 963

Chander Prakash
V. Sambasiva Rao
D. V. A. Raghava Murthy *Editors*

Smart Small Satellites: Design, Modelling and Development

Proceedings of the International Conference on Small Satellites, ICSS 2022

Springer

Lecture Notes in Electrical Engineering

Volume 963

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Editors
Chander Prakash
Division of Research and Development
School of Mechanical Engineering
Lovely Professional University
Phagwara, Punjab, India

D. V. A. Raghava Murthy
Centre for Space Research
Lovely Professional University
Phagwara, Punjab, India

V. Sambasiva Rao
Crucible of Research and Innovation
Centre for Research in Space Science
and Technology
PES University
Bengaluru, Karnataka, India

ISSN 1876-1100 ISSN 1876-1119 (electronic)
Lecture Notes in Electrical Engineering
ISBN 978-981-19-7197-6 ISBN 978-981-19-7198-3 (eBook)
https://doi.org/10.1007/978-981-19-7198-3

This Springer imprint is published by the registered company Springer Nature Singapore Pte Ltd.
The registered company address is: 152 Beach Road, #21-01/04 Gateway East, Singapore 189721, Singapore

Preface

Smart Small Satellites: Design, Modelling and Development presents select proceedings of International Conference on Small Satellites and Its Applications (ICSS-2022) and aims to a comprehensive and broad-spectrum picture of the state-of-the-art research, development and commercial prospective of various discoveries conducted in the real-world Smart Small Satellites, applications and their services. The thematic issue also covers the involvement of various advanced software-driven techniques that need to be employed for deploying efficient power management system, application-based optimum payload designs, telemetry and telecommand, advanced navigation and RF systems, flight and ground software, structure, mechanism and materials, spacecraft autonomy, quality, testing and reliability for designing the small satellites through advanced computational procedures for a variety of applications. Here, the authors provide graduate, postgraduate, doctorate students, faculty and scientists with an in-depth account of the evolutionary behaviour of Smart Satellites and their Engineering for educational, societal and industrial applications. The issue also covers application of advanced and functional material for development of small satellites and payloads. The book can be a valuable reference for beginners, researchers and professionals interested in design, modelling and development of smart small satellites through advanced computing technologies.

Phagwara, India — Chander Prakash
Bengaluru, India — V. Sambasiva Rao
Phagwara, India — D. V. A. Raghava Murthy

Contents

About the Editors

Prof. Chander Prakash is working as a Professor and Dean (Associate), Division of Research and Development, Lovely Professional University, Punjab, India. He is Adjunct Professor (Honorary position) at Institute for Computational Science, Ton Duc Thasng University, Vietnam. His area of research is Materials Science and Manufacturing. Dr. Prakash has authored more than 250 research articles in journals, conference proceedings, and books. In 2018, 2019, 2020, and 2021 he received the Research Excellence Award for publishing the highest number of publications at the University. He is also featured in "World Ranking of Top 2% Scientists" in the 2021 database (Published: 19 October 2021)". He has edited 23 books and three authored books for various reputed publishers like Springer, Elsevier, CRC Press, and World Scientific. He is the series editor of the book "Sustainable Manufacturing Technologies: Additive, Subtractive, and Hybrid, CRC Press Taylor and Francis. He is serving editorial board member of peer reviewer intranational journals "Cogent Engineering" and "Frontiers in Manufacturing Technology". He is serving as Guest Editor of 21 peer-reviewed SCI-indexed Journals. He is an active member of the Institute of Electrical and Electronics Engineers (IEEE), the Institution of Engineering and Technology (IET), and the Indian Science Congress Association (ISCA).

Dr. V. Sambasiva Rao is Professor in the Electrical and Communications Engineering Department in PES University and Director of the Crucible of Research and Innovation (CORI), Bangalore. An engineering graduate from College of Engineering, Kakinada, (Andhra University), he obtained his Ph.D. from BITS, Pilani, and was associated with ISRO in various capacities for 37 years, till his retirement as Deputy Director from ISRO Satellite Centre in June 2011. In ISRO, he was responsible for the development of high bit rate data transmitters for all IRS series of satellites and various RF and microwave systems in S, C, X, Ku and Ka bands for IRS and INSAT missions and was also associated with the planning of communication satellites and development of associated technologies.

Prof. D. V. A. Raghava Murthy is Adjunct Professor & Advisor to Centre for Space Research, Division of Research and Development lovely Professional University,

Punjab. Prior to join LPU, Prof Murthy was Director, Aerospace Research in Vel Tech University, Chennai, Tamil Nadu. Apart from that Prof. Murthy worked in ISRO as Systems Engineer after his M.Sc.(Tech) from NIT Warangal and worked on numerous satellite projects, including Bhaskara-II, TES, and IRS satellites. He was Project Director of Cartosat-1, IMS-1, YouthSat, SARAL and first Project Director of Chandrayaan 2. He had also been involved in small satellite projects till 2013, when he became Director of the Earth Observations System in ISRO Head Quarters and was responsible for Earth observing satellites, missions and applications till his retirement in 2016. Additionally, Prof. Murthy started a Society for Small Satellite Systems (SSSS) in 2017 and currently, holding a position of Secretary in SSSS. The society provides a common forum to ISRO and DRDO scientists, academicians, and Industrialists/ executives / start-ups to have discussions and conferences for research, innovations and growth of industry in space technology as well as applications. Under his leadership, several national and international level mega events are organized to uplift the space related activities.

Miniaturized TR Modules for Radar Imaging Payloads: A Review of Materials to Methods for Manufacturability

Vinod S. Chippalkatti and Rajashekhar C. Biradar

Abstract Radar Imaging payload of a satellite has Synthetic Aperture Radar comprising of large number of Transmit Receive modules that form the active elements. These modules essentially have the function of transmitting or receiving the horizontal and vertical polarized signals that generate multipolar beams. To produce reliable and large volumes for onboard use, the need for TR module design to be manufacturable is a critical requirement. In addition, the cost-effective payload requirements combined with weight volume constraints make these modules to be mandatorily miniaturized. The miniaturization uses advances in thermal packaging technologies with judicious combination of attachment and interconnect processes. Starting from the selection of materials with electrical, mechanical, and thermal properties and their suitability for high frequency operations, enhancing the density of electronics for high-reliability performance become the key success factors. This paper presents a detailed review of the materials for manufacturing methods of space grade TR modules.

Keywords TRModules · MMICs · Radar imaging · LTCC · Miniaturization · Ceramic substrates

1 Introduction

Radar technology has significantly evolved over the last four decades, and arrays have seen the paradigm shift from mechanical to electronic steering. These electronically steered beams offer several system advantages. Hence the phased array technology takes the prime spot for space applications. The radar imaging for earth observation using remote sensing techniques is considerably popular.

V. S. Chippalkatti (✉)
Centum Electronics Limited, REVA University, Bangalore 560106, India
e-mail: vinod@centumelectronics.com

R. C. Biradar
REVA University, Bangalore 560106, India

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_1

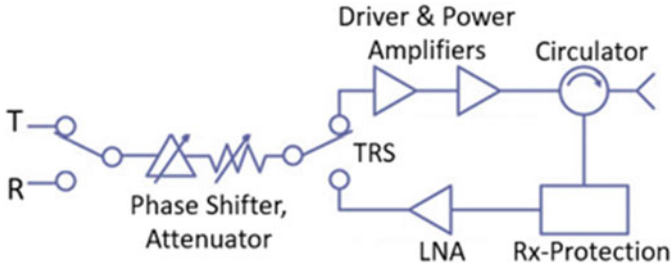

Fig. 1 Basic blocks of a TR module

Transmit Receive (TR) modules are the essential basic building blocks of an active phased array radar. These enable the last stage of amplification for transmitted signals and first stage of amplification for the received signals. They also control the phase and amplitudes of the signals to facilitate the electronic beam steering. The TR modules consisting of RF, digital, power, and mechanical sub-elements, address the structural, thermal, and functional performance of the SAR payload.

A typical TRM, in its common path consists of attenuator, phase shifter, power amplifiers in transmit path, low-noise-amplifier, switching elements, controlling, and limiting elements in the receive path, as shown in Fig. 1.

In an active phased array radar, the TR modules are expected to have higher output power, lower noise figure, desired gain in both transmit and receive paths, optimal pulse rise/fall time, and wider operating temperature. For space applications, the TR modules are generally based on hybrid microelectronics technology which combines active semiconductor devices and passive interconnections within a package. The Synthetic Aperture Radar (SAR) satellite payload hosts hundreds of TR modules controlling the beam steering in azimuth and elevation direction [1]. By controlling large number of radiating elements, each associated with a TR module, the phased array payload can achieve increased range, nano-seconds scan speed, higher accuracy and resolution, and higher system stability [2]. To realize these many space grade TR modules, the design must consider right materials for the best and highly reliable performance and equally importantly, they must be manufactured in a qualified infrastructure using the certified processes by the approved personnel. The processes must be manufacture-friendly for repeatable and reliable delivery of large-scale TR modules. The end criteria should be that the TR modules are cost effective, thermally, and mechanically performing and lightweight. Miniaturization with right packaging techniques for TR modules results in the lightweight and reliable payload for SAR satellites.

The subsequent sections of this paper cover the TR modules packaging criteria, materials selection considerations, different options available, multiple interconnection methods, the need for miniaturization, and comparison of some of the options. The manufacturability and testability aspects of large-scale TR modules for space Radar Imaging payload are also discussed.

2 Packaging Considerations for Space TR Modules

The space grade electronic modules demand more functionality in smaller size, weight, and volume. The packaging solutions for TR modules are expected to be lighter, smaller, more complex operating at higher frequencies and with increased electronic component density. This presents sufficient challenges to RF designers, packaging experts, and materials specialists. All of them need to co-exist and cooperate to realize miniaturized and performing TR modules for space. The general criteria for TR module packaging is described in Fig. 2 [3–6].

The packaging is also implemented in three levels. (1) Device or carrier level, (2) Interconnection board level, and (3) Mechanical housing level. The end objective of all three levels of packaging is to meet the considerations as mentioned above. The integrated TR modules are required to meet the electrical performance comprising power handling, bandwidth, noise figure, minimum reflection, and distortion. The level-1 packaging focuses on thermal conductivity, lower thermal expansion, and hermeticity. The level-2 packaging prioritizes on heat dissipation and mechanical strength aspects. The level-3 packaging results in lighter structure, better mechanical strength, and heat out flow [7]. Figure 3 gives an example of packaging at all 3 levels. In addition to the above, the product engineering for space TR modules necessitates addressing manufacturability and testability aspects.

During the process of packaging design of space TR modules, the following modeling and simulation studies are carried out before finalizing the configuration of the electronic components, attachments, and interconnections. A typical modeling of a wire bond on MMIC chip on a substrate, transmission line modeling of a QFN chip, and thermal analysis model are given in Fig. 4. The coupled-π model method uses inductors with magnetic coupling and capacitive elements as the equivalent circuit model for QFN, the HFSS simulation model elements can be calculated from measured data or EM simulator scattering parameters [7].

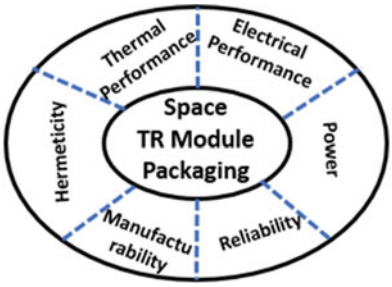

Fig. 2 Packaging considerations for a space TR module [3]

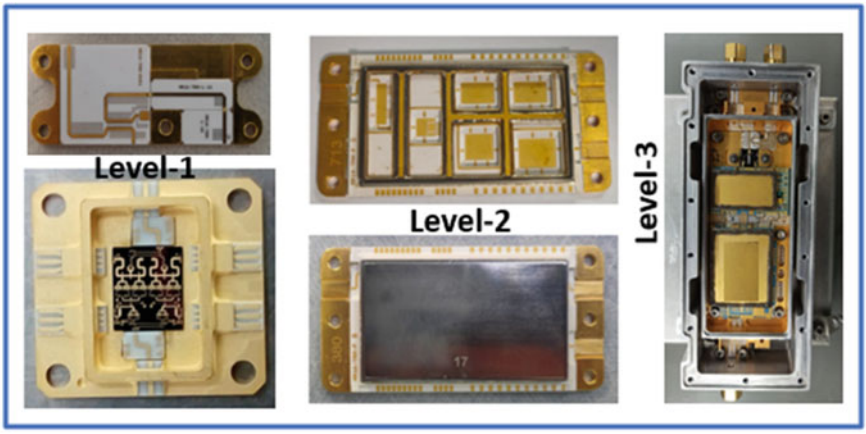

Fig. 3 Multi-level packaging of space TR module

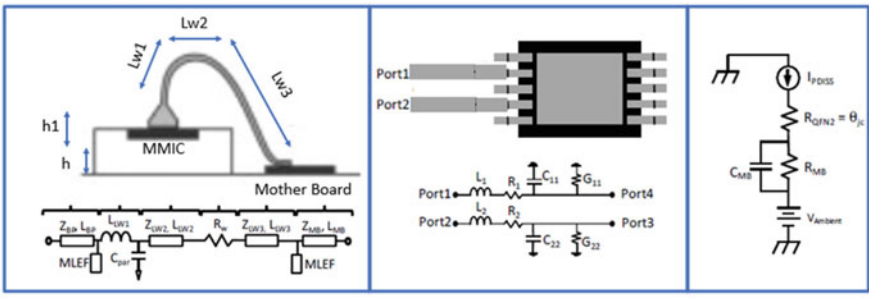

Fig. 4 Modeling for attachments and interconnects

3 Materials for Miniaturization

The choice of materials and their implementation have an immense impact on the TR module performance, size, and reliable functionality. The electrical parameters of the materials comprise dielectric constant, loss tangent, semiconductor dielectric properties, and electrical conductivity of circuit tracks [8]. The mechanical parameters consist of thermal conductivity, thermal expansion, stress, strain, sheer, and young's modulus.

Most of the TR modules are fabricated using ceramics with processes such as thick film, thin film, high temperature cofired ceramics (HTCC), and low temperature cofired ceramics (LTCC) [9–12]. The ceramics in general offer ideal characteristics for hi-reliability packaging and have preferable properties such as high young's modulus resulting in inherent stability, easy wire bond-ability, low losses, high thermal conductivity, and highly reliable microelectronics on ceramics at extreme temperatures. The physical features of the package for TR modules, as also seen in

Table 1 Key packaging materials with their important parameters

Material	Diel const	Loss tangent	Thermal cond (W/mK)	CTE (ppm/oC)
Alumina	9.2	0.003	25	5.4
LTCC (ferro)	5.9	0.0012	2–4	5–8
LTCC (DuPont)	7.9	0.0045	2–4	5–8
AlN (HTCC)	5.8	0.005	150	3.5
Mid/High Tg FR4	4.5	0.018	–	–
Polyamide	4.06	0.006	–	–
Silver (Ag)	–	–	429	19.8
Gold (Au)	–	–	318	14.2
Copper (Cu)	–	–	380	16.5
Aluminum (Al)	–	–	240	22
Tin (Sn)	–	–	67	22
GaAs	–	–	55	5.9

Fig. 3, consist of striplines, microstrips, cavities and several dc, rf and ground layers. For higher frequencies, the package material should be manufacturing friendly to reach superior electrical, mechanical, and thermal performance. Table 1 gives the important parameters of some key dielectrics and packaging materials used in space TR modules at microwave frequencies.

Some of the TR modules use combination of these ceramics. In certain cost-sensitive applications, the printed circuit boards are also used as the carriers. Materials like FR-4 have limited applications for relatively lower frequencies of only a few gigahertz. Laminates with lower dielectric loss and stable properties are preferred over FR-4. Table 2 gives the trends of materials used in space TR modules.

4 Manufacturing Processes

The space TR modules are manufactured in clean rooms of Class-1000 to Class-10000 with all key processes carried out under laminar flow tables of Class-100. A typical miniaturized, chip, and wire type of TR module manufacturing is shown in Fig. 5. The processes are generally classified into attachments, interconnections, and hermetic sealing [13].

The attachment process comprises various attachments for die, substrate, interconnection terminal, and lid. Table 3 provides various attachment processes and materials. The X-ray inspection for void-free attachment ensures reliable thermal performance.

The interconnection process comprises various types of wire bonding and in certain cases soldering of components/connectors. Generally, gold wire bonding of 1 mil dia is popular and meets most of the current requirements. In certain cases,

Table 2 Material trends in space TR modules

Sl no.	Category	Current practices	Improving trends and future
1	Components	Single chip functions. MESFETS, GaAs, HEMT	MCMs, MMICs, Multifunction Core chips, P-HEMTs, HBTs
2	Substrates	Thick and thin film on alumina substrates	HTCC and LTCC substrates, AlN. Substrates as integrated part of the package. 2D/3D packaging
3	PCBs (for lower freq.)	FR4, Hi Tg FR4, RT duroid	High performance laminates, LCPs, MCM-L
4	Mechanical housing	Kovar, aluminum alloys, molybdenum based mechanical housing. hermetically sealed co-axial feed throughs	Integrated Cavities In LTCC, Composites (Alsic), Planar Feed Throughs
5	Connectors	Coaxial connectors	Pressure contacts and RF field couplings, vertical Interconnects

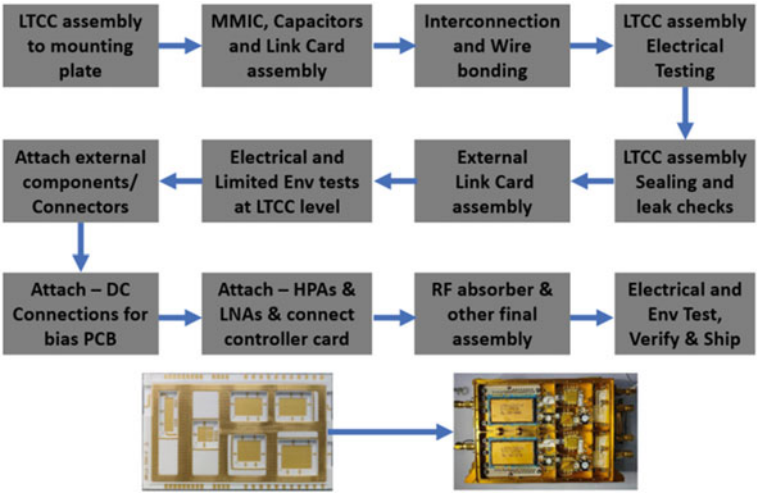

Fig. 5 Manufacturing flow of a typical space TR module

Table 3 Attachment processes and materials

Attachment process	Key characteristics	Materials
Die attach	Lower Cure temperature, higher thermal conductivity, good adhesion strength, lower CTE mismatch between materials attached, excellent shear strength	Solder pastes, Solder preforms, conductive and non-conductive epoxies or films
Substrate attach		
Interconnection Terminal attach		
Lid, Housing attach		

Fig. 6 Space TR module assembly line

multiple gold wire bonds or ribbon bonding is used. TR module production facilities use semi-automatic and automatic wire bonders. Out of the two types of wire bonding, the wedge bonding is preferred to ball bonding for RF applications since the smaller loop height minimizes bond inductance improving the performance of the TR modules.

To achieve the required hermeticity for TR modules, the RF feed throughs, dc-pins, micro-D connectors, and package lids must be sealed. Processes such as solder sealing, seam sealing, and laser welding are followed depending on the size, volume, and materials to be sealed. An important part of the space TR modules assembly line is shown in Fig. 6.

5 Manufacturability, Testability, and Reliability

In the last two decades, for civilian applications, the earth observation techniques using remote sensing have significantly increased. For realizing the large volumes of repeatable TR modules, fully or semi-automated manufacturing lines are needed. Radar imaging satellites across the globe have hundreds of TR modules onboard their payload electronics performing over the satellite mission life. Indian Radar imaging satellites have 576 TR modules in C band in each of the satellites. The Envisat of European Space Agency has 320 modules and Radarsats of Canadian Space Agency have 512 TR modules each [14, 15].

To realize, highly reliable TR modules, the process and the product design teams must work together. The cross-functional team approach with clear focus on manufacturability and testability aspects of TR modules can result in reliable and producible

volumes making the production process time and cost compliant. This also has several challenges. The radar system designers are challenged with the need for incorporating power conditioning, thermal management, digital integration, complex filtering, passive components, and EMI mitigation in a single TR module. The process designers' contribution in the form of yield improvements and the test engineers' contribution in the form of high-speed test automation system ensure speedy and reliable production of space TR modules. The quality assurance team also has a significant role to play, through various reliability assessments like derating, structural, thermal, reliability estimation, worst case circuit analysis (WCCA), failure mode effects and criticality Analysis (FMECA), and fault tree analysis (FTA) [16]. The quality control steps incorporate the compliance to the traceability, workmanship standards, test and evaluation procedures, and delivery of data packs. These further ensure the system performance in extreme stress conditions.

6 Conclusions

The space TR modules are reliability and performance drivers for SAR satellites. The materials, packaging, and assembly techniques play a crucial role in determining the performance. The innovations in the use of the latest materials and processes result in more efficient and reliable subsystems for the future. The miniaturization and manufacturing technology developments are hugely driving the large-scale realization of high density and more efficient TR modules.

Acknowledgements The authors acknowledge the support from REVA University for carrying out the research, contributions of the process and production staff of the Space division at Centum Electronics Bangalore, and the scientists from Indian Space Research Organization for their significant contributions towards large number of Space TR modules realization at Centum.

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B-Dot Controller Simulation for a 3U CubeSat: BMSCE Upagraha

V. Sankar

Abstract The B-Dot Controller is an attitude control algorithm used in the detumbling of satellites. It uses the Earth's magnetic field to detumble the satellite in orbit. The law used to perform detumbling in a B-Dot Controller is called B-Dot Law. This paper consists of a detailed explanation of the B-Dot Controller and the B-Dot Law, as well as, the results of a simulation of the B-Dot Controller run on MATLAB. The simulation is run for J2 orbit propagation for a 3U CubeSat in both, the presence and absence of a gyroscope on board the CubeSat. Appropriate noise and bias have been considered while coding the simulation, and a basic filtering process has been included in the code. The result of the simulation shows graphically (on an Angular Velocity vs. Time graph) the time taken by the CubeSat to detumble at different values of Initial Angular Velocity and Magnetorquer Capacity while also considering different lengths of the major cycle in the OBC while reading input from the sensors.

Keywords B-Dot controller · Attitude control · B-Dot law

1 Introduction

The satellite, when released into orbit, is continuously rotating about all its axes. The process of slowing the rotation of the satellite in orbit is called Detumbling. Detumbling using a B-Dot Controller requires power to be consumed at the magnetorquers, which are responsible for the detumbling to occur using the magnetic field of the Earth. The magnetic field of the Earth interacts with the magnetic field produced by the magnetorquer to create a retarding force, thereby slowing down the rotation of the satellite. Recent papers have explored the stability of the B-Dot Control Law and found that the law is stable as long as the satellite is within a significant range of the Earth's magnetic field in order to interact with it or if the satellite's magnetic

V. Sankar (✉)
Department of Mechanical Engineering, BMS College of Engineering, Basavanagudi, Bengaluru, India
e-mail: sankarsambhuy2k@gmail.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_2

field is co-axial to that of the Earth [1]. Another paper has assessed the stability and failure analysis of the B-Dot Law for a dusk-dawn sun-synchronous orbit for LEO satellites and determined that the B-Dot Law is highly stable and robust [2]. Another paper done on the B-Dot Control detumbling has revisited the topic of B-Dot Law and developed a novel convergence-based algorithm to prove the viability and stability of the B-Dot Controller [3]. A paper published on the use of B-Dot Law in RADARSATs has proved the B-Dot Law to be robust, simple and requiring minimal sensory data [4].

Since the power that can be provided by the satellite is finite, the most efficient method must be realized in order to use less power while detumbling the satellite while taking a time constraint for the detumbling into consideration (around 2 orbits). Most CubeSats are also incapable of accommodating a gyroscope. This calls for testing of the B-Dot Controller in the absence of a gyroscope. This paper analyses the time and magnetorquer current density taken to implement the B-Dot Controller on a 3U CubeSat for different sampling rates, at different magnetorquer capacities, for a constant initial tumbling rate of the satellite in the absence and presence of a gyroscope on board.

2 B-Dot Law

The B-Dot Law is the law that guides the working of a B-Dot Controller in the detumbling of a satellite. This controller works on the basis of magnetic torque application through the interaction of magnetic fields using magnetorquers. Magnetorquers are used to retard excess momentum induced during the launch of the CubeSat into orbit. This is done in order to prevent saturation of reaction wheels [5].

Magnetic control torques provide several merits such as smooth application, limitless mission life and omitting of catastrophic failure modes in near-earth missions. Its uses include initial acquisition, precession control, nutation damping and momentum control [5].

The torque generated by the magnetorquers is given by

$$L = m \times B \tag{1}$$

where m is the magnetic dipole moment produced by the magnetorquers in A.m^2 and B is the local geomagnetic field strength with respect to the satellite Body frame in T [6]. The magnetic dipole moment produced is the cross product of the angular velocity of the CubeSat and geomagnetic field vector multiplied by the gain of the satellite. It is given by

$$\dot{B} = \omega \times B, \text{ in the presence of gyroscope data} \tag{2}$$

$$\dot{B} = \frac{dB}{dt}, \text{ in the absence of gyroscope data} \tag{3}$$

$$m = k \times (\dot{B}/|\dot{B}|) \tag{4}$$

$$L = m \times B \tag{5}$$

where k is the gain. The gain is an arbitrary value decided by the power need and ideal detumbling time of the satellite, and ω is the angular rate of the satellite expressed in rad/s [5].

The initial torque of the satellite is parallel to the Angular Velocity, ω. The Magnetic Moment (m), being a cross product of ω and B, is perpendicular to both ω and B. The angular momentum produced due to the magnetorquers is therefore anti-parallel to the initial torque and angular velocity of the CubeSat. This causes the angular rate of the satellite to decrease, producing a gradual detumbling effect [5] (Fig. 1).

The residual torque of the satellite is calculated as follows:

$$T = L - (\omega \times (I.\omega)) \tag{6}$$

$$T = I.\alpha \tag{7}$$

where I depicts the moment of inertia of the 3U CubeSat in kg.m^2 and α is the angular acceleration in rad/s^2 [5].

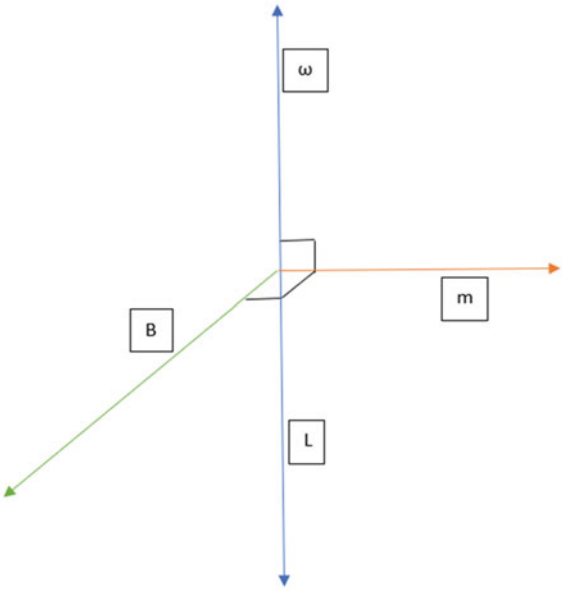

Fig. 1 The direction of B-Dot control vectors

3 Modelling

See Fig. 2.

3.1 Euler Angles

The Euler angles are a set of three angles that depicts the attitude of a rigid body in a 3D space with reference to a fixed coordinate frame [5]. These three angles were initially considered to easily input the orientation of the CubeSat. They were later converted to Quaternions for the purpose of computation of spacecraft dynamics. The values of the Euler angles were assumed to be the following:

$$\begin{gathered} \varphi = 0 \\ \theta = (90 - latitude) \times \frac{\pi}{180} \\ \psi = longitude \times \frac{\pi}{180} \\ Side\ real\ angle, s = 281 + 0.0041667 \times t \end{gathered} \tag{8}$$

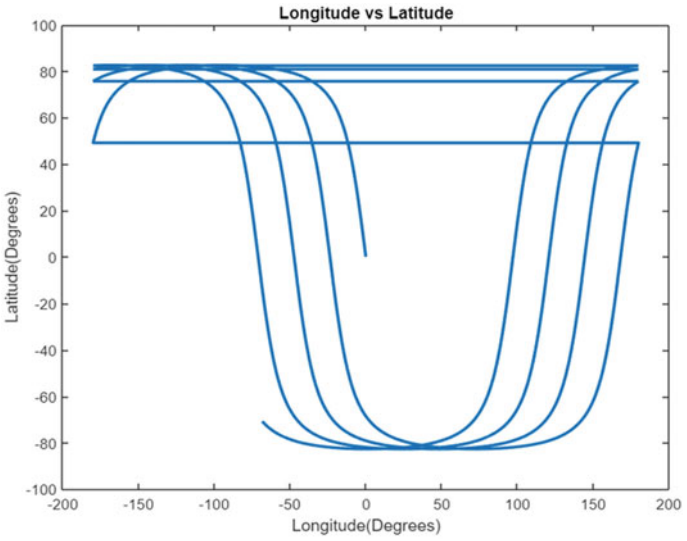

Fig. 2 Latitude versus longitude for a polar sun-synchronous orbit

3.2 Quaternions

The quaternion is a numeric framework that broadens real numbers into a four-dimensional domain. Quaternions can be utilized to depict rotations of coordinate systems, and they provide a singularity-free portrayal of kinematics.

Quaternions are represented as follows:

$$q = q_4 + \hat{i}q_1 + \hat{j}q_2 + \hat{k}q_3 \tag{9}$$

where q1, q2, q3 and q4 are real numbers and $\hat{i}$, $\hat{j}$ and $\hat{k}$ are unit vectors.

Euler angles are converted to quaternions using the following matrix:

$$\begin{aligned} q_1 &= \sin\left(\tfrac{\varphi}{2}\right)\cos\left(\tfrac{\theta}{2}\right)\cos\left(\tfrac{\psi}{2}\right) - \cos\left(\tfrac{\varphi}{2}\right)\sin\left(\tfrac{\theta}{2}\right)\sin\left(\tfrac{\psi}{2}\right) \\ q_2 &= \cos\left(\tfrac{\varphi}{2}\right)\sin\left(\tfrac{\theta}{2}\right)\cos\left(\tfrac{\psi}{2}\right) + \sin\left(\tfrac{\varphi}{2}\right)\cos\left(\tfrac{\theta}{2}\right)\sin\left(\tfrac{\psi}{2}\right) \\ q_3 &= \cos\left(\tfrac{\varphi}{2}\right)\cos\left(\tfrac{\theta}{2}\right)\sin\left(\tfrac{\psi}{2}\right) - \sin\left(\tfrac{\varphi}{2}\right)\sin\left(\tfrac{\theta}{2}\right)\cos\left(\tfrac{\psi}{2}\right) \\ q_4 &= \cos\left(\tfrac{\varphi}{2}\right)\cos\left(\tfrac{\theta}{2}\right)\cos\left(\tfrac{\psi}{2}\right) + \sin\left(\tfrac{\varphi}{2}\right)\sin\left(\tfrac{\theta}{2}\right)\sin\left(\tfrac{\psi}{2}\right) \end{aligned} \tag{10}$$

$$q = \begin{bmatrix} q_1 \\ q_2 \\ q_3 \\ q_4 \end{bmatrix}$$

Quaternions can be converted back to Euler angles using the following formulae:

$$\begin{aligned} \varphi &= tan^{-1}\left(\frac{2(q_1.q_4 + q_2.q_3)}{1 - 2({q_1}^2 + {q_2}^2)}\right) \\ \theta &= sin^{-1}(2(q_4.q_2 + q_1.q_3)) \\ \psi &= tan^{-1}\left(\frac{2(q_1.q_2 + q_3.q_4)}{1 - 2({q_2}^2 + {q_3}^2)}\right) \end{aligned} \tag{11}$$

3.3 Reference Frames

NED Frame

The code uses a file containing the latitude, longitude and altitude values of the satellite for 2 orbits at every 128 ms (minor cycle size). These values are then passed into an IGRF Model uploaded to the MathWorks official website by Drew Compston. The values of latitude, longitude and altitude are passed into this IGRF model, and the

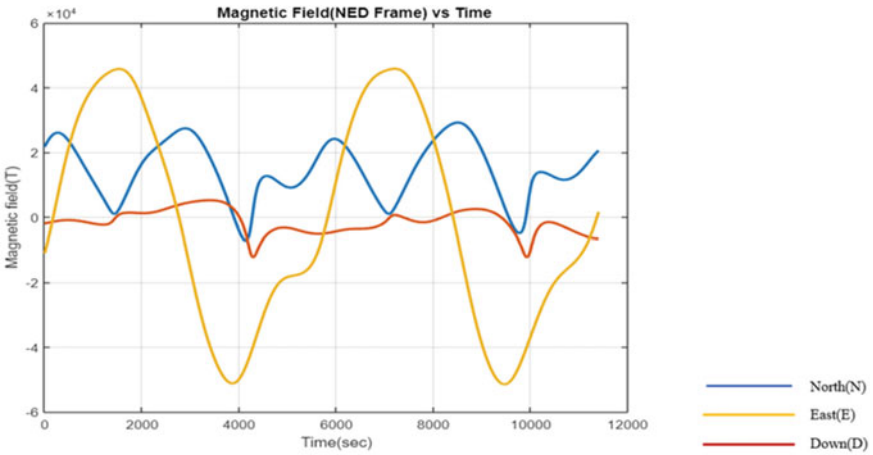

Fig. 3 Magnetic field in NED frame

Magnetic Field is obtained in the NED frame. N and E represent the tangential northward and eastward directions, respectively, with respect to the Earth. D represents the radial direction towards the centre of the Earth (nadir) (Fig. 3).

ECEF Frame

In the ECEF Frame, the coordinates are represented as X, Y and Z, and the frame of reference is geocentric. The X-axis passes through the prime meridian on the equatorial plane, Z-axis passes through the geographic north pole and Y-axis is calculated as the cross product of the Z- and X axes, respectively [7]. The values of magnetic field strength in the NED frame are converted to that in the ECEF frame using the following transformation matrix (Fig. 4):

$$B_{ECEF} = \begin{bmatrix} -\cos(\theta) \times \cos(\psi) & -\sin(\psi) & -\sin(\theta) \times \cos(\psi) \\ -\cos(\theta) \times \sin(\psi) & \cos(\psi) & -\sin(\theta) \times \sin(\psi) \\ \sin(\theta) & 0 & -\cos(\theta) \end{bmatrix} \times B_{NED} \quad (12)$$

ECI Frame

The ECI frame takes into consideration the rotation of the Earth. In the ECI Frame, the coordinates are represented as X, Y and Z, and the frame of reference is geocentric. The primary plane contains the equator and the positive X-axis is oriented in the vernal equinox direction [7]. The Z-axis is oriented in the direction of the geographic North Pole and the Y-axis is the cross product of the X- and Z axes [7]. The values of the magnetic field in the ECEF frame are converted to the ECI frame using the following transformation matrix (Fig. 5):

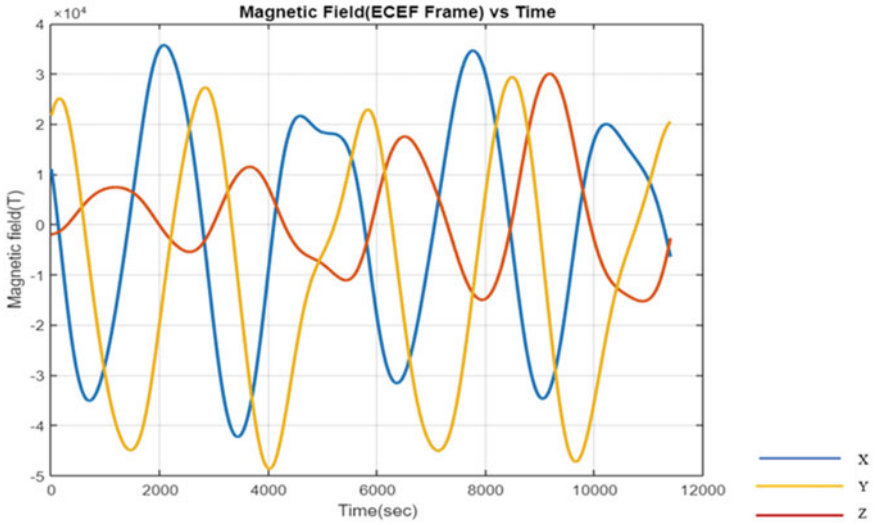

Fig. 4 Magnetic field in ECEF frame

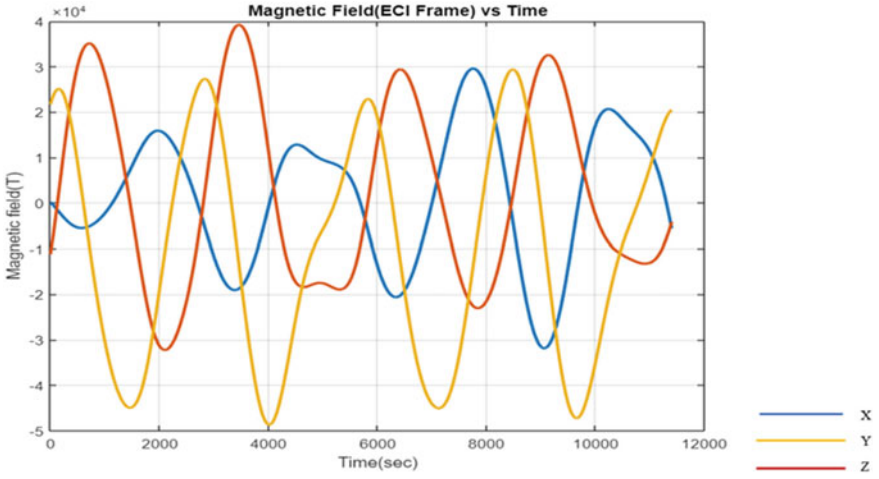

Fig. 5 Magnetic field in ECI frame

$$B_{ECI} = \begin{bmatrix} \cos(s) & -\sin(s) & 0 \\ \sin(s) & \cos(s) & 0 \\ 0 & 0 & 1 \end{bmatrix} \times B_{ECEF} \tag{13}$$

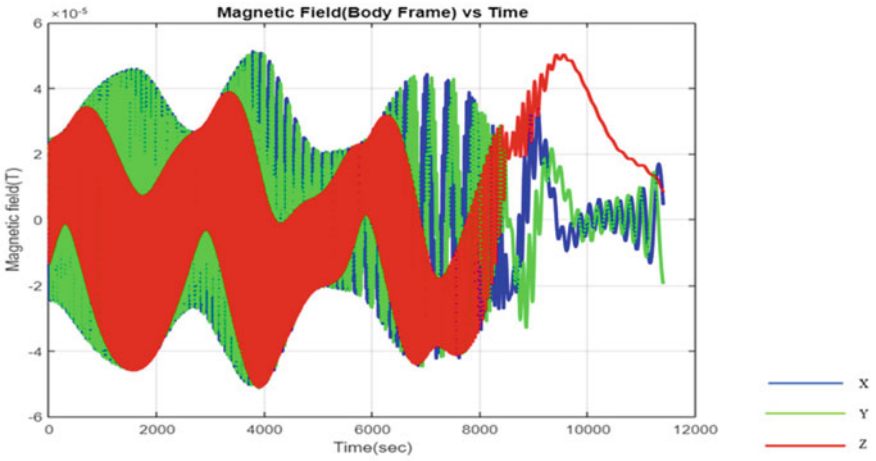

Fig. 6 Magnetic field in body frame

Body Frame

The magnetic field detected by a satellite is a function of its orientation with respect to the Earth. Therefore, the magnetic field experienced by a tumbling satellite is a function of its angular velocity. The inertial frame considering the orientation of the CubeSat is known as the Body frame. The magnetic field vector in the CubeSat body frame helps us determine the magnetic field acting on the satellite at every instance and helps us detumble the satellite. The following figure shows the magnetic field in the body frame for the CubeSat during the process of detumbling (Fig. 6).

Initially, when the satellite is spinning at a high rate, the magnetic field surrounding it changes at a similar rate but as the satellite gradually detumbles, the angular rate slowly declines causing the magnetic field rate to slowly decline as well. This is the basis of the B-Dot Controller, where the angular rate is always proportional to the change in the Magnetic Field of the satellite.

4 Simulation

4.1 Assumptions

- Earth constants:
  - Radius = 6.371*106 m
  - Mass = 5.972*1024 kg
  - Sidereal Rate = 0.004166667°/s
- Orbital Parameters:

- Orbit type = Polar Sun-Synchronous Orbit
- Inclination = 97.5°
- Eccentricity = 0°
- Orbit Period = 94 min
- Semi Major Axis = 6878.1 km
- Velocity at Perigee = 7613 m/s

- Satellite:
  - Mass = 6.5 kg
  - Altitude (above sea level) = 500 km
  - Dimensions = 10 cm * 10 cm * 30 cm
  - Initial Sidereal Angle = 281°
- Moment of Inertia of the satellite about different axes:
  - $I_x = 0.35$ kg.m^2
  - $I_y = 0.35$ kg.m^2
  - $I_z = 0.4$ kg.m^2
  - Initial Angular Velocity = 35°/s about all axes
- Sensor and Magnetorquer:
  - Magnetorquer Capacity = 1/1.5 A.m^2
  - Magnetometer

    Noise = ± 1*10–7 T
    Bias = ± 4*10–9 T
  - Gyroscope

    Noise = ± 0.005 rad/s
    Bias = ± 0.001 rad/s
  - Sensor Efficiency = 90%
- Other simulation Parameters:
  - Timestep = 128 ms
  - Sensor sampling rate = 5 * 128 ms or 8 * 128 ms
  - Initial Orientation of satellite [φ, θ, ψ] = [0°, 0°, 0°]

5 Results

5.1 With Gyroscope

See Table 1 and Fig. 7.

Table 1 Results of B-Dot controller simulation using gyroscope data

Magnetic moment (Am^2)	Sampling rate	Detumbling time	Angular RATE (°/s)
1	5 ×128 ms	9200 or 1.61 orbits	35
1	8 × 128 ms	9500 or 1.67 orbits	35
1.5	5 × 128 ms	6700 or 1.18 orbits	35
1.5	8 × 128 ms	6800 or 1.2 orbits	35

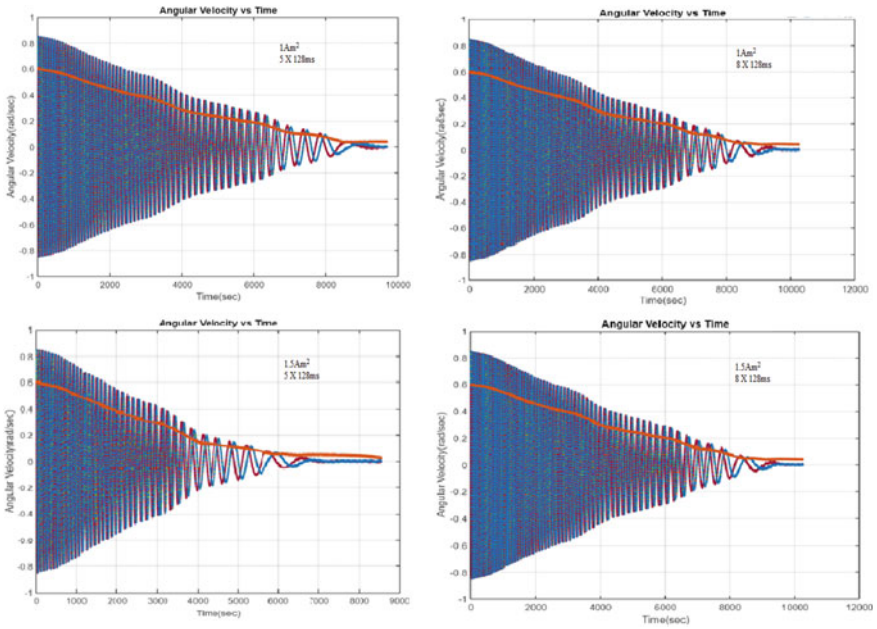

Fig. 7 Detumbling plots using gyroscope data

5.2 Without Gyroscope

See Table 2 and Fig. 8.

Table 2 Results of B-Dot Controller simulation without using gyroscope data

Magnetic moment (Am^2)	Sampling rate	Detumbling time	Angular rate (°/s)
1	5 × 128 ms	9200 or 1.61 orbits	35
1	8 × 128 ms	9500 or 1.67 orbits	35
1.5	5 × 128 ms	6700 or 1.18 orbits	35
1.5	8 × 128 ms	6800 or 1.2 orbits	35

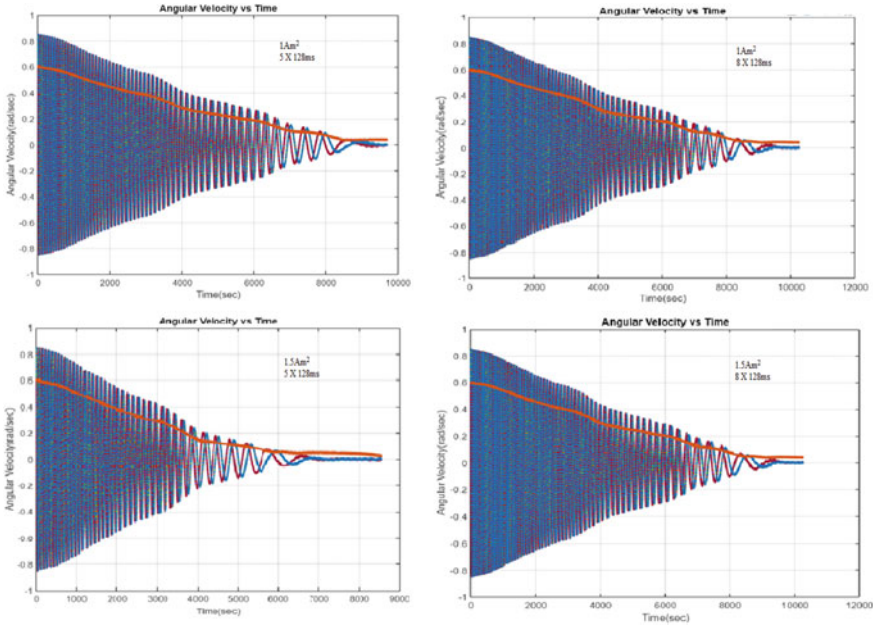

Fig. 8 Detumbling plots without using gyroscope data

The results of the simulation show that the B-Dot control algorithm can be successfully simulated with the presence and absence of a gyroscope, while retaining the same efficiency. Therefore, the gyroscope can effectively be omitted from the process of B-Dot control. The two forms of the B-Dot formula may also be used simultaneously in order to accommodate for when either one of the formulae yields a B-Dot value of zero. This further increases the efficiency of the detumbling process.

6 Conclusion

The B-Dot Controller Algorithm was simulated successfully in MATLAB and the detumbling plots of Angular Velocity versus Time were generated for different values of Magnetic Moment (Magnetorquer Capacity) and sampling rates. The simulation was conducted for both, the presence and absence of a gyroscope in the CubeSat.

6.1 Inferences

- From the results of the simulation, it can be concluded that detumbling using the B-Dot Controller Algorithm can be implemented without the use of a gyroscope

with similar results to that with the use of a gyroscope, thereby making the satellite more cost- and energy-efficient.
- The two B-Dot formulae may also be used simultaneously in order to accommodate for cases when either formula may yield a B-Dot value of zero.
- The optimum major cycle size was found to be 5*128 ms as it takes lesser time to detumble the CubeSat.
- Although the CubeSat detumbles faster at 1.5 $A.m^2$ magnetic moment, the power required is more and detumbling at 1 $A.m^2$ magnetic moment is feasible in terms of time taken for detumbling and power requirement.

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Overview of On-Board Computing Subsystem

Manoj S, Sannidhi Kasturi, Chandrakala G. Raju, H. N. Suma, and Jayanthi K. Murthy

Abstract In the era of wireless communication, satellites play a very important role in making wireless communication feasible. Satellite comprises many subsystems such as On-Board Computing, Power, Telemetry Tracking and Control, Structure, Payload, Thermal, etc. On-Board Computing handles all communication between each subsystem and is also responsible for data processing and data handling. The Field Programmable Gate Array (FPGA)-based On-board Computing (OBC) boards are being designed with the microcontroller instead of the traditional OBC design which included a single standard microcontroller. These FPGAs also provide lower power consumption and are also fault-tolerant. Different interface protocols can be designed within the FPGA such as Universal Asynchronous Receiver-Transmitter (UART), Serial Peripheral Interface (SPI), Inter-integrated Circuits (I2C) for interfacing different sensors into the OBC board. This paper is a detailed survey regarding the overview of the On-Board Computing subsystem.

Keywords On-board computer · Field programmable gate array · Modes of operation · Data handling · Sensor interfacing

Manoj S (✉) · J. K. Murthy
Department of Electronics and Communication Engineering, BMSCE, Bangalore, India
e-mail: manoj.ec19@bmsce.ac.in

S. Kasturi
Department of Computer Science and Engineering, BMSCE, Bangalore, India

C. G. Raju
Department of Information Science Engineering, BMSCE, Bangalore, India

H. N. Suma
Department of Medical Electronics, BMSCE, Bangalore, India

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_3

1 Introduction

A satellite is a combination of different subsystems, each working to perform specific tasks. On-Board Computer (OBC) is the brain of the satellite which is responsible for monitoring temperature, pressure, direction, all telemetry and telecommand signals, and memory management [1]. The main function of the OBC is to communicate with different subsystems and also to the ground station. OBC subsystems carry out the processing of science data (such as payload data), and housekeeping data and send it to the ground station when requested through tele commands. The next section of this paper provides the design of the onboard computing subsystem. The different modes of operation and interfacing of different sensors are discussed in Sects. 3 and 4 of this document, respectively. Section 5 shows us the data handling done by the OBC. Sections 6 and 7 depict the common problems encountered during the development of the OBC, and some of the proposed solutions for the same, respectively.

2 Design of OBC

OBC can be designed using an FPGA-based model, which helps all subsystems to run parallelly in a hierarchical relationship. The design using the FPGA can be done in the form of a finite state machine working in major and minor cycles. The goal is to design a system that uses the same power provided by the satellite but fits in a smaller fixed space and also interface with the control signals of the satellite that are already present [2].

2.1 Hardware Architecture

The OBC subsystem hardware is realized either using a System On-Chip (SOC) FPGA or using a microprocessor/microcontroller. The efficient hardware design is to use both FPGA and a microprocessor running in parallel as shown in Fig. 1. The FPGA is used to interface different sensors using different protocols into the OBC. The microprocessor is used for processing housekeeping data. The microprocessor initializes and transfers the control to the processor present in the FPGA.

- **SOC FPGA**. Main processing unit responsible for data handling and interfacing different sensors
- **Microprocessor**. For housekeeping inside the OBC
- **Rx, Tx**. Receiver and Transmitter
- **Analog Sensors**. Includes Course analog sun sensors, thermistors, solar panels and battery sensors
- **Analog Interface**. Interfacing all analog sensors to the OBC board
- **Digital Sun Sensors, GPS**. For location and altitude adjustment.

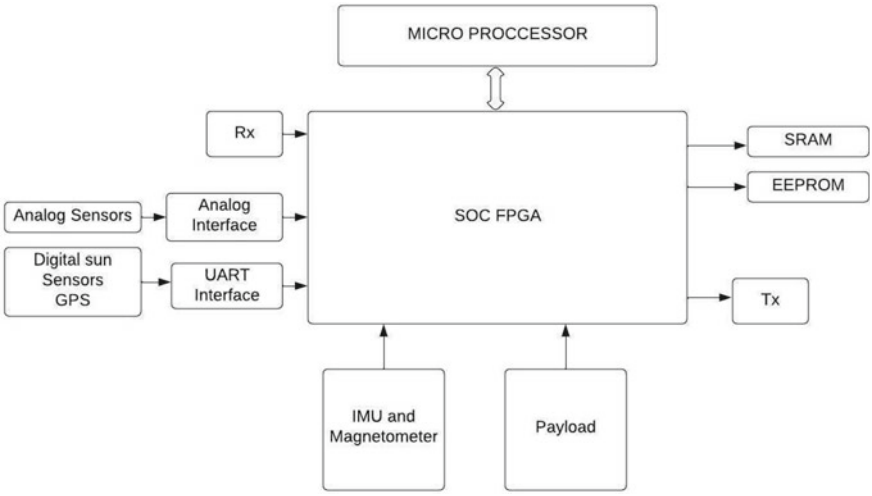

Fig. 1 Depicts the overview of OBC subsystem

- **UART Interface**. Interfacing digital sensors and GPS to the OBC board
- **IMU and Magnetometer**. For monitoring the orientation and angular velocity of the satellite
- **Payload**. Payload sensors like camera and IR imaging devices.
- **SRAM**. For storing temporary data during data processing
- **EEPROM**. Storing parametric data of the system

Microprocessor Selection. The microprocessor for the OBC needs to be selected keeping different aspects such as power consumption, operating temperature, operating voltage, packaging I/O, and serial bus compatibility into consideration. Following steps are followed to select the best-suited microprocessor for our mission-

- The first step is to shortlist different core design manufacturers such as Atmel, ARM, Texas Instruments, etc.
- Based on the above-mentioned parameters microprocessors are selected and compared with different manufacturers.
- The last step is to compare each shortlisted microprocessor individually and select the best suited for our requirements [3].

Different microprocessors used in different missions

- Atmel 32-bit microcontroller AVR32- AT32UC3A0512 is used as the main processing unit in the Cube Sat developed by the Cape Peninsula University of Technology, South Africa [3].
- Norwegian University of Science and Technology (NTNU) Test Satellite uses ATSAMV71Q21 microcontroller in the UHF radio range and AT32UC3C0512C microcontroller in the VHF radio range [4].

- The PISAT Nano satellite launched by the Crucible of Research and Innovation Laboratory of PESIT, India, used an Atmel 32-bit microcontroller AVR32-AT32UC3A0512 with a clock speed of 12 MHz [5].

2.2 Software Architecture

Attributes of a good software. The OBC software requirements specification is the most crucial part of the OBC software. Following are the characteristics to adhere to while designing the software [4]–

- Minimal complexity
- Ease of maintenance
- Loose coupling/high cohesion
- Extensibility, Reusability and portability.

Onboard autonomy. The onboard autonomy in any satellite can be distinguished in three different ways as shown below-

- The commanding level can be set such that only low-level commands are executed in the initial phase of the mission. The commanding level is increased after testing the satellite in the orbit. The high-level commands are converted into sequential low-level commands on the satellite for execution.
- The intelligent payload data processing is considered as the second autonomy wherein a particular data is selected, stored, and processed by the data processing algorithm.
- The highest autonomy is the artificial intelligence of the satellite to carry out its instructions and self-decision-making without relying on the ground station or any other system [2].

Mission control system. The mission control system looks after the satellite from the point of launch till the end of the mission. The mission control system is a part of the ground station which monitors all aspects of the machine by sending telemetry and telecommand data from the ground station to the satellite. The most common mission control system (MCS) software is the satellite control and operation system 2000 (SCOS 2000). The SCOS has been used by the European space agency in several space missions like Cryosat, Galileo FOC, and MetOp-A [6].

3 Modes of Operation

3.1 Modes of Operation Based on Battery Capacity

As proposed by Arnesan and Kiaer, the modes of operation can be divided into three sections–

Critical Mode. The OBC switches to the critical mode when the battery capacity is less than 25% of the maximum battery capacity.

Avoidance Mode. The OBC switches to the critical mode when the battery capacity is between 25 and 50% of the maximum battery capacity.

Normal Mode. The OBC switches to the critical mode when the battery capacity is between 50 and 100% of the maximum battery capacity [4].

3.2 Modes of Operation Based on Contingency

The contingency operation as seen in the Flying Laptop satellite developed from Institute of Space Systems, Universität Stuttgart, can be classified as follows–

Level I Contingency (Idle Mode). The satellite enters the idle mode due to insufficient battery charge as mentioned above.

Level II Contingency (Safe Mode). The satellite enters into the safe mode due to the failure of any primary sensors such as altitude determination sensors. This mode triggers the altitude control system into the detumbling mode [2].

4 Interfacing of Different Sensors to OBC

Interfacing different sensors into the OBC is the major aspect in the development of an On-Board Computing subsystem of a nanosatellite. For interfacing different sensors we use different protocols based on the sensor datasheet. The different protocols include SPI, I2C, and UART.

Inter-integrated circuit (I2C) bus is generally used for communicating with different sensors and for data read operation. Serial-peripheral interface (SPI) bus is usually used where the data is of a larger magnitude that needs to be transferred. SPI can also be used in the interface between the OBC and the Power subsystem [7]. Universal Asynchronous Receiver Transmitter (UART) protocol is used for digital sun sensor and GPS interface.

5 Data Handling

The majority of the data coming into the OBC subsystem comprises science data which includes data coming from payloads and other sensors onboard. OBC also receives housekeeping data continuously from communication devices.

5.1 Payload Data Processing

The main purpose of a satellite is to gather data, process it, and send it back to the ground station. The data gathering is generally carried out by the payloads present onboard. This data coming from the payload needs to be reduced so that there is an efficient transfer from the satellite to the ground station. The processing of the data can be done in any of the following methods–

- The redundancies in the data are removed by compressing the data by various methods.
- The data can be analyzed on the satellite before sending it to the ground station. This process takes up a long implementation time and also affects computational performance.
- The data can be screened such that only a particular part of the data is extracted and sent to the ground station [2].

6 Common Obstacles Encountered While Designing OBC

6.1 Reliability

Reliability is always an important requirement on a space mission because if a failure occurs in space it cannot be repaired and usually results at the end of the mission, although increasing the reliability of the system is directly proportional to the increase in the cost.

6.2 Space Radiation

When the satellite is in space, radiation produced by particles emitted from either the sun (solar radiation) or from outside of the solar system, Galactic Cosmic Rays (GCRs) can cause degradation of the satellite, ultimately leading to the failure of the electronic and electrical systems in either the space vehicle or the satellite. Single event upsets (SEU) are the errors caused by radiations in microelectronic components. Single Event latch-ups (SEL) indicate the failure of a semiconductor device in responding to any input signals [4].

6.3 EEPROM Errors

Errors observed in the microcontroller EEPROM in the OBC affect the log register of the commands processed by the OBC, whose origin is suspected to be related to

single event upsets (SEU), which can cause an increase in the OBC resets. These errors and OBC resets bring about change in the satellite time and result in the loss of the last received commands [8].

7 Fault Tolerance Methods

7.1 Watchdog Timer

A hardware timer is set on-board which resets itself at a particular predefined interval of times is known as the Watchdog timer. This timer is used for fault isolation and to safeguard the OBC from failures such as interface bus failures.

Watchdog can be used in a hierarchical order for better implementation. Software Watchdog threads are used OBC software [7].

7.2 Radiation Associated with Fault Tolerance for FPGA

The SEU and SEL are caused due to radiation effects. The SRAM-based FPGAs such as ZYNC 7000 are very sensitive to radiations. The upsets associated with PL fabric can be removed by resetting the memory configurations of the upsets followed by a whole system resets. The operation of FPGA in a radiation environment can be carried out with techniques such as mitigation and scrubbing [7].

7.3 Radiation Associated with Fault Tolerance for Flash Memory

Flash memories are generally susceptible to radiation; therefore, an additional boot image is stored in n EEPROM. This allows updating the software on flash while there is a fallback in the EEPROM. Memory scrubbing can be included in the flash memory with the help of error-correcting codes such as Hamming codes [7].

7.4 Multilevel Reset Mechanism

A multilevel reset scheme is used to remove SEU and SEL problems. The resets can be done in different ways such as autonomous reset of just the OBC's system on module. The reset can also be done to the entire spacecraft by sending a signal to

the power subsystem. The reset is also done by sending a command from the ground station using a telecommand [9].

8 Conclusion

The overview of the On-Board Computing subsystem of a Cube Sat is discussed in this paper which includes the design of the hardware using a SOC FPGA and microprocessor. The working of satellites in different modes and data handling capability is key in the functional aspect of the OBC subsystem. Some of the obstacles encountered in designing OBC are discussed with the possible solutions for the same.

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Thermal Management Scheme for SWIR IDDCA Used in Space Payloads

Bharat Ram Meena, Maneesh Pawar, Shekhar Tomar, Umesh Kumar, and Manvendra Singh

Abstract A Passive thermal management scheme is devised while taking various Opto-thermal, Opto-mechanical & space environmental constraints into consideration. The finite element model of the thermal management scheme is established in NX NASTRAN to analyze the design w.r.to the given payload and satellite design parameters. The scheme is based on flexible thermal straps made of copper material. This scheme will help in achieving the desired thermal management while isolating the IDDCA assembly from the external vibrations and loads. The scheme is validated through implementation on the actual IDDCA & measuring the change in temperature w.r.to time at critical locations.

Keywords Thermal straps · IDDCA · Thermal interface materials

1 Introduction

Integrated Detector Dewar Cooler Assemblies (IDDCA) used in SWIR space payloads can produce heat up to 65 W during the operations. This high amount of heat may lead to a rise in the temperature of the components of the IDDCA assembly itself. The temperature rise may result in the breakdown of the Opto-electronics components of the Detector Dewar. Continuously operating the detector at elevated temperature leads to a reduction in the life of this high-value device. So thermal management is required to achieve the optimum performance of the SWIR IDDCA.

Thermal management is also important to protect the optical performance of the Electro-Optical Payload. The heat dissipated by the IDDCA will affect the optical tolerances of the optical system. Such systems are designed for a very narrow operating temperature range and tight optical tolerances. Variations in temperature and optical tolerances of the Payload will lead to performance instability and reduction in mission life [1].

B. R. Meena (✉) · M. Pawar · S. Tomar · U. Kumar · M. Singh
Aero and Spaceborne Systems Division, Instruments Research and Development Establishment, Dehradun 248008, India
e-mail: bharatmeena.irde@gov.in

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_4

As the IDDCA houses, Focal plane arrays (FPA) are the main imaging element of a detector and they are very sensitive to the surrounding vibrations and jitters. Vibrations transmitted to them through any external source may result in poor optical performance and blurred images. So, the designed thermal management scheme should isolate or have minimum transmitted vibrations and external loads [2].

There are various techniques used for extracting the excessive heat from such Electro-Optical Devices. Both active and passive thermal management schemes are deployed depending on the amount of heat to be rejected, and the cost & life of the mission [3, 4]. Active thermal control systems require heating or cooling the device using electrically powered heaters or coolers. The active thermal control systems add complexity to the systems and may result in the reduction of the reliability of the mission [5]. The passive Thermal management systems such as Thermal straps, provide a very cheap and reliable heat transfer mechanism [6].

2 Methodology

The research is aimed at the design, analysis, and validation of efficient thermal management for a SWIR IDDCA used in space applications. This device consists of two parts: (a) Compressor assembly and (b) Dewar assembly. The parts are connected through a Stainless-Steel pipe through which cool Helium gas is transferred between the compressor and Dewar. In this process, heat is rejected at the surfaces of the Compressor and Dewar and areas highlighted in Fig. 1a are allowed to use for thermal management.

The temperature requirement for compressor and Dewar during the operations is that the skin temperature must not exceed Ta + 10 °C (Ta is the ambient temperature of the room) at any point.

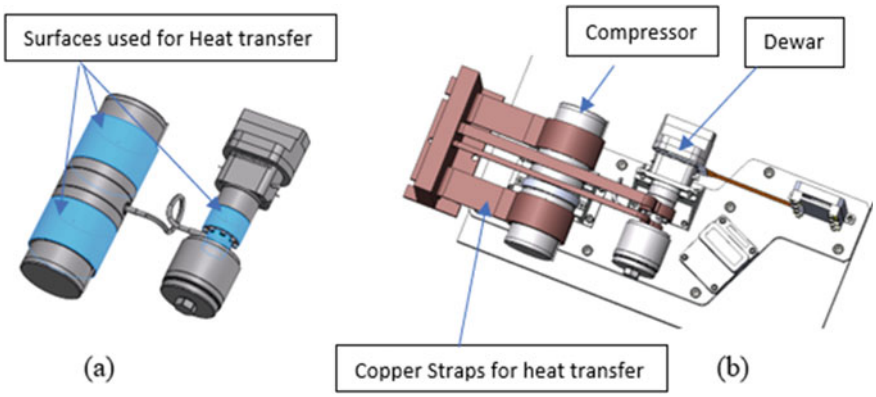

Fig. 1 **a** SWIR IDDCA. **b** SWIR IDDCA with thermal management scheme

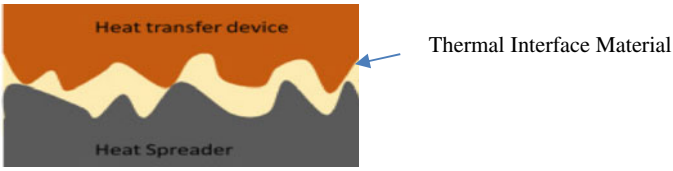

Fig. 2 Application and implementation scheme of thermal interface material [1]

The space environment presents a unique challenge in using such high heat dissipating devices, unlike terrestrial applications, the heat can be removed through conduction and radiation [1].

To transfer the excess heat from the Compressor and Dewar surfaces, a passive conduction-based heat transfer mechanism is used. Four cylindrical surfaces are specified for heat transfer, so conductive straps are designed as shown in Fig. 1b. The ends of the straps connected to the IDDCA are designed as per the assembly requirements. The other ends of the straps are terminated on a heat sink.

Because of the surface roughness at the microscopic levels between the IDDCA surface and Thermal Straps, there will be an air gap. This air gap works as a thermal resistance resulting in a drastic reduction in heat transfer and poor thermal interface. For the improved thermal interfaces between the Thermal straps and Heat emitting surfaces, a thermal pad made of thermal interface materials (TIM) is used. This TIM is very soft and can deform itself as per the interface requirements. In this process, they remove the air between the Thermal straps and Thermal surfaces resulting in improved thermal coupling [1]. Figure 2 shows the implementation scheme of the Thermal Interface Material.

Flexible Thermal Straps become very essential when excess heat is transferred from vibration sensitive devices such as IDDCA and cryocoolers in close proximity. Thermal straps conduct heat from IDDCA to the Heat sink while limiting the amount of mechanical vibrations and loads transferred to the IDDCA and vice versa. Thermal straps are generally made from flexible, highly conductive materials such as Copper, Graphite and Aluminum. These straps, if made from pure metals, provide superior thermal performance at cryogenic temperatures. [2, 6]

Thermal straps conduct heat while minimizing mechanical strain and vibration between the system components [1, 2, 6–9]. They are often used with cryocoolers to transfer waste heat to be rejected because they can thermally couple a system to the cryocooler, while still offering some level of mechanical isolation.

2.1 Material Selection

In the thermal management scheme, there are two external materials used to complete the scheme (i) Thermal Straps and (ii) Thermal Interface Material (TIM). Careful

Table 1 Thermal properties of the available structural materials

Material	Thermal conductivity (W/mK)	Thermal diffusivity (mm^2/s)
Silver	418	165.63
Copper	397	111
Gold	310	127
Aluminum	167	97
Iron	55.6	23
Titanium	15.6	11

selection of these two materials is very important for an effective and durable thermal management scheme.

The material for Thermal straps is Oxygen-Free High Thermal Conductivity (OFHC) Copper. It is chosen for its high thermal conductivity and Favorable thermal diffusivity. These two factors are responsible for quick heat transfer from source to sink [2, 6, 9]. Other than that Copper has a long heritage of space applications. It is also available in various forms such as sheets, cables and plates. The material properties of the available materials are listed in Table 1.

The Thermal Interface Material (TIM) chosen is Indium foil with a thickness of 100–120 μm. Indium is chosen for its Softness and Malleability, Thermal Conductivity and Low Thermal Resistance [1, 9].

3 Results and Validation of the Scheme

The finite element model approach is used to optimize the thickness and length of the straps using NX NASTRAN. The connecting ends of the strap are designed as per the mating geometry of the IDDCA assembly. Copper is chosen as the material for straps as it has one of the highest thermal conductivities and is easily available in the market at cheaper prices.

The temperature profile of the IDDCA assembly is shown in Fig. 3. While simulating the thermal management scheme, the ambient temperature taken is 23.5 °C and the temperature of the Heat sink is taken at 15 °C. The maximum rise in the temperature in the steady-state conditions is ~1.86 °C.

The thermal management scheme is validated in the lab through experiments. The actual IDDCA is operated for one hour and the temperature rise was recorded at various locations. The entire validation scheme is shown in Fig. 4.

To measure the temperatures at two locations: (i) at the surface of the compressor and (ii) at the heat sink two sensors have been mounted. At both locations, thermocouples with very high precision are mounted. These two sensors record the temperature at these two locations during the operation of the Device.

The results demonstrate that the rise in the temperatures at two critical locations was not more than 1.8 °C. The rise in the skin temperature of the IDDCA assembly

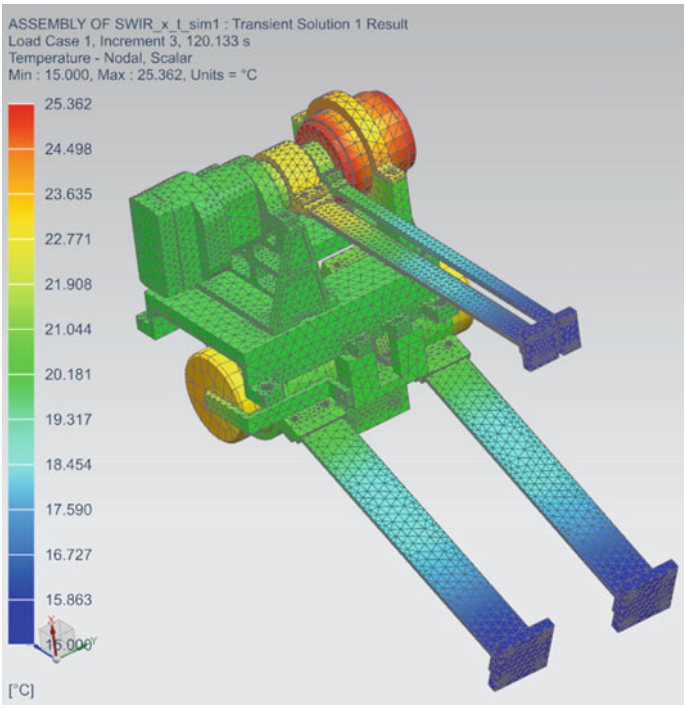

Fig. 3 Temperature profile of the IDDCA assembly obtained through FEA

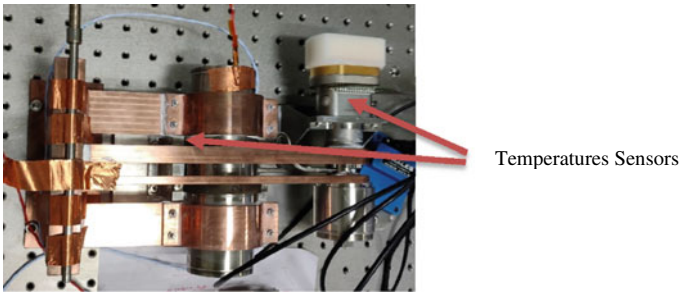

Fig. 4 SWIR IDDCA with thermal management scheme and sensors

is plotted in Fig. 5. Other than this the results are in line with the Finite Element analysis results.

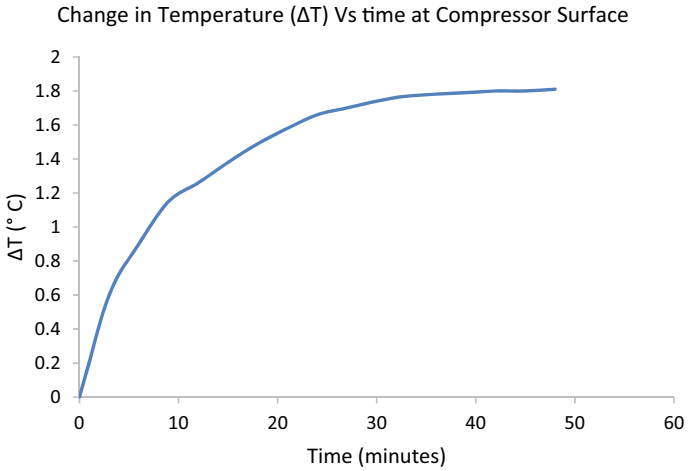

Fig. 5 Change in temperature of compressor skin w.r.to time

4 Conclusion

The heat from IDDCA for space applications is removed mainly through conduction in the space vacuum environment. Therefore, the most effective method to remove heat from IDDCA assembly is through Thermal straps made from OHFC Copper. The flexibility in the Thermal straps isolates the IDDCA from the external vibrations and loads. To improve the Thermal Interface between Heat emitting surface and Straps, a Flexible Thermal Interface Material (TIM) is used as sandwich material. TIM is required to reduce the thermal contact resistance by filling in the air gaps between the IDDCA surface and Thermal straps. The scheme is validated through lab experiments by measuring the temperature of the skin of the IDDCA during the operation.

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EO Characterization of SATURN SWIR Detector Array

Maneesh Pawar, Bharat Ram Meena, and Manvendra Singh

Abstract For precise panchromatic and hyperspctral imaging, it is essential to model the transfer function of complete imaging system. The modeling mandates accurate determination of, EO parameters of detector array, optical system transfer function and their dependence on thermal and vibration variations. This paper presents the methodology and experimental setup for characterization of the EO parameters for SATURN SWIR integrated detector array and Dewar cooler assembly (IDDCA) to determine the charge to voltage function (CVF), linearity, readout noise, dark current, non-uniformity, array operability and Full well capacity (FWC), electrical dynamic range (DR). The presented method uses the photo-detector linear signal model to generate a photon transfer curve (PTC) which is further used to calculate the SWIR detector EO parameters.

Keywords Hyperspecral imaging · Photon transfer curve · EO parameters · Readout noise

1 Introduction

The SATURN SWIR IDDCA consists of mercury cadmium telluride (MCT) detectors with 30um pixel pitch and large well capacity of 0.5 M e– with extremely low noise of 150e– which enables system architects to design a high signal-to-noise (SNR) imaging system to capture signatures of targets with high efficacy from low earth orbits. Because of the state-of-art specifications, SATURN SWIR IDDCA have been used extensively to develop various space-borne EO payloads for panchromatic, multispectral and hyperspectral imaging applications [1–3]. Though the manufacturer provides the EO parameters in the detector datasheet, those measurements are often done in factory-controlled environment. Therefore, it is always scientifically appropriate to characterize the EO parameters of any detector array in operating

M. Pawar (✉) · B. R. Meena · M. Singh
Vision Instruments (Aero and Space Borne Systems) Division, Instruments Research and Development Establishment, Dehradun 248008, India
e-mail: maneesh.pawar.irde@gov.in

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_5

conditions for precise system modeling as any deviation from the datasheet value may lead to erroneous results especially in the system designed for radiometric measurements [1]. Photon transfer curve method, relies on a linear signal model for any photo-detector, and is a widely accepted method for calculating all major EO parameters [4].

2 Methodology and Experimental Setup

The photo-response of any photo-detector determines the ability to convert the incident photons into the electrons and further into voltage for a fix integration time. The voltage is digitized using analog-to-digital converters to produce the digital number (DN), which is proportional to the incident irradiance on photo-detector. The photon transfer curve is generated by observing and recording the photo-response of photo-detector post digitization in form of digital images from the SWIR detector array for varying irradiance.

2.1 System Configuration

The SWIR detector array is interfaced with a FPGA-based proximity electronics via a flex cable, which hosts multiple ADCs to digitize image signals carried by multiple analog output channels. The SWIR detector array has an in-built cryocooler, for cooling the FPA to cryogenic temperature, which is controlled and regulated by the cooler electronics. The cooler and the proximity electronics are powered by a 12VDC LabView controlled power supply. The analog signals are digitized by the ADCs. The digitized values are buffered and sent over to LabView processing units by the FPGA.

The LabView processing unit [5] captures the image frames from the proximity electronics in real-time over the CAMLINK interface. The software for acquisition, processing the image frames and algorithm implementation for EO parameters calculation, has been developed in LabView on the processing unit. The integrating sphere (with in-built quartz and plasma lamps) is used as a uniform light source which has enough power spectral distribution to cover the entire SWIR range. The integrating sphere irradiance is controlled by a computer controller. The illumination intensity, in the pre-calibrated integrating sphere, can be varied by simply turning on and off the lamps of the source. The interfacing details are provided in Fig. 1.

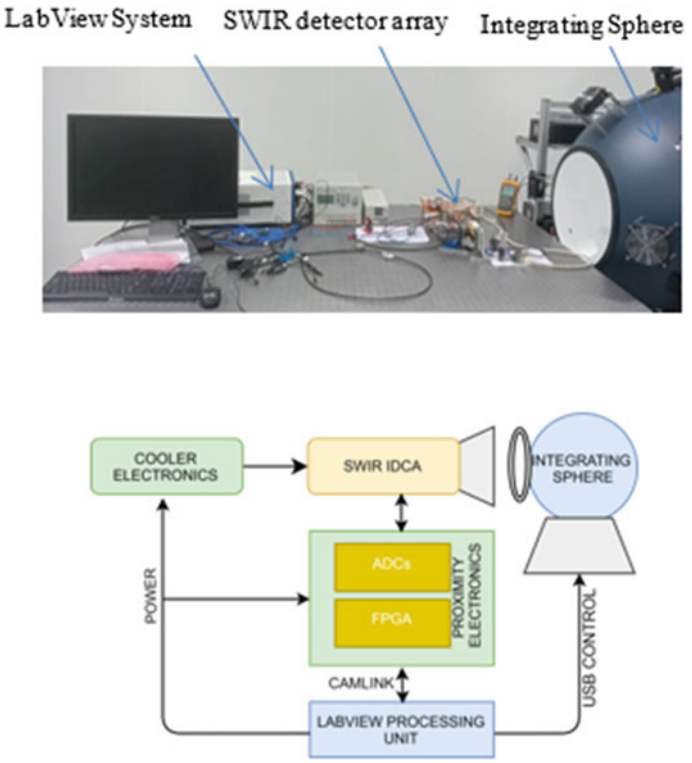

Fig. 1 Instrumentation setup diagram (top) and actual (bottom) for SWIR detector array characterization

2.2 Measurement of CVF, FWC and Linearity, EDR, Array Operability

To estimate the CVF, a set of images is captured at fixed integration time for each varying illumination from the dark to the saturation levels. The set of images captured at each intensity level is used to estimate the temporal noise and the dark offset corrected mean. The plot of temporal noise and dark offset corrected mean for each sample set provides the PTC as shown in Fig. 2. The slope of the PTC for linear region gives the value of the CVF.

It is intuitive that at FWC, the output of all photodetectors will be identical and will attain the maximum value of the quantization code in ADC. The temporal noise must start to reduce drastically at images captured at saturation level. Therefore, the point in the PTC, where the temporal noise starts to fall gives the FWC in terms of the DNs, which can further be converted to electrons by using CVF and QE. To assess the Linearity, the dark offset corrected mean output signal from each set of observations is plotted against the irradiance of the source for each illumination

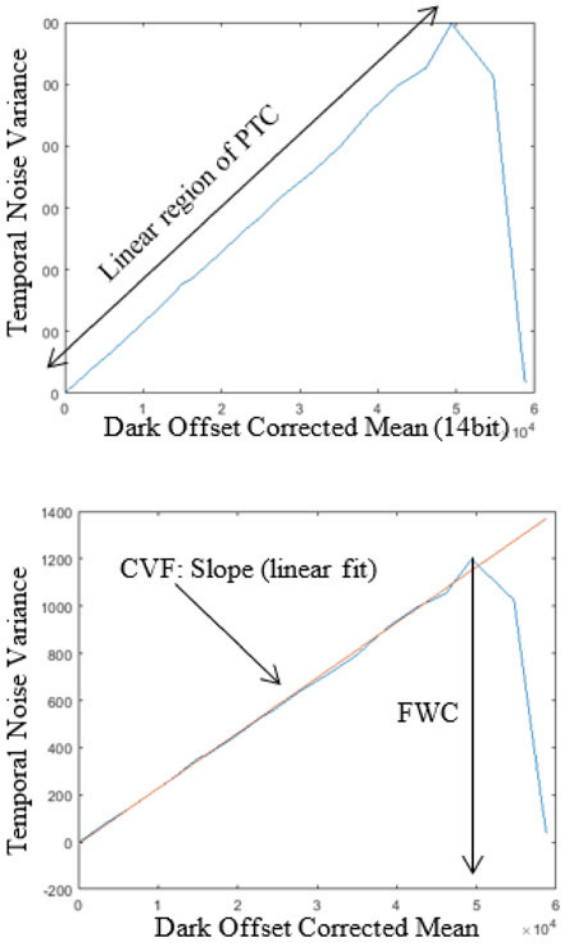

Fig. 2 Temporal noise vs. mean plot showing linear region (top), CVF and FWC (bottom)

levels. The Linearity measures the peak deviation of the output signals from the best fit linear behavior between 10% and the 90% of the signal range. The EDR is estimated by measuring the voltage difference across any analog output of IDDCA during dark and saturation level irradiance exposure. The array operability is calculated by estimating the number of defect pixels in FPA whose response is fixed against any irradiance level. This can easily be determined by divergence of pixel DN value from mean for uniform illumination [6–10].

Fig. 3 Dark Image at shorter (top) and longer (bottom) integration times

2.3 Readout Noise, Dark Signal and Dark Signal Non-Uniformity

The readout noise is a cumulative effect of shot noise, column and amplifier noise, ADC quantization noise. The cumulative Readout noise can be evaluated by estimating the temporal variance of photodetector over preferred integration time in a thermally regulated dark environment. The dark signal is a temperature-dependent phenomenon, which results in electron–hole pair generation due to thermal random processes in the absence of incoming photons.

The dark signal is measured by acquisition of two image sets, at shorter and longer integration time shown in Fig. 3 respectively. The dark signal (e−/sec) is obtained by dividing the mean of the difference image by the difference of integration time. The DSNU is measure of the spatial non-uniformity of the dark images, which is evaluated by estimating the standard deviation of the dark image [6–10].

2.4 Photo Response Non-uniformity

The aforementioned parameters were characterizing the individual photo-detector. The overall value for the entire FPA is often expressed as the mean value of a particular parameter for all photo-detectors. The non-uniformity in general deals with the difference in behavior of the individual photo-detectors for same number of incident photons.

The PRNU is not considered to be noise but a response anomaly due to fabrication imperfections, poor photo-detector design, photo-detector size, capacitance variations etc. [6–10]. The non-uniformity among the SWIR FPA detectors is shown in Fig. 4.

Fig. 4 Non-uniformity in a section of SWIR image

3 Results and Discussion

For accurate measurement of EO parameters, the stability of the uniform light source and FPA temperature are extremely important. Therefore, during each exposure, the images were only grabbed after stabilizing the integrating sphere for 30 min after setting the desired intensity levels. For ascertaining the FPA temperature stability, the FPA is allowed to cool-down at 160 K via the cryo-cooler and LabView unit measures the FPA temperature every 10 ms. The automatic acquisition only takes place when FPA temperature stability is within the limits of ± 0.5 K.

The Table 1 shows the measured and datasheet values for all EO parameters under scrutiny. The datasheet doesn't disclose the values of CVF, dark signal and DSNU. However, as all other parameters mentioned in the datasheet are matching with the measured values within extremely narrow margins, therefore the measured parameters without ground truth can be trusted to be reasonably accurate. Though, there are no large variations in the observed values from the mentioned values but for the readout noise, the first set of measurements were almost identical to that of manufacturer given numbers, so the experimented was repeated thrice and a mean of all the experiment was taken.

4 Conclusion

In the proposed experiment, the sensor has gone under exhaustive EO characterization to determine all important parameters in controlled laboratory environment. The measured values are matching with the manufacturer values within acceptable limits. The small fluctuation in values on readout noise and FWC will have negligible effect on overall SNR of the imaging system.

Table 1 Comparison of measured and ground truth EO parameters

Parameters	CVF (DN/e−)	FWC (e−)	Linearity	Readout noise (e−)	Dark Signal	DSNU (DN)	PRNU	Dynamic range (V)	Array operability (%)
Measured value	0.0225	0.487 Me−	<99%	161	365 DN/s	136 DN	<6.3%	3.05	99.5
Datasheet value [2]	Not given	0.5 Me−	<99.5%	150	Not given	Not given	<7%	3.0	99.5

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Hardware and Simulation Comparison of Synchronous Buck Topology for Hi-Rel Applications

Thadisetti Kanaka Nagaraju, Nishanth B. Kulkarni, S. Pradeep, and Bhoopendra Kumar Singh

Abstract The present Paper presents the Design and Development of Synchronous Buck-Converter with output 20 V/3.9 A for achieving higher efficiency of up to 97% with the input voltage range of 28–36 V and operating at a switching frequency of 200 kHz for HiRel applications. The proposed Synchronous Buck converter is a part of the power supply used to power various subsystems and pay loads Hi-Rel systems. Efficiency calculations will be estimated with the help of a simulation software LT-Spice and compared with the hardware test results. High voltage synchronous and current mode controlled Integrated Chip IC is used with external MOSFETs. In addition to efficiency Load regulation of <1% and Output ripple voltage of <1% is achieved in this design.

Keywords Buck regulator · Synchronous buck converter · Current mode control · Hi-Rel application · High efficiency

1 Introduction

DC–DC Converters are core to many industries like Defence and Space organizations. DC–DC converters can be used as power supplies for various payloads, RF subsystems in Hi-Rel (High Reliability) applications and motion controls in many automotive industries. These DC–DC converters are classified as step-up and step-down converters based on the input and output voltage ranges. Introduction of switching mechanism into the dc–dc converters has brought us a very highly efficient, tighter regulation and smaller size converters, which are most important parameters where size is the bigger constraint like space applications. This is achieved by operating the converter at a higher switching frequency and by using special topologies rather than the conventional topologies. For this reason, the synchronous buck converter is introduced [1, 2] in place of the conventional buck converter to avoid the losses in the freewheeling diode of the buck converter.

T. K. Nagaraju (✉) · N. B. Kulkarni · S. Pradeep · B. K. Singh
Centum Electronics Limited, Bengaluru, India
e-mail: nagarajutk@centumelectronics.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_6

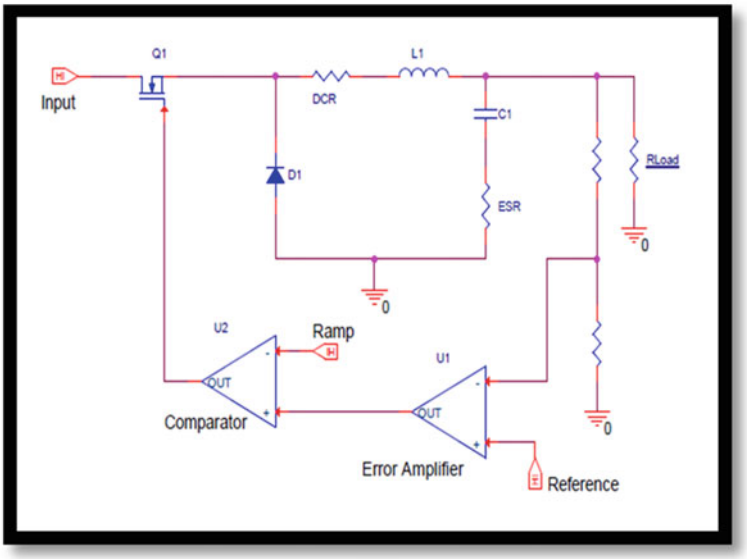

Fig. 1 Conventional buck converter

2 Conventional Buck Converter

Figure 1 shows the circuit for Buck Converter. Basically, buck converter will be used when the output is required less than the input voltage. The excess energy will be stored in the inductor when the Mosfet is turned ON. The inductor current flows through the load and charges the output capacitor.

During the OFF state stored energy in the inductor is supplied to the load through the freewheeling diode since the inductor cannot change the flow of current direction instantaneously, the capacitor also discharges through the load during the off time of the MOSFET to compensate the ripple current created by the inductor for maintaining the DC load current. Buck converter waveforms are shown in Fig. 2.

3 Synchronous Buck Converter

The circuit diagram in Fig. 3 shows the Synchronous Buck Converter. The Sync-buck converter is different from the conventional buck converter, in which the diode is replaced by Mosfet (Bottom MOSET). Bottom MOSFET will acts as a freewheeling diode and avoids the conduction losses during ON time since Mosfets have very low Rds. The operation of both top and bottom MOSFETs is synchronized with each other means when the top MOSFET is ON, the bottom MOSFET will be OFF and

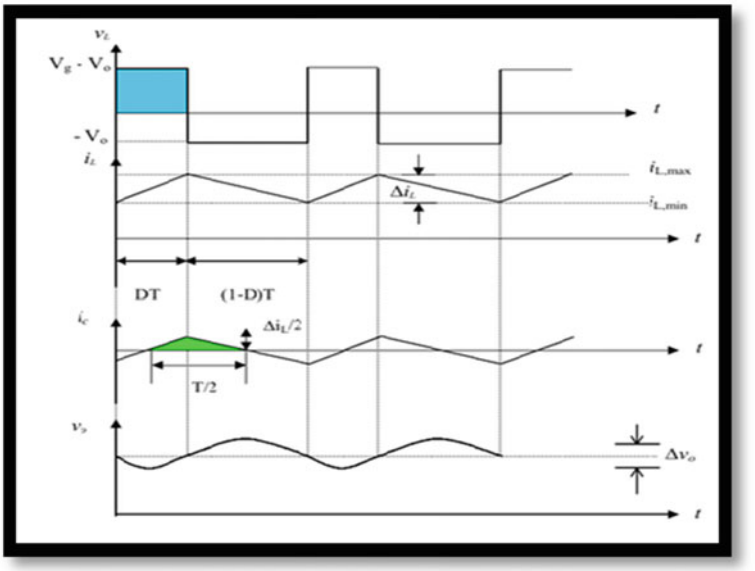

Fig. 2 Buck-converter waveforms

vice versa. So it is named as the synchronous Buck converter. Figures 3 and 4 explain the operation of the Synchronous Buck Circuit and waveforms.

Detailed Comparison of the Buck converter with the Schottky diode and Synchronous buck converter with MOSFET is compared in terms of cost, size and efficiency as explained in [1, 2]. Design and hardware implementation of the high efficiency Synchronous Buck Converter for Hi-Rel Application is explained in the subsequent sections. The proposed sync buck converter is used as high output voltage POLs (Point of loads) in space applications for subsystems.

4 Implementation of Synchronous Buck Converter

Converter is designed for the specifications given in Table 1.

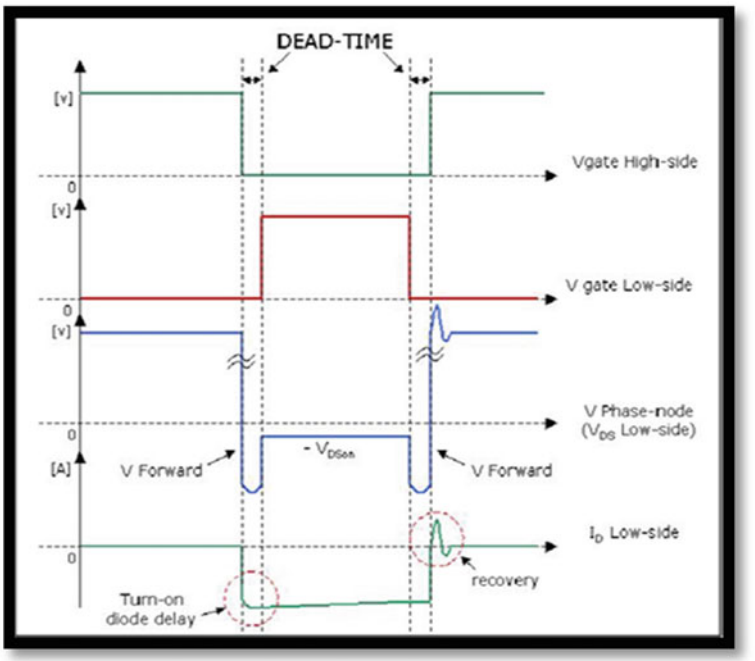

Fig. 3 Synchronous buck converter

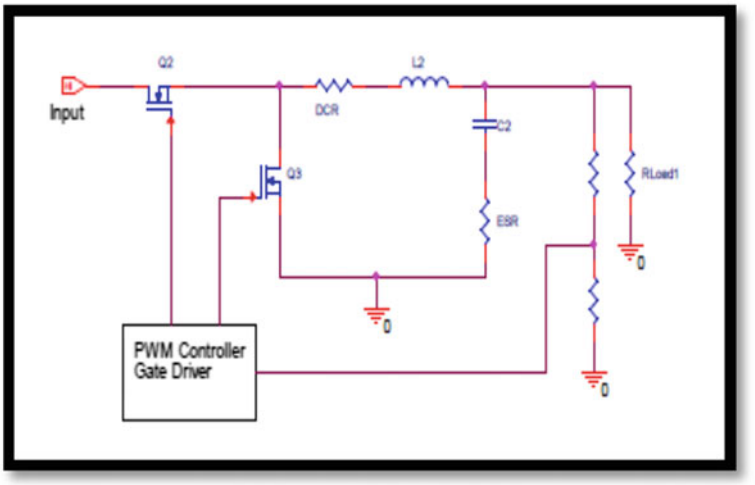

Fig. 4 Synchronous buck converter waveforms

Table 1 Specification

Parameter	Range
Input voltage	28–36 V
Output voltage	20 V
Output current	3.9 A
Efficiency	>96.5%
Switching frequency	200 kHz
Load regulation	<1%
Ripple	<1% of output voltage

4.1 Selection of Switching Device

Selection of the MOSFET depends on many parameters. Here, are few parameters which are very important while selecting a MOSFET [3].

- Maximum input voltage determines the Drain voltage (Vds) of the MOSFET.
- Switching losses because of higher Qg and Coss, Conduction losses because of Rdson.
- Size of the MOSFET depends on the output current capability and thermal properties.
- Cost of the MOSFET depends on the die size, package and production volume.

Losses in the Switching device play a major role to determine the efficiency of the converter. We will be discussing different losses as well in the switching devices. Conduction losses are because of the Drain source resistance in the top and bottom MOSFETs can be calculated using the below equations.

$$P_{COND(TOP)} = I_{OUT(MAX)}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$P_{COND(BOTTOM)} = I_{OUT(MAX)}^2 \times R_{DS(ON)} \times \frac{(V_{IN} - V_{OUT})}{V_{IN}} \tag{2}$$

Switching losses in the MOSFET are because of the rise and fall time which can be formulated as below.

$$P_{sw(TOP)} = \frac{1}{2} \times V_{in} \times I_{out} \times \left(t_r + t_f\right) \times F_{sw} \tag{3}$$

$$P_{sw(BOTTOM)} = \frac{1}{2} \times V_D \times I_{out} \times \left(t_r + t_f\right) \times F_{sw} \tag{4}$$

Loss generated by the output capacitance of the top and bottom MOSFET can be formulated as shown.

$$P_{coss(TOP)} = \frac{1}{2} \times \left(C_{oss_{TOP}}\right) \times V_{in}^2 \times F_{sw} \tag{5}$$

$$P_{coss(BOTTOM)} = \frac{1}{2} \times \left(C_{oss_{BOTTOM}}\right) \times V_{in}^2 \times F_{sw} \tag{6}$$

Loss due to charging the gate of the MOSFET is known as Gate Charge loss and can be calculated as below.

$$P_{G(TOP)} = \left(Q_{g_{TOP}}\right) \times V_{gs} \times F_{sw} \tag{7}$$

$$P_{G(BOTTOM)} = \left(Q_{g_{BOTTOM}}\right) \times V_{gs} \times F_{sw} \tag{8}$$

Total MOSFET losses can be concluded as below.

$$P_{TOP(TOTAL)} = P_{COND(TOP)} + P_{Tsw(TOP)} + P_{coss(TOP)} + P_{g(TOP)} \tag{9}$$

$$\begin{aligned} P_{BOTTOM(TOTAL)} = {} & P_{COND(BOTTOM)} + P_{Tsw(BOTTOM)} \\ & + P_{coss(BOTTOM)} + P_{g(BOTTOM)} \end{aligned} \tag{10}$$

4.2 Input Capacitor

Most of the designs concentrate only on output capacitors, whereas selection of the input capacitor also plays major role in the design of the Buck Converter. We will be seeing a large ripple current at the input side, which in turn leads to power dissipation in the capacitor, if we select high ESR Capacitor. This will reduce the efficiency of the converter. The ripple current will interact will ESL and cause voltage spike which leads to unwanted noise

$$C_{INB} = \frac{V_{OUT} \times I_{OUT(MAX)}}{\Delta V_{IN} \times f_S \times V_{IN(MIN)}} \tag{11}$$

4.3 Output Capacitor

The main function of the output capacitor is to maintain the output voltage and limit the output ripple voltage as per specification. The impedance of the capacitor determines the ripple voltage. Major parameters of impedance are equivalent series resistance (ESR), equivalent series inductance (ESL) and capacitance. Higher ESR

can cause higher power dissipation because of ripple current which will increase the internal temperature of the capacitor and will limit the aging of the capacitor and a higher ESL can cause ringing. So, a capacitor with lower ESR and ESL needs to be selected. From the basic equation of current through the capacitor the below capacitance equation can be formulated [4].

$$C_{out} = \frac{10^6}{8 \times F_{sw} \times \frac{\Delta V \times 10^{-3}}{\Delta I \times I_{out}} - ESR} \tag{12}$$

4.4 PWM Controller

PWM signals can be generated either by using the voltage mode or the current mode control. The Current Mode Control has advantages of faster response time, better gain bandwidth product and pulse by pulse current limiting.

LT3845 is a current mode controlled PWM IC. It has a programmable switching frequency and soft start. It has an input voltage range of up to 60 V and output voltage range up to 36 V. It has a better regulation accuracy and quiescent current and supply current during turn off as low as 120 μA and 10 μA, respectively [5].

4.5 Control Loop/Closed Loop Circuit Design

It is very important in a closed loop system to design the control loop of the converter [6–10]. Power stage open-loop transfer function is derived by small signal analysis and Type-3 compensation is implemented to obey the following stability conditions.

- DC gain is maintained at large to minimize the steady-state error between the reference voltage and output.
- To maintain less error amp ripple or output ripple at the switching frequency, DC Gain at the switching frequency is maintained small enough.
- At cross-over frequency, open loop power stage phase shift lags by 180° as shown in Fig. 5**.** The feedback loop is designed to achieve a phase margin of more than 45° and bandwidth of more than 10 kHz.

Bode Plot graph for a power stage of a Buck converter is shown in Fig. 5.

Bode plot of the designed synchronous buck converter is shown in Fig. 7 the Gain margin is −14.389 dB, the Phase margin is 68.047° and the gain cross-over frequency is 14.3 kHz.

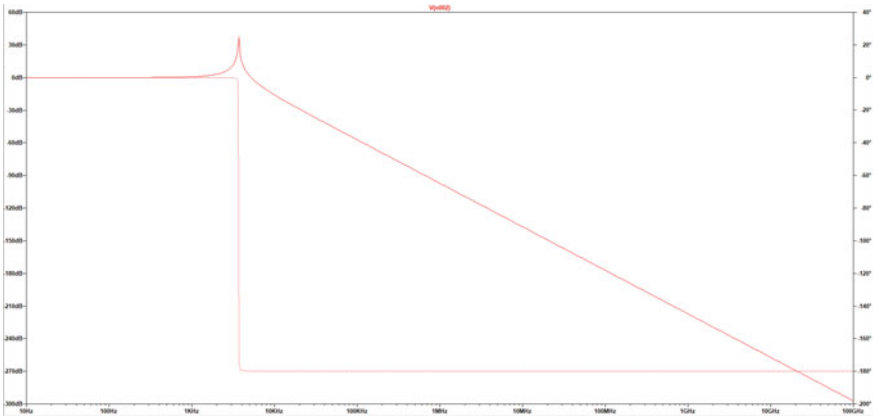

Fig. 5 Open loop frequency response of buck converter power stage

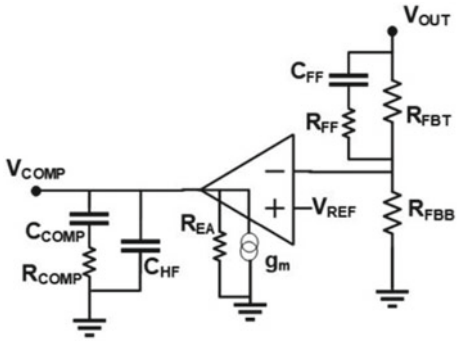

Fig. 6 Schematic of Type III error compensation network

4.6 Programming the Switching Frequency

Decision of the operating frequency gives us a conundrum of the trade-off between efficiency and size. Lower switching frequency reduces the losses in the converter but increases the size of the converter. Higher switching frequency reduces the size but increases the losses and affects the efficiency. Considering this, to achieve the required efficiency in the proposed converter, the controller switching frequency is programmed for 200 kHz by using a single resistor from the Fset pin to the ground

$$Rset = 8.4 \times 10^4 \times f_S^{(-1.31)} \tag{13}$$

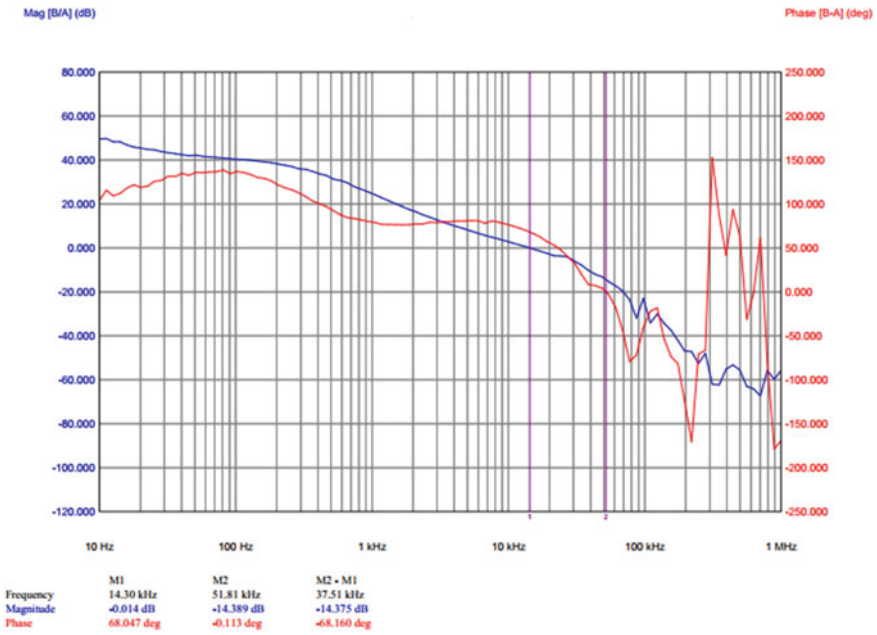

Fig. 7 Bode plot of the proposed converter

4.7 Programmable Current Sense

The current sense resistor, R_{SENSE} is the programmable current sense that depends on the maximum required load current. The sense resistor acquires feedback from the current through the inductor. The maximum threshold of the selected IC is 100 mV. Hence the peak current in the inductor will be 100 mV/R_{SENSE}. The maximum output load current (Iout(max)) is the difference of the inductor peak current and 50% of the ripple current peak, ΔIL.

R_{SENSE} can be calculated by providing enough margin for the ripple current and component tolerances and is given by Eq. (14).

$$R_{SENSE} = \frac{70\text{mV}}{I_{OUT(MAX)}} \tag{14}$$

4.8 Programmable Soft-Start

Soft start capacitor controls the rate of rise of output voltage. It also regulated input inrush current and output voltage overshoot. Soft start capacitor is charged by an

internal 2 μA reference. If feedback pin voltage exceeds the threshold of soft start pin voltage, Dc control voltage is lowered resulting in the reduction of inductor current. This decreases the rate of rise of output voltage. The desired soft-start time (tss) is programmed via the Css capacitor as in Eq. (15)

$$Css = \frac{2\mu\text{A} \times t_{SS}}{1.231\text{V}} \tag{15}$$

4.9 Output Inductance

The key parameters accountable for the selection of the Inductor are Volt-second product, Peak saturation current, RMS current and minimum inductor size required. For a given, the minimum inductance value for a given in the equation below in Eq. (16).

$$L \geq V_{OUT} \times \frac{\left(V_{IN(MAX)} - V_{OUT}\right)}{f_S \times V_{IN(MAX)} \times \Delta I_L} \tag{16}$$

5 Simulation

Simulation of the synchronous buck converter using LT3845 has been as shown in the Fig. 8 and results are shown below.

The input supply range is changed from 28 to 36 V at Minimum load to Maximum load conditions. The efficiency and Load regulation are tabulated in Tables 2 and 3.

5.1 Simulation Results

Synchronous buck converter simulation is done, and waveforms are presented in Fig. 9. Figure 9a–e shows the Top and Bottom MOSFETs gate waveforms, Top and Bottom MOSFETs drain waveforms, and output Ripple voltage waveform, respectively.

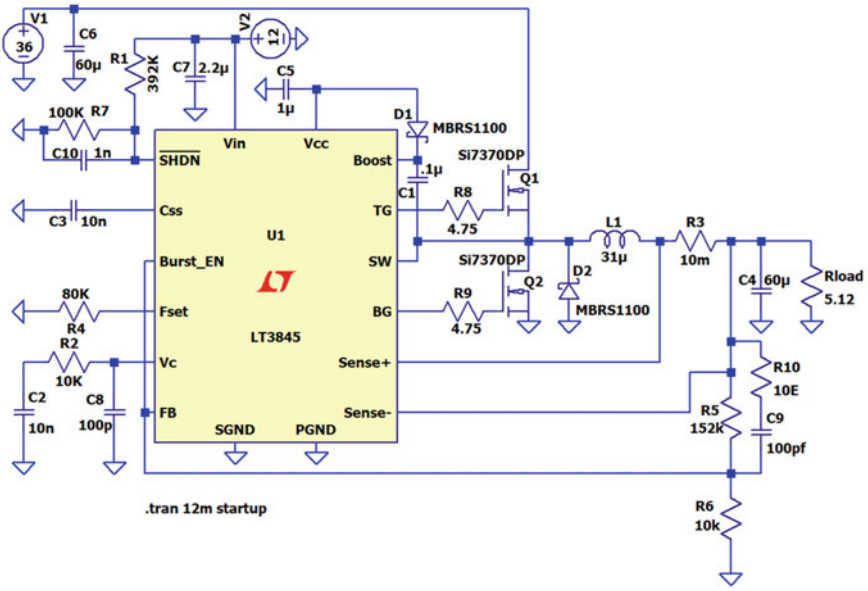

Fig. 8 Simulation of synchronous buck converter using LT3845

Table 2 Load regulation for synchronous buck converter

Vin in volts	Output voltage in volts		Load regulation
	No load	Full load	
28	20.08	20.07	0.01
33	20.08	20.07	0.01
36	20.09	20.08	0.01

Table 3 Efficiency for synchronous buck converter in simulation

Input voltage (V)	Input current (A)	Voltage	Current	Efficiency (%)
28	2.94	20.07	3.9	95.04
33	2.49	20.07	3.9	95.21
36	2.28	20.08	3.9	95.31

6 Hardware Results

Synchronous buck converter hardware assembly is done, and the test results are as shown in Tables 4 and 5.

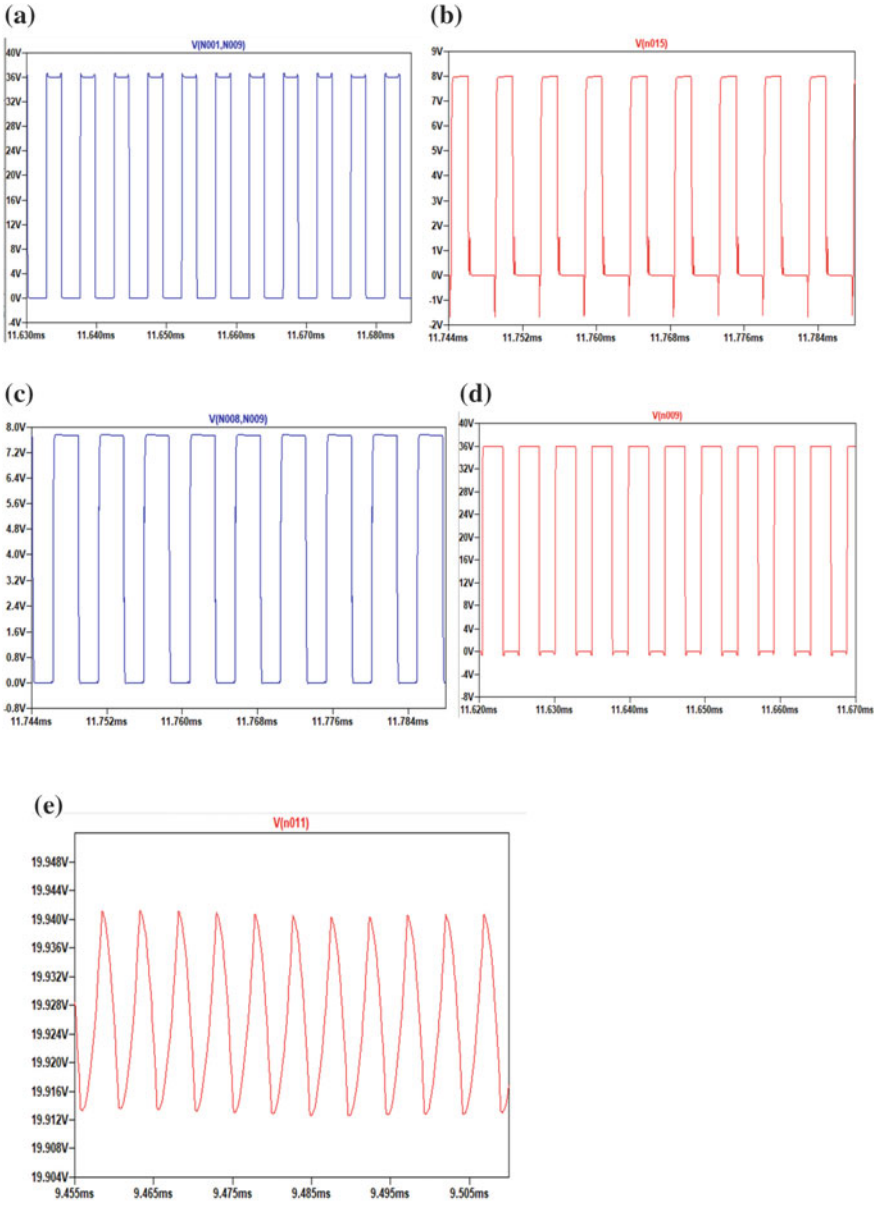

Fig. 9 **a** Top MOSFET gate waveform. **b** Bottom MOSFET gate waveform. **c** Top MOSFET drain waveform. **d** Bottom MOSFET drain waveform. **e** Ripple voltage

Table 4 Load regulation for converter

Input voltage (V)	Output voltage @ no load (V)	Output voltage @ full load (V)	Load regulation (%)
28	20.059	20.043	0.060
33	20.059	20.046	0.065
36	20.058	20.046	0.060

Table 5 Efficiency for synchronous buck converter in practical condition

Input voltage (V)	Input current (A)	Output voltage (V)	Output current (A)	Efficiency (%)
28.03	2.867	20.043	3.9	97.26
33.05	2.441	20.046	3.9	96.92
36.01	2.245	20.046	3.9	96.69

Practical waveforms are presented in Fig. 10. Figure 10a, b shows the Top and Bottom MOSFETs gate waveforms respectively. Figure 10c, d shows the Top and Bottom MOSFETs Drain waveforms respectively. Figure 10e shows the output Ripple voltage waveform.

7 Conclusion

High Voltage and Current mode controlled high efficiency synchronous buck converter is designed with an output voltage of 20 V/3.9 A using LT3845 Synchronous step-down controller IC. Results are verified by comparing the simulation model and hardware model having output of 20 V/3.9 A with an input voltage range of 28–36 V. Efficiency of up to 97% is achieved in addition to very good load regulation accuracy of <1% and output ripple voltage of <1% achieved successfully.

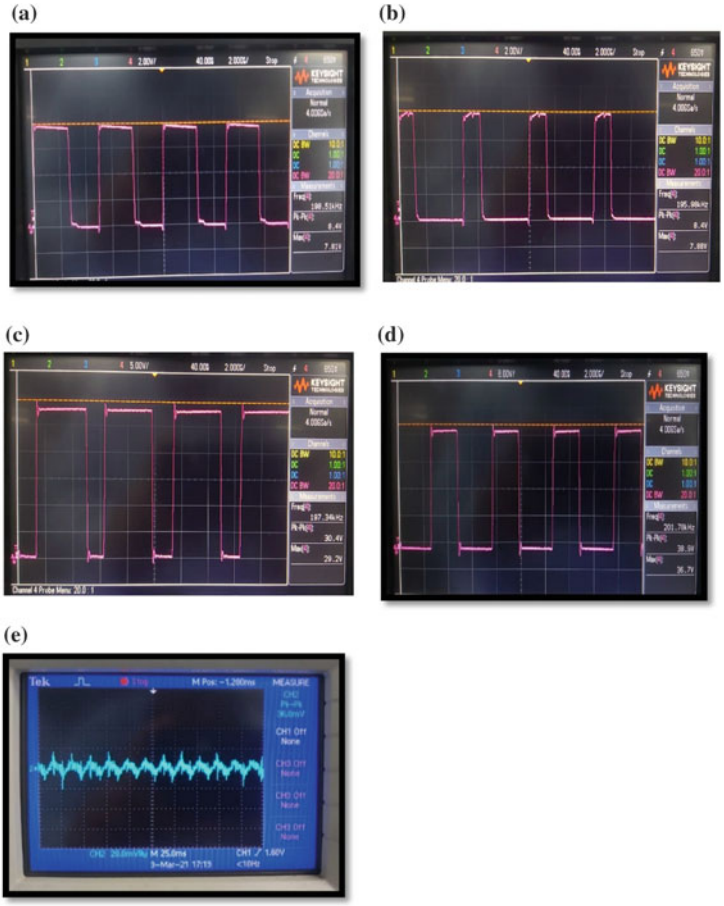

Fig. 10 Practical results. **a** Top MOSFET gate waveform, **b** bottom MOSFET gate waveform, **c** top MOSFET drain waveform, **d** bottom MOSFET drain waveform, and **e** ripple voltage waveform

Acknowledgements We are grateful to Mr. Mallavarapu Apparao, Managing Director, Centum Electronics Limited, Bangalore for his encouragement and constant support for this work.

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Design and Implementation of 32 W Dual Output Forward Converter with Bias Feedback for Spaceborne Systems

S. Pradeep, T. K. Nagaraju, Bhoopendra Kumar Singh, and Vinod Chippalakatti

Abstract This paper is focused on the hardware implementation of a forward converter with feedforward, voltage mode control topology, Bias feedback technique and coupled inductor for better load and cross regulations were used. This converter will operate at 500 kHz switching frequency and uses UC2825 PWM controller which can operate both in voltage and current mode control. PWM controller has better soft start, maximum control on duty, under voltage and higher frequency operation. A dedicated winding is provided for feedback which will also power up the control circuitry. It has protections such as under voltage and over power. The proposed converter is a very highly reliable one and will be used for space applications.

Keywords Switched mode power supply · Forward converter · Feedforward voltage technique

1 Introduction

Nowadays Switched mode power converters are widely used because of the reduced size and high efficiency compared to liner power supplies. SMPS has some other advantages like reduced weight, low power dissipation. Some of the applications of switched mode power supplies include battery charger, lighting, defense, aerospace, and other electronic devices [1]. One of the widely used converter in DC–DC converter is the Forward converter. To implement all of the above, the feed forward voltage control mode is used.

DC–DC converters are extensively utilized to get better regulated output, electrical isolation, and multiple output. Forward converters use transformers to increase or decrease the output voltage (depending on the transformer turns ratio) and they will provide a galvanic isolation to transfer energy from the source to the load [2]. They have multiple output windings, so it is possible to provide both higher and lower voltage outputs simultaneously.

S. Pradeep (✉) · T. K. Nagaraju · B. K. Singh · V. Chippalakatti
Centum Electronics Ltd., Bengaluru, India
e-mail: pradeeps@centumelectronics.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_7

In this paper we will also be discussing about the design of the feedforward forward converter, coupled inductor and bias feedback technique. Usually to control the output feedback needs to be provided which will be from secondary, but we will be using bias/auxiliary winding as the feedback [3].

2 Converter Specification

32 W Dual output DC–DC Converter is designed for the following specifications:

Input voltage range: 24–46 V
Switching frequency: 500 kHz
Output parameters: 3.8 V/4 A, 5.6 V/3 A
Efficiency: ≥75%
Line regulation: <1%
Load regulation: ≤3%
Ripple and noise: <50 mV
Load transient: <100 mV
Overpower protection: >150%

2.1 Block Diagram

Figure 1 represents the block diagram of 32 W Dual output DC–DC Converter.

Figure 1 shows the block diagram of the forward converter and operation of all circuitries involved in the forward converter.

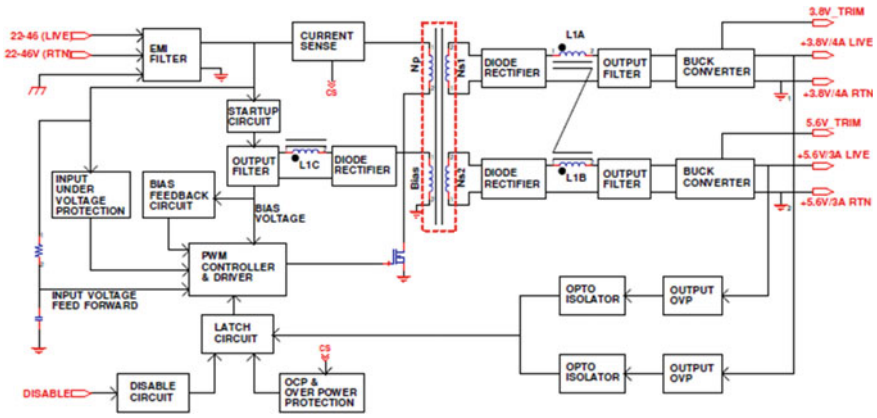

Fig. 1 32 W dual output DC–DC converter block diagram

EMI filters are designed and placed at the input section near to the input connector to meet the EMI/EMC requirements. 5 kHz cut-off frequency (1st order) is the requirement for input filtering. 1 stage Common Mode filter (CM Filter) is considered in this design for a nominal input current of 3 A to eliminate the common mode noise and meet the EMI/EMC requirement. Differential Mode filter (DMI filter) is to eliminate Differential Mode noise and meet the EMI/EMC requirement. When MOSFET is ON current flows from primary of transformer and energy is coupled to the secondary. Secondary voltage will be rectified by diode rectifier and goes through a low pass filter to reduce the ripple amplitude of the output voltage.

The start-up circuit will help PWM to turn on MOSFET initially. Once the MOSFET is conducting, the forward transformer will be energized resulting in the regulated output at the bias winding. Bias winding also called as House Keeping winding will power the auxiliary circuits such as PWM, Control and Protection circuits. Bias voltage is kept more than the start-up voltage. Bias winding voltage is used for feedback an appropriate voltage divider circuit to regulate the output voltages within specified level. Input UVP (Under Voltage protection) circuit is designed around 22 V with 2 V hysteresis. i.e., once the circuit is ON, the turn OFF will occur @ 22 V during under voltage condition whereas the turn ON threshold will be around 24 V. Input OPP (Overpower protection) circuit is designed for more than 150% i.e., at a minimum input voltage, OPP will trigger at 155% of the nominal power whereas the maximum input voltage OPP will trigger at 160% of the nominal power.

3 Design Consideration

3.1 Conventional Forward Converter

The Forward converter transfers energy instantly from primary to secondary and does not rely on the Forward transformer for energy storage. Utilization of the transformer can be increased by having better magnetizing inductance and no air gap. Transformers need to be provided with reset to avoid saturation. Secondary side LC filter ensures a lower ripple voltage. Figure 2 shows the circuit of the generalized forward converter. When MOSFET ‘M’ is turned on the primary winding is applied with input voltage. Based on the number of turns secondary voltage will be reflected and rectified through the diode and passed to the low pass filter than to the load [4]. When MOSFET ‘M’ is turned OFF primary winding is opened, and the current through both primary and secondary becomes zero. The freewheeling diode provides path for the magnetic current with the help of a tertiary winding. It is because when the MOSFET is OFF a huge voltage will be developed across the primary winding which needs to be dissipated. This can be done using one more winding which reduces power loss. It is also called Reset winding.

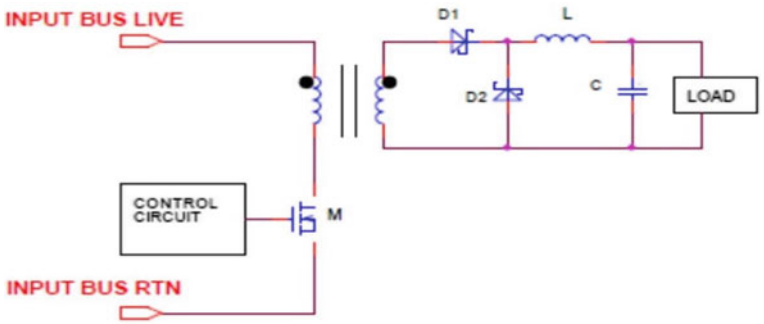

Fig. 2 Generalized forward converter

3.2 *Selection of Transformer*

The two major selection criteria for transformers are power handling capacity and area product of the transformer (Eq. 1). Here, we are calculating the area product for the forward converter and selecting the core accordingly [5, 6].

$$A_P = \frac{\left(\sqrt{D_{max}} \times P_{OUT} \times \left(1 + \frac{1}{Eff}\right)\right)}{K_W \times J \times 10^{-6} \times B_M \times F_{SW}} \tag{1}$$

Once the area product is calculated, core is selected along with the number of turns required, turns ratio needs to be calculated. Primary, Bias, and Secondary number of turns will be calculated as follows (Eqs. 2–4).

$$Np = \frac{Vin\ \min \times D\ \max}{Ac \times 10^{-6} \times B_M \times F_{SW}} \tag{2}$$

$$Ns = (Vout/Vbias) \times Nbias \tag{3}$$

$$Nbias = \text{Turns ratio} \times Np \tag{4}$$

Proposed converter operates at maximum duty cycle of 50% with efficiency more than 70%.

3.3 *Feedforward Voltage Technique*

When a closed loop control system is involved to control the output, we need to sense the output voltage and compare it with a reference voltage. Error voltage generated will be compared with a fixed ramp and will be fed back to PWM controller IC to

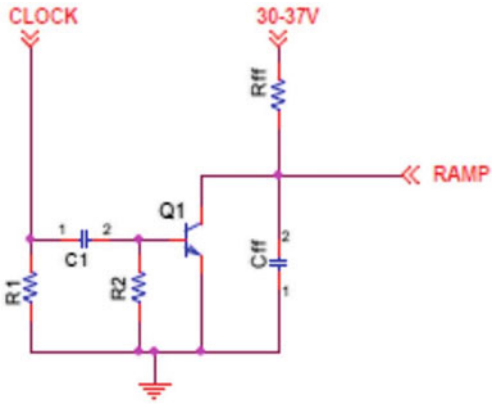

Fig. 3 Feedforward topology

change the duty cycle accordingly. Sensing the output voltage with change in load and feeding the signal to the primary controller will increase the response time of the system or the converter [2]. Figure 3 shows the circuit of the feedforward topology.

When supply on the capacitor is charged through supply and when the clock pulse is high, the transistor is turned on and the capacitor is discharged through the transistor. This changes the slope of ramp with change in input voltage. This ramp voltage is compared with error voltage and which in turn changes the duty cycle of PWM pulses. Hence, it makes the system respond faster with change in input [7].

Coupled inductor is like the transformer but based on the application in which it is used it is named as the coupled inductor. Major applications where it is used are Forward, Flyback and SEPIC converters. In multi-output DC–DC converter coupling of inductors will act as the filter and improved cross regulation and ripple current. It also has a lower leakage inductance. In our design we are using the coupled inductor for bias and output. Since bias is a control circuitry for output, we have one output of 3.8 V/4 A, second output of 5.6 V/3 A and bias output is 12 V/0.05 A. Design steps for coupled inductors are like calculating a filter inductor and are as follows: Area product of the coupled inductor is calculated as shown below (Eq. 5).

$$\mathrm{Ap} = \frac{L \times \left(Iout \times \left(1 + \frac{K}{2}\right)\right)}{\mathrm{Kw} \times \mathrm{Bm} \times \mathrm{J} \times 10^{-6}} \tag{5}$$

Number of turn's calculations (Eq. 6).

$$\mathrm{N} = \frac{L \times \left(Iout \times \left(1 + \frac{K}{2}\right)\right)}{\mathrm{Ac} \times 10^{-6} \times \mathrm{Bm}} \tag{6}$$

As bias winding is coupled with the output inductor, we need to calculate the bias winding inductor also. It can be linked based on the number of turns of the primary and secondary.

$$\text{Nbout} = \text{Nb/Ns1} \times \text{Np} \tag{7}$$

4 Hardware Results

The test is carried out ambient, negative temperature of −40° and positive temperature of +75°. The test results at full load condition and half load condition are disclosed in a tabular form. Also, ripple voltage and efficiency values are tabulated in the tables below. Experimental readings of the converter are shown below. From Figs. 4 and 5, we observe drain voltage stress across the MOSFET during the OFF period which is less than the designed value. We observe less ringing which is due to snubber resistor and capacitor. Figures 6 and 7 show the ripple voltage of the output which is less than the specifications designed (Tables 1 and 2).

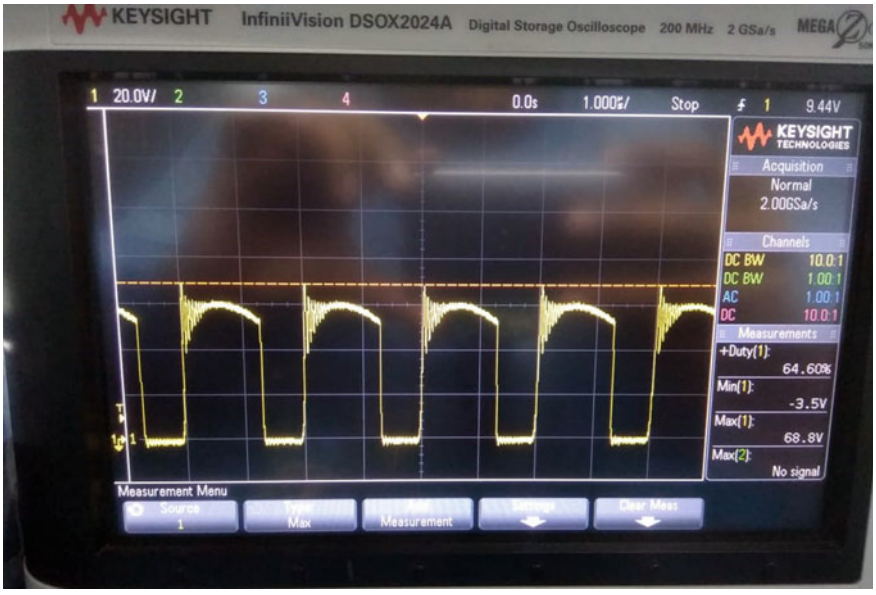

Fig. 4 Drain source voltage of MOSFET at 37 V

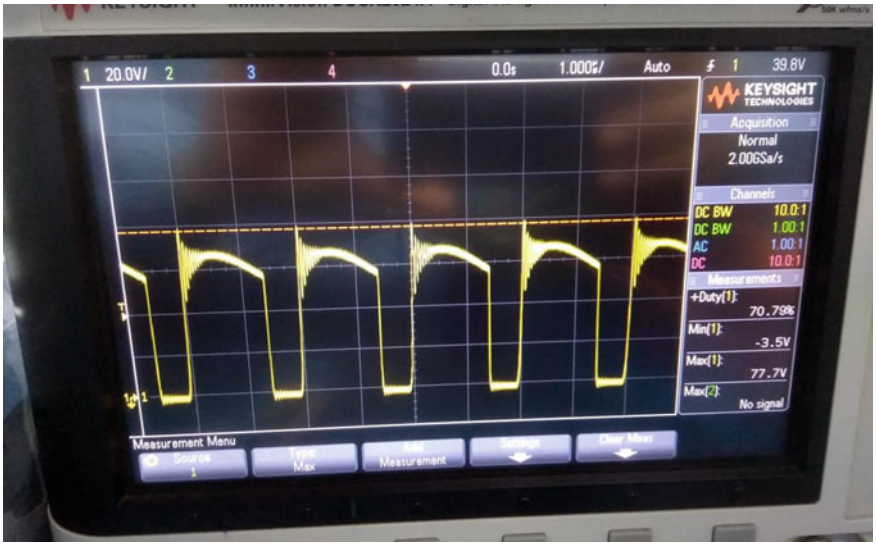

Fig. 5 Drain source voltage of MOSFET at 45 V

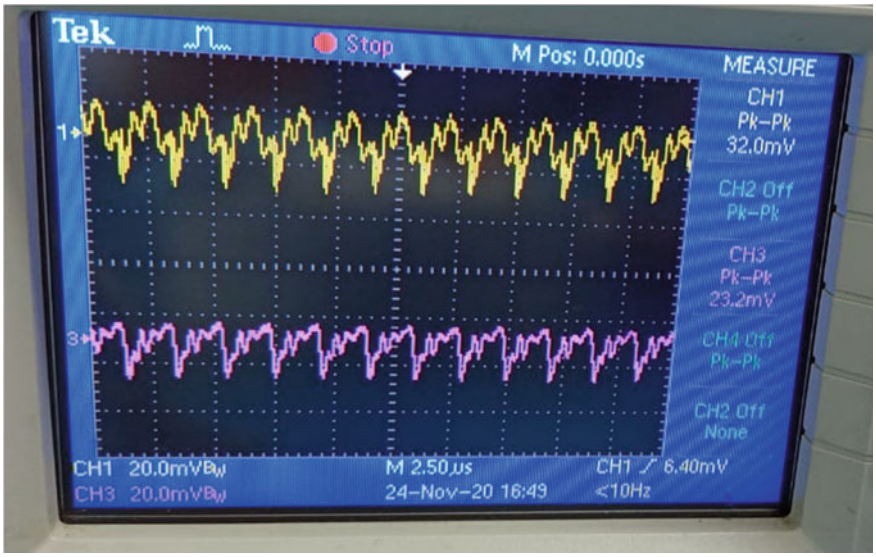

Fig. 6 Ripple at 37 V @full load

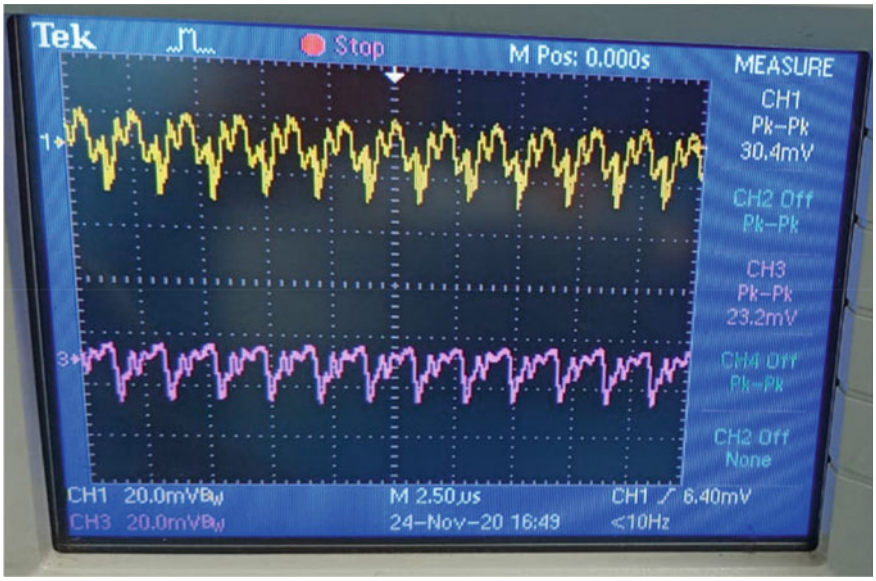

Fig. 7 Ripple at 45 V @full load

Table 1 Efficiency at 50% load

Vin (V)	Iin (A)	Vout1 (V) (3.8 V)	Iout1 (A)	Ripple voltage (mV)	Vout2 (V) (5.6 V)	Iout2 (A)	Efficiency (%)	Ripple voltage (mV)
24	0.969	3.818	2	31.2	5.597	1.5	68.82	21.6
37	0.632	3.822	2	30.4	5.605	1.5	68.37	22.4
46	0.520	3.827	2	29.6	5.611	1.5	66.78	21.6

Table 2 Efficiency at 100% load

Vin (V)	Iin (A)	Vout1 (V) (3.8 V)	Iout1 (A)	Ripple voltage (mV)	Vout2 (V) (5.6 V)	Iout2 (A)	Efficiency (%)	Ripple voltage (mV)
24	1.770	3.818	4	32.8	5.597	3	75.30	23.2
37	1.15	3.822	4	32.0	5.605	3	75.22	23.2
46	0.922	3.827	4	30.4	5.611	3	75.49	26.1

5 Conclusion

The proposed Forward converter is designed, implemented as a hardware, and tested under all environmental conditions. The converter is meeting all the necessary electrical specifications in the input voltage range of 24–46 V. The converter is tested in

the temperature range from −40 to +70 °C and decided based on the requirement. The converter performance has features of low ripple voltage, better line regulation and good load transient response. Protection against under voltage, short circuit and input over power is provided to improve the reliability of the power supply. The converter is having a maximum efficiency of 76% at the nominal load and 82% at the maximum load.

Acknowledgements We are grateful to Mr. Mallavarapu Apparao, Managing Director, Centum Electronics Limited, Bangalore for his encouragement and constant support for this work.

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Design and Implementation of High Frequency Single Output Forward Converter for Space Application

M. R. Ramkumar, C. V. Bhanuprakash, Bhoopendra Kumar Singh, and Vinod Chippalakatti

Abstract Forward Converter topology is very much favored for designing Power Supply Units in space applications, due to its modest structure and the nature of imparting perfect isolation between the input and output. The proposed converter is designed using single switch forward converter topology operating at 500 kHz. A continuous and regulated output of 5 V/8 A is generated from an input range of 18–50 V using voltage mode control through magnetic isolation along with the input voltage feed forward technique. Lossless snubber is incorporated to improve the core reset process. Converter efficiency is greater than 75% at full load. Inhibition and protection circuits are incorporated. The complete converter is also realized using hybrid microcircuit technology in addition to PCB.

Keywords Hybrid · Inhibit · Efficiency · Lossless snubber · Voltage feed forward · Magnetic isolation

1 Introduction

Forward Converter topology is very much favored for designing Power Supply Units in space applications, due to its modest structure and nature of imparting perfect isolation between the input and output. Multiple outputs can be implemented easily. Forward converter has high current carrying capabilities which is an added advantage to use this topology from lower to medium power applications. There is absence of right half plane zero in transfer function unlike in fly back. This paves the way for easier design of the control loop of the forward converter [1].

Transformer design comprises of 2 major constraints. Since DC voltage is applied to the transformer through a switch (MOSFET), an appropriate track is required for energy dissipation to reset the core. Otherwise the core will saturate and the converter will start to malfunction. Along with this, leakage inductance of the transformer comes into picture. Since primary MOSFET drain voltage is already twice the input

M. R. Ramkumar (✉) · C. V. Bhanuprakash · B. K. Singh · V. Chippalakatti
Centum Electronics Ltd., Bengaluru, India
e-mail: ramkumarmr@centumelectronics.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_8

voltage, leakage inductance will be added as spike which may sometimes cause MOSFET to cross its reverse drain voltage ratings. So considering all these summed up voltages, a high rated switch will be selected. A lossless or non-dissipative snubber is adopted along with the RCD snubber to re-circulate the stored energy and enhance efficiency [2].

Conventional technique of obtaining multiple output involves linear regulators. The vital drawbacks of this include cost, size and power loss. Linear regulators occupy more space and corresponding IC's are expensive. Linear regulators are best suited for low voltage drop specification [3].

The Forward Converter is a gleaned from BUCK Converter; so the design principle for the secondary LC filter follows the buck derivations. In this paper, a continuous and regulated output of 5 V/8 A (40 W) is generated from an input range of 18–50 V using input voltage feed forward technique along with magnetic isolation. Two levels of type-3 and 1 level of type-2 controllers are adopted to enhance the loop stability.

2 Forward Converter Working Principle

A forward converter with lossless snubber is adopted in this converter. To maximize the efficiency along with the LCD snubber, a parallel combination of the output rectifier diodes is incorporated to reduce on time voltage drop across diodes. Due to the presence of both RCD and LCD snubber, a significant amount of leakage inductance is reduced, which in turn reduces voltage stress across MOSFET [4].

Figure 1 depicts the configuration of the single switch forward converter topology. This topology has 2 modes of operation which is explained below.

MODE 1: Switch M1 is closed. It's depicted in Fig. 2.

In this mode, switch M1 is turned on. The input current flows through the primary windings of the main transformer. Core will be magnetized and voltage will be generated on the secondary winding. Forward diode D1 will be biased. This will energize the output inductor and current in it will rise. This will supply the load.

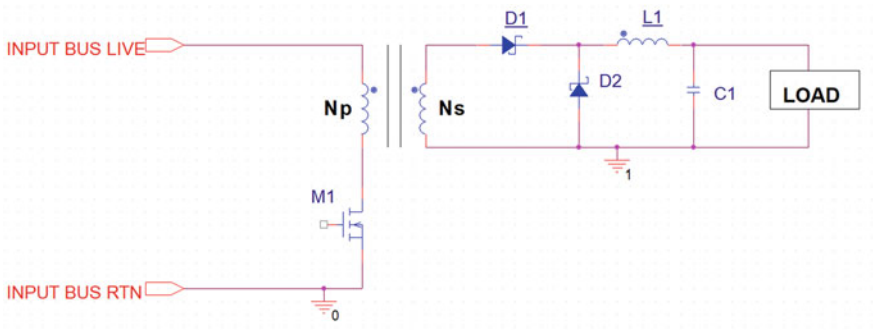

Fig. 1 Forward converter topology

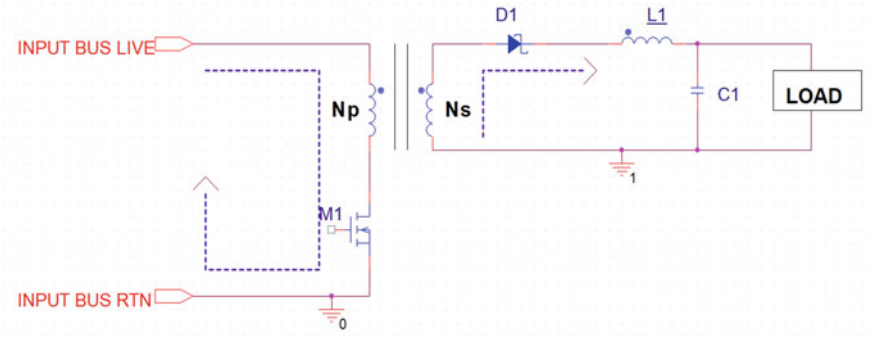

Fig. 2 MODE-1 operation

Ferrite core is used for the main transformer and Inductor realized using the powder core. The powder core will give an inherent air gap which is essential to control the loop [5].

MODE 2: Switch M1 is opened. It's depicted in Fig. 3.

In this mode, switch M1 will be turned off. The freewheeling diode gets forward biased. The stored energy in the output inductor will circulate through the load [5]. The residual energy in the transformer during this cycle needs to be removed; otherwise this energy gets accumulated in each cycle and the core will saturate. RCD snubber is incorporated to dissipate this residual energy. Secondary diodes also consist of snubbers to reduce secondary diode stress caused due to leakages in the reflected secondary voltage.

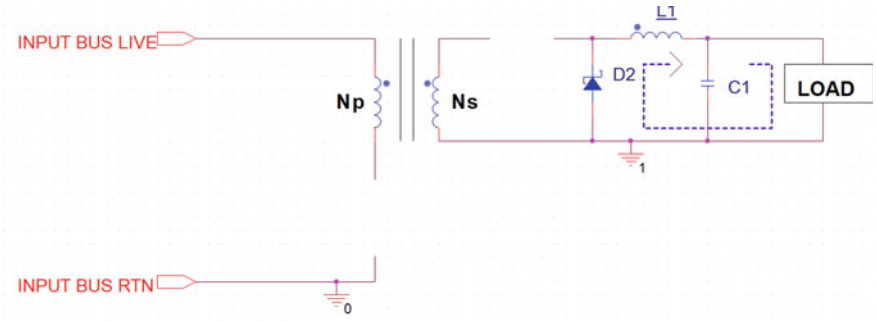

Fig. 3 MODE-2 operation

2.1 Proposed System

The proposed system incorporates single switch forward converter topology. Input voltage from 18 to 50 V is applied through the CMI and DMI filtering circuit. An auxiliary 11 V bias voltage is supplied to power up the control circuit ICs.

Once the control circuit turns on, the transformer will get coupled and produce raw output voltage at the secondary side. A part of the output voltage is injected to the feedback generator circuit. The output of the generator is magnetically separated, rectified and applied to Pulse generating IC. This error signal is compared with ramp voltage to produce the gate pulse. A high current driver is used to boost the gate pulse signals. This boosted signal is used to drive MOSFET to produce a regulated 5 V output. The system consists of 2 levels of type 3 controllers to adjust loop response. Additionally, feed forward technique is adopted to dynamically alter the ramp according to changes in the input voltage.

Parallel combination of the output forward and freewheeling diodes is encompassed to reduce on stage voltage drop due to high output current. This helped to improve the efficiency. Along with this protection circuits are implemented for voltage and current protection of the converter from surge, spikes and deviations. The proposed system is depicted in Fig. 4.

Table 1 provides the list of blocks and their corresponding function in the proposed system.

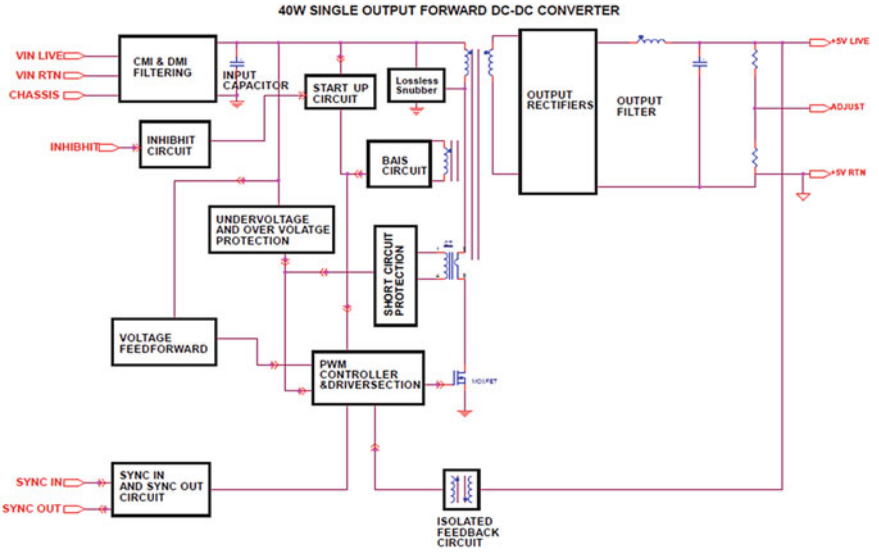

Fig. 4 Block diagram of the proposed system

Table 1 Blocks and functions of the proposed system

Blocks	Functions
CMI and DMI filter	For reducing the conducted emission from the equipment
PWM controller	PWM signal generation
Inhibit circuit	To turn off converter externally
Startup circuit	To produce bias voltage for initial cycles of PWM signal generation
Output rectifier and filter circuit	To obtain pure DC signal and eliminate voltage ripple content
Gate driver	Power MOSFET driver IC with high current and high voltage ratings
OVP/UVP and OCP circuit	To protect converter from input voltage deviations and output current variations
Bias circuit	Continuous voltage supply for PWM IC, gate driver and protection circuits
Isolated feedback	To provide magnetic isolation between primary and secondary
Voltage feed forward	Circuit to adjust ramp as per input voltage variations
Lossless snubber	Used to reset or recirculate the absorbed energy
Sync in circuit	To change converter operating frequency as per external injection

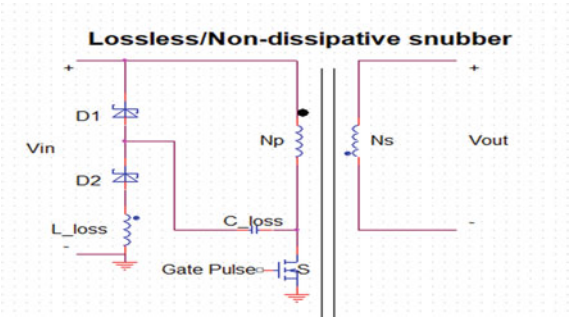

Fig. 5 Lossless snubber circuit

2.2 Lossless Snubber (Non-dissipative Snubber)

Figure 5 shows the LCD snubber circuit adoption in the DC–DC converter.

The above figure depicts implementation of the lossless snubber in the converter. The energy stored in the snubber capacitor (C_loss) will be re-circulated through the switch and the inductor (L_loss) in the next cycle.

The criteria to achieve better snubber design and enhance efficiency are:

1. C_loss > Coss

   Where Coss = MOSFET common source output capacitance.

   Snubber reset time < MOSFET off time.
2. L_loss will be sum of primary inductance and leakage inductance. Off time of MOSFET will be considered at maximum duty cycle. Based on these values snubber capacitance will be calculated [6].

3 Forward Converter Specification and Design

The specifications of the proposed converter are as follows:

Minimum input voltage	18 V
Nominal input voltage	28 V
Maximum input voltage	50 V
Output voltage	5 V
Output current	8 A
Switching frequency	500 kHz
Maximum duty cycle	0.64
Input over voltage protection	53 V
Input under voltage protection	15.5 V
Over current protection	10.4 A (130%)
Maximum transient voltage	300 mV
Maximum ripple voltage	50 mV
System efficiency	>75%

3.1 Power MOSFET Selection

Due to magnetic leak energy, the voltage stress seen across MOSFET will be always be twice the maximum input voltage. Considering the de-rating factor also, 250 V rating MOSFET is selected.

Selected: BUY25CS12J, 250 V, 12 A@25 °C, 0.130 Ω and TO-220 package.

3.2 Rectifier Diode Selection

Rectifying diodes will be affected by both the reflected voltage on the secondary side and pulsed current.

Selected: 16CYQ100C, 100 V and 16 A.

3.3 PWM Controller IC Selection

The converter switching frequency is 500 kHz.

Selected IC: UC2825 [7].

Make: Texas Instruments.

It is a radiation hardened space grade component. In order to calibrate the desired switching frequency, RT and CT pins of PWM are tuned, by choosing the CT value from the datasheet for specific temperatures and the corresponding RT value is calculated.

The PWM IC has inbuilt error amplifier and ramp generator. The error voltage is compared with the ramp signal. If the error signal is more PWM IC output will be high else low. Thus, it produces variable width pulses [8].

4 Results and Waveforms

Figure 6 shows the PCB placement of the components.

The test is performed at ambient, negative temperature (−40 °C) and positive temperature (+85 °C). The test results at full load condition are tabulated below.

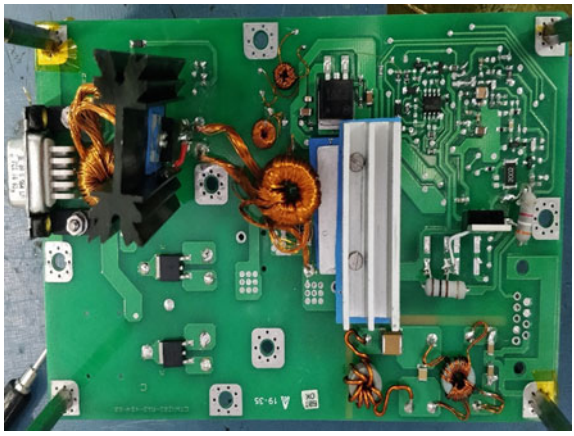

Fig. 6 Forward converter placement

In addition, line regulation, load regulation, efficiency and loop response data are tabulated below.

4.1 Experimental Status

The hardware experimental results are logged below at full load condition (8 A).
Table 2 depicts converter efficiency at different temperature conditions.
Tables 3 and 4 provide converter line and load regulation data, respectively.
Table 5 provides loop response of the converter.

Table 2 Converter efficiency at different thermal conditions

A: room/ambient temperature			
Input voltage (V)	Input current (A)	Output voltage (V)	Efficiency (%)
18	2.784	5.012	80.0
28	1.785	5.011	80.2
50	1.045	5.011	76.7
B: −40 °C (negative temperature cycle)			
Input voltage (V)	Input current (A)	Output voltage (V)	Efficiency (%)
18	2.751	4.994	80.7
28	1.773	4.995	80.5
50	1.018	4.996	78.5
C: +85 °C (positive temperature cycle)			
Input voltage (V)	Input current (A)	Output voltage (V)	Efficiency (%)
18	2.784	5.027	80.3
28	1.771	5.027	81.1
50	1.071	5.027	79.1

Table 3 Converter line regulation

Input voltage (V)	Load condition (%)	Line regulation (10 mV)
18	10	0
	100	1
50	10	0
	100	0

Table 4 Converter load regulation

Input voltage (V)	Output voltage: 5 V(25 mV)
18	1
28	0
50	1

Table 5 Converter loop response at nominal input voltage

VIN = 28 V			
Load condition (%)	Cross-over frequency (Fc)	Gain margin (GM) (dB)	Phase margin (PM) (degree)
10	1.70	41.93	92.41
100	11.58	28.75	73.79

4.2 Waveforms

The drain voltage, output diode stress, ripple voltage and load transient are captured using DSO at nominal voltage and full load condition.

Also bode plot captured using the AP300 instrument at nominal voltage and full load condition.

Figures 7 and 8 depict MOSFET and diode stress, respectively.

Figures 9 and 10 depict ripple voltage and load transient at full load, respectively.

Figure 11 depicts loop response of the converter at 28 V full load.

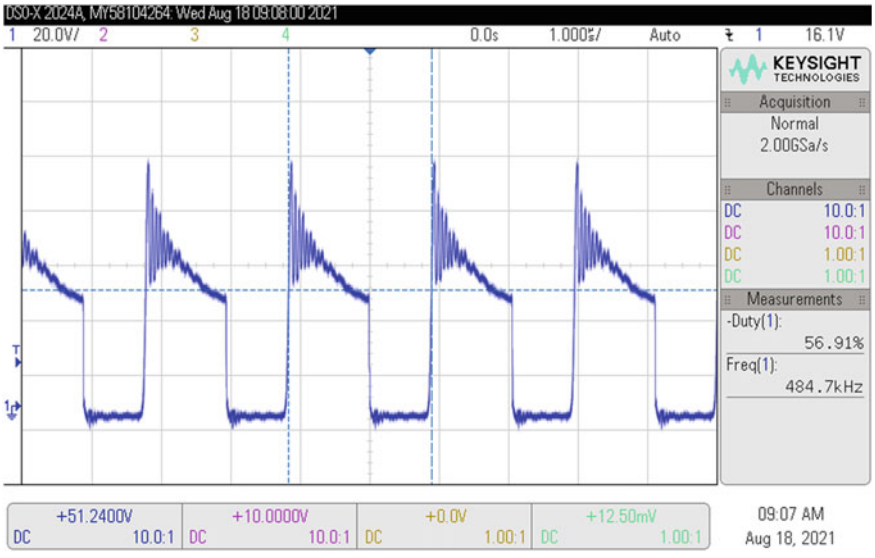

Fig. 7 MOSFET drain voltage at 28 V full load

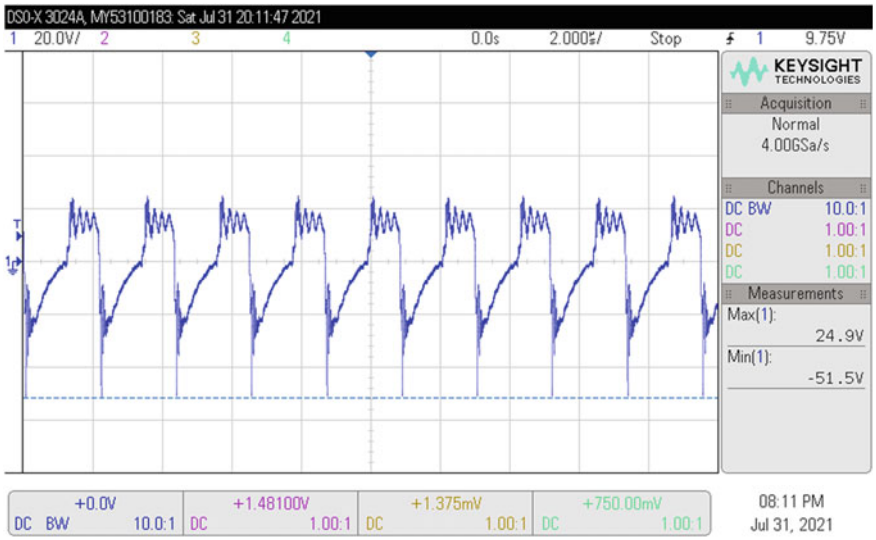

Fig. 8 Output diodes stress at 28 V full load

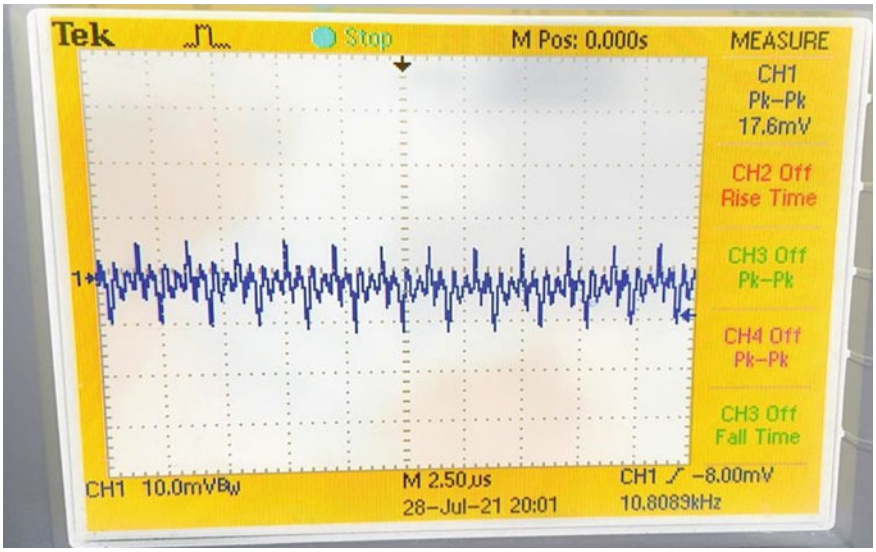

Fig. 9 Ripple voltage at 28 V full load (<50 mV)

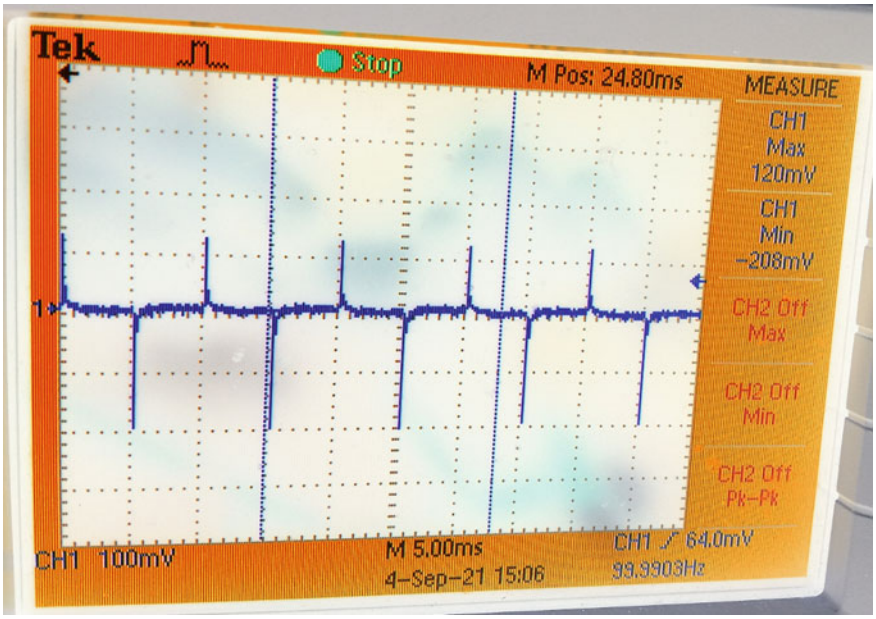

Fig. 10 Load transient at 28 V full load (<300 mV)

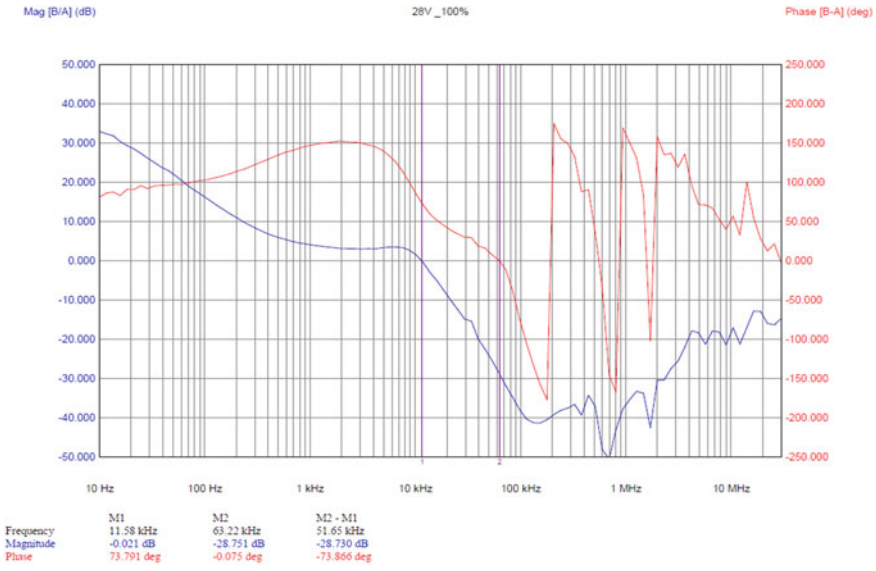

Fig. 11 Loop response at 28 V full load (GM < −10 dB and PM > 60°)

5 Conclusion

The single switch forward converter is analyzed for various parameters including efficiency, load and line regulation, load transient and loop response. All hardware results met desired specifications. Converter can sustain variable thermal conditions without degradation in efficiency. After testing in different environmental conditions, it can be effectively employed in space applications [9].

Acknowledgements We are grateful to Mr. Mallavarapu Apparao, Managing Director, Centum Electronics Limited, Bangalore for his encouragement and constant support for this work.

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Design and Implementation of High Power Pulsed Output DC-DC Converter

M. Harish Kumar, K. E. Rayees, Bhoopendra Kumar Singh, and Vinod Chippalkatti

Abstract This project is aimed at design and implementation of high-power pulsed output DC-DC converter for space application. Interleaved flyback topology is used to reduce the stress in the primary transformer, main power MOSFET and secondary diodes. Interleaved flyback converter topology has the benefits of reduced RMS current in the input capacitors, reduced peak currents in transformer windings and reduced EMI due to the result of reduced peak currents. Hence interleaving enables the converter topology to operate at increased power levels. Pulsed Power DC-DC Converters are used for powering the transmitter and receivers in various types of Radars such as Pulse Doppler Radar, Terminal Doppler Weather Radar and Synthetic Aperture Radar (SAR). Transceivers in satellites need pulsed power for RF Circuit, the RF circuit requires High frequency voltage with minimum rise time, fall time and output ripple. To generate the pulsed output the rectified output voltages are connected through the pulse modulator circuit.

Keywords High power pulsed outputs · Interleaved flyback topology · PWM controller · Pulse modulator · OCP

Abbreviations

$V_{in\ (min)}$	Minimum supply voltage
$V_{in\ (max)}$	Maximum supply voltage
V_{out}	Output voltage
P_{out}	Output power
I_{out}	Output current
V_D	Diode voltage

M. H. Kumar (✉) · K. E. Rayees · B. K. Singh · V. Chippalkatti
Centum Electronics Ltd., Bangalore, India
e-mail: harishk@centumelectronics.com

K. E. Rayees
e-mail: rayeeske@centumelectronics.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_9

η	Efficiency
D_{min}	Minimum duty cycle
D_{max}	Maximum duty cycle
N_p	Primary Number of turns
N_s	Secondary Number of turns
T_{ratio}	Turns ratio of transformer
Kw	Window factor
J	Current density
B_m	Magnetic flux density
A_w	Window area
A_c	Cross section of core
A_p	Area product of core
f_s	Switching frequency
$V_{ds,max}$	MOSFET Maximum drain to source voltage
V_{clamp}	Clamp Voltage
I_{ppeak}	Peak primary current
L_{leak}	Leakage inductance
L_{sn}	Snubber inductance
C_{sn}	Snubber capacitance

1 Introduction

Flyback converters are simple in its design and are of low cost as they use a relatively small number of components and therefore this topology is most widely used for low power applications. These converters also have disadvantages such as poor efficiency, high switching loss, high EMI noise and high switch voltage stress [1]. Hence an interleaved flyback converter is implemented in this design to overcome these drawbacks.

By using an Interleaved flyback topology, it is possible to operate the converter at increased power levels. Interleaved flyback topology is used to reduce switching losses, output ripple voltage and current and to reduce the size of the output capacitor [2, 3].

RCD snubbers have the simplest structure and therefore low cost and can be used to reduce the voltage spike on the MOSFET switch, but the switching losses are dissipated through resistors and thus reduce the efficiency of the converter [4]. Alternatively, a non-dissipative LC snubber is implemented in this design which have the benefit of improving the converter efficiency due to the absence of dissipative element. This snubber consists of capacitor, inductor and diodes [5].

In voltage mode control there is a single voltage feedback path, where gate pulses are generated by comparing error voltage signal with constant ramp waveform. The main disadvantages of this mode are slow response, and the loop gain varies with input voltage. In current mode control, the inductor current is sensed and compared

Table 1 Pulsed output voltage and current rating

Sl. no.	Pulsed output voltage (V) 2.5 kHz with 10% duty	Output current (A)		
		Minimum	Nominal	Maximum
1	45	6	10	12
2	26	1.25	1.75	2.5

to a control voltage derived from the error amplifier output to generate gate pulses [3]. Hence this mode will have high feedback loop stability and faster load transient response.

Pulse Modulator circuit is used to generate the pulsed outputs. The secondary filtered voltage will be fed to the pulse modulator circuit, and it will generate the required pulsed outputs with good line and load regulations.

2 Converter Specifications

The proposed converter Electrical specifications are shown below.

- Input voltage range: 60–75 V
- Output power: 60.5 W Average (Pulsed)
- 605 W Peak (Pulsed)
- Number of outputs: 2
- Efficiency: $\geq$75%
- Line regulation: $\pm$1%
- Load regulation: $\pm$1%
- Switching frequency: 100 kHz.

Voltage and current rating of two pulsed outputs of the proposed converter is given in Table 1.

3 Block Diagram

Block diagram of the High-power pulsed output converter is shown in below Fig. 1.

The block diagram of the High-power pulsed output converter is as shown in Fig. 1. The converter operates at a switching frequency of 100 $\pm$ 5 kHz. Input voltage of the converter is 70 V $\pm$ 5 V. Built in EMI Filter is considered in the input side to meet the EMI/EMC requirements. Input supply is fed to the main power transformer through the input filter. Telecommand circuit is used to control the turn ON and turn OFF of the converter. Converter will be turned ON by applying the turn ON command from external source. Once the turn ON command is applied, the start-up circuit gets activated and it will generate a voltage of approx. 10.6 V at input pin of PWM

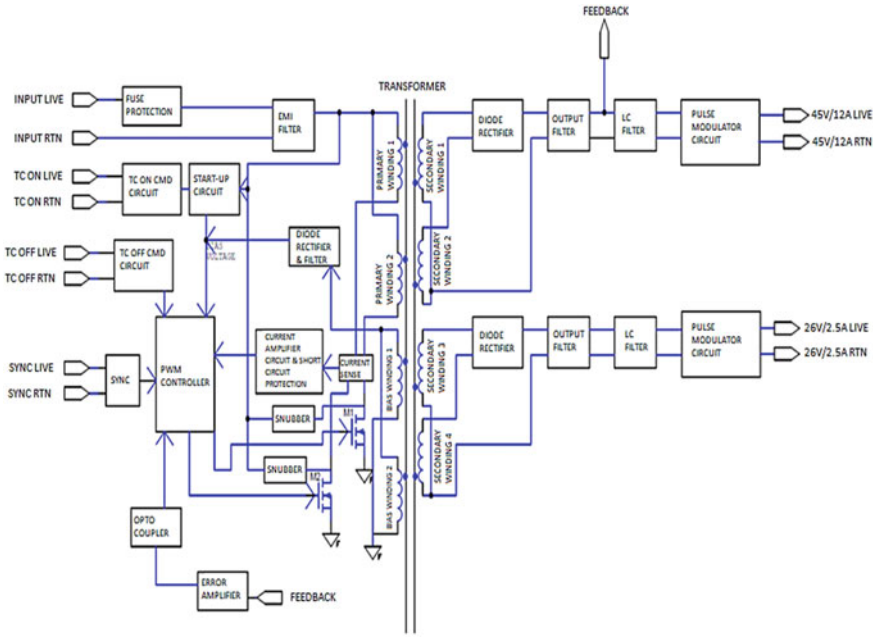

Fig. 1 Block diagram of high-power pulsed output converter

IC. The PWM IC will generate the gate pulse and MOSFET will turn on. During the ON period of the MOSFET, energy is stored in the primary inductor and in the OFF period of the MOSFET energy stored in the primary inductor is transferred to the secondary side by transformer action. Once the energy is transferred from primary side to secondary side of the transformer bias winding is energized. The bias winding will generate the voltage and there on the bias will power the PWM IC and all other control circuits. Also, all the secondary voltage will be generated. Current mode control method is used here. Converter is protected from over current and short circuits. Over current protection circuit is available which will sense the input current.

Secondary side winding voltage is rectified by using rectifier diode and filtered by using both output filters. Main Feedback is connected from the 45 V output. The secondary filtered voltage is fed to the pulse modulator circuit and based on the control signal it will generate the required pulsed outputs.

4 Design Procedure

Design of main power transformer, selection of main Power MOSFET switches, secondary rectifying diode, and non-dissipative LC snubber are important to meet the requirement of High-power pulsed output converter.

4.1 Selection of MOSFET

Interleaving operation of converter requires two identical Power MOSFETs. Based on the below factors MOSFETs are selected

- Drain to Source Voltage (VDS) and drain current rating (Id)
- Low $R_{ds,on}$
- Switching frequency
- Operating and storage temperature.

The N channel MOSFET selected in this design is JANSR2N7477T1 $V_{ds} = 250$ V, $R_{(ds,on)} = 0.061\ \Omega$, $I_d = 37$ A Operating and storage temperature -55 to 125 °C.

4.2 Selection of Secondary Rectifying Diode

The secondary side output rectifying diode is selected based on secondary reflected voltage and secondary current. Normally Schottky diodes are used, Because of its

- Low forward voltage drop
- Fast recovery time
- Low power consumption
- It can operate high frequency.

The Schottky diodes selected in this design are,

- SHD125146PSSQ—200 V, 15A, VF = 0.7.
- SC200H100A5P—100 V, 30 A, VF = 0.74 V.

Power Transformer Design. A flyback transformer works by storing energy in the form of a magnetic field during the first half-cycle and then releasing that energy with reverse terminal voltage. During turn on period of MOSFET, the current flows in the primary side and during turn off time it flows in the secondary side of the flyback converter.

Flyback transformer core will be selected based on the area product calculation. The area product is the product of the core cross section (Ac) and window factor (Aw).

$$A_p = A_c A_w \tag{1}$$

Area product (A_p) is calculated by the formula given below

$$A_p = \frac{L_p I_{pp}(A_{po} + A_{p1})}{K_w J B_m 10^{-}6} \tag{2}$$

$$\mathrm{A_{po}} = \mathrm{I_{prms}} + \mathrm{T_{ratio1}I_{srms1}} + \mathrm{T_{ratio2}I_{srms2}} + \mathrm{T_{ratio3}I_{srms3}} \tag{3}$$

$$A_{p1} = T_{ratiobias} T_{biasrms} \tag{4}$$

For better design of the Power transformer, Kw, Bm and J are selected. The transformer core will be selected with an area product greater than the calculated value.

Selectedcore: C055381 Toroidal MPP Powder Cores, $\mathrm{A_L} = 43 \pm 8\%$ nH/T^2

The transformer turns ratio is given by

$$\mathrm{T_{ratio}} = \frac{N_s}{N_p} = \frac{(\mathrm{V_{out}} + \mathrm{V_D})}{\mathrm{V_{in(min)}}} \frac{(1 - \mathrm{D})}{\mathrm{D}} \tag{5}$$

The primary and secondary winding turns are given by

$$N_p = \frac{V_{in(\min)}}{B_m A_c \times 10^{-6} f_s} \tag{6}$$

$$N_s = N_p T_{ratio} \tag{7}$$

Gauge of wire and number of strands are decided depending on the output current rating. In flyback converter with multiple output, it is difficult to attain cross regulation. This can be done by optimizing the winding strategy of the transformer.

Following techniques are used to achieve good cross regulation

- Use of a split primary winding
- The sequence for winding is done in such a way that the first layer of the winding is made as the inner-most winding, and the second layer is wound on the outside.
- For better coupling and minimized leakage inductance, the secondary with the highest output power must be placed closest to the primary.
- Secondary windings having only a few turns should be spread over the full length of the bobbin window instead of being bunched together to maximize coupling to the primary.
- For a better coupling tight winding need to be done.
- The measured leakage inductance should be less than two percent of the primary winding inductance.

4.3 LC Snubber Design

A non-dissipative LC snubber used in a flyback converter is shown in Fig. 2 which consists of inductor, capacitor and diodes.

The MOSFETs V_{ds} maximum value is given by

$$V_{ds,max} = V_{in(max)} + V_{clamp} \tag{8}$$

Clamping Voltage, $V_{clamp}$is calculated by applying KVL to the mesh formed by L_{leak}, L_m, C_{sn}, and D_1 as

$$V_{clamp} = (V_{out} + V_D)\frac{N_p}{N_s} + I_{ppeak}\sqrt{\frac{L_{leak}}{C_{sn}}} \tag{9}$$

Snubber capacitor $C_{sn}$is derived from the above equation as,

$$C_{sn} \leq \frac{I^2_{ppeak} L_{leak}}{[V_{ds,max} - V_{in(max)} - \frac{N_p}{N_s}(V_{out} + V_D)]^2} \tag{10}$$

The upper limit for the snubber inductance is given by

$$L_{sn} \leq \left(\frac{D}{f_s \pi}\right)^2 \frac{1}{C_{sn}} \tag{11}$$

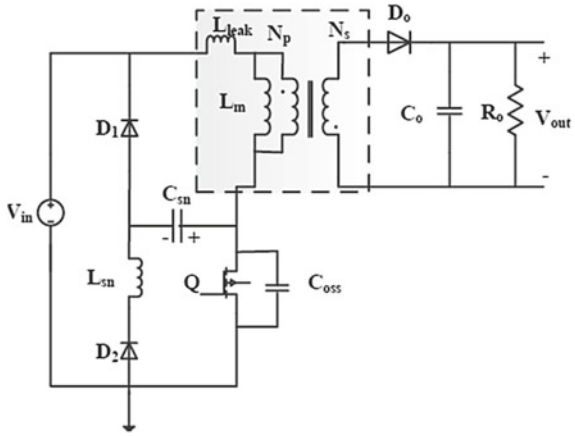

Fig. 2 A non-dissipative LC snubber used in a Flyback converter

5 Pulse Modulator

Pulse modulators are used to provide constant pulsed output voltages regardless of changes in input voltage or load current. The pulse modulators are connected in the secondary side of flyback converter to obtain better efficiency and load & line regulation.

Pulse Modulator circuit implemented in this design is shown in Fig. 3.An N-channel Power MOSFET is used as series pass element in the secondary side. When load current increases, the feedback circuit of converter increases the gate to source voltage of MOSFET thereby reducing the MOSFET's resistance to increase the output voltage. Likewise, when the load current decreases, the feedback circuit of converter increases MOSFET's resistance to reduce the output voltage. The required pulsed outputs are obtained by MOSFETs turn on turn off operation. Since MOSFET is connected at high side of the secondary, a boosting circuit is necessary to provide sufficient gate voltage to trigger the MOSFET. To control the rise and fall time of the pulsed output voltages, gate capacitance requires fast charging and discharging action which is provided by a parallel combination of R, C and D that is connected to the MOSFET.

Output Raw capacitor Calculation

$$P * Ton = \frac{C(Vmax^2 - Vmin^2)}{2} \tag{12}$$

In the Eq. (12) P- Power in watt, Ton- Pulse ON time in us, Vmax- max raw voltage in V, Vmin- min raw voltage in V, C- Output capacitor in uF.

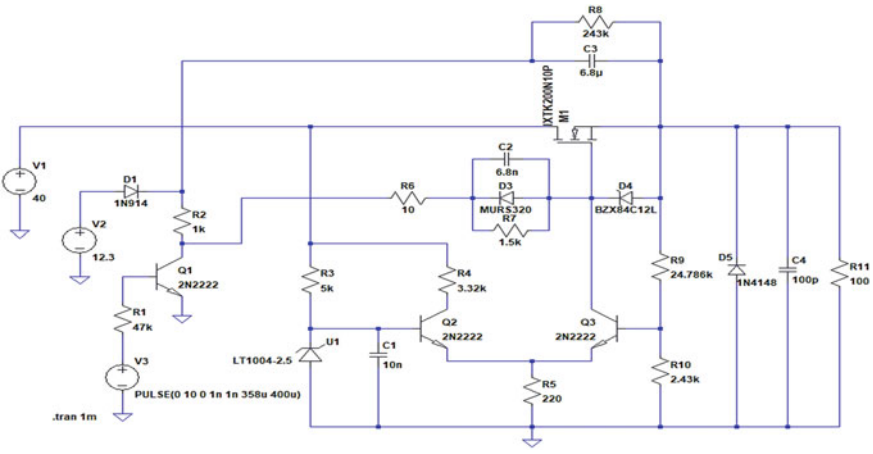

Fig. 3 Pulse modulator circuit

1.45 V Pulsed Output

Power—540 W

Ton—40 us

Vmax—48 V

Vmin—47.9 V

Calculated value of Raw capacitor is 472uF.

2.26 V Pulsed Output

Power—65 W

Ton—40 us

Vmax—28 V

Vmin—27.6 V.

Calculated value of Raw capacitor is 233 uF.

6 Overcurrent-Protection (OCP) Circuit

The OCP circuit is a protection feature that limits the output current to a safe level to prevent any damage to the converter from overload conditions. The OCP circuit detects the overcurrent by sensing the current through a current transformer. The current that is sensed through a current transformer is then compared with a fixed reference value. If the sensed component is greater than the reference value, the shutdown pin of PWM IC will go high and stops the gate pulse to the MOSFET and the converter goes OFF.

Over current protection (OCP) circuit is shown in Fig. 4.In this design a current transformer is used for sensing the primary current and will provide the secondary voltage which is set by the burden resistor R1. This voltage is then fed to an RC filter to eliminate the high frequency noise. The filtered voltage is amplified by a gain amplifier and fed to a noninverting pin of error amplifier. At inverting pin of error amplifier, a 2.5 V reference is set. Once the input current exceeds 125% of the rated primary current, the output pin of error amplifier will go high, and this signal will drive the shutdown pin of PWM IC and makes the converter go OFF.

7 Test Results and Waveforms

The test setup of the proposed converter is shown in Fig. 5. It consists of interleaved flyback converter, power supply, function generator, digital storage oscilloscope,

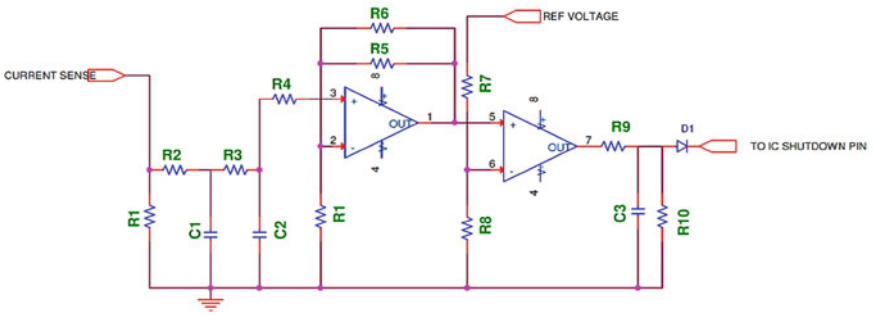

Fig. 4 Over current protection (OCP) circuit

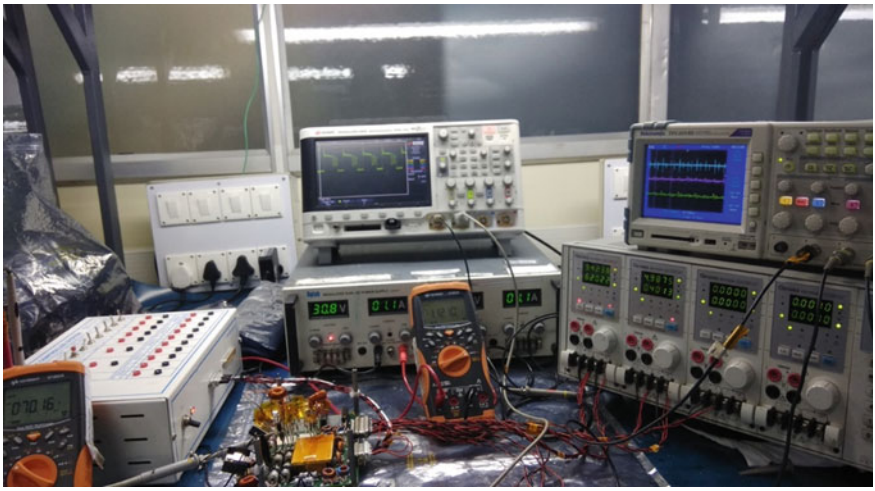

Fig. 5 Test setup of interleaved flyback converter

electronic load, and multimeter. The supply voltage is varied from 62 V to 74 V at minimum, nominal and maximum load conditions.

7.1 Efficiency at Nominal Input Voltage and at Different Load Conditions

Efficiency of the converter is measured at 70 V input and at maximum and nominal load conditions shown in Tables 2 and 3.

Table 2 Efficiency at nominal input and maximum load

	Vout (V)	Iout (A)	Pout (W)
45 V pulsed output	44.8	1.2	53.76
26 V pulsed output	25.9	0.25	6.475
Total Pout (W)			66.25
Vin (V)	Iin (A)	Pin (W)	Efficiency (%)
70	1.19	83.02	79.8

Table 3 Efficiency at nominal input and nominal load

	Vout (V)	Iout (A)	Pout (W)
45 V pulsed output	44.8	1	44.8
26 V pulsed output	25.9	0.175	4.5325
Total Pout (W)			49.3325
Vin (V)	Iin (A)	Pin (W)	Efficiency (%)
70	0.90	63.25	78

7.2 Line and Load Regulation

Line regulation is defined as the ability of the power supply to maintain its specified output voltage over changes in the input line voltage. It is expressed as the percent of change in the output voltage relative to the change in the input line voltage.

$$\%\text{LineRegulation} = \frac{V_{outmax-input} - V_{outmin-output}}{V_{outnom-output}} * 100 \tag{13}$$

Load regulation is defined as the ability of the power supply to maintain its specified output voltage over changes in the load conditions.

$$\%\text{LoadRegulation} = \frac{V_{outmin-load} - V_{outmax-load}}{V_{outnom-load}} * 100 \tag{14}$$

The line and load regulation test results of two pulsed outputs are shown in Tables 4 and 5 (Fig. 6).

Table 4 Percentage line and load regulation of 45 V pulsed output

Vin (V)	Output voltage (V)			Load regulation (%)
	Minimum load	Nominal load	Maximum load	
62	44.92	44.9	44.8	0.267
70	44.92	44.9	44.8	0.267
74	44.95	44.92	44.82	0.289
(%) Line Regulation	0.07	0.04	0.04	

Table 5 Percentage line and load regulation of 26 V pulsed output

Vin (V)	Output voltage (V)			Load Regulation (%)
	Minimum load	Nominal load	Maximum load	
62	25.92	25.9	25.9	0.077
70	25.92	25.9	25.9	0.077
74	25.95	25.92	25.92	0.116
(%) Line Regulation	0.12	0.08	0.08	

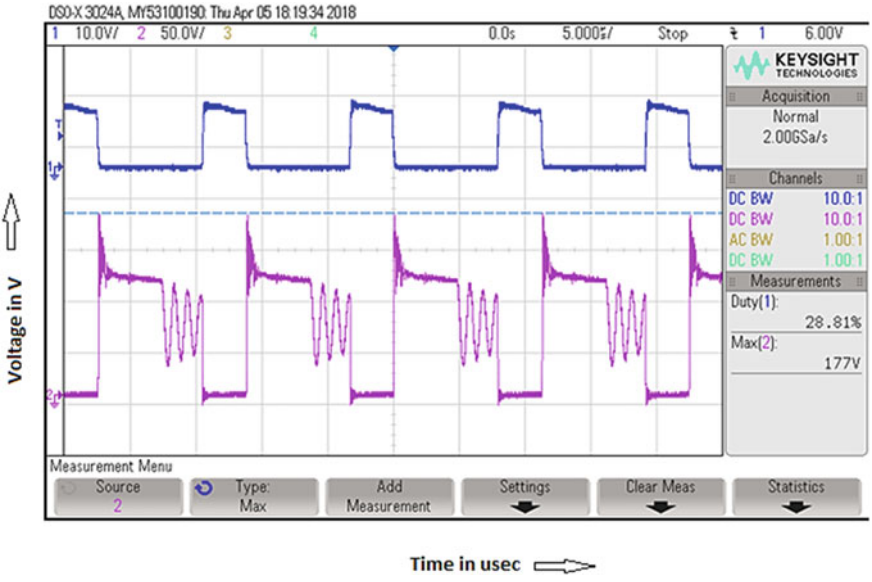

Fig. 6 Drain voltage waveform (purple) with respect to gate voltage waveform (blue)

8 Conclusion

High power pulsed output interleaved flyback converter has been implemented using current mode control technique and pulse modulators. Pulse modulators provide a constant pulsed output voltage regardless of changes in load current or input voltage.

Output voltages are regulated well within the desired value with proper design of the feedback circuit and pulse modulator circuit.

Acknowledgements We are grateful to Mr. Mallavarapu Apparao, Managing Director, Centum Electronics Limited, Bangalore for his encouragement and constant support for this work.

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EMI Reduction of Forward Converter with Backshells and Copper Braid for Space Application

Prakash Guthi, B. L. Santosh, Bhoopendrakumar Singh, and Vinod Chippalkatti

Abstract This paper explains the design and development of EMI/EMC compliant high reliability space grade power supply unit (PSU). Electro Magnetic Interference (EMI) is the possible interference to other electronic equipment. Due to the EMI system performance may effect, to take that need to design the proper EMI filter design and proper harness. Electronic Magnetic Compatibility (EMC) is defined as the ability of devices and systems to operate in their electromagnetic environment without impairing their functions and without faults and vice versa. Electronic equipments must function properly in its natural electromagnetic ambient. But due to the increasing usage of electronic equipment the natural ambient is polluted by the electromagnetic fields. This means if all the equipments have to co-exist then each should work in the specified electromagnetic field and as well should not radiate more than the specified amount. Similarly, while electronic equipments draws power from the mains, it should not pollute the mains more than the specified amount as well should work in the presence of specified amount of mains noise. This means equipments are compatible electromagnetically. EMI filters are used in converter to attenuate the flow of noise current through the power line to and from the converter. Inbuilt EMI/EMC filter of converter is compiled to MIL-STD-461E. There are four elements in EMI they are CE-Conducted Emission, RE-Radiated Emission, CS-Conducted Susceptibility and RS-Radiated Susceptibility.

Keywords EMI/EMC · Forward converter · CE · CS · RE · RS

1 Introduction

The Electromagnetic Interference (EMI) is the unwanted coupling of noise from one circuit to another. Two elements of EMI are illustrated below.

P. Guthi (✉) · B. L. Santosh · B. Singh · V. Chippalkatti
Centum Electronics Limited, Bengaluru, India
e-mail: prakashg@centumelectronics.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_10

1.1 Conducted EMI

Unwanted coupling of signals via conduction through parasitic impedances, power and ground connections. The propagation path requires a conductive medium like wires or some metallic structure. Two types of tests are there to check the compliance of equipment due to conducted EMI.

1. Conducted emission test
2. Conducted susceptibility test.

1.2 Radiated EMI

Unwanted coupling of signals via radio transmission. Two types of tests are there to check the compliance of equipment due to radiated EMI.

Radiated emission test

Radiated susceptibility test

A DC-DC Converter [1] is operated at an input voltage of 36 V. It not only draws power from the 42 V Input Bus but also switching noises are injected into the 36 V Input Bus. This is called CE. These conducted noise reaches the other electronic equipments via 36 V input bus which are connected to the same input Bus. DC-DC Converter [2] also radiates noise and that is picked up by nearby analog circuits and electronic equipments. This is called RE. DC-DC Converter operating at 36 V input bus, it is expected to receive the conducted noise/spikes as well from the 36 V input bus and the appearance of these spikes partially at the output of the DC-DC Converter can be seen. And these spikes affect the nearby equipments connected to the same input bus. DC-DC Converter must be able to withstand these spikes without failing and should maintain the output voltage within specification. This is called CS. DC-DC Converter must able to withstand certain amount of radiated electromagnetic field from the nearby equipments and it is called RS.

2 Converter Specifications

PSU is designed for the following specifications:

a. **Converter-1**
   Input voltage range: 24–36 V DC.
   Total output power: 9 W.
   No. of outputs: 1 output.
   PSU (Conv-1) Output: 15 V/0.6A.
   Load regulation (50–100% load): ±2%

Line regulation: ±1%
Operating frequency: 150 kHz.
Ripple: <30 mV Vrms.
Spike: <75mVpk-pk.
Efficiency (100% load): ≥70%
Input under voltage protection (IUVP).
Input over current protection (IOCP).
Output over current protection (OOCP).
Output short circuit protection (OSCP).

b. **Converter-2**

Input voltage range: 24–36 V DC.
Total output power: 91.4 W.
No. of outputs: 3 output.
PSU (Conv-2) Output: 5.3 V/12A.
: 5.4 V/4.5A.
: −5 V/0.7A.
Load regulation (50–100% load): ±2%
Line regulation: ±1%
Operating frequency: 150 kHz.
Ripple: <30 mV Vrms.
Spike: <75mVpk-pk.
Efficiency (100% load): ≥70%
Input under voltage protection (IUVP).
Input over current protection (IOCP).
Output over current protection (OOCP).
Output short circuit protection (OSCP).
Output over voltage protection (OOVP).

3 Block Diagram

The power supply unit block diagram is shown in Fig. 1. PSU has three Relays as shown in Fig. 1. Relay-1, Relay-2 and Relay-3 commands (CMDs) will be supplied from relay test jig. These relays operated at an amplitude of 26 V ± 2 V with the help of relay on command, which is applied for 64 ms ± 5 ms duration. The output from Arduino board is a low voltage magnitude pulse and this is not sufficient to turn on the relay, hence high voltage driver IC MIC2982 is used to increase pulse magnitude. According to the specification, a programme has been developed for Arduino board, and based on coil connection in the relay pulses were given to turn on or turn off the relay. The Relay-1 is used to control operation of common for the both converters i.e. converter-1 and converter-2. Relay-2 will be used to turn on/off converter-2 and similarly Relay-3 for converter-1.

The PSU has built-in EMI filter and this EMI filter includes CMI (common mode inductor) and DMI (differential mode inductor). Other than EMI filter PSU also has

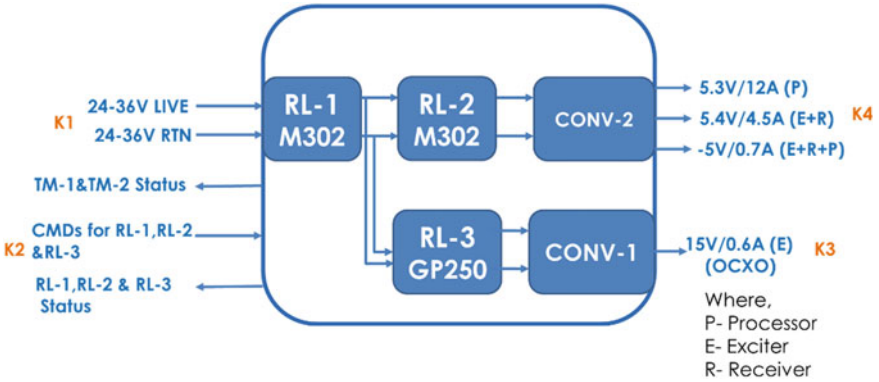


Fig. 1 Converter block diagram

start-up circuit, Isolation Transformer, PWM Controller, Driver IC for MOSFET, secondary rectifiers followed by regulators like Mag-Amp and LDO's, Protection circuits (IUVP, IOCP, OOVP, OSCP and OOCP). Implementation of a synchronous buck converter will comply the following MIL-STD-461E EMI/EMC tests:

CE-102: Conducted Emissions, Power and interconnecting leads, 10 kHz to 10 MHz.

CS-101: Conducted Susceptibility, High sides of Power leads only, 30 Hz to 150 kHz.

CS-114: Conducted Susceptibility, all interconnecting cables, 10 kHz to 200 MHz.

CS-115: Conducted Susceptibility, all interconnecting cables, Impulse Excitation.

RS-103: Radiated Susceptibility, Unit with all cables (2 MHz to 40 GHz).

RE-102: Radiated Emissions, Unit with all cables, 10 kHz to 18 GHz.

4 CMI and DMI Filter Design Calculations

4.1 Common Mode Noise Calculation

Primary side Power MOSFET is mounted on the heatsink as shown in Fig. 2. The heatsink capacitor (nearly 100pF) will charge across the drain of the MOSFET to double the V peak MOSFET. The charging and discharging of heatsink capacitor is one of the major sources of the Common Mode Noise.

Typical value of heat sink capacitor ($C_{heatsink}$) is 100pF. Peak voltage across the MOSFET is calculated as follows:

$$V_{peak\_MOSFET} = V_{inmax} \cdot \left(1 + \frac{N_p}{N_{reset}}\right) = 42 \cdot \left(1 + \frac{8}{8}\right) = 84\ Volt \qquad (1)$$

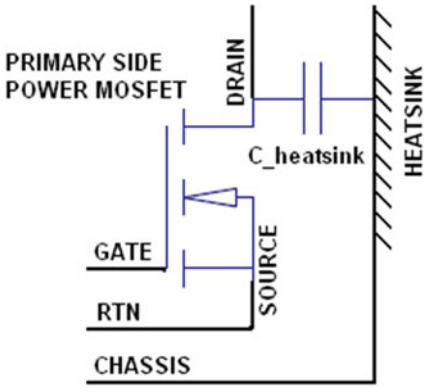


Fig. 2 Primary side power MOSFET and heatsink

Voltage amplitude at zero frequency is given as

$$V_{amplitude\_zero\_freq} = 2 \cdot V_{peakMOSFET} \cdot D_{max} = 2 \cdot 84 \cdot 0.4 = 67.2 \text{ Volt} \quad (2)$$

Voltage amplitude at the first harmonic of the first break point frequency is calculated as follows:

$$V_{amplitude\_first\_harmonic\_of\_first\_break\_freq} = \frac{V_{amplitude\_zero\_freq} \cdot F_{first\_break\_point}}{2 \cdot F_{first\_break\_point}} = 33.6 \text{ Volt} \quad (3)$$

The amplitude of the first harmonic sine wave component of the first break frequency that is present at the Drain of the switching Power MOSFET is applied to the RAW Bus through the heat sink capacitor. The capacitor is charged & discharged through 50Ω LISN (Line Impedance Simulation Network) resistor. The voltage developed across the 50Ω resistor at the first harmonic of the first break frequency is calculated as below:

$$V_{CM\_NOISE} = \frac{\left(\frac{V_{amplitude\_zero\_freq} \cdot F_{first\_break\_point}}{2 \cdot F_{first\_break\_point}}\right) \cdot 50}{50 + \left(\frac{1}{2 \cdot \pi \cdot (2 \cdot F_{first\_break\_point}) \cdot C_{heat\_sink}}\right)} = \frac{\left(\frac{67.2 \cdot 1.114 \cdot 10^5}{2 \cdot 1.114 \cdot 10^5}\right) \cdot 50}{50 + \left(\frac{1}{2 \cdot \pi \cdot (2 \cdot 1.114 \cdot 10^5) \cdot 100 \cdot 10^{-12}}\right)} = 0.2335 \text{ Volt} \quad (4)$$

Where: VCM_NOISE is the common mode noise.

4.2 Differential Mode Noise Calculation

Square wave current is drawn by switching Power MOSFET. This square wave current is partly coming from the 36 V RAW BUS while the remaining switching current coming from the Input capacitor 'C' as shown in Fig. 3. The current drawn from the 36 V RAW BUS produces a noise voltage. If I1 is the current from 'C' and I2 is the current from the 36 V RAW BUS, then

$$\frac{I_2}{I_1} = \frac{w \cdot L_{ESL}}{w \cdot (L_1 + L_2)} = \frac{L_{ESL}}{100\ \mu\text{H}} \tag{5}$$

where: L1 and L2 are the inductors [3] of LISN

LESL is the ESL (Equivalent series Inductance) of capacitor 'C'.

w is the radial frequency.

The Typically, LESL value can be 10 nH.

EMI [4] filter will be designed for the nominal output power of 79 W. The Flat-topped pulse Input Current (Ipft) can be calculated as

$$I_{pft} = \frac{P_{out\_nominal}}{\eta \cdot V_{in(min)} \cdot D_{max}} = \frac{79}{0.7 \cdot 32 \cdot 0.4} = 8.82\ \text{Amp} \tag{6}$$

RESR = 0.46 Ω.

Noise Voltage across 50 ohm resistor is calculated as below

Noise Voltage due to RESR of the Capacitor

$$V_{noise2} = I_{pft} \cdot R_{ESR} = 8.82 \cdot 0.46 = 4.0572\ \text{Volt} \tag{8}$$

Total noise voltage

$$V_{noise} = V_{noise1} + V_{noise2} = 0.0441 + 4.0572 = 4.1013\ \text{Volt} \tag{9}$$

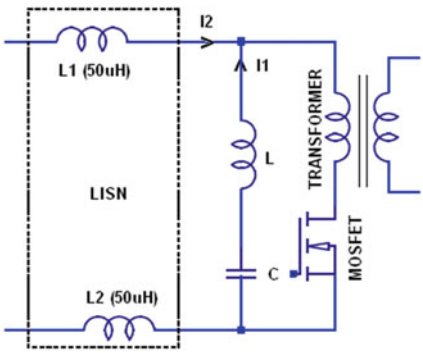


Fig. 3 Current path during the switch on of the Power MOSFET

The differential mode noise voltage at the first harmonic of the first break frequency

$$V_{DM\_NOISE} = V_{noise} \times D_{max} = 4.1013 \times 0.4 = 1.6405 \text{ Volt} \tag{10}$$

4.3 Common Mode and Differential Mode Filter Calculation

The noise voltage beyond the second carrier frequency 'f2' will be very small. Therefore, total noise is the summation of common mode noise and differential mode noise. Hence,

$$V_{EMI\_NOISE} = V_{CM\_NOISE} + V_{DM\_NOISE} = 0.2335 + 1.6405 = 1.874 \text{ Volt} \tag{11}$$

Let's, take safety factor 2.

$$V_{EMI} = F_{Safety} \cdot V_{EMINOISE} = 2 \cdot 1.874 = 3.748 \text{ Volt} \tag{12}$$

Select the allowable noise spec in dB from the graph of CE102 (MIL-STD-461E) shown in Fig. 4.

From the CE102 graph, allowable EMI noise is

$$V_{EMI\_Allowable} = 72 \text{ dB}\mu\text{V}$$

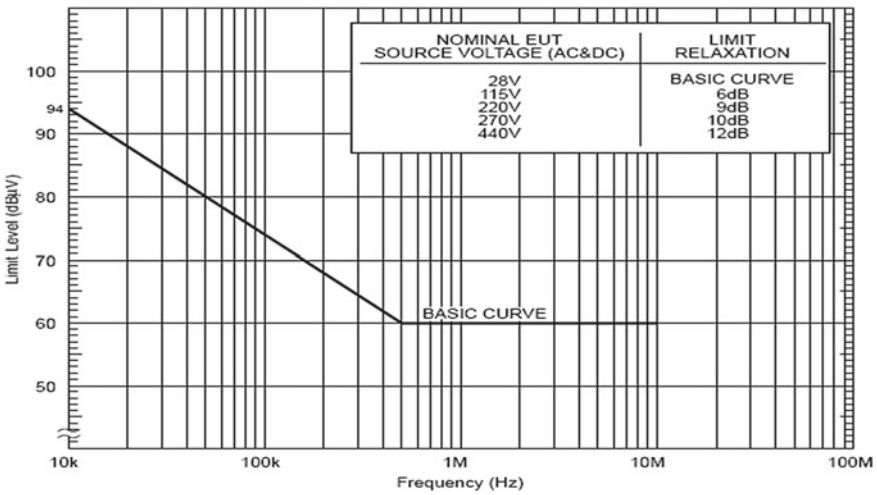


Fig. 4 CE102 limit

The above noise given in dBμV can be converted into volts as follows

$$V_{EMI\_Allowable} = 10^{\left(\frac{72}{20}\right)} \cdot 10^{-6} = 3.98107 \cdot 10^{-3} \tag{13}$$

Select the appropriate amount of CM & DM noises

$$V_{CM} = 1.24 \times 10^{-3}\text{V}$$

$$V_{DM} = V_{EMI\_Allowable} - V_{CM} = 3.98107 \cdot 10^{-3} - 1.24 \cdot 10^{-3} = 2.741 \times 10^{-3}\ \text{Volt} \tag{14}$$

Common mode filter (Inductor and Y-Capacitors) components can be calculated based on the required cut off frequency (Fcutoff_freq_CM) to suppress the common mode noise as follows:

$$F_{cutoff\_freq\_CM} = \frac{2 \cdot F_{first\_break\_point}}{\sqrt{\frac{F_{safety} \cdot V_{CM\_NOISE}}{V_{CM}}}} = \frac{2 \cdot 1.114 \cdot 10^5}{\sqrt{\frac{2 \cdot 0.2335}{1.24 \cdot 10^{-3}}}} = 11480.679\ \text{Hz} \tag{15}$$

Let's select: Y capacitor

$$C_Y = 100\ nF$$

Common mode inductor value can be calculated as follows:

$$L_{CM} = \frac{1}{(2 \cdot \pi \cdot F_{cutoff\_freq\_CM})^2 \cdot 2 \cdot C_Y} = \frac{1}{(2 \cdot \pi \cdot 11480.679)^2 \cdot 2 \cdot 100 \cdot 10^{-9}} = 960.89 \cdot 10^{-6} H \tag{16}$$

Selected value for Common mode inductor is (L_CM = 1400 × 10^(-6) H).

Differential mode filter (Inductor and X-Capacitor) components can be calculated based on the required cut off frequency (Fcutoff_freq_DM) to suppress the differential mode noise as follows:

$$F_{cutoff\_freq\_DM} = \frac{2 \cdot F_{first\_break\_point}}{\sqrt{\frac{F_{safety} \cdot V_{DM\_NOISE}}{V_{DM}}}} = \frac{2 \times 1.114 \cdot 10^5}{\sqrt{\frac{2 \cdot 1.6405}{2.741 \times 10^{-3}}}} = 6.439 \cdot 10^3 \text{Hz} \tag{17}$$

Let's select: Differential Mode Inductance value $.L_{DMI} = 116 \cdot 10^{-6} H$

X-Capacitor can be calculated as follows:

$$C_X = \frac{1}{(2 \cdot \pi \cdot F_{cutoff\_freq\_DM})^2 \cdot L_{DMI}} = \frac{1}{(2 \cdot \pi \cdot 6.439 \cdot 10^3)^2 \cdot 116 \cdot 10^{-6}} = 5.266 \cdot 10^{-6}\ \text{F} \tag{18}$$

Selected value for X-Capacitance value is 22 μF, 100 V.

5 Experimental Results

5.1 CE102 and RE102 Results

PSU hardware is designed, analyzed and implemented. The converter is tested for input voltage range from 24 to 36 V from 10% load to maximum load operating at 150 kHz. The test setup for the CE and RE is shown in Figs. 5 and 6 respectively. Test Results of CE102 and RE102 are shown in Table 1.

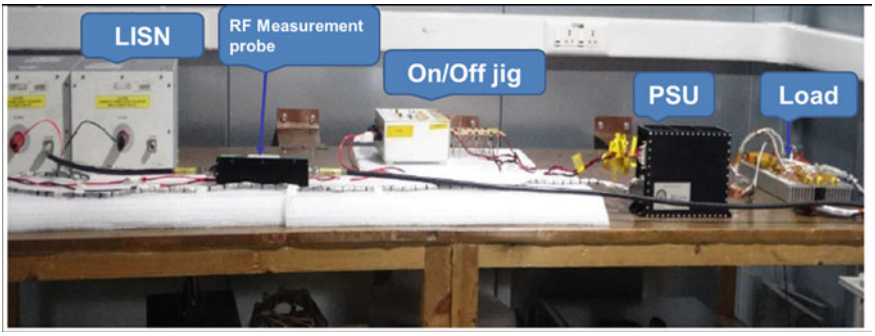
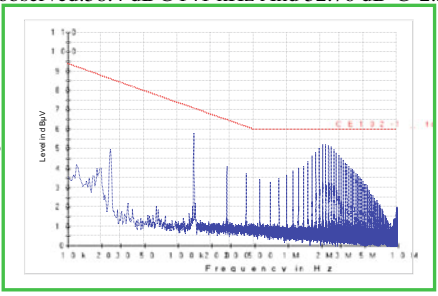
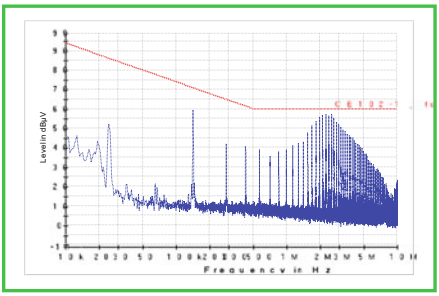
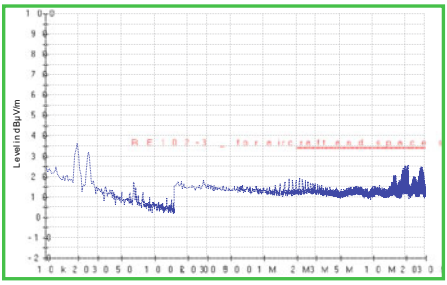


Fig. 5 CE102 test setup

Fig. 6 RE102 test setup

Table 1 CE102 and RE102 test results

S. no.	Connector connections	Results
1	CE-102 • Input connector: TPS + Backshell • CMD connector: PTFE + Braid + Backshell • O/P connector: TPS + Backshell	LIVE to chassis Peak observed:58.4 dB@141 kHz And 52.76 dB @ 2.24 MHz **PASS**   RTN to chassis Peak observed: 59.5 dB@141 kHz And 57.6@ 2.24 MHz **PASS**
2	RE102 • Input connector: TPS + Backshell • CMD connector: PTFE + Braid + Backshell • O/P connector: TPS + Backshell	 10 kHz to 30 MHz –26.4 dB @20 MHz

5.2 CS-101 Results

Injected AC voltage of 2Vrms from 30 Hz to 5 KHz and later derating to 0.2Vrms at 150 KHz on input line.

Output ripples were observed during the test and the results are within the specification.

Test setup and limit curve for CS-101 [4] are shown below (Table 2).

Table 2 CS-101 test results

Frequency	Applied noise Voltage Level		Vout ripple (pk-pk) (mV)			
			VOut1 5.3 V/12A	VOut2 5.4 V/4.5A	VOut3 -5 V/0.7A	VOut4 15 V/0.6A
	Vp_p	Vrms	spec < 265 mV	spec < 270 mV	spec < 250 mV	spec < 750 mV
30 Hz	5.66	2	21.8	18.4	18.4	6.4
50 Hz	5.66	2	21.8	18.4	18.4	6.4
75 Hz	5.66	2	21.8	18.4	18.4	6.4
100 Hz	5.66	2	21.8	18.4	18.4	6.4
200 Hz	5.66	2	21.8	18.4	18.4	6.4
300 Hz	5.66	2	22.4	18	19.2	5.6
400 Hz	5.66	2	22.4	18	19.2	5.6
500 Hz	5.66	2	22.4	18	19.2	5.6
600 Hz	5.66	2	21.6	17.6	18.4	6.4
700 Hz	5.66	2	21.6	17.6	18.4	6.4
800 Hz	5.66	2	21.6	17.6	18.4	6.4
900 Hz	5.66	2	21.6	17.6	18.4	6.4
1 kHz	5.66	2	20	17.6	18.4	5.6
1.5 kHz	5.66	2	20	17.6	18.4	6.4
2 kHz	5.66	2	20	17.6	18.4	6.4
3 kHz	5.66	2	21.6	17.6	18.4	5.6
5 kHz	5.66	2	21.6	18	18	5
7 kHz	5.46	1.93	21.6	17.6	18.4	5.6
9 kHz	5.29	1.87	21.6	17.6	18.4	5.6
10 kHz	5.20	1.84	21.6	17.6	18.4	5.6
15 kHz	4.84	1.71	21.6	17.6	18.4	5.6
20 kHz	4.47	1.58	20	17.6	18.4	6.4
25 kHz	4.13	1.46	21.6	17.6	18.4	5.6
30 kHz	3.82	1.35	21.6	17.6	18.4	5.6
50 kHz	2.83	1	21.8	18.4	18.4	6.4
100 kHz	1.27	0.45	21.8	18.4	18.4	6.4
150 kHz	0.57	0.2	21.8	18.4	18.4	6.4

6 Conclusion

Proposed converter is tested satisfactorily for all the specifications as per MIL-STD-461E which is delivering outputs 5.3 V/12A, 5.4 V/4.5A, −5 V/0.7A and 15 V/0.6A. The design and development of EMI/EMC filter has been done and detailed EMI/EMC tests as per MIL-STD-461E have been conducted successfully. The design procedure was verified with experimental results. Different harness types have been tested and CE, RE, CS and RS results are satisfactory with the following harness types i.e. Input connector: TPS wire with Backshell, CMD connector: PTFE wire over copper braid with Backshell, Output connector: TPS wire with Backshell and connector gasket.

Acknowledgements We are grateful to Mr. Mallavarapu Apparao, Managing Director, Centum Electronics Limited, Bangalore for his encouragement and constant support for this work.

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Automatic Gain Control for High Dynamic Signals Using Feedforward Technique

Aparna Bhuvanagiri, M. Prakruthi, and Ranjit Kumar Dora

Abstract This paper proposes Automatic Gain Control (AGC) implementation using feedforward technique to ensure the input signal dynamic range is not in saturation level or below noise tolerance level for the succeeding analog to digital converter (ADC) block. Using this technique, AGC implementation and Received Signal Strength Indicator (RSSI) measurement can be done simultaneously. AGC is a closed loop feedback control system which adjusts the arbitrary received signal strength to a predetermined level. It is employed to delimit the dynamic range of the signal and hence reducing the power consumption of ADC. RSSI is used to determine the signal strength at the input of the receiver. It is estimated by measuring the voltage at the detector whose output voltage is proportional to the input signal level. In the proposed design, AGC maintains the constant output signal level of -20 ± 2 dBm for the input signal varying from -58 to -1 dB with a dynamic range of 57 dB.

Keywords Automatic gain control · Dynamic range · Variable gain amplifier · Log detector · Received signal strength indicator

1 Introduction

AGC adjusts the gain of the VGA such that the output level is maintained constant to a desired level for varied input signal level. This is needed to ensure that the input signal dynamic range for the succeeding ADC block doesn't fall below noise level as

A. Bhuvanagiri (✉) · M. Prakruthi · R. K. Dora
Centum Electronics Ltd, Bengaluru, India
e-mail: aparnab@centumelectronics.com

M. Prakruthi
e-mail: prakruthim@centumelectronics.com

R. K. Dora
e-mail: ranjitkumard@centumelectronics.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
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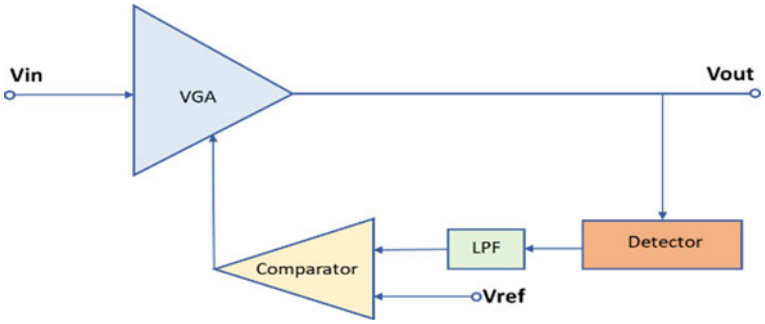

Fig. 1 Feedback architecture

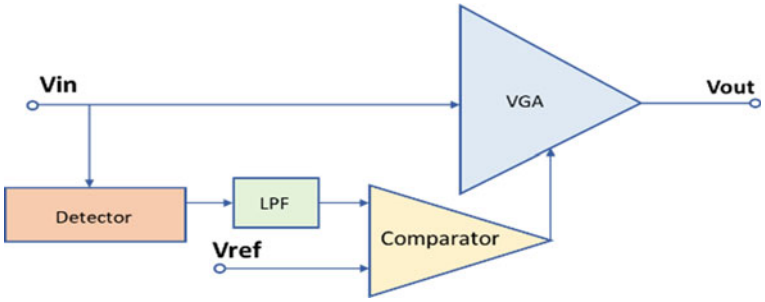

Fig. 2 Feedforward architecture

well as saturated with large signal [1, 2, 9]. AGC system consists of VGA, detector, LPF and comparator as shown in Figs. 1 and 2.

There are two types of architectures in AGC circuitry: 1. Feedback Architecture, 2. Feedforward Architecture. In feedback technique (Fig. 1), the sampled output signal is detected by a detector and compared with a reference using a comparator. This comparator output signal is fed as the control signal for varying the gain of VGA to maintain a constant output level. In this technique, the input dynamic range needed by the detector is low and has high linearity. The main drawback of this technique is the instabilities with high settling time or high compression or expansion [1, 3, 11].

In feedforward technique (Fig. 2), the input signal is split and fed to VGA and detector simultaneously. The detected voltage is compared with a reference and the comparator output is given as a control signal to VGA to maintain constant output level [1, 4].

The main advantage is the absence of instability problem and zero settling time. Also, RSSI can be measured simultaneously. Only drawback of this technique is that the detector requires high input dynamic range. AGC has applications in radio, television and radar systems. It is generally employed in receivers.

2 Methodology

In this proposed design, Feedforward technique is implemented as the detected output can be used as RSSI. This technique comprises of VGA, Detector, Low pass filter and Comparator.

The VGA is the heart of the AGC circuit. It amplifies or attenuates the incoming signal to the desired optimal level according to a gain function, G (V_{ctrl}), which depends on a control signal voltage V_{ctrl} provided by the loop [10]. The block diagram of VGA is shown in Fig. 3. VGA impacts the main AGC specifications such as bandwidth, noise and harmonic distortion. VGA should neither limit the frequency of operation nor the linearity of the system to obtain the best overall performance [5, 6].

RF detector samples the input signal fed to it and generates a DC output voltage proportional to the input power. RF detectors are generally used to control and measure RF power in wireless systems. The two basic types of RF detectors are Logarithmic detector and RMS detector [7, 10].

Log detectors are used for CW and pulsed signals with low crest factor. They have fast response times. For Log detectors, the output detected voltage is proportional to the log variation of the input signal. RMS detectors are used for signals having very high crest factor (Fig. 4) like higher order QAM, PSK and spread spectrum signals. For RMS detectors, the output voltage is proportional to RMS voltage of the input signal [6, 7].

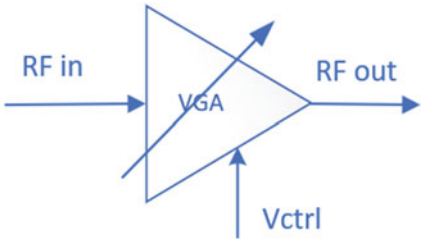

Fig. 3 Block diagram of variable gain amplifier

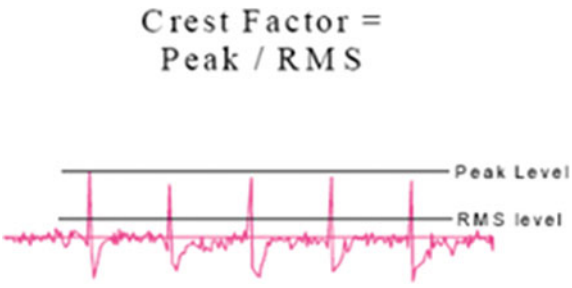

Fig. 4 Crest factor of any arbitrary signal

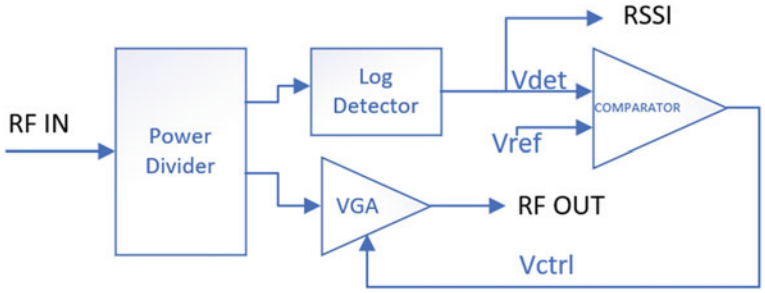

Fig. 5 Proposed design block diagram

In this proposed design, Feedforward technique is implemented so that a single detector is used for AGC loop control as well as RSSI measurement. The block diagram is as follows (Fig. 5).

The input signal is split and fed to VGA and Detector. The VGA chosen is an analog voltage-controlled VGA. A log detector is used in the design which converts input dBm signal to rms voltage. This RMS voltage is filtered to reduce the ripple and is fed to a comparator. This compares the detected signal with the reference voltage and the difference is fed as control signal to VGA, varying the gain of VGA in such a way as to keep its output level constant. The voltage present at the output of the detector is used to determine the received signal strength of the receiver (RSSI).

3 Design

The main design involves calculating the reference voltage and gain of the Op-Amp based comparator. In this design, unity gain is maintained (Figs. 6 and 7).

The input signal range that is fed to VGA, is determined by analyzing the power divider insertion loss. The output of the VGA needs to be maintained at −20 dBm. For a particular input power, the value of Vctrl is determined to get −20 dBm. Vctrl for our design varies from −0.6 V to 0.6 V. The input power for which Vctrl is

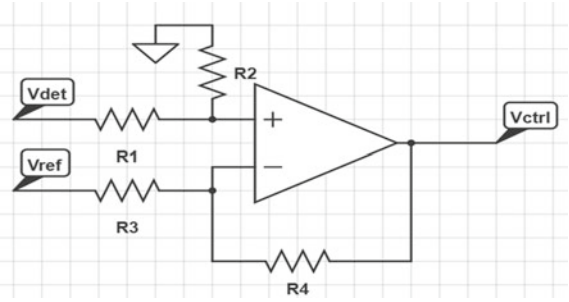

Fig. 6 Op-Amp based comparator

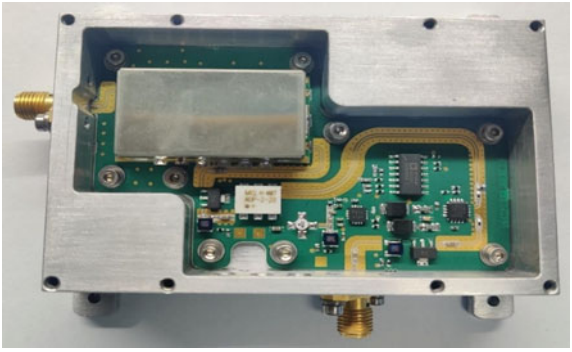

Fig. 7 Receiver Section with Feedforward AGC module

zero is measured and for that input, power corresponding detected output voltage is measured. This detected voltage is used as the reference voltage for the comparator.

In the current design, for VGA input power of −35 dBm, the RF OUT strength of −20 dBm is achieved with a control voltage (Vctrl) of 0 V. Therefore, the detected voltage at −35 dBm is used as reference voltage to the comparator. That reference voltage was found to be 1.06 V.

The unity gain Op-Amp comparator design is shown in Fig. 6.

$$R1 = R2 = R3 = R4 \tag{1}$$

Vctrl is calculated as follows [8].

Assuming ideal Op-Amp, input current drawn is almost zero.

$$\mathrm{VR2} = \mathrm{Vdet}/2 \tag{2}$$

Let V- is the voltage across Op-Amp negative terminal node.

$$\mathrm{V}- = \mathrm{Vdet}/2 \tag{3}$$

Apply KCL at Op-Amp negative terminal node.

$$\mathrm{Vdet}/2 - \mathrm{Vctrl} = -\mathrm{Vdet}/2 + \mathrm{Vref} \tag{4}$$

$$\mathrm{Vctrl} = \mathrm{Vdet} - \mathrm{Vref} \tag{5}$$

In this design, all the Resistors are chosen to be 10 K Ohm. Fig. 7 shows the section of receiver where the feed forward AGC is implemeted.

Table 1 VGA measured results

RF in (dBm)	Vctrl (V)	RF in (dBm)	Vctrl (V)
−6	−0.587	−36	+0.042
−8	−0.538	−38	+0.082
−10	−0.499	−40	+0.120
−12	−0.460	−42	+0.159
−14	−0.417	−44	+0.201
−16	−0.373	−46	+0.240
−18	−0.333	−48	+0.279
−20	−0.289	−50	+0.322
−22	−0.249	−52	+0.361
−24	−0.210	−54	+0.401
−26	−0.165	−56	+0.445
−28	−0.126	−58	+0.484
−30	−0.085	−60	+0.524
−32	−0.042	−62	+0.582
−34	−0.003	−63	+0.625

4 Measured Results

Initially, VGA and Log detector blocks are tested individually to determine the reference voltage needed at the comparator input.

For VGA, the input signal is varied from −63 dBm to −6 dBm, the control voltage Vctrl is varied for each input signal level to get an output signal level of −20 dBm as listed in Table 1. At input signal level of −35 dBm, the control voltage is zero. The detected voltage at this input level is measured for calculating the reference voltage of comparator.

For Log detector, the input signal is varied from −63 dBm to −6 dBm and the rms detected voltage (Vdet) is measured as listed in Table 2. At −35 dBm, Vdet is around 1.06 V. This voltage is used as reference voltage Vref at the input of comparator.

The circuit is connected according to the proposed block diagram and the RF input signal is varied from −1 dBm to −58 dBm (57 dB dynamic range) and reference voltage Vref is kept at 1.06 V. and RF input level versus output level is plotted (Fig. 8). The VGA output is found to be -20 ± 2 dBm.

5 Conclusion

This AGC circuit is designed using feedforward technique and the output level of -20 dBm $\pm$ 2 dBm is maintained. The dynamic range of the input signal is considered 57 dB. For signals whose input dynamic range is around 50 dB, the output signal

Table 2 Log detector measured results

RF in (dBm)	Vrms (V)	RF in (dBm)	Vrms (V)
−6	1.677	−36	1.036
−8	1.635	−38	0.998
−10	1.595	−40	0.962
−12	1.554	−42	0.922
−14	1.514	−44	0.881
−16	1.47	−46	0.839
−18	1.428	−48	0.799
−20	1.383	−50	0.758
−22	1.338	−52	0.720
−24	1.302	−54	0.682
−26	1.260	−56	0.630
−28	1.218	−58	0.600
−30	1.175	−60	0.570
−32	1.133	−62	0.547
−34	1.09	−63	0.533

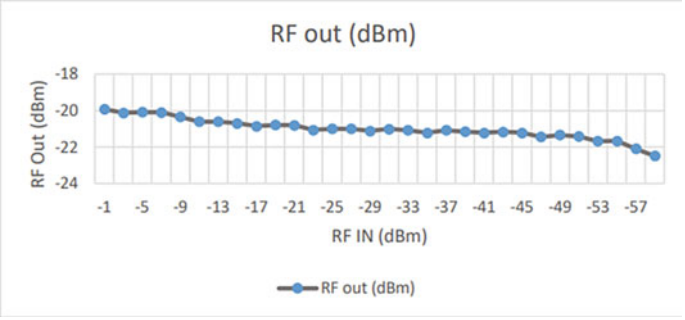

Fig. 8 Automatic gain control plot

variation can be reduced to 0.5 dBm. The detector output can be tapped, amplified using an Op-Amp and can be used as RSSI indication. Further, another VGA can be cascaded and implementing a log detector by cascading multiple log amplifiers can improve the dynamic range of the AGC.

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Solar Panel Deployment Mechanism for Nano-Satellite

Amit Kamboj, Aditya, Anoop Kumar Srivastava, K. Balaji, Abhishek Kumar, B. P. Nagaraj, H. N. Suresha Kumar, and Alok Kumar Shrivastava

Abstract A new solar panel deployment mechanism for nano-satellites is developed and successfully deployed on-orbit with an objective of achieving modularity and optimization in terms of mass and volume. The modular hinge mechanism simplifies ground testing and can be operated in Earth's gravity, thereby eliminating the need for gravity compensation system for solar panel deployment. The miniature hinge is configured without locking linkages and holds the panel by ensuring positive spring torque at the end of deployment. Similar existing miniature hinge mechanisms either lack indication switch or use fragile elements like tape springs. Hinge design presented in the paper addresses all such limitations. After hold down release, panel rotates by 90°, hits the stopper bracket of the hinge and rebounds. The panel oscillates few times before eventually settling down in the deployed state. Deployment dynamics of the solar panel is modeled in a multi-body dynamics tool, MSC ADAMS and analyzed to evaluate settling time. It is important to evaluate settling time as it governs the timeline of the sequence of mission critical events to be executed by satellite's on board computer. The peak angular velocity of the satellite during deployment is evaluated using the developed dynamics model. The evaluated peak reaction body rates and deployment settling time are compared with the actual on-orbit observations for the nano-satellite.

Keywords Solar panel · Deployment · Dynamics · On-orbit and hinge mechanism

1 Introduction

Solar panels are the primary source of power generation for the satellite. The configuration of the solar panel is governed by satellite configuration and power requirements. Panels are stowed during launch to meet the launch vehicle constraints and

A. Kamboj (✉) · Aditya · A. K. Srivastava · K. Balaji · A. Kumar · B. P. Nagaraj · H. N. Suresha Kumar · A. K. Shrivastava
Spacecraft Mechanisms Group/Mechanical Systems Area, U R Rao Satellite Centre, Indian Space Research Organisation, Bangalore 560017, India
e-mail: amitkam@ursc.gov.in

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_12

stiffness requirements. On reaching the intended orbit, the panels are deployed into their final deployed configuration.

The panels are held in stowed condition using a hold-down mechanism, which resists the launch loads. Spring driven hinges are employed to drive the panels after hold-down release. Conventionally, the hinges are positively locked after the panel reaches deployed orientation. Due to extremely small size and mass constraints, the miniaturized hinges for nano-satellite are not designed with lock mechanism.

This paper presents the configuration of the new hinges, with higher spring torques for deployed stiffness and for deployment tests under Earth's gravity conditions. It also studies the deployment behavior of solar panel in absence of an active locking mechanism, and evaluates the impact of the solar panel deployment dynamics on the nano-satellite. The hold-down mechanism is under patent and is not addressed in this paper.

2 Literature Survey and Option Studies

Solar panels for nano-satellites have been employed in body-mounted [1] and deployable [2] configurations. The concept of extendible solar arrays for nano-satellite has also been explored [3]. In addition, work is being carried out on origami based solar array deployment concepts [4].

For deployable solar panels, a variety of hinges have been developed for Nanosat/CubeSat class of satellites ranging from torsion spring based to tape spring based hinges with or without locking provisions. Hodoyoshi Project [5] of Japan employed helical spring for deployment and locking. Single spring was used for deployment and engaging of the latch for locking. Xatcobeo mission [6] used torsion spring based single hinge for the deployment and flat spring for latching of the hinges at the end of deployment. Tape spring based single component hinges with self-locking capabilities as proposed in [7] are an optimized solution. The work in [8] discussed the deployment analysis of tape spring hinge in detail. The deployment hinges of KufaSat [9] and IMT 3U [10] incorporate torsion spring based hinges. The hinges after deployment butt against the hard stopper without latching. In [11], the work presented the verification of solar panel deployment in microgravity conditions in parabolic flight path.

Hinges for Hodoyoshi Project and Xatcobeo mission deployed multiple panels in a single array and used latch mechanism which invariably introduces friction. The main disadvantage of tape springs is that they are prone to cracking due to mishandling as they are made up of thin sheet metals. Hinges for Kufasat lacked inbuilt deployment indication switches. Absence of a single optimized solution resulted in the design of a new hinge and deployment mechanism.

Most fundamental requirement for the mechanism for nano-satellites is the optimization of mass. Moreover, in order to make the overall testing proposal simple, hinges are required to be designed to deploy under Earth's gravity (1 g) condition. This requires increased hinge torque and thus improves the deployed stiffness of

the panel and allows the elimination of a dedicated latch mechanism resulting in a compact mechanism. Considered options for the hinge mechanism are shown in Fig. 1.

A miniaturized hinge using plain journal bearing as shown in option C is implemented which is deployed using a torsion spring. After deployment by 90°, the fork-end bracket butts against the stopper on eye-end bracket. The deployment indication is obtained by making use of a leaf switch wherein electrical contact is established when the outboard bracket touches both the live and return indication leaves.

3 Solar Panel Deployment Mechanism

The nano-satellite consists of two deployable solar panels mounted on two opposite decks of the satellite. The panels are held in stowed condition by a hold-down mechanism. After hold-down release, spring driven hinge mechanism rotates the panel about the hinge axis. The panel rotates by 90°, hits the stopper bracket on the hinge and rebounds. The panel oscillates a few times before eventually settling down in the deployed state. Positive spring torque by the deployment torsion springs holds the panel in the deployed state against folding back. The stowed and deployed view is shown in Fig. 2.

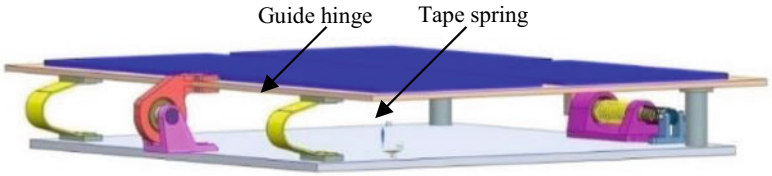
Two configurations of solar panels, as listed in Table 1, are analyzed and details are presented in Sect. 4.

4 Multi-Body Dynamics Analysis

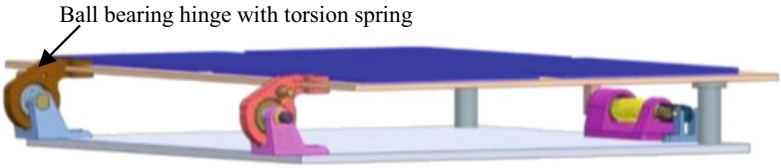
4.1 Settling Time Analysis for Single Panel

Time history for the panel oscillations to die-down is evaluated for configurations1 and 2, for both ground and on-orbit deployment simulations. Analysis is carried out by developing the multi-body dynamics model in MSC ADAMS. Measured hardware characteristics viz., mass, inertia, torsion spring characteristics, dissipative forces etc. are modelled. Effects of 1 g forces are considered for ground deployment simulation. Contact is simulated at the hinge stopper interface to represent the physical behavior. Contact stiffness is derived using finite element analysis whereas the damping coefficient for the contact is obtained from the ground test results.

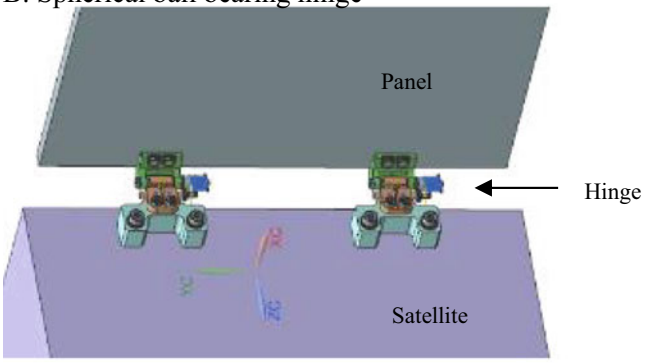
Results. Time taken for the panel to settle in the deployed state is presented in Fig. 3 for on-orbit scenario. The actuation of hold-down initiates at $t = 0$ s and hold-down release is assumed to occur nominally at $t = 1$ s. It can be observed that deploying solar panel touches the mechanical stopper at 90° of deployment, bounces back and forth several times and finally settles down in intended deployed condition. The time for ground deployment is more as the hinge friction due to self-weight of



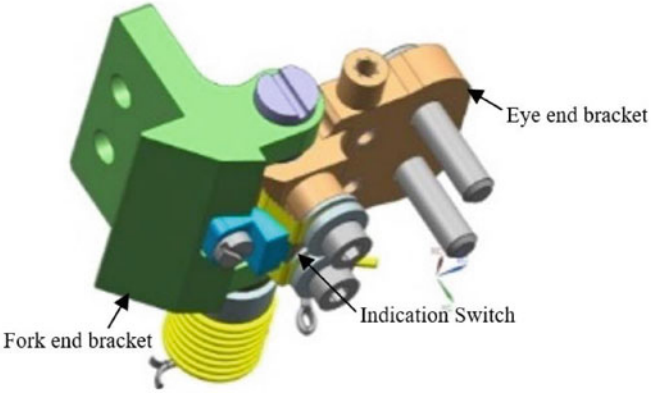
A. Tape spring hinge



B. Spherical ball bearing hinge

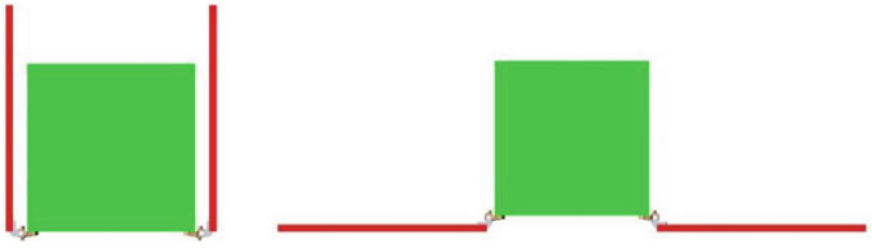


C-1: Configuration of plain journal bearing hinge



C-2: Detailed design of plain journal bearing hinge

Fig. 1 Options considered for hinge design



a. Stowed b. Deployed

Fig. 2 Stowed and deployed view of nano-satellite solar panels

Table 1 Two configurations of solar panels

Configuration	Solar panel		
	Dimensions	Mass	Inertia (about hinge)
1	250 × 235 × 20 mm	250 g	0.6E-2 kgm^2
2	335 × 250 × 20 mm	399 g	1.4E-2 kgm^2

the panel influences the ground deployment. The results for both ground and on-orbit deployment are summarized in Table 2.

It is observed that the number of oscillations, corresponding time period and the final settling time for config-2 solar panel is higher when compared to config-1. This

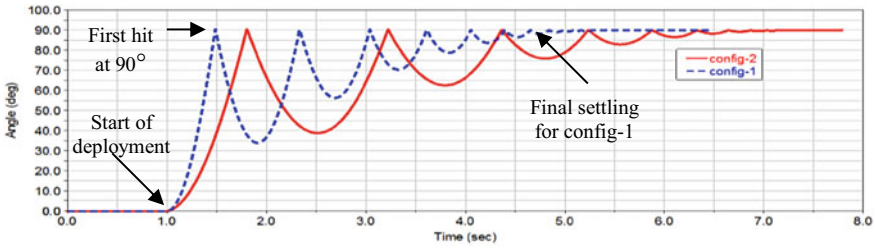


Fig. 3 Deployment angle (degree) versus time (s) for on-orbit deployment simulation

Table 2 Time line of events

S. No	Event	Ground time (s)		On-orbit time (s)	
		Config1	Config2	Config1	Config2
1	First hit at 90°	1.48	1.84	1.47	1.80
2	Final settling at 90°	4.0	5.2	4.8	6.7

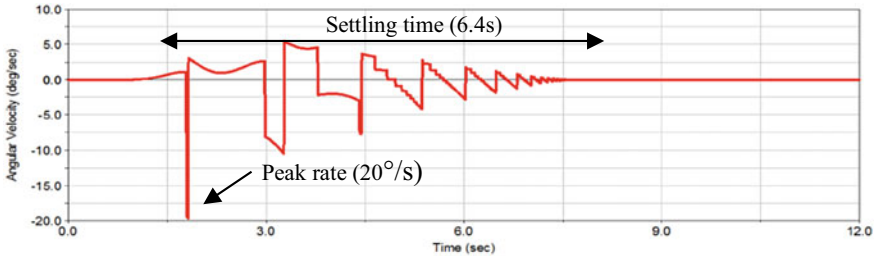


Fig. 4 Nano-satellite angular velocity during deployments—Analysis

is attributed to the fact that config-2 has a higher mass moment of inertia, resulting in lower frequency and hence longer time period of oscillation.

The hinge brackets are also analyzed for the latch-up loads due to deployment and it is observed that stress margin exists over yield strength of the bracket.

4.2 Spacecraft Body Rates During Deployment

Multi-body dynamics model of the nano-satellite along with both the solar panels is developed in MSC ADAMS and analysis is carried out for measured hardware parameters including the overall mass and inertia of the spacecraft. The simultaneous deployment of both solar panels is carried out which induces reaction rates on the nano-satellite. The rates induced on the spacecraft and the time taken by the rates to settle down are evaluated.

Results. The nano-satellite angular velocity (body rate) about the axis parallel to hinge axis of solar panel is presented in Fig. 4. A peak rate of nearly 20°/s is observed with a settling time of 6.4 s.

4.3 On-Orbit Deployment Observations

The analysis results are compared with on-orbit performance data obtained through spacecraft telemetry. The actual body rates observed during on-orbit deployment of the solar panels are presented in Fig. 5. It is observed that the peak body rate change of nearly 14°/s is observed with a settling time of nearly 5.6 s. The status indication changes of both solar panels from 'stowed' to 'deployed' is also presented. The comparison between analysis prediction and on-orbit observation is shown in Table 3.

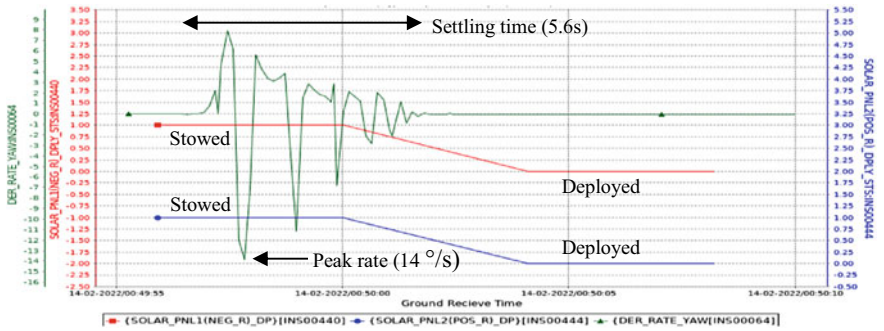


Fig. 5 Nano-satellite angular velocity during deployments—On-Orbit observations

Table 3 Comparison of analysis predictions and on-orbit observations

	Peak rate	Settling time
Analysis prediction	20°/s	6.4 s
On-orbit observation	14°/s	5.6 s

5 Conclusions

A compact hinge mechanism for solar panel deployment is developed to meet the mass and size constraints for nano-satellite. The miniature hinge is configured without an active lock mechanism. Torsion spring is designed to ensure margins for deployment in Earth's gravity.

Behavior of deploying panels in absence of an active lock at hinge is analyzed together with its impact on the nano-satellite. Two configurations of the panel with different sizes are considered. It is observed that the config-2 panel takes 1.9 s longer to settle down after deployment due to its higher inertia and lower frequency. This calls for a longer monitoring time for deployment event by the on board computer (OBC). It implies that after deployment initiation, OBC must wait before other critical spacecraft events are executed. Even though the settling time increases, the clear advantage of using a bigger panel is the increased area for solar cells and hence more power for the satellite. The config-2 panel is implemented for the nano-satellite.

During the on-orbit deployment, both panels are commanded to deploy simultaneously. For this scenario, analysis results predict a peak body rate change of 20°/s and a total settling time of 6.4 s. Actual on-orbit observations indicate a peak rate of 14°/s and settling time of 5.6 s. The observed settling time is in good agreement with the analysis prediction. However, as the rate build up is very fast, the existing on-orbit data sampling rate may not be fine enough to capture the actual peak and this contributes to the observed difference in predicted and observed rate. The overall trend of the satellite body rate observed on-orbit also compares well with the analysis prediction as shown in Figs. 4 and 5.

Acknowledgements Authors would like to express their gratitude towards Director URSC, Shri M Shankaran for the opportunity to work on the said project and exhaustive reviews which lead to flawless performance on-orbit. Gratitude and appreciation is extended towards Shri K Prakash, Shri Umesh BV and Shri P Balamohan for the untiring effort towards system realization and testing.

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Design and Development of an Electrical Power System for a 3U Cubesat

M. Varsha, J. Stephen, S. Divya, and R. S. Geetha

Abstract Electrical Power System (EPS) is an important component of a satellite. The design and implementation of EPS to cater to the power demand of all the subsystems of the satellite is a challenging task. This work details the design and simulation of an efficient Electrical Power System for a 3U CubeSat. The objective is to build and launch a student satellite in Low Earth Orbit and perform on-orbit operations to demonstrate the imaging of the Earth's surface, high altitude operations, and de-orbiting maneuver. The EPS was designed taking into consideration the power requirement from all the subsystems of the satellite. The system design includes a battery tied bus consisting of surface mounted and deployable solar panels, Lithium-ion batteries with over-voltage and under-voltage control. The EPS also involves the design of a highly efficient controllable power distribution system consisting DC–DC Converters which are capable to provide 3.3 V and 5 V regulated DC supply as well as unregulated supply.

Keywords Surface mounted and deployable solar panels · Electrical power system (EPS) · Power budget · Upper threshold potential (UTP) · Lower threshold potential (LTP) · DC–DC converters · Lithium-ion battery

M. Varsha (✉) · J. Stephen · S. Divya · R. S. Geetha
Department of Electrical and Electronics Engineering, B.M.S College of Engineering, Bengaluru, Karnataka 560019, India
e-mail: varsha.ee18@bmsce.ac.in

J. Stephen
e-mail: stephen.ee18@bmsce.ac.in

S. Divya
e-mail: divyas.eee@bmsce.ac.in

R. S. Geetha
e-mail: rsgeetha.eee@bmsce.ac.in

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_13

1 Introduction

A Nanosatellite is a satellite with a mass ranging from 1 to 10 kg. The power usage of nanosatellites is restricted due to the power generation ability of each satellite and the power which may be delivered to systems, usually less than 30 W [1]. CubeSats are a type of nanosatellite with typical dimensions: 10 cm × 10 cm × 30 cm and are 3U in size. They must meet a set of strict requirements that govern things like shape, size, and weight. Because of the power requirements and limits, CubeSats must adhere to a stringent power budget. Because of the narrow surface available for solar panels and the limited bulk and space to accommodate batteries, they have limited energy sources. The main advantages of CubeSats are lower cost, faster production, and easier deployment to perform high risk scientific experiments [2]. They are getting growing attention in the academic and industrial space fields, and they can be utilized in low-cost technology demonstrations for advanced space engineering concepts [3].

The proposed satellite is a three-axis stabilized imaging satellite. It is a 3U CubeSat weighing 5 kg. Using Telemetry and telecommand, all subsystems must be controlled and managed during mission operations [4]. The requirements, specifications and design details of the Electrical Power System are detailed in this article.

The Electrical power system generates, stores, conditions, controls, and distributes power under the specified voltage limits to the payload and bus [3]. The EPS is classified mainly into three subsections namely,

Power generation using Solar Arrays.
Power storage with the help of Battery.
Power conditioning and distribution using DC–DC converters.

The EPS is regarded as a critical component of the satellite, as the mission would be terminated without it. As a result, having a reliable and steady power system is critical. The sizing of batteries and solar panels is determined by the payload(s) requirements and the mission's lifetime [3]. Different modes of operation, such as detumbling mode and contingency operations, were considered when sizing the solar array.

Solar panels charge the batteries with blocking diodes that protect against reverse polarity. It protects the solar panel from being damaged if it is connected to the input in the wrong way. Power is subsequently delivered to various subsystem loads from the solar panels via 5 V and 3.3 V DC–DC Converters and unregulated power buses or from battery as well. To prevent damage from a short circuit, these buses feature over-temperature and over-current protection, and the battery has under-voltage protection to prevent a total discharge [3].

Table 1 Orbital parameters

Parameter	Value
Orbit type	Polar sun synchronous
Orbit altitude	500 km
Orbit inclination	97.5 deg
Orbital period	95 min
Sunlit duration	62 min
Eclipse duration	33 min

2 Requirements for EPS Design

2.1 Orbital Parameters

Analyzing the orbital parameters is the first step in designing the power system. The kind of orbit, its inclination, and its altitude are the three major satellite orbital factors that determine the EPS design. They're used to calculate the sunlit and eclipse periods, as well as the orbit period and the solar angle (β) between the orbit plane and the Earth–Sun line [3]. Table 1 shows the proposed 3U CubeSat's orbital parameters.

2.2 Load Power Data

The EPS has to fulfill the power demands of all the other subsystems which are involved in various satellite operations using 3.3 V and 5 V voltages from a fault tolerant power distribution network. The power requirements within the satellite vary during time and are not correlated with the power production, requiring the use of a battery even in illuminated conditions [5]. It varies depending on modes of operation of the satellite such as Payload Operation mode, detumbling mode, 3 axis acquisition mode and data transmission mode. The peak and continuous power consumptions of various subsystems in an orbit during sunlit and eclipse time is shown in Table 2. The payload of the satellite is a high-resolution Camera which captures the images of the Earth's Surface. The payload operation takes place three to four times in a day only during the sunlit time. The power requirement during the payload operation is given in Table 3.

3 Design

The designed Electrical Power system consists of power source, energy storage, power regulation and control, power conversion and distribution [6]. The energy is transferred from the source to the subsystem loads through the main power bus and

Table 2 Continuous power and peak power consumption of subsystem loads

Subsystems	Continuous power (W)		Peak power (W)	
	Sunlit	Eclipse	Sunlit	Eclipse
TTC and OBC	2.05	2.05	2.05	2.05
ADCS	3.27	3.27	9.45	9.45
Heaters for battery	1	0	1	0
RF communication	2.96	2.96	2.96	2.96
Payload (standby mode)	0.38	0.38	0.38	0.38
Total	9.66	8.66	15.84	14.84

Table 3 Power consumption during the payload operation

Subsystems	Components	Power (W)
Payload	Nanocap C1U (for acquisition and processing)	1.3
RF communication	Payload transmitter and receiver	1.5
	Power amplifiers for downlink payload	2.18
	Low noise amplifiers	0.71
Thermal control system (TCS)	Heaters (for camera)	1.10
Total		6.8

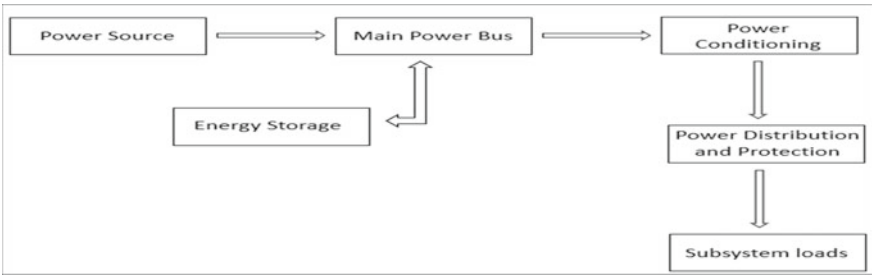


Fig. 1 General schematic of EPS

it is monitored and controlled by the Onboard control system. The general schematic of the entire process is shown in Fig. 1. The arrow mark shows the direction of flow of energy.

3.1 Solar Panels

The Solar Panel is the primary energy source, which provides the necessary voltage and current to the CubeSat components of various subsystems. And solar array sizing

Table 4 Specifications of solar cell

Parameter	Value
Voc	2.7 V
Isc	0.457 A
Vmp	2.411 V
Imp	0.4428 A

Table 5 Total power consumption

Sunlit continuous power	9.662 W
Eclipse continuous power	8.662 W
Total duration of payload operation per day	50 min
Average payload power over one day (Ppl)	0.235 W

depends on the load requirements as well as the efficiency of the converters used to get the required power efficacy. In this work, the AZURE Space TJ Solar Cell 3G30C was selected as per the requirements. It is a 30% Triple Junction GaAs Solar cell; It has a cell dimension of 39.55 * 68.98 mm, with parametric values necessary for design as shown in Table 4 [7].

The 3U model of a CubeSat was used as reference to carry out the solar panel sizing and configuration design [8]. The power to which the solar array has to be sized depends on sunlit and eclipse continuous power, average payload power over the duration of one day, charge power fed to the battery during sunlit time and losses in the series elements such as DC–DC Converters and solar cell blocking diodes.

The average payload power has been calculated based on the number of payload operations taking place in one day. According to the satellite requirements, 4 to 5 payload operations lasting for 8–10 min each take place where the satellite comes into the visibility of the ground station. The estimated total power consumption is shown in Table 5.

Based on the data obtained from Table 5, the charge power and the total bus power is calculated using Energy Balance equations which is as follows.

$$Wh^{-} = P_e * T_e \tag{1}$$

where,

Wh^{-} Watt hour requirement during eclipse mode.
P_e Eclipse Continuous Power.
T_e Eclipse duration.

$$Wh^{+} = K * Wh^{-} \tag{2}$$

where,

Wh^+ Watt hour that has been fed to the Battery.
K 1/Efficiency of Battery.

$$Pch = \frac{Wh^+}{Tsl} \tag{3}$$

where,

P_{ch} Charge power that has to be fed to the Battery.
T_{sl} Sunlit duration.

$$P_{bus} = P_{sl} + P_{ch} + P_{avg} \tag{4}$$

where,

P_{bus} Total Power required at bus end.
P_{sl} Sunlit Continuous Power at bus end.
P_{avg} Average Payload Power at bus end.

Determination of Orbit Duration.

The time taken by the satellite to complete one orbit in the Low Earth Orbit, and the duration of Sunlit and eclipse time each was determined with the help of a Simulation Software known as System Tool Kit (STK). The default satellite object was loaded in the software, and the Polar sun synchronous orbit type was selected. The simulation results obtained are summarized in Table 6.

Thus, the total orbit time was determined to be 95 min (1.583 h) with sunlit duration being 62 min (1.03 h) and eclipse duration being 33 min (0.55 h). With this data, the computation of charge power was calculated as described in the following section.

Computation of Charge Power.

The energy balance Eqs. (5)–(8) are used to compute the necessary charge power required for the battery during sunlit time. From Table 6, the eclipse duration is 0.55 h. Table 5 gives the eclipse continuous power at the load end. Including the losses in the power conditioning and distribution gives the eclipse continuous power at the main bus [10]. Considering a typical 85% efficient power conditioning and distribution

Table 6 Orbital duration from STK

Mode	Sunlit time	Eclipse time
Time stamp	12:08:55 to 13:10:30	13:10:35 to 13:43:30
Total duration	62 min	33 min
Total orbit time		95 min

unit and Battery efficiency of 90%, the energy required to be fed to the battery during sunlit time and the charge power is computed which is shown in Table 7.

The total power required at the main power bus is a sum of Sunlit continuous power, charge power and average payload power at the main power bus considering 15% loss in the power conditioning and distribution unit of the EPS. The heaters present in the satellite are supplied from the unregulated bus which has to be considered in the bus power requirement separately. The power required to be generated by the Solar Array is given by the Eq. (6).

$$P_{bus} = P_{sl} + P_{ch} + P_h + P_{avg} \tag{5}$$

$$P_{sa} = P_{bus} + P_l + P_{marg} \tag{6}$$

where, P_{bus}: Total power required at the main bus.

P_L: Power loss in the solar cell blocking diodes.

P_{mar}: 15% Marginal Power.

P_h: Power required for heaters.

Solar Panel Configuration.

The proposed solar panel configuration is shown in Fig. 2. It consists of one surface mounted and three deployable panels oriented at single plane with each panel having seven 30% Triple Junction GaAs Azure Space solar cells in series. This was chosen based on the power required to be generated by the solar array as shown in Table 8. The deployable panels were mainly. considered since the type of orbit chosen is polar sun synchronous orbit. The specification of the proposed configuration is as shown (Table 9).

The power generated by the three panels when it is subjected to extreme temperature conditions is shown in Table 10.

Table 7 Charge power and energy requirements

Total eclipse duration (T_e)	0.55 h
P_e (load end)	8.66 W
P_e (bus end)	10.19 W
Whr^-	4.76 Whr
Whr^+	5.29 Whr
P_{ch}	7.05 W

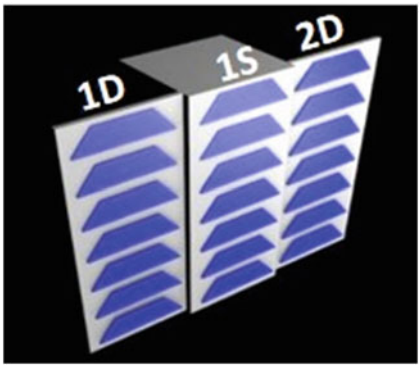


Fig. 2 Proposed solar panel configuration

Table 8 Power requirements at load end and bus end

P_{sl} (load end) without heater	8.66 W
P_{sl} (bus end) without heater	10.18 W
P_h	1 W
P_{ch} (bus end)	7.05 W
P_{avg} (bus end)	0.28 W
P_{bus}	18.5 W
P_L	1 W
P_{sa}	22.5 W

Table 9 Solar panel specifications

No of cells per panel	7
Voltage at maximum power	16.85 V
Current at maximum power	503 mA
Average open circuit voltage per panel	18.8 V
Average short circuit current	520 mA
Maximum power generated per cell	1.2 W
Maximum power generated per panel	8.4 W
Maximum power generated by 3 panels	25.2 W

Table 10 Power generated at different temperatures

Temperature	Power generated by each solar panel	Power generated by three panels
At 28 °C	8.4 W	25.2 W
At 55 °C	8 W	24 W
At 100 °C	7 W	21 W

3.2 Battery

An electric battery is made up of one or more electrochemical cells with connections externally that can be used to power electrical equipment [11]. The battery acts as a secondary energy source during the eclipse, as the solar panel cannot generate power. Thus, the power generated by the panels during sunlit mode is used to charge the battery and this energy is used to power the subsystem loads during the eclipse mode.

State of the art commercial 18,650 Li-ion cells were selected; rated for 3.5 V, 3.5Ah Table 11. The configuration of the battery is decided based on the duration of detumbling mode shown in Table 12, which is five orbits, and the load to be supplied during the eclipse mode, which is for a duration of 33 min shown in Table 13.

The satellite, when released into orbit, is continuously rotating about all its axes. The process of slowing the rotation of the satellite in orbit is called Detumbling [12]. Detumbling using a controller known as B-Dot Controller requires power to be consumed by the magnetic torques, which are responsible for the detumbling to occur using a magnetic field. The time constraint for this process is considered as 5 orbits based on the simulation results of the ADCS Subsystem.

Table 11 Specifications of a single Li-ion cell

Nominal voltage of Li-ion cell	3.5 V
Maximum charge voltage per cell	4.2 V
Ampere hour capacity of cell	3.5 Ahr

Table 12 Power requirements during detumbling mode

Subsystem	Voltage (V)	Power (W)
TTC and OBC	3.3	2.04
ADCS	5	5
Total (Considering 85% converter efficiency)		8.28

Table 13 Power requirements during eclipse mode

Subsystem	Voltage (V)	Power (W)
TTC and OBC	3.3	2.04
ADCS	3.3	2.1
RF	3.3	1.5
Payload	3.3	0.38
ADCS	3.3	1.18
RF	3.3	1.46
Total (Considering 85% converter efficiency)		10.18

Table 14 Detumbling mode and eclipse mode energy requirement

Mode	Power	Duration	Energy required
Detumbling mode	8.28 W	475 min (5 orbits)	65.55 Whr
Eclipse mode	10.18 W	33 min	5.60 Whr

The detumbling mode energy requirement and eclipse mode energy requirement has been shown in Table 14.

Energy rating of the battery:

$$Ns * Np * Vn * Ahr \tag{7}$$

where, N_s: No of battery cells in series.

N_p: No of battery cells in parallel.

V_n: Nominal voltage of each battery cell.

Ahr: Ampere hour capacity of each battery cell.

The Watt hour capacity or energy rating of the battery is given by Eq. (7). The specifications of the selected battery are shown in Table 15.

By preventing the battery from discharging by more than 30% of its SOC during the detumbling mode, it should be taken care that sufficient energy is available for subsequent orbital operations. Thus, watt hour requirement during detumbling must not exceed 70% of battery's total energy capacity. Also, the watt hour requirement during eclipse mode must not exceed 20% of battery's total energy capacity [9]. Such a comparison summary was carried out between different battery configurations which led to the selection of 3S-3P (3 series–3 parallel) configuration for Li-ion Battery.

Power Conditioning Unit

The Power Conditioning unit is an integral and most critical part of the Electrical Power Subsystem in a 3U Satellite. It is responsible for providing the conditioned power to all the subsystem loads. It improves the quality of the incoming unregulated power from the bus and supplies the current to all the subsystem loads at required voltages for them to function properly. The Power Conditioning unit present in the

Table 15 Battery specifications

Configuration	3S-3P
Nominal voltage	10.5 V
Maximum charge voltage	12.6 V
Energy rating of the battery (E)	110.5 Whr
Energy used during the eclipse mode (20% of E)	22.5 Whr
Energy used during the detumbling mode (70% of E)	77.18 Whr

Table 16 Specifications of DC–DC converter

Input voltage range	3.4 V to 42 V
Maximum continuous output current	5 A
Switching frequency range	0.2 MHz to 3 MHz

proposed EPS consists of two Step-down DC–DC Converters which convert the bus voltage to 3.3 V and 5 V providing a maximum current of 5A respectively.

The LT8640 Step-down DC–DC Converter IC was chosen for its high efficiency, low ripple, ultra-low EMI, high operating junction temperature, adjustable PWM Frequency and resistor programmable variable output voltage [14]. It provides 3.3 V and 5 V. The internal switches used in the IC have ultra-low Drain to source resistance and ultra-low quiescent current. The specifications of the IC are shown in Table 16.

The input voltage to the Step-down DC–DC Converter in the proposed EPS is the bus voltage which is maintained at 10.5 V–12.6 V based on the voltage of battery and the solar array voltage. The inductor is chosen based on the required output voltage and switching frequency. The output voltage is set with a resistance divider circuit connected between the output and the feedback pin of the Converter. The resistor values are chosen according to:

$$R_1 = R_2 * \left(\frac{V_{out}}{0.970} - 1 \right) \tag{8}$$

The design parameters for obtaining 3.3 V and 5 V from the Converter is shown in Table 17. The schematic of the Step-down Converter IC for providing 3.3 V and 5 V is shown in Figs. 3 and 4. The R2 value of both 3.3 V and 5 V converter has been slightly decreased from the designed value to obtain 3.5 V and 5.2 V to account for voltage drops in the Power distribution switches connected between the Step-down Converter and the subsystem loads.

The DC–DC Converter IC Models were simulated on Ltspice Software from Analog Devices to test its working. The input voltage is 12 V which can be considered as the bus voltage. The respective output voltage waveforms are shown in Fig. 5.

Table 17 Design parameters

Parameters	3.3 V converter	5 V converter
Switching frequency	1 MHz	1 MHz
R1	1 MHz	1 MΩ
R2	412 kΩ	243 kΩ
L	2.2 uF	3.3 uF
Rt	41.2 kΩ	41.2 kΩ

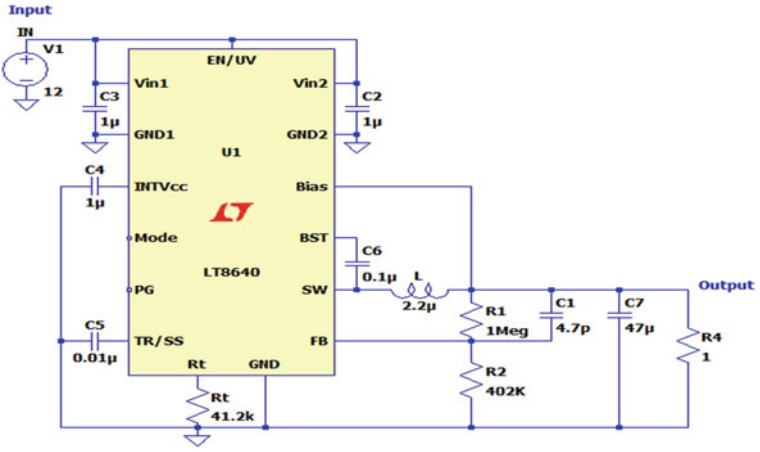


Fig. 3 3.3 V converter (LT8640)

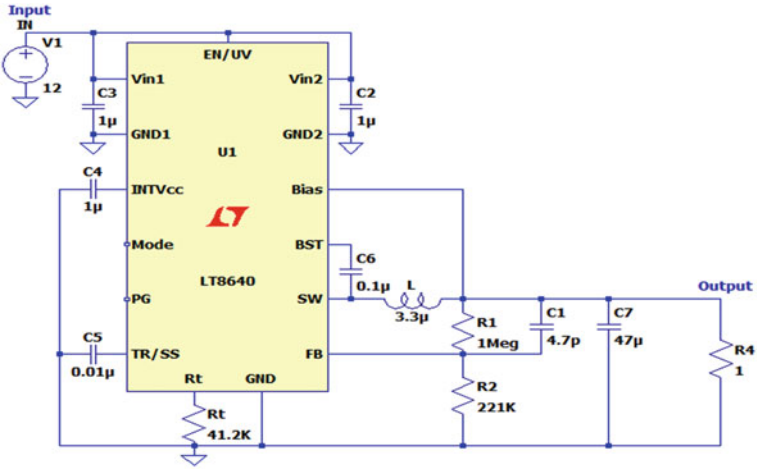


Fig. 4 5 V converter (LT8640)

4 Block Diagram of EPS and Simulation

Figure 6 shows the schematic of the proposed Electrical Power system for the 3U Satellite. The type of Power system architecture for the proposed EPS is Battery tied bus. 1S, 1D and 2D represent one surface mounted and two deployable panels connected in parallel each consisting of 7 cells in series. A 3S-3P Battery consisting of nine 3.5 Ahr Li-ion cells is connected to the main bus. The shunt MOSFET Switches which are connected between the Solar panels and the bus provides overcharge and undercharge control of the Battery. The gate terminals of the three shunt switches are

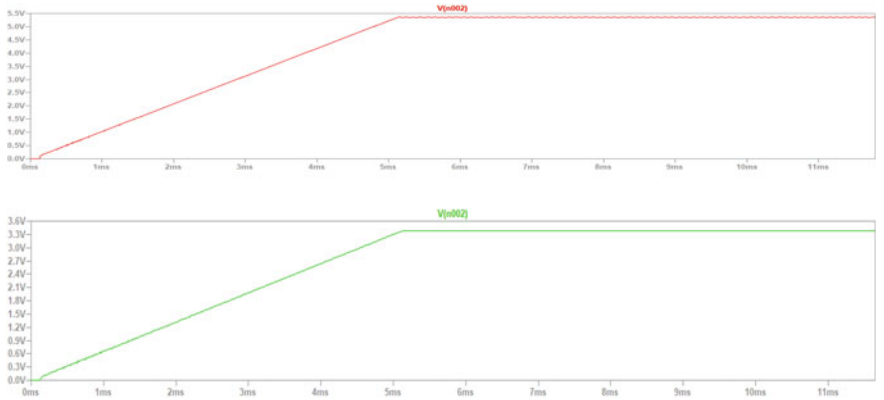


Fig. 5 Converter output voltage waveforms

controlled by the OBC Subsystem of the Satellite. This is known as UTP-LTP Bus Control where UTP and LTP stands for upper threshold potential and LTP stands for lower threshold potential. The control mechanism is explained below.

Consider a case of Battery charging from the panels during the sunlit time. The full charge voltage of the Battery is 12.6 V. Initially, the Battery voltage is low and the shunt switches are open. Now, the Battery starts charging with a current, whose value is the difference of Source and Load. As shown in Table 18, when voltage across the Battery reaches UTP Level, shunt switches are turned on which shunts the panel strings sequentially. Now the Battery starts discharging through the load and when Voltage reaches LTP Level, the shunt switches are turned off sequentially which connects the panel string to the Battery. The operation of the two shunt switches is explained below.

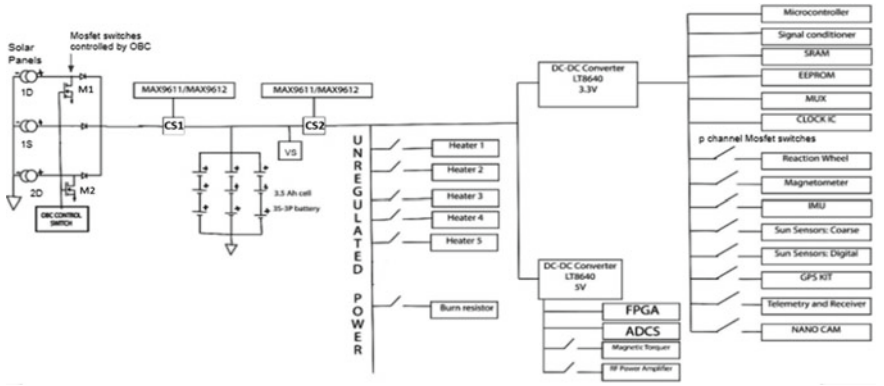


Fig. 6 EPS schematic

Table 18 UTP and LTP for the shunt switch operation

Shunt switches	LTP value (Strings ON)	UTP value (Strings OFF)
M1	12.1 V	12.5 V
M2	12.2 V	12.6 V

When the Battery voltage reaches 12.4V, MOSFET M1 is switched on and the panel 1D gets shunted.

When the Battery reaches full charge voltage of 12.6V, the MOSFET M2 is turned on and the panel 2D gets shunted.

Then 1S panel string will always be on and serving the S/C loads and at no time all panels will be shunted ensuring that the EPS Design supports the load requiring greater than one solar array string current.

A Current sense Amplifier 1 (CS1) is connected at the solar array output which measures the current supplied by the solar array during sunlit. The sensor element of the current sense amplifier is just a resistor and will be connected in series. So, the resistance of the resistor must be as low as possible. The current sense resistor will be 10 or 20 milliohms. When 1A current flows through this resistor, the voltage across the resistor will be around 10 mV–20 mV. This voltage output signal will be amplified to 3.3 V or 5 V by the current sense amplifiers for the spacecraft telemetry.

Another Current Sense Amplifier 2 (CS2) is connected to the bus after the Battery which measures the current supplied by the battery to all the subsystem loads during eclipse. The difference between the values of CS1 and CS2 will give the battery charge current in sunlit. If the difference in current is negative, then that means Battery is discharging in sunlit. If the difference is positive, then Battery is charging in sunlit. This difference data will be captured in the spacecraft telemetry and thereby the status of the Battery will be known. Since the step-down DC–DC Converters are getting the supply either from battery or solar panels, two sensors are more than adequate to get to know the power consumed by different subsystems of the spacecraft. A Voltage sensor VS is also connected to the bus after the Battery. It consists of a simple potential divider circuit which is used to limit the voltage to MUX, DEMUX, A to D Converters or D to A Converters.

The unregulated power generated at the bus is fed to the five heaters which maintains the temperature of the Battery and the Payload (Camera) of the Satellite. The heaters will be supplied with unregulated Power only during the sunlit and will be switched off during the eclipse as Battery discharge itself is sufficient to keep the temperature at the optimum level.

The unregulated power is converted to regulated power with the help of step-down DC–DC Converters. The first LT8640 Converter IC provides 3.3 V Output to Payload (Camera) and some of the loads of OBC, ADCS, and RF Subsystem as shown in the schematic. The second LT8640 Converter provides 5 V Output to some of the loads such as FPGA (TTC and OBC), Magnetic Torquer (ADCS) and RF Power Amplifier. A power distribution switch which is basically a p-channel MOSFET is connected between the Converter and some of the loads in order to have a control on supply to the

loads based on the requirement. Some of the loads such as Microcontroller, SRAM, EEPROM, and MUX are not provided with the switch since they are responsible for capturing the spacecraft telemetry and hence will be kept ON throughout the orbit.

The MATLAB Simulation Model of the EPS is shown in Fig. 7. It consists of Solar Panel Model, Battery Model along with Power Conditioning and distribution Model. The Solar Panel Model is shown in Fig. 8. Each block in the model is made of seven solar cells in series whose arrangement is shown in Fig. 9. Three such blocks each representing the surface mounted and deployable panels are parallelly connected to form a Solar Panel Model [13]. The simulated V-I and P-V characteristics of a solar cell is shown in Fig. 10. It is observed that the performance drops when the cell operates at maximum voltage point. The Solar Cells in 7S-3P configuration provides the necessary power required as per the calculations. The Shunt switches are connected in parallel to each panel, to dissipate the excess power generated by shunting the respective panel, if the battery voltage is above a certain threshold during charging.

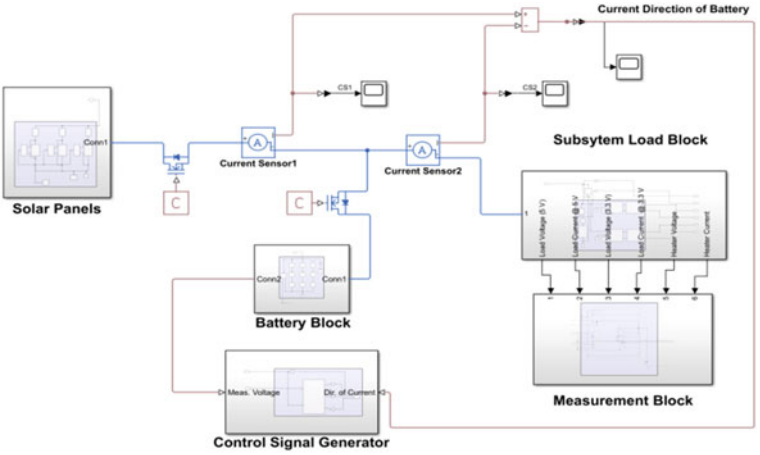
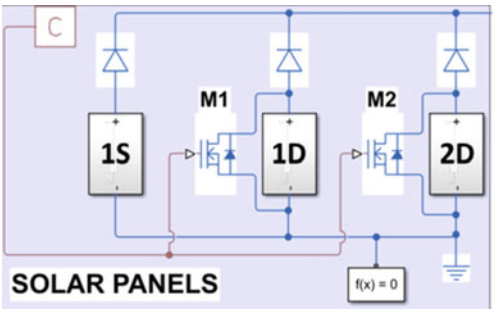


Fig. 7 MATLAB simulation model of EPS

Fig. 8 Solar panel block



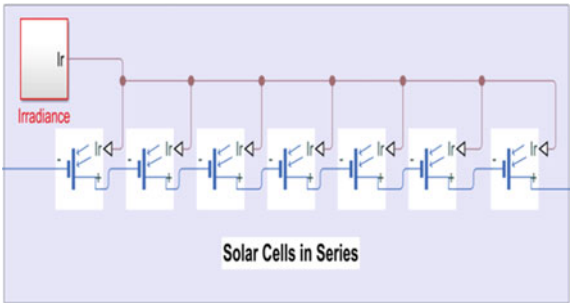


Fig. 9 Seven cell series arrangement in a solar panel

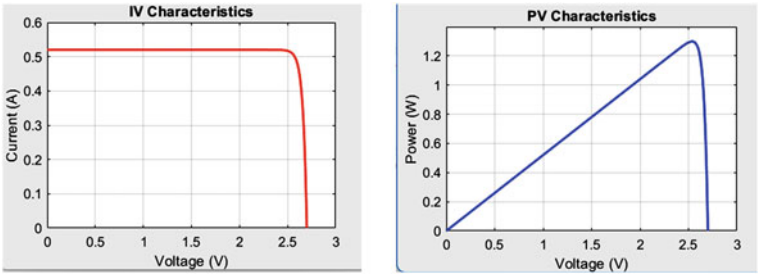


Fig. 10 Typical characteristics of solar cell from the simulation

And the switch turns off when the voltage across the battery drops below the threshold during discharge. The secondary-source battery simulation model is shown in Fig. 11. The Li-ion cells are in 3S-3P configuration. The voltage across the battery is measured to control the operation of the shunt switches connected across the panels.

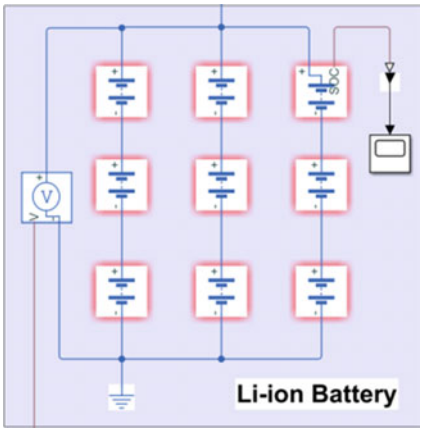


Fig. 11 Li-ion battery model

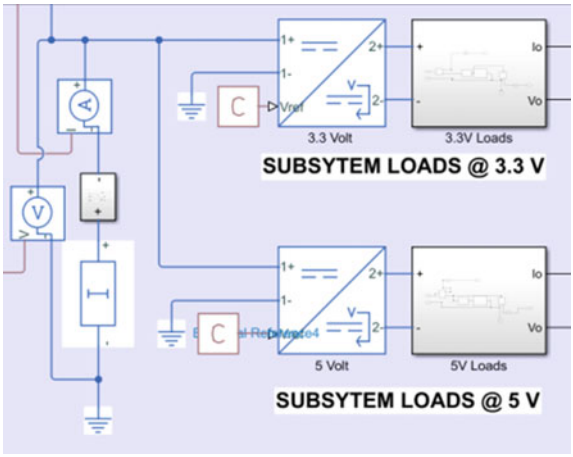


Fig. 12 Power conditioning and distribution model

The Control Signal Generator Model and the corresponding circuit for UTP and LTP Control of the Battery are shown in Fig. 13. The two voltage values are modeled as constant reference blocks, and the UTP and LTP switch checks if the measured battery voltage has exceeded the threshold during charge or discharge respectively. The charge and discharge of the battery is inferred from the current sensors, which measure the current from Solar panels and current to the load. This enables the generator to generate the necessary control signal which controls the shunt switches across the panels.

The Power Conditioning and Distribution Model are shown in Fig. 12. It consists of 3.3 V and 5 V DC–DC Converters which provides the regulated power to subsystem loads. The subsystem loads are divided into three parts, the load which requires unregulated power and the loads which require regulated power at 5 and 3.3 V respectively. The load current is modeled as constant current load as required. The corresponding Load Voltage and Current waveforms obtained are shown in Fig. 14. The load power drawn from the system is shown in Fig. 15 which shows a drop in power drawn in eclipse as battery heaters will be switched off during the eclipse.

5 Conclusion

In this paper, the design of an Electrical Power system for a 3U CubeSat is described considering the power requirements of different subsystem loads of the satellite. The Solar panels and Battery sizing were carried out based on the load requirements during various modes of satellite operation such as Sunlit mode, eclipse mode, payload mode and detumbling mode. The design and selection of efficient Step-down DC–DC Converters were carried out and its operation was verified in

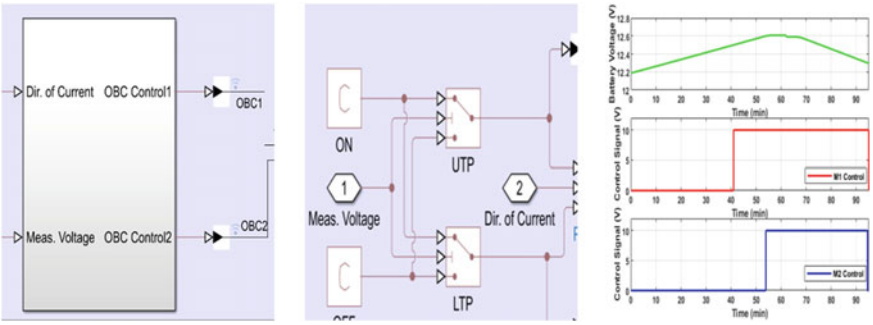


Fig. 13 Control signal generator simulation model, circuit and control signals

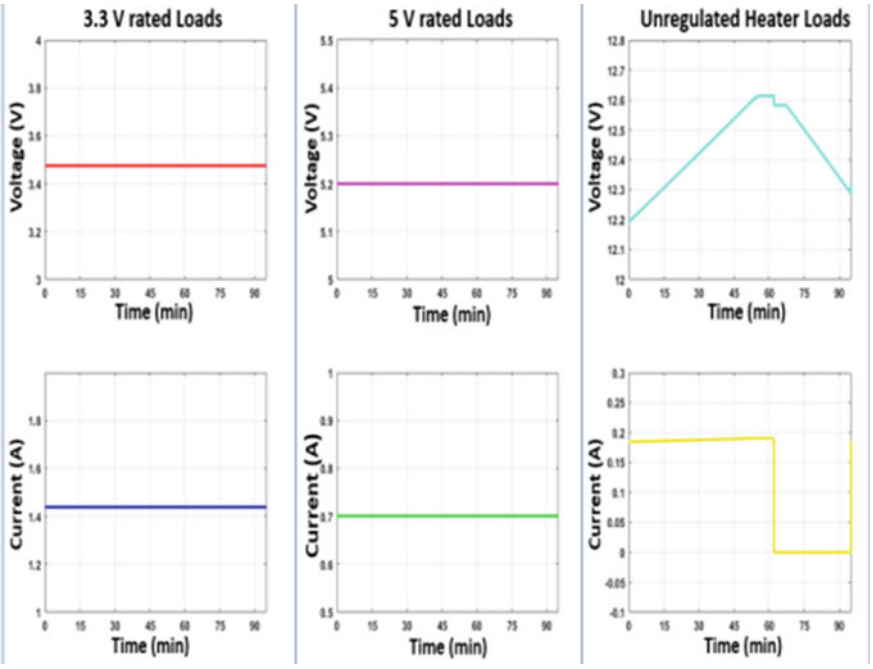


Fig. 14 Load voltage and current waveforms

simulation. The EPS Schematic was implemented and has been presented whose key features include overvoltage/undervoltage protection using MOSFET Switches, current sensing, battery status capturing, efficient Power conversion and distribution. The EPS Simulation was carried out on MATLAB to demonstrate the Power Consumption of the subsystem loads during on-orbit operation and UTP-LTP Control Signal Generation for Battery Protection.

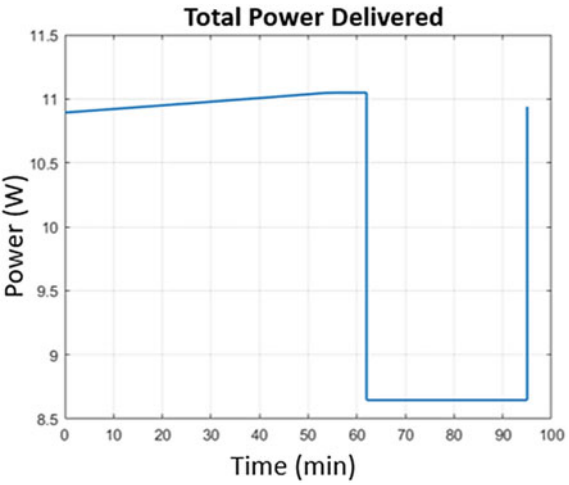


Fig. 15 Load power waveform

Acknowledgements We thank our mentors Shri. C D Sridhar, Dr. Vallivarthi Keshav Raju, Dr. Sambashiva Rao and Dr. Venugopalan Srinivasan for their constant guidance and support throughout the project. We are very grateful to Dr. H N Suma and Dr. Jayanthi K Murthy from B.M.S College of Engineering for their continuous encouragement. We also thank the management and Principal Dr. S Muralidhara for the opportunity to contribute to this project. It was indeed a great learning experience.

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Solar Panel Based Wireless Power Bank Works in a Small Satellite Power Management System

Shahriar Mahmud and Shakti Raj Chopra

Abstract The goal of this study is to create a wireless power bank for mobile phones and other devices using solar panels. Using sunlight as its primary source of energy, which can be used successfully daily or in the event of a calamity. It has constructed a solar panel that turns solar energy into electrical energy. The utility model shows a solar energy wireless charger, which is a lithium battery charger that can use solar energy and transmit electricity wirelessly. A charging pedestal and an electric energy emission pedestal make up the charger. A power supply management module, an electric energy emission module, an electric energy reception module, an electric energy receiving rectification voltage stabilization module, and a lithium battery charging module together comprise an interior section. The battery output current (almost 10,000 mA/h) so that the current is capped at 2000 milliamps. Only a few components are used in the design, resulting in a low-cost and extremely portable device.

Keywords Solar panel · Wireless charging · Photovoltaic · Inductive coupling

1 Introduction

Cell phones are becoming the most widely used mode of communication in practically every country on the planet. These days, power banks are one of the must-have items. Even power banks, however, require charging. To do so, the power bank must be charged using a power outlet.

There are already over 5 billion mobile phones in use, and the number is growing as technology improves and production costs decrease. Everyone is tired of the wires, connections, and plugs that are used in technological devices nowadays. A smart society necessitates smart technology that does not rely on wires and connections and instead operates wirelessly and automatically. As a result, wireless charging

S. Mahmud · S. R. Chopra (✉)
Lovely Professional University, Phagwara, Punjab, India
e-mail: shakti.chopra@lpu.co.in

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_14

has become the market's largest boom. Due to their widespread use in smartphones, laptop computers, Bluetooth headsets, tablets, cordless phones, and game controllers.

The fundamental issue is that a phone battery's typical lifetime is less than 10 h with moderate usage. For folks on the move or working, this is quite inconvenient. People must bring wall phone chargers to recharge their phones.

The latest solar phone power bank technology is a separate gadget that absorbs light from a small solar panel and then transfers it to the phone. Customers still need to carry another device in addition to their cell phones as a result of this process.

1.1 Background Study

The universality and growth of mobile devices have imposed ever-higher demands on charging convenience, while the green in mobile device consumption processes has become increasingly vital for today's energy security. Because of the differences in mobile device models, traditional mobile phone chargers have significant limitations in terms of charger type and interface, resulting in a greatly reduced ease of use. Because the existence of data wire has caused certain problems, a portable power source is also required. On the other hand, the mobility of portable power sources has prompted a demand for energy emergency action if there is a lack of power outside in the event of a power outage. The function of solar-generated electric power attracts more attention at times. The utility model object is to overcome the problem that currently exists with current conventional mobile phone lithium battery chargers. A type of solar energy radio charger has been proposed, which uses solar energy as an energy resource supply and delivers electrical energy via a high-frequency signal, allowing lithium batteries to be charged efficiently and wirelessly. Nowadays most people have many cell phones and laptops. It's difficult to carry multiple chargers for each technological item. To solve this difficulty, we devised a method of charging both computers and smartphones with a single device. The search for a plug point to charge our gadget is another issue with charging devices, especially while everyone is out of the station. One viable answer to the aforementioned issue is solar charging [1-2]. The wireless sensor node is powered by a combination of photovoltaic and thermoelectric generators [3].

Solar panels are frequently used in conjunction with backup rechargeable batteries. However, in this project, DCDC conversion is required to give the correct power to the system from the solar energy generated [4]. The goal of deploying a wireless solar mobile charger is to provide electricity for free using a sustainable energy source, and it will provide a better choice for those who travel long distances with their mobile phones [5]. A power bank is a portable gadget that uses its built-in batteries to provide power via a USB connector. They are recharged using a USB power supply. A power bank is made up of rechargeable Lithium-ion or Lithium Polymer batteries that are housed in a protective case that is governed by a printed circuit board (PCB) that offers a variety of protection and safety features [6]. A smartphone can be charged using one of two techniques. The first is to use the seebeck

effect to convert the smartphone's heat into electricity, and the second is to use a solar panel to turn the smartphone's illumination into electricity. As a result, the smartphone is automatically charged when resources are generated. If the power reaches a specific level, a threshold value is set to charge the smartphone automatically [6]. Within social, legal, and environmental norms, a wireless power bank is permissible. For social purposes, a wireless power bank is more convenient for recharging devices. Wireless power banks are used as safety detecting devices. Because it may recharge the device without a connection, wireless power banks help to lessen the impact of environmental regulations and safety measures [7]. Solar photovoltaic technology can be combined with wireless power transfer to interact with the available solar energy (WPT). The primary purpose of a solar photovoltaic system is to distribute electrical energy gathered wirelessly to various small-scale power applications [8].

2 System Model and Problem Description

High-frequency square wave circuit for generating, amplifier buffering, power amplifier part, transmitting coil and former limit building-out capacitor, after described transmitting coil and building-out capacitor parallel connection of former limit, be connected to the circuit of power amplifier part, the one-level power voltage supply of being exported by voltage-stabilizing output circuit; after the output of high-frequency square wave circuit for generating, amplifier buffering, power amplifier part, transmitting coil and former limit building-out capacitor, after described transmitting coil and building-out. The model necessitates the use of basic hardware components to complete the task at hand.

2.1 Solar Panel

Solar panels [2], [9] are energy-absorbing devices that turn sunlight into electricity or heat. Solar cells are used to make solar panels. A solar panel is made up of many tiny solar cells. To convert sunlight to electricity, a semiconductor called silicon is employed in the solar panel. The solar panel has p-type and n-type semiconductors, which allow electrons to move from positive to negative and produce power (Fig. 1).

2.2 Charging Kit for Wireless Devices

When charging gadgets, wireless charging [10] eliminates the need for a cord. A wireless charger may charge any battery-powered appliance by just placing it near a wireless power transmitter or an authorized charging station. The cornerstone of

Fig. 1 Solar panel absorbing sunlight

wireless charging is Faraday's law of induced voltage, which is widely used in motors and transformers (Fig. 2).

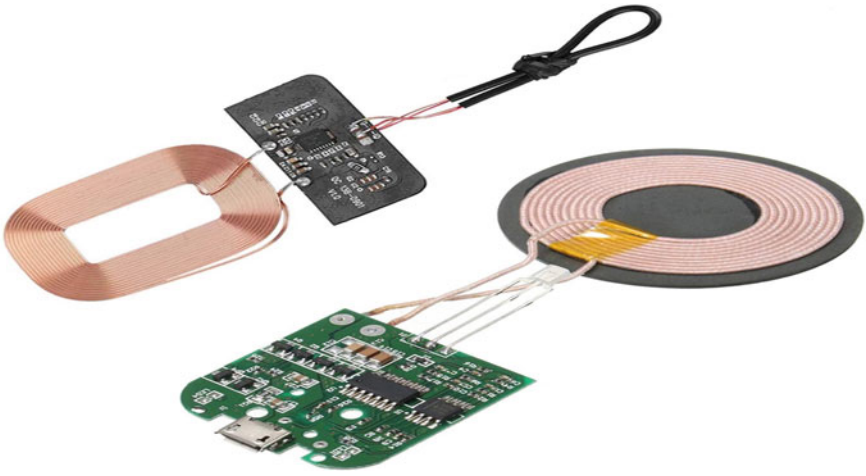

Fig. 2 Charging pad

2.3 USB Port

Our solar power bank features a USB Power Socket with an output current, and the component, specifically the USB socket, can be utilized as an intermediary for transmitting electric power between the solar panel and the end device, such as a power bank or a mobile phone [10].

2.4 Circuit Diagram and Working

- Solder the 1N4001 wire to the solar panel's positive side.
- Solder the two leads from a battery pack to the two 1N4001 wires connected to the solar panel. (Make sure the positive and negative are in sync.)
- Connect the battery pack's positive and negative leads to the 5v USB charging circuit.
- Check the voltages and currents with a multimeter and see whether the led on the USB charging circuit lights up.
- Place the battery pack and the rest of the circuit into the container on the back of the solar panel.
- Finally, join Using a micro USB cable, connect the wireless charging pad to the USB charging circuit.
- On top of everything, place the charging pad. Keep in mind that the wireless receiver must be linked to your computer to be able to charge your phone
- Depending on whether you're charging or not, you can also turn the battery pack on or off (Fig. 3).

3 Result and Discussion

The LM317T input voltage regulation loop can find the maximum power operating point of a solar panel's power characteristic, allowing it to use the solar panel's full capacity. This paper will allow me to develop a power bank that is both dependable and inexpensive. This is quite compact and can easily fit into any space. It's also suitable for small electronic equipment.

4 Conclusion and Future Scope

Solar energy is renewable and can be used for a variety of applications, including wireless solar mobile power banks. These are simple, portable, and can be used by anyone, especially in remote areas. Normally, wireless power banks consume a lot of power, but because we use renewable energy, this is not an issue. Overcharging

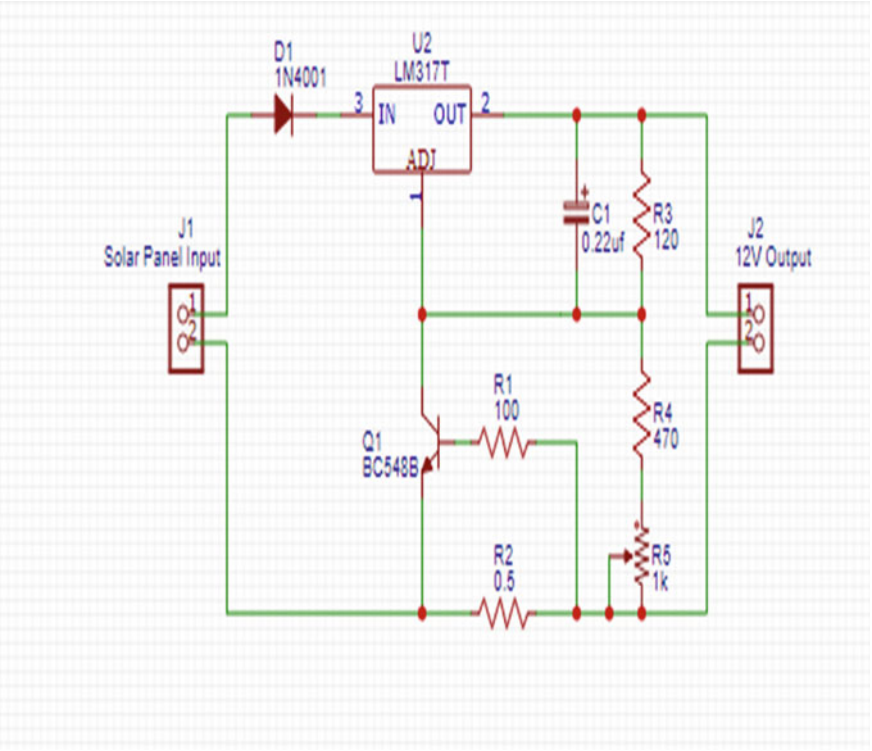

Fig. 3 Circuit diagram

is extremely unlikely. There is a lower risk of a mobile mishap. It will also protect against electric shock and will be very user and environmentally friendly.

Although there are numerous standard power banks and on-plug chargers for certain devices, this study mostly focused on how Solar Panel Based Power is efficient on electronic gadgets. This study or prototype would be more complete, meaning full and far-reaching, if it included more gadgets, such as laptops, which would have offered a much more detailed base and would have required more time, money, and other resources.

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Design and Computational Analysis of Parallel Flow Heat Exchanger with Effectiveness Improvement Technique

D. Sujay, B. Abhiram, P. Akshay Kumar, C. K. Jayanth, and Akhila Rupesh

Abstract Execution of a heat exchanger with a rough surface and grooved tube to increase the surface area for heat exchange. Because there are larger surface cross-sectional areas on the outside grooved surface of the tube (fins), heat exchange is faster. Furthermore, it is used to exchange hot and cold liquids as well as to lower the temperature of hot liquid by the exchange of hot to cold liquids. The research of parallel flow heat exchangers with rectangular finned type configuration with 2D investigation has been carried out in this work under various stream parameters.

Keywords Double pipe heat exchanger · LMTD · Parallel flow · Rectangular fins · Thermal analysis of heat exchanger · CATIA V5 · Ansys fluent

1 Introduction

The hot and cold fluids enter at the same end, flow in the same direction, and exit at the same end in a parallel flow arrangement. The direction of fluid flow within the exchanger determines the modes of operation and effectiveness of heat exchangers. Because the exit temperature of the cooled fluid can approach a limiting degree, parallel flow heat exchangers are used. While a parallel flow design can be useful in some circumstances, when the limiting temperature is reduced, channeling issues or freezes can arise at shutdown. Since the heat transfer rate in parallel flow heat exchanger is less, the extended groove surfaces called "fins" have been incorporated in order to increase the effectiveness of the exchanger and we preferred rectangular fins to be more effective.

D. Sujay · B. Abhiram · P. Akshay Kumar · C. K. Jayanth · A. Rupesh (✉)
Department of Aeronautical Engineering, Mangalore Institute of Technology and Engineering, Moodbidri, Karnataka, India
e-mail: akhilarupesh56@gmail.com

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_15

2 Literature Review

It has been found that the overall concept of the mean diameter of an aerosol system's disperse phase has shown to be quite useful. It is defined by a single set of indices that are depending on the specific type of aerosol system in question. In heat and mass transfer aerosol systems, the idea of mean diameter is valid [1]. The heat transfer characteristics of multi-layered heat exchangers were investigated theoretically. The issue was modeled as a 2D conjugated problem with three phases: two fully developed laminar flows and the exchanger wall [2]. In most heat exchanger models, convection is assumed to be dominant, allowing diffusion to be neglected, and hyperbolic PDE will be the resulting model. This hyperbolic system degenerates when the flow velocity is little or zero, and controllability is lost. To address the problem, a full flux model was developed with a parabolic approximation to the hyperbolic equations. It was shown that the whole flux model can be utilized for set point control and tracking even with zero flow [3]. The design will give a high rate of heat transfer. The coefficient of heat transfer is determined by the type of design used, and consequently has an impact on the surface area required to achieve the desired degree of heat exchange. Most heat exchangers use a combination of parallel and serial flow patterns [4].

3 Methodology

The parallel flow heat exchangers have been designed using CATIA software. Figure 1 shows the designed heat exchanger, and Fig. 2 shows the cut section view of the designed parallel flow heat exchanger.

CATIA V5 software was used to design the parallel flow heat exchangers. The designed heat exchanger is shown in Fig. 1, and the cut section view of the designed parallel flow heat exchanger is shown in Fig. 2. It was examined with a specific heat exchanger model dimension based on conventional dimensions. As demonstrated in the accompanying figures, we used CATIA V5 software to create a heat exchanger model. Initially, we chose the size and diameter of the heat exchanger tube based

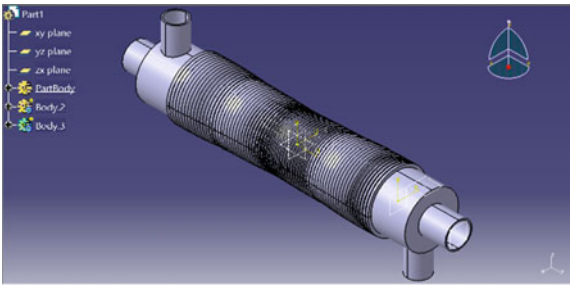

Fig. 1 Design of heat exchanger using CATIA V5 software

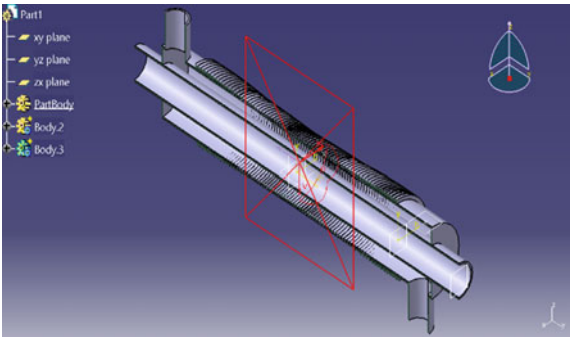

Fig. 2 Cut section of heat exchanger using CATIA V5 software

on the pressure drop and Reynold's number requirements. When compared to tube diameter, tube length had a negligible impact on pressure drop through the tubes. As the dimensions shown in the above design sketch, the inner diameter of the tube is 18 mm, outer diameter of the tube is 40 mm, length of the tube is 340 mm, and pitch of the fins is 5 mm. The next phase in the design was to decide where the tube and baffle should be placed to achieve the same pressure drop and Reynold's number requirements as the tube side. The heat transfer area was analyzed once all of these criteria were accomplished. Other features of the exchanger were achieved by adjusting the standard if the exchanger was under-designed. Common modifications included changing tube and tube lengths, as well as increasing the number of rectangular fins. As a result, pressure decreases and Reynold's number fluctuates. In order to achieve all criteria, a continuous approach was designed in which the exchanger's specs were adjusted regularly. Both are also carefully built to account for exchanger fouling and aging.

4 Result and Discussion

Flow study was performed on the intended parallel flow heat exchanger using Ansys Fluent software. The temperature distribution at the outflow surface for the Rectangular finned type is shown in Fig. 3. The Thermal Analysis of a Rectangular Finned Configuration is shown in Fig. 4. The temperatures at the outflow and inlet are shown in Figs. 5 and 6, respectively.

The heat transfer properties of double tube heat for parallel flow were studied using CFD Ansys Fluent, and the results were calculated. Heat transfer performance in a parallel flow design has been proven to be within error limits in studies. Water-to-water heat transfer qualities and tubes of the same length and diameter were simulated. For a cold intake of 300 K and warm inlet of 320 K, create a ring space with the same inlet temperature. Examine the parallel flow heat exchanger; the output current has a huge temperature differential (hot output, cold output). Heat transfer

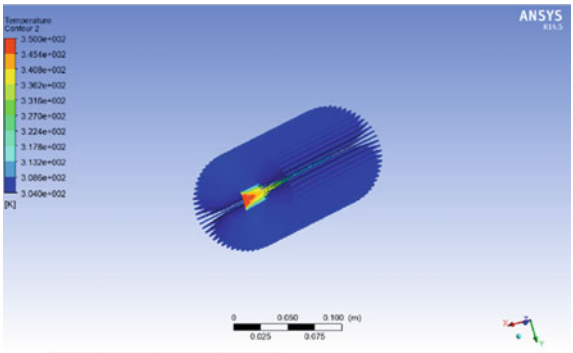

Fig. 3 Temperature distribution at outlet surface for rectangular finned type

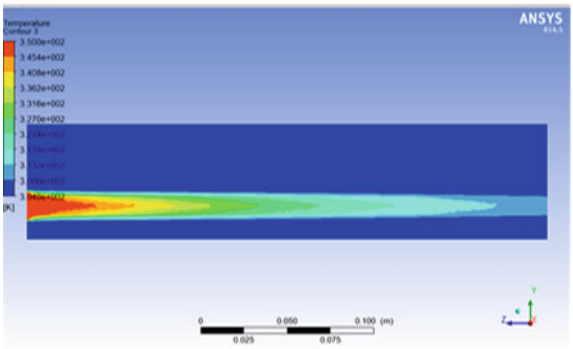

Fig. 4 Thermal analysis of rectangular finned configuration

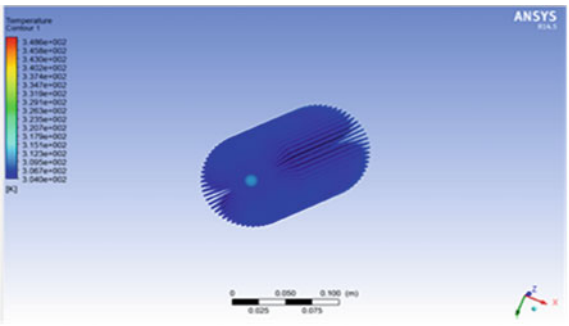

Fig. 5 Temperature distribution at outlet

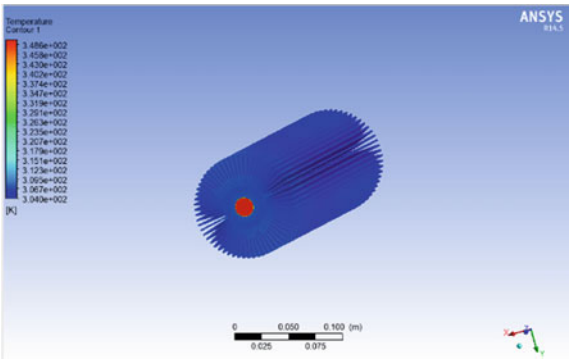

Fig. 6 Temperature distribution at inlet

enhancement in a heat exchanger can be achieved in a variety of ways depending on the plan and length of the heat exchanger, and we have used rectangular fins (extended surfaces).

5 Conclusion

CATIA V5 was used to show the fins with various setups, and CFD Ansys Fluent was used to investigate the hotness transfer rate. The rectangular fins have a higher hotness movement rate than the cylinder with no balances and all other types of fins comparatively, according to the data. As a result, we computed the effectiveness of a parallel flow type of heat exchanger while incorporating the effectiveness improvement technique by fins. The project has been concluded by design and computationally analyzed.

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FPGA Implementation of TTC and OBC for a Cubesat

R. Sathyanvesh, Jayanthi K. Murthy, Chandrakala G. Raju, and H. N. Suma

Abstract This paper describes the implementation of the telecommand decoder and telemetry data encoder on FPGA for cube satellite operations. The objective is to design and launch a student satellite in Low Earth Orbit and perform on-orbit operations to demonstrate the imaging of the Earth's surface, high-altitude operations and de-orbiting maneuver. The Telemetry, Tracking and Telecommand (TTC) and On-Board Computer (OBC) subsystem implementation allow the CCSDS-compliant ground stations to communicate with the satellite to facilitate telemetry, telecommand and ranging functions throughout the life of the satellite mission. The use of FPGA in space missions provides high computational power, and parallel processing at relatively lower power consumption. Telemetry encoder and telecommand decoder are implemented in HDL Verilog, and simulation is conducted in the Vivado design suite for Xilinx Zynq 7000 FPGA.

Keywords TTC · FPGA · Command and data handling · Telecommand · CCSDS standards

1 Introduction

With the advancements in space technologies and increase in the space research, the number of space operations being conducted has been increased. The number of small satellites has been increased from a few tens to around thousands in the past decade. ISRO has provided launch facilities for around 18% of total satellites

R. Sathyanvesh (✉) · J. K. Murthy
Department of Electronics and Communication Engineering, BMSCE, Bangalore, India
e-mail: sathyanvesh.r@gmail.com

C. G. Raju
Department of Information Science Engineering, BMSCE, Bangalore, India

H. N. Suma
Department of Medical Electronics, BMSCE, Bangalore, India

C. Prakash et al. (eds.), *Smart Small Satellites: Design, Modelling and Development*, Lecture Notes in Electrical Engineering 963,
https://doi.org/10.1007/978-981-19-7198-3_16

launched in the past decade [1]. The support from space organizations has led to satellite development missions at the academic level.

The design of the cube satellite has the following constraints—(a) The Total power that can be generated for the operation of the satellite depends on the area of the solar panels that can be placed over the satellite, hence for smaller cube satellites, generating more power is tedious. (b) The space that is available to place the components required for the operation and control is also less, which makes the designers choose components with lesser dimensions. As per the research specified in [2], most satellites are using microcontrollers and an FPGA for performing OBC operations. The same can be witnessed in the OBC system present in [3] that consists of an AVR Microcontroller and an anti-fuse FPGA.

The component miniaturization, high computational capability, complex payload support and cost reduction are the key insights of the space research that needs to be addressed. The above key insights can be addressed using space-grade FPGA. The design of the TTC and OBC systems using the FPGA is discussed in this paper.

The use of FPGA over microcontrollers provides versatility. The space-grade FPGAs are radiation hardened which has protection from various space radiations. FPGA consists of logic elements and reconfigurable interconnects that facilitate the wiring of the logic elements. The addition of the Microprocessor along with the programmable logic increases the performance and speed of the operations. It eliminates the interfacing overhead between the processor and FPGA and also provides enhanced features.

2 Materials and Methods

2.1 Block Diagram

Figure 1 shows the block diagram of the operations of the TTC subsystem at the ground station.

The telecommands are crucial commands sent to the satellite from the ground station to control the operations of the satellite. The commands are generated, encoded, formatted and sent from the ground station. The received telecommands are in the form of Communication Link Transmission Units (CLTU). These consist of the frame start sequence, command and tail sequence. Hence, Frame synchronization is done before decoding and validating the command. The data from the ground station may be randomized. In such cases, de-randomization is done before decoding and validation. The communication system is developed as per recommendations of the Consultative Committee for Space Data Systems (CCSDS).

The Telemetry data and payload data acquired in the satellite are transmitted to the ground station. Before transmission, the data is formatted and encoded. The Convolution coding with a constraint length of seven and a Code rate of ½ is used

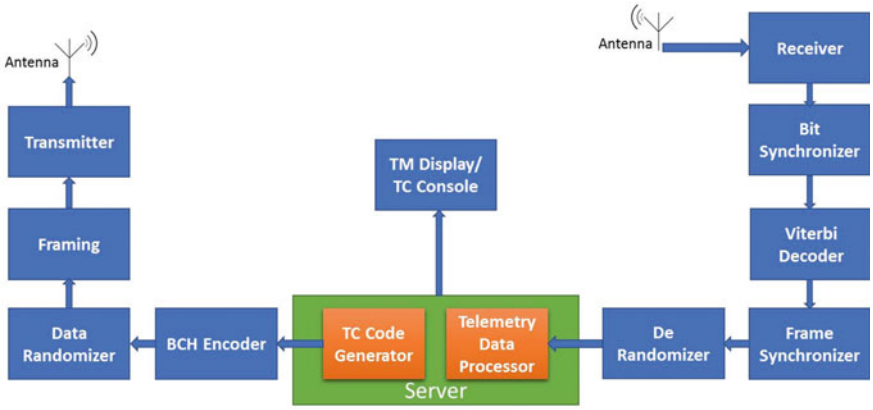

Fig. 1 Block diagram of TTC at ground station

as per the CCSDS recommended standards. The data transmitted from the satellite is received at the ground station and processed. The main operations involve

- Telemetry data processing—The housekeeping data and the payload data sent from a satellite will be received at the ground station during the visibility period. The data received is formatted and processed.
- Telecommand generation and transmission consists of command generation, encoding, formatting and transmitting telecommands to the satellite during the visibility period of the satellite from the ground.

The block diagram shown in Fig. 2 presents various blocks of the satellite along with the sensors and actuators. The telecommand decoding section has the following blocks—Frame synchronization, Frame inversion correction, de-randomization, error detection and validation. The telemetry section includes formatting the data along with frame sync, Forward Error Correction Coding (½ Convolution coding).

2.2 Design Details

Telecommand Frame

The Telecommand frame also called Communication Link Transmission Unit (CLTU) is designed as per the CCSDS Standards. The CLTU as per CCSDS has accommodation for n codewords. In this paper, the telecommand frame is modified and considered to accommodate only one codeword per frame. Figure 3 shows the telecommand frame format.

- Frame Sync Word—The Frame Sync word is also called start pattern. It delimits the CLTU frames. It is a 16-bit pattern and is as follows:

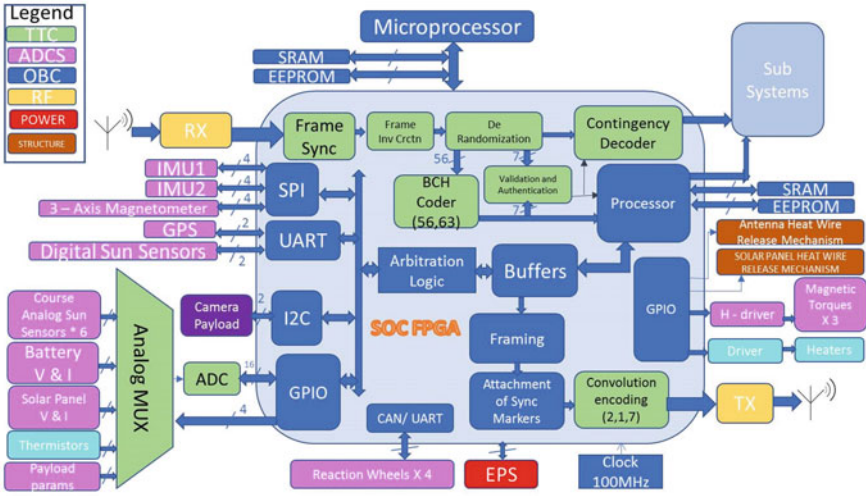

Fig. 2 Block diagram of a satellite

Frame Sync Word 16 bits	Telecommand Code word 64 bits	Tail Sequence 64 bits

Fig. 3 Telecommand frame format

- 1 1 1 0 1 0 1 1 1 1 0 0 1 0 0 0 0
- The Telecommand Codeword—This is an encoded telecommand. BCH encoding scheme is used to encode the telecommand. The telecommand is of 56 bits which after encoding becomes 63 bits. A filler bit is appended to make it a 64-bit codeword.
- Tail Sequence—The tail sequence is of 64 bits. It is a non-correctable pattern that helps in delimiting the CLTU frames by stopping the decoding process. The non-correctable pattern is generated by altering the parity bits. The decoding of the tail sequence will generate an error to halt the decoding process.

Telecommand decoder unit

Frame Synchronization.

The CLTU comes under the coding layer of the telecommand channel service according to the CCSDS norms. CLTU is preceded by the acquisition sequence and succeeded by the idle sequence in the physical layer. Hence for incoming data, frame synchronization needs to be performed to identify the start of the frame. The frame synchronization pattern used is EB90 in hexadecimal [5].

Frame Inversion Correction.

BPSK modulation scheme is used at the transmitter of the ground station while transmitting the data over a noisy channel. BPSK has two constellation points positioned 1800 apart. At the receiver end, phase ambiguity may occur. Hence, while checking for the frame synchronization pattern, 146Fh (inversion of EB90h) is used along with EB90h to detect frame inversion.

De-Randomization.

The incoming signal must have a minimum bit transition delay in order to maintain the bit synchronization with the received telecommand. Hence, a randomizer is used to randomize the encoded data while transmitting it at the ground station. De-randomizer is used to obtain the encoded codeword.

The randomization sequence used is as per the CCSDS [6] recommendations and is as follows.

$$h(x) = x8 + x6 + x4 + x3 + x2 + x + 1$$

BCH Decoder.

BCH coding is used at the satellite to perform error detection of the received telecommand.

BCH Codes—BCH codes are the subset of cyclic codes whose generator polynomials have roots carefully specified so as to give good error-correcting capabilities. BCH codes are 't' error-correcting codes as they can detect and correct up to 't' random errors per codeword. The recommended standard BCH coding is BCH (63,56) code as per CCSDS; it has the capability of detecting 3 errors and correcting a single random error bit. The generator polynomial for BCH (63, 56) is $x7 + x6 + x2 + 1$. Figure 4 shows the 64-bit BCH codeword.

Since the execution of single error command may lead to the failure of the entire satellite operation, BCH codes are used to detect the error at the satellite end. The 64-bit data is ripped to extract 56-bit message data and is then BCH coded to generate 7-bit parity. The generated parity is compared with the received parity bits to detect and discard any erroneous commands. Figure 5 shows the Blocks involved in BCH decoder.

The message bits are sent to the BCH coder to encode the message bits to generate the 7 parity bits. The generated parity bits are compared against the parity bits received from the ground station in the verification and authentication block. If they match, then the authentication signal is generated to indicate the command is valid. This

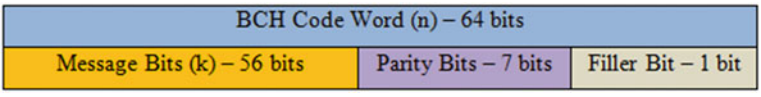

Fig. 4 BCH codeword [7]

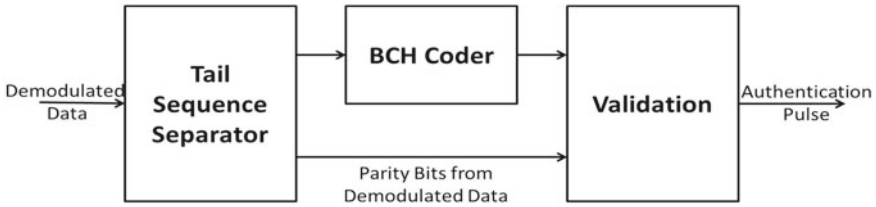

Fig. 5 Telecommand decoder

signal is fed to the processor and contingency decoder for further processing of the telecommand. The command counter is incremented. If the command is invalid, then it is discarded and the same is notified to the ground station. The 56-bit serial data is converted to parallel before giving it to the processor.

Telemetry Encoder Unit

Data Acquisition.

The function of the telemetry involves the acquisition of data from on-board sensors and transmitting this information to the ground. The telemetry data includes spacecraft resources, health, orbit and timing data, and operation scientific data. Each sensor uses various protocols to communicate with the master system on board. Hence, the interfaces such as SPI, I2C and UART are designed in FPGA to acquire this data from sensors. Sensor data includes analog data. Hence, Analog Multiplexer and ADC are used to acquire this data. The data is acquired at regular intervals from the sensors. Arbitration logic is used to sample sensor data at regular intervals. The acquired data is stored in the buffer.

Data Formatting.

The telemetry data is formatted before transferring it to the ground for synchronization and error control purposes. The formatting of data includes creating a frame which consists of the various sensor data. The frame consists of sub-frames. Each sub-frame will be filled with the sensor data. Based on the sampling rate, the data from a particular sensor may appear in each sub-frame or may appear in alternate frames or maybe once in the main frame. As an illustration, IMU sensor data is sampled at a higher rate, hence it will appear in each sub-frame, whereas temperature data appear once in the main frame. The frame synchronization pattern is F9A42BB14. It is added at the start of each frame. The frame structure is as per CCSDS recommendations [4] (Fig. 6).

Convolution Encoder.

Convolution codes are continuous error-correcting codes. Convolution codes generate parity symbols when the Boolean function is used in sliding applications to run over the data. Convolution operation is performed with the generator polynomial

Transfer Frame Primary Header	Transfer Frame Data Field			
	Sub Frame 1	Sub Frame 2	.....	Sub Frame N

Fig. 6 Transfer frame structure

and the data. Convolutional codes have the ability to perform economical maximum likelihood soft decision decoding which is beneficial.

Code rate of the encoder and depth of the encoder are characteristics to define convolution code. [n, k, K] format is used to represent convolution codes. n/k is used to represent code rate, where n denotes the input data rate and k denotes the symbol rate of output. K denotes the depth of the encoder and K−1 inputs constitute the output of the encoder. K indicates the number of memory elements in the generator polynomial. It is also called the maximum possible number of states of the encoder (typically 2^y).

2.3 *Implementation*

Telecommand decoder unit

Figure 7 consists of the various modules involved in the telecommand reception, decoding and validation. It also shows the flow of the signals and data path for the incoming command till the generation of the authentication signal (Fig. 7).

Frame Synchronization.

The RF receiver generates a control signal Rx_Frame to indicate the incoming data. It also provides serial data and a clock to the telecommand decoder unit. The frame

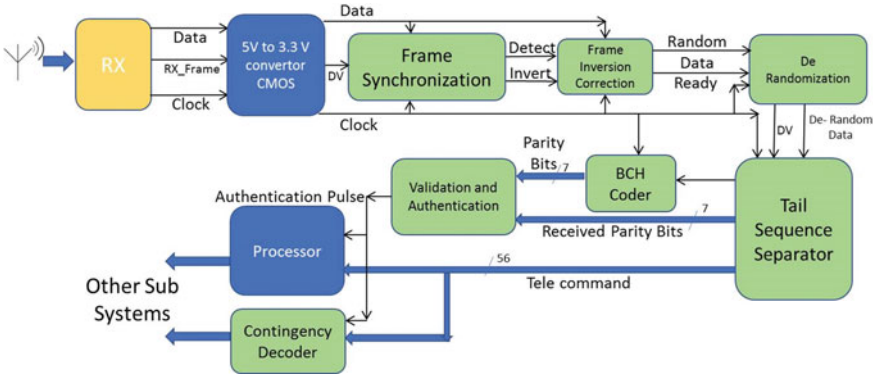

Fig. 7 Telecommand decoder unit

synchronization module of the decoder unit scans for the valid frame synchronization word. Once, the frame synchronization word is detected, DETECT signal is generated to indicate the valid CLTU (Fig. 8).

Frame Inversion Correction.

If the frame synchronization module detects the inverted frame, then it generates an INVERT signal along with the detect signal. Based on the signals generated, the Frame inversion correction block inverts the data before sending it for further processing. The Frame inversion correction module generates a data-ready signal along with the data to indicate valid data (Fig. 9).

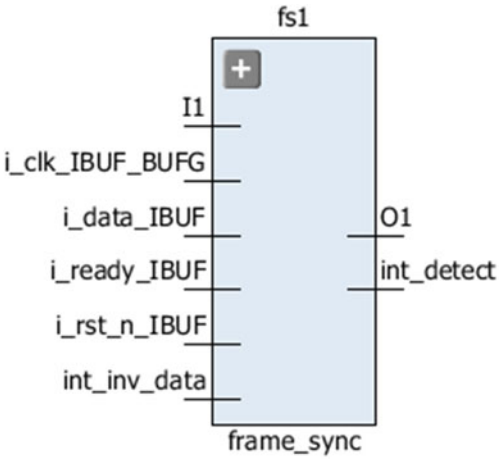

Fig. 8 Frame synchronization module

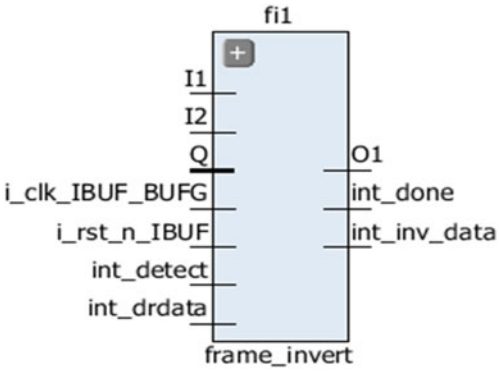

Fig. 9 Frame inversion correction module

De-Randomization.

The data-ready signal from the frame inversion correction module is monitored for valid data and the incoming data is XORed with the random sequence generated. The module generates the data valid signal along with the de-randomized data. The randomization sequence used as per the CCSDS recommendations is as follows:

$$h(x) = x8 + x6 + x4 + x3 + x2 + x + 1$$

The randomizer logic diagram is shown in Fig. 10.

The bit pattern generated using the above polynomial repeats every 256 bits. The shift registers are initialized to all 1's at the start of each codeword (Fig.10).

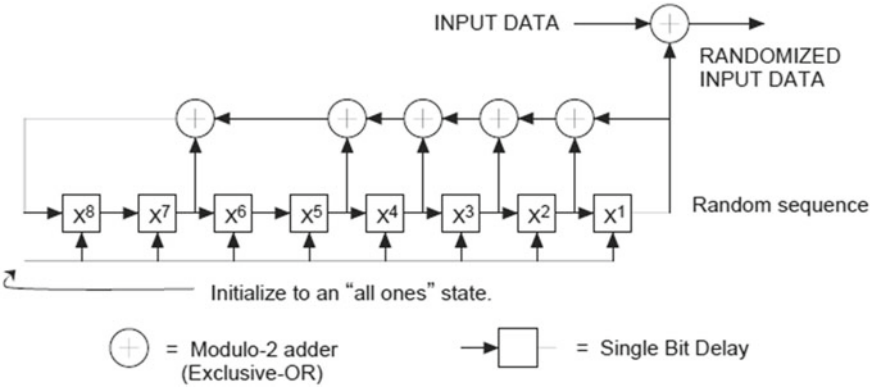

Fig. 10 Logic diagram of randomizer [5]

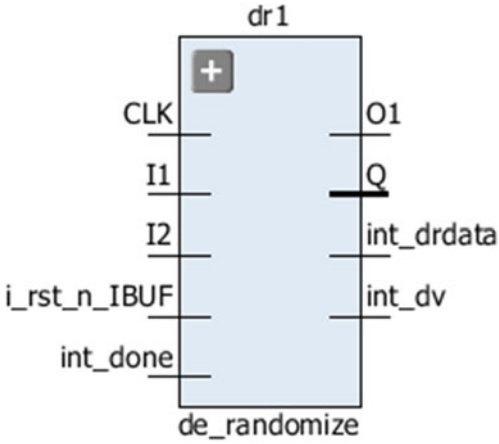

Fig. 11 De-Randomization module

BCH Coder.

The telecommand decoder implementation requires the separation of tail sequence parity bits and then feeding the message bits to the BCH encoder. Once the encoder generates the parity bits, they are compared with tail sequence parity to generate an authentication signal.

The BCH encoder has been designed using Linear Feedback Shift Register (LFSR) as shown in Fig. 12. The period of the entire process is 63 clock cycles. The encoder is implemented as per the CCSDS standard using the generator polynomial. The register cells P0 to P6 represent the parity bit, with P0 being MSB and P6 being LSB. The encoder is implemented using 3 switches.

- Switch 1: Facilitate in getting information bits (0–56).
- Switch 2: Facilitate in getting parity bits (57–63).
- Switch 3: Facilitate in adding filler bit (forced to 0) (64) (Fig. 12).

Telemetry Encoder

Figure 13 shows the hardware implementation of the convolution encoder as per CCSDS [6] with constraint length k = 7 and a code rate ½ (Fig. 13).

The function generators for the encoder are defined by

$$g1 = [1, 1, 1, 1, 0, 0, 1]$$
$$g2 = [1, 0, 1, 1, 0, 1, 1]$$

In octal form, the generators are (171, 133).

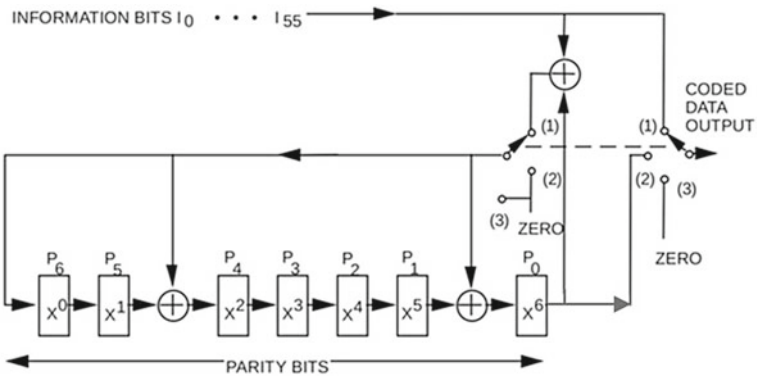

Fig. 12 Hardware implementation of BCH code [5]

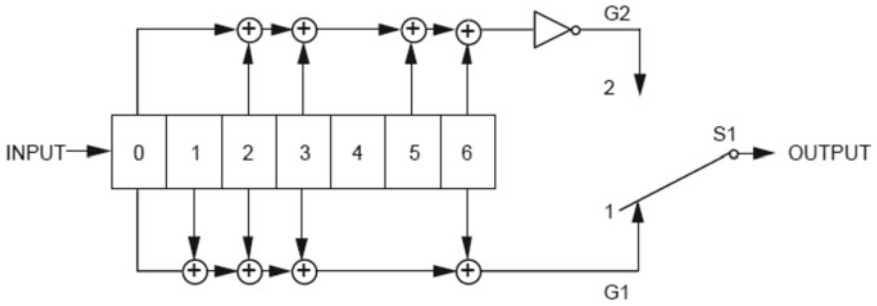

Fig. 13 Convolution encoder with k = 7 and code rate = ½ [6]

3 Results and Discussion

3.1 Simulation

The simulation of the telecommand decoder unit and the telemetry encoder has been done using the Vivado design suite (Fig. 14).

The simulation result in Fig. 14 shows the serial data and clock as inputs to the telecommand decoder unit. The data is frame synchronized, and de-randomized after the reception. The data is BCH encoded and validated. If the data is valid, the 56-bit telecommand and the authentication signal are available at the output. The same is shown in the simulation result Fig. 14.

The input to the telemetry encoder is serial data. This data is encoded at the code rate of ½. For each input bit of data, two output bits are generated. The telemetry encoder operation is synchronized with the global clock. The incoming data is encoded and transmitted to the ground station. The simulation result in Fig. 15 above reflects the same.

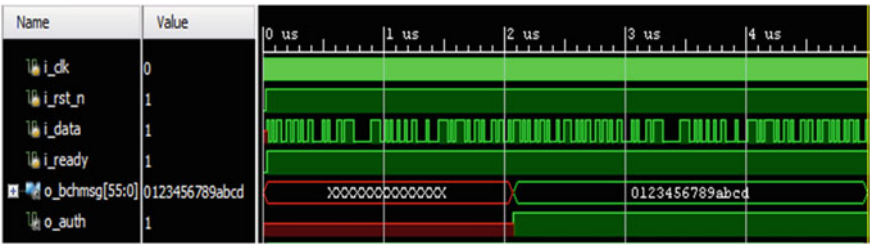

Fig. 14 Simulation result of telecommand decoder unit

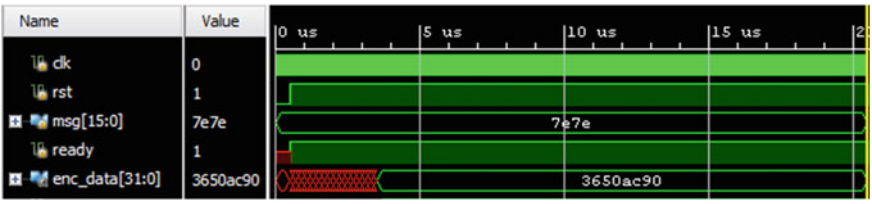

Fig. 15 Simulation result of telemetry encoder

3.2 Synthesis

The synthesis report of the telecommand decoder unit shown in Fig. 16 consists of the device utilization as well as the power report of the design in Xilinx Zynq 7000 series FPGA. The synthesis report of the telemetry encoder shown in Fig. 17 consists of the device utilization as well as the power report of the design in Xilinx Zynq 7000 series FPGA (Figs. 16 and 17).

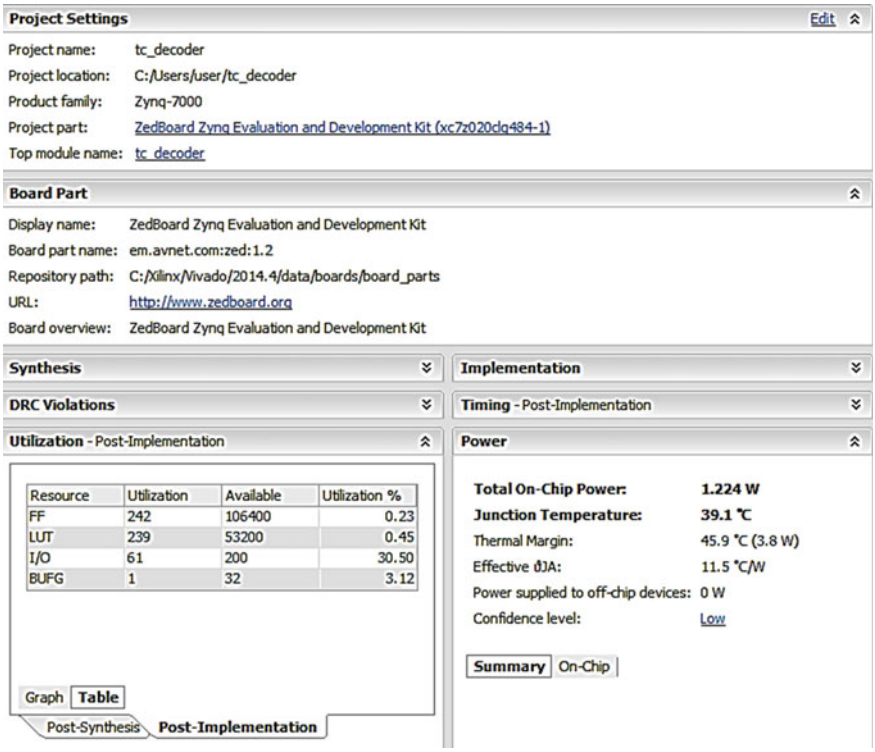

Fig. 16 Synthesis report of telecommand decoder

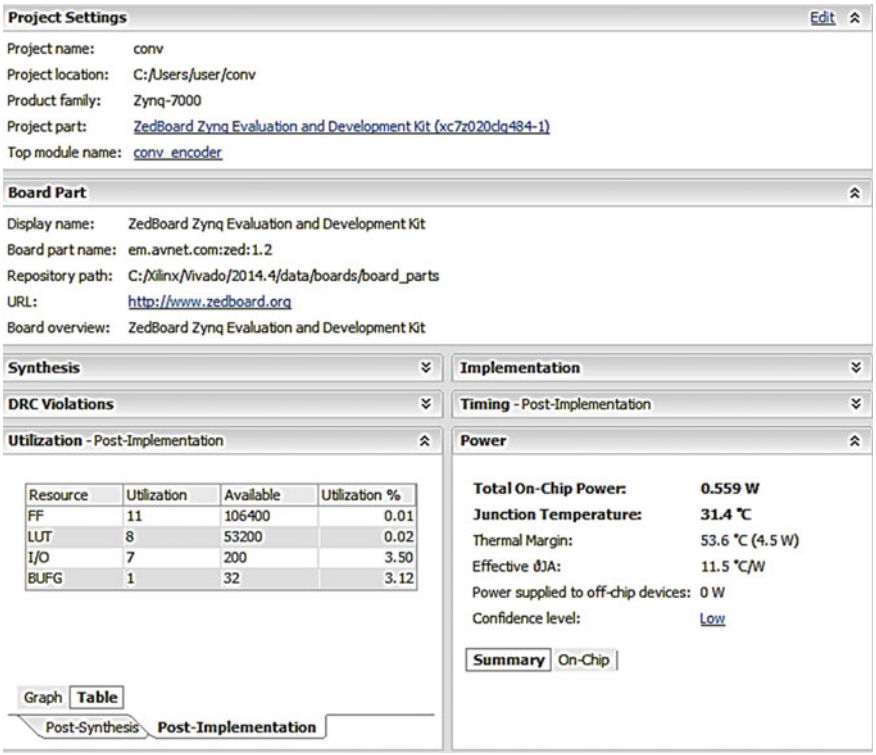

Fig. 17 Synthesis report of telemetry encoder

4 Conclusion

This work describes the design of telemetry encoding and telecommand decoding techniques developed for a CubeSat which is implemented on FPGA using the hardware description language Verilog. The design is as per CCSDS recommendations and can be reconfigured based on the new requirements that arise during the design cycle. The functions are tested using the Vivado design suite simulator for Xilinx Zynq 7000 series FPGA. The simulation results are reliable and stable.

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