Impact of High-Performance Transistor on Performance of Static Random Access Memory for Low-Voltage Applications

Bhawna Rawat and Poornima Mittal

Abstract In this paper, four SRAM bit cells, two each of 6T and 7T (using typical and high-performance transistors), are described. Their performance is compared in terms of static noise margins, leakage current, write time, and global variation. The cell with most stable static noise margin values is the 7T1 cell with value of 91 mV for both read and hold operation, while its write margin is 120 mV. The weakest performance is recorded for the 6T cell with 0 mV read static noise margin. It also registers the highest leakage current values of 441 and 116 pA for Q = '0' and '1', respectively. The cell with best write time requirement of 30 ns is the 7T1 cell. Whereas, in terms of global variation analysis, the cell that outperforms against others is 6T1 with least variation in its hold, read, and write margin values for maximum variation caused by fabrication inconsistencies.

Keywords High-performance transistor · Write time · Global variation · Leakage current

1 Introduction

Static random access memory is an indispensable component of most microprocessors. It is a common component for most processing-based circuits. With the growing market appetite for low power, portable devices, the designing for circuit components has shifted to the nanometer vicinity. This decline in technology node facilitates power reduction, high-density integration, and economic feasibility for the device. But, it also subjects the cell to noise susceptibility and process variations [1]. Additionally, at lower technology node, the leakage power caused by sub-threshold

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current dominates the total power dissipation for the design. Conventionally, reduction in leakage is achieved by supply voltage (V_{DD}) scaling; but this results in speed and noise margin degradation for the bit cells [2, 3]. The near-threshold operation due to nominal V_{DD} has low leakage power consumption and has lesser degradation in speed, compared to sub-threshold region [4]. It is also observed that technology node scaling may also degrade read and write margin for the cell. Therefore, to improve cell performance using high-performance transistors in the cell design is an alternative approach.

Standard MOSFET can be designed with varying threshold voltages (V_{TH}), the cell with nominal threshold voltage is referred to as standard threshold voltage cell. The V_{TH} for the cell can be altered by varying the channel doping; as the channel doping increases, the gate V_{TH} increases, because the gate voltage needed to deplete more majority carries before a minority carrier channel can be formed [5]. A high-performance transistor is a device that has lower V_{TH} in comparison with a typical transistor. The advantage of using high-performance transistors for designing SRAM bit cell is that they provide a convenient mechanism to improve the delay for the circuit [6]. Therefore, in this paper, two different topologies for 6T and 7T SRAM bit cells are discussed. For each bit cell topology, a typical cell and a high-performance-based cell are taken into consideration. This is done to analyze the impact of a high-performance transistor on the functioning of a bit cell. The 6T cell has been the industry benchmark for a long duration, due to its high packaging density and fast differential sensing [7]. But its performance has suffered significantly due to the drastic scaling in technology node and the reduction in V_{DD} [8]. Therefore, researchers have proposed different 7T bit cell topologies. The 7T cell is able to achieve commendable results at lower technology node and scaled V_{DD}, without adding much area penalty to the cell. Therefore, 7T cells are also gaining popularity. Consequently, to study the impact of high-performance transistor on the bit cell performance, two cells of 6T and 7T topology each are considered in this paper. The cells described in the paper are evaluated for static noise margin, leakage current, write time, and global variation analysis. The rest of the paper is categorized into four sections—Sect. 2 details the topology of the different 6T and 7T cells, while the simulation results for all the cells are analyzed in Sect. 3. Section 3 is further divided into four subsections each dedicated to static noise margin, leakage current, write time, and global variation analysis, respectively. The findings of the paper are comprehensively summarized in Sect. 4.

2 Different SRAM Bit Cell Topology

Various bit cell topologies are reported in literature. All cells in this paper are designed at 32 nm technology node, and the width dimensions for all the bit cells are shown in Table 1. The 6T cell has been the most prevalent SRAM cell, due to its fast sensing, symmetrical topology, and high packaging density. The schematic for the conventional 6T cell is illustrated in Fig. 1a. The data storage core for the 6T cell

Table 1 Transistor width dimension for different SRAM bit cells (in nm)

	M1	M2	M3	M4	M5	M6	M7
6T	64	64	96	96	128	128	–
6T1	64	64	166	96	128	128	–
7T	64	64	96	96	128	128	64
7T1	64	64	96	96	128	128	64

is composed of a back-to-back connected inverter pair (M1-M3 and M2-M4). This internal core for 6T is accessed via transistors—M5 and M6; the access transistors works in conjugation with the bitline pair—BL and BLB, signals to perform the read and write operation. For a very long duration, the 6T SRAM bit cell was the industry standard for cache memory implementation. But with technology node reduction and scaling of V_{DD}, the performance for the 6T SRAM bit cell has experienced a tremendous decline. Therefore, researchers have modified the 6T SRAM bit cell topology to improve its performance. One such 6T cell (6T1) was described by Suvarna and Mikie in 2019 [9]. The schematic design for 6T1 is depicted in Fig. 1b, and it is a modified version of the 6T design, which uses both access transistors to perform both the read and write operation. While, the 6T1 SRAM cell resolves the conflict by isolating the access transistors for the two operations; the M5 transistor works in conjugation with WBL during the write operation, whereas the M6 transistor along with RLB is responsible for the read operation. Another modification that is made in the 6T1 cell in comparison with the 6T is cell that the M3 transistor in the inverter core is always biased in the cut-off region; as the gate and drain for the transistor are shorted.

An SRAM bit cell topology consisting of seven transistors (7T) was reported by Aly and Bayoumi [10] in 2007. The 7T cell has differential ended topology and is reliant on BL and BLB for both its access operations—read and write operation. In the 7T cell, the information is retained by the inverter couple (M1-M3 and M2-M4). The mutual connection between the inverter couple is reliant on transistor M7, controlled by signal; W. The M7 transistor has the ability to connect/disconnect the back-to-back connection between the inverter couple as per need of the circuit. The main function for the M7 transistor is to reduce the mutually connected inverter pair to a cascaded inverter topology when the cell is operational in write mode. Else, the mutual feedback between the inverters is maintained. Therefore, the 7T cell is operational differentially for read mode and single-ended for write mode. The schematic of the 7T cell is illustrated in Fig. 1c.

A different 7T cell (7T1) design was described in 2021 by Rawat and Mittal [11]. The 7T1 cell is a modification of the 7T design and uses a high-performance NMOS transistor in its topology. In the 7T1 cell, the information is retained by an inverter pair formed by transistors M1-M3 and M2-M4. The mutual connection between the inverter couple is facilitated by the M5 transistor. The access operations - write and read, for the cell are single ended in nature performed via M6 and M7 transistors, respectively. The diagrammatical representation for the 7T1 cell is presented in the

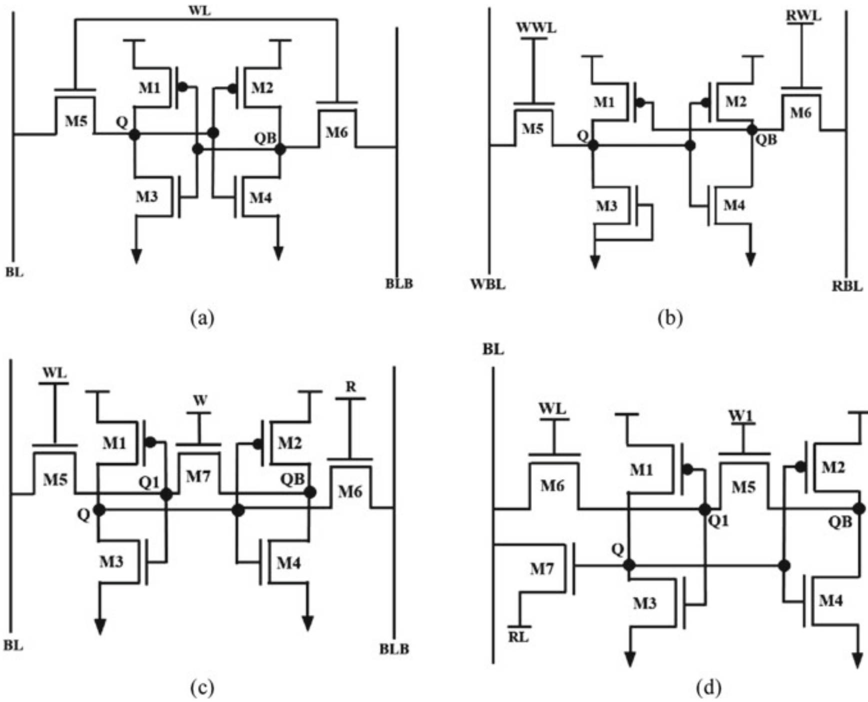

Fig. 1 Circuit representation for the **a** 6T, **b** 6T1, **c** 7T, and **d** 7T1 SRAM bit cell

Fig. 1d. A high-performance NMOS transistor (M3) helps in facilitating a faster writing for the cell. As the write delay for the circuit is inversely reliant on the $V_{DD} - V_{TH}$ factor; as the V_{TH} for the bit cell decreases, the $V_{DD} - V_{TH}$ factor increases, and thereby the write delay decreases.

3 Experimental Results and Analysis

3.1 Noise Margin Analysis

With the reduction in technology, node a cells vulnerability to noise increases. Also, as the V_{DD} for the bit cell is scaled, the impact of noise on the cell becomes prominent. A cell is required to be operational for three different operations—read, write, and hold. Consequently, for each cell, the noise margin resilience to each operation is to be calculated. The resilience of an SRAM bit cell to noise margin is measured using the static noise margin (SNM) metric for the read and hold operation. Whereas, for the write operation, the write margin (WM) is calculated. The SNM is determined as the side of the largest square that fits inside the smaller lobe of the butterfly curve

[12]. While, the WM for the bit cell is defined as the difference between the WL voltage and the BL voltage during the trip point [13]. The static noise margins for the three operations—read, write, and hold for the 6T, 6T1, 7T, and 7T1 cells are compared in Fig. 2, and the values are shown in Table 2.

As can be observed, the SNM value for 6T1 and 7T1 is same for the hold and read operation. The same is attributed to the single-ended topology of the read operation for the cell. But the employment of M3 in the cut-off region throughout the operation of the 6T1 cell has negatively impacted its SNM value. Whereas, the SNM values for 7T1 cell are fairly high. The SNM values for hold and read operation are different for the 6T and 7T cell owing to their differential read operation. A differential read operation causes the read current to pass through the storage node of the cell, thereby increasing its susceptibility to noise. This results in decrement in SNM value for the cell during the read operation. While, on the basis of WM all the cell register, a similar values as can also be inferred for Fig. 2, except 7T cell, which registers a very high WM value of 164 mV.

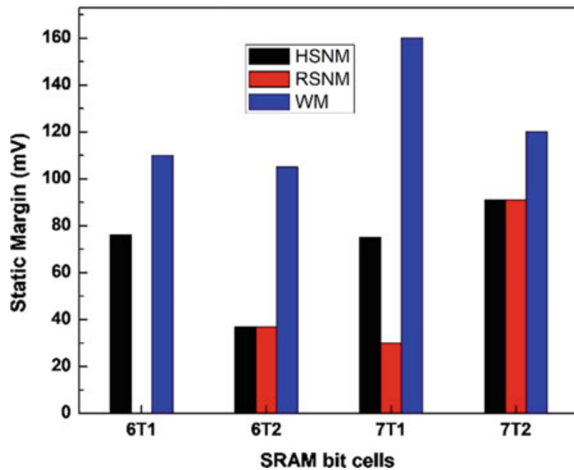

Fig. 2 Graphical comparison of static noise margin values for various SRAM bit cells

Table 2 Performance of all the SRAM bit cells for static noise margin, leakage current, global variation, and write delay

	Static noise margin (mV)			Leakage current (nA)		Global variation (mV)			Write delay
	HSNM	RSNM	WM	Q = 0	Q = 1	HSNM	RSNM	WM	
6T	76	0	110	441	116	53	0	98	50
6T1	37	37	105	229	50	21	18	50	100
7T	75	30	160	31	4	56	0	100	130
7T1	91	91	120	28	3.5	68	68	90	30

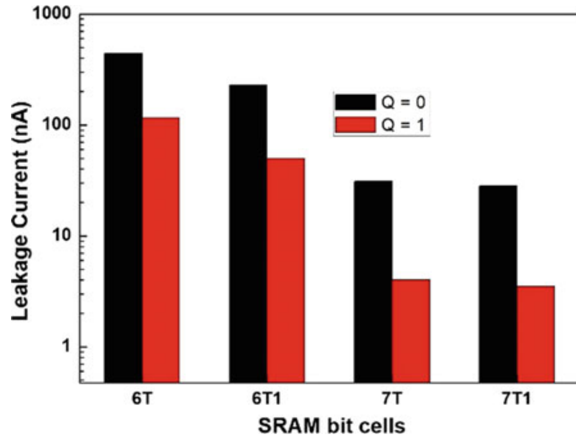

Fig. 3 Comparison of the leakage current values obtained for Q = '0' and Q = '1' for the different SRAM cells

3.2 Leakage Current

One of the major concerns of the circuits designed in the nanometer vicinity is the increased propensity of leakage current. The decreased channel length for the device facilities easy conduction of electrons in the OFF state, thereby resulting in high leakage current. As a consequence, evaluation of leakage current for circuits designed at lower technology node is essential. For an SRAM circuit, the leakage current is caused by three major components—gate leakage, sub-threshold leakage, and reverse junction leakage [14]. The different SRAM cells described in the paper are all evaluated for leakage current. As expected, the 6T cells register higher leakage in comparison with the 7T cells. This is because both the 6T cells were designed with higher aspect ratios for higher performance. But, the 6T1 cell was reported in 2019 and is an improvement over the 6T cell; consequentially, its leakage current is lower than the 6T1 cell. Both 7T designs have better leakage current performance when compared with the 6T designs. But of the two 7T cells, the 7T1 cell had slightly better performance; the single-ended circuitry for the 7T1 cell reduces the leakage current outlets for the 7T1 cell. The 7T SRAM bit cell being of the differential ended nature has a slightly higher leakage current. The leakage current values for the different cells are graphically compared in Fig. 3 and listed in Table 2.

3.3 Write Delay Analysis

During the write operation, the SRAM bit cell has to deliberately cause a discharge event through the bitline (s) to result in a data change at the storage node. Consequently, write operation for an cell is the most time-consuming process. Therefore, it usually is the process that determines the minimum timing requirement for the cell. As a result, it is a parameters that defines the timing analysis for the bit cell.

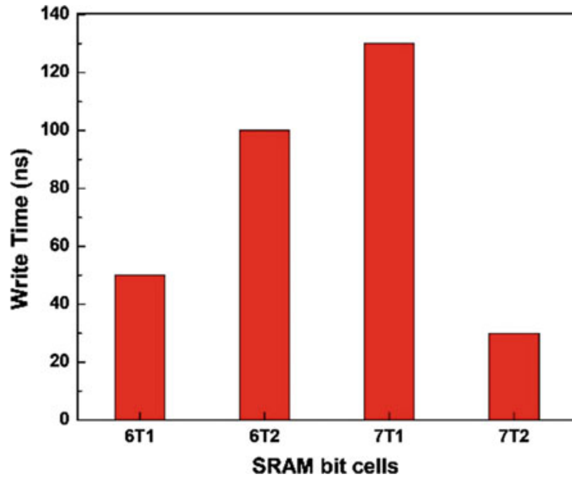

Fig. 4 Graphical comparison for the write time values for the different SRAM bit cells

The different cells are compared for the write timing requirement in Fig. 4, and the values are listed in Table 2.

The highest write time is required by the 7T cell of 100 ns to perform a successful write operation. This is because the 7T cell reduces the back-to-back inverter pair topology to a cascaded inverter configuration during the write operation (this improves cells stability to noise) but does not take any additional remedy to improve the write time for the cell. A similar topology is used by 7T1 cell as well, but it relies on a high-performance NMOS (M5) to enhance the write time requirement for the cell. Also, the 7T cell was reported for 180 nm technology node and 1.1 V supply voltage, whereas the analysis is being performed at a fairly low technology node. Thereby, impacting the performance for the 7T cell. The 6T cell on the other hand has fairly fast write operation; this is in keeping with the differential nature of the cell. Whereas, the 6T1 SRAM bit cell is single-ended and therefore witness a rise in write time requirement.

3.4 Global Variation Analysis

A variation in performance of a circuit designed at nanometer vicinity can be observed due to fabrication imperfections such as oxide thickness, line edge roughness, and discrete random dopant [15]. These fabrication imperfections are accounted for and analyzed using the global variation analysis. This analysis is used to determine the maximum range of variation in the SNM of a bit cell when it is subjected to maximum variation due to fabrication imperfections.

A cell is deemed resilient to global variations if the variation in its static noise margins is minimal for worst case global variation. In this sections, the cells are compared for the range of variation that a cell may observed because of global

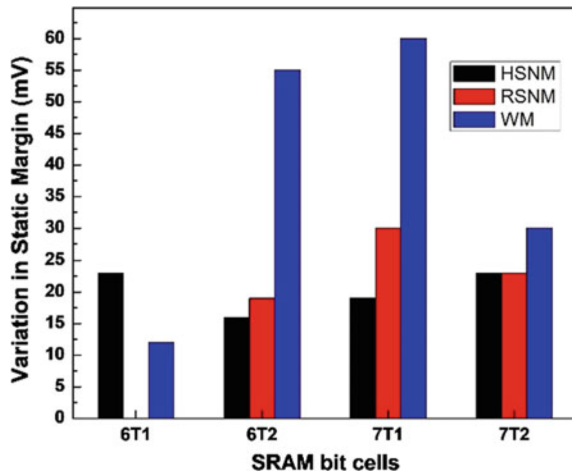

Fig. 5 Graphical comparison for the maximum variation in the static noise margin values for different SRAM bit cell under global variation

variation. The highest variation in performance for the hold operation is for the 7T1 cell, while the least variation in performance is observed for 6T1 cell. While, for the read operation, the cell with the highest variation in performance is for 7T cell, while the least is for 7T1 cell. The write margins for the 7T cell are highly vulnerable to global variations. While, the WM is least vulnerable for the 6T cell. The variation in the static noise margin values for all the operation of a cell is graphically compared in Fig. 5 and shown in Table 2.

4 Conclusion

SRAM bit cells form the core for designing cache memory, which are a prevalent form of memory used in most microprocessors. With the declining technology node to increase cell packaging density and scaling supply voltage to minimize the power requirement, the performance of the bit cell has plummeted. The conventional SRAM bit cell has experienced decline in its performance, so SRAM bit cells designed using high-performance transistors are being reported in the literature. In this paper, a comparison of typical SRAM cell with high-performance transistor-based SRAM cell is performed. Four SRAM bit cell topologies, 2 each (1 typical and other high-performance transistor-based) of 6T and 7T, are described. Their performance in terms of static noise margins, leakage current, write time, and global variation analysis is presented in the paper. The 7T1 cell with the most stable static noise margin value of 91 mV for both read and hold operation, while its write margin is 120 mV. The cell with the weakest static noise margin performance is the 6T cell as it registers a failure in read operation as its read static noise margin value is 0 mV. It is also the cell that registers the highest leakage current values of 441 pA and 116 pA for Q = '0' and '1', respectively. But this cell has a superior performance in terms of write

time, with a timing requirement of 50 ns; a cell with an even better write time is the 7T1 cell, with a write time requirement of 30 ns. Whereas, in terms of global variation analysis, the cell that outperforms against other cells is the 6T1 cell with the least variation in its hold, read, and write margin values for maximum variation caused by fabrication inconsistencies.

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