Design and Simulation of High Performance Hybrid Full Adder Using CMOS 45 nm Technology

S. Jayamangala, T. Pullaiah, J. Sunilkumar, and M. Sivakumar

Abstract The new blended model is mostly utilized in the designing process of an arithmetic circuitry. The efficiency of a full adder with the factors of holding time, potential charge utility and the strength of the circuit is highly based on how efficiently the circuit will work. From this project, a large speed, low power consuming count of ten transistors logic circuit is designed, and it generates effective fluctuations at the same time with effective delay at output. The performance efficiency of the designed circuit is calculated by simulating it in a tanner software using 45 nm technology. The established circuit decreases the PDP factor at least by 15% than already existing XOR–XNOR models. In this project we are introducing two different designs of full adders those are designed in this article by using the already designed XOR–XNOR circuitry and existed sum and carry generating blocks. The designed full adders provides 10–40% betterment in words of power fluctuation product in the comparison of other models. To calculating the driving capacities the proposed full adders are fixed in multistage full adder circuits. Outputs show that two of the designed full adders generate the better results for a larger count of data bits in all the full adders.

Keywords Multistage adder · High fluctuation · Blended full adder · Logic circuit

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1 Introduction

Present days the people are showing interest to do smart work to manage their regular activities without any time inconsistency. So the people are attracted by the technological circuits. People not only concentrating on the designing process they are also thinking about to do the work in fast and efficient way. To design those type of electronic systems the designers will concentrate on size of the circuit and speed and energy efficient related designs [1]. The electronic systems highly containing the arithmetic circuits to calculate the efficiency of output. Basically the summer is a main building block for the different logical blocks. These circuits are mostly utilized to transfer the data in related designs [2]. They are also used in 1/3 of power utilized microprocessors. To improve the working of the adders along with the whole design at the same time.

To design a full adder we required a few static CMOS logic models to be presented. These logics can be mainly differentiated in 2 different ways: unblended and blended model of designing. In classical model of designing process the full adder is manufactured in a unic block using transistors [3]. The terminated adder is an example of this designing model. For this circuit we are using 24 active elements to build a above and below parts of a full adder. It is generates effective fluctuating results. The main demerit that the circuit is having a large forward capacitor and is connected to a pair of N&P type transistors these can decreases the performance efficiency of the circuit. Other design for the unblended model of designing process is inverting moving transistor logic related adder [4, 5]. This circuit generates high speed and high swing output with an excellent driving capacity due to large speed multi stage, coupled transistor model and reversing at the output. It has high potential loss because of more number of inner connections in the design. We are able to design a full adder by using differential transistors [5]. The differential transistors having a demerit is that high threshold voltage drop. When the inputs are given as "10" through the pair of N&P transistors. We did not get the same output at the full adder These XOR–XNOR signals must have highly effective input and output signals.

2 Literature Survey

New technology is coming in to the VLSI designing process. As technology is changing as well as the specification designs of the system is also changing. The advanced technology is mostly concentrating on less area occupation and low power consumption and also it is concentrating on high accessing speed. These Styles are trying to have a reduced fluctuations [6, 7]. With this designing process may using 0.18 um technology and we are testing the testbench setup that measures the power consumption at full adder inputs. In this project we also concentrate on energy efficiency by reducing the size of the design. We are using different technologies to

calculate the power consumption, Energy efficiency and how much area was occupied by the design of the system on chip (SOP).

In the process of working on digital signal processing we are using digital circuits like microprocessors, microcontrollers, and full adders. Which all are works on the processing the images in digital way [7]. To get the accurate designing process of a full adder we mostly concentrate on circuitry speed, area and power utilization of the circuit. To minimize the potential utility we are using different techniques like GDI design and blended transistor logic model here we are designing ripple carry adder for the wide range of applications. To design adder we are eliminating the usage of XOR/XNOR logic gates. Normally addition is the most common arithmetic operation that has to be performed using adder to design full adder we are using CMOS transistor designing process. From this paper we designed an adder by utilizing the blended CMOS logic model. It divides the entire circuit into three modules. In the first stage we can observe XOR XNOR logic circuitry [8] which generates the effective outputs and it also have good driving capacity. The second stage contains the sum circuitry which gets the input from the first stage and which produces the effective sum as output. First stage which takes the inputs from the input circuit elements which feeds its outputs to the second stage and to the third stage [9]. From the second stage we are getting sum as output and from the third stage we are getting carry as output. We proposed this hybrid CMOS multistage adder block to reduce the utilization of the potential, fluctuation between the carry input and output. In conventionally we are designing the complementary pass transistor logic (CPL) to get an effective output by reducing the transistor count [10].

3 Existing Techniques

For Fig. 1 we are giving the inputs ABC as 110, i.e., $A = 1$, $B = 1$, $C_{\text{in}} = 0$. For the XOR circuitry we are giving the inputs A&B as 11 so that both the PMOS transistors P1&P2 will become off and will generate the output as 0(zero) [10, 11]. The NMOS transistors N3 and N4 are fed with 1 and 1 so that the transistors are getting on so that the entire input is getting connected with GND so that the output becomes 0 which will store in X. The $X = 0$ is given as input to the N5 transistor and it becomes off, so the final output of XOR circuitry is 0, i.e., XOR = 0. For the XNOR circuit we are giving 1, 1 as input to the NMOS transistor those are N1&N2 so that the transistors are getting on it will generates the output as 1 [12, 13]. A&B is given to the PMOS transistors P3&P4 which become off so that which generates the output as 0 which output is giving as input to the transistor P5. Hence, it's become on. The final output through the XNOR circuitry is 1 (Fig. 2).

The author proposed a circuit of 6 T XOR XNOR logic block to design a conventional full adder. This design showed two complementary feedback boosters utilized to reuse the low performance signal in differential mode when the two inputs have unique logic. This circuit has high delay for the inputs of the same pair of logic values; outputs of this final circuit get their last voltage levels in two stages. This problem is

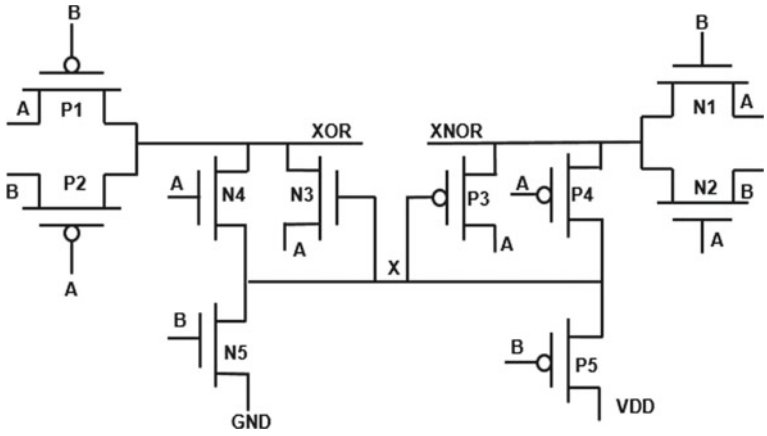

Fig. 1 Existing schematic of XOR XNOR circuit

solved by Chang. This proposed circuit generates better driving capacity, full swing at output [13]. The X-coupled diagram attaches an excess parasitic element to the XOR XNOR circuit at results. Table 1 shows the comparison table for XOR and XNOR gates at Full Swing and at partial swing. In the change method there are some defaults that are improved by Naseri and Timarchi which are designed for 12 T [14]. This circuit can take less power, produces a better delay. The XOR XNOR circuit has further changes to its better way of implementation. Even in the final circuitry we also find some mistakes when we are simulating that design by using the tanner 13 tool. In this project we are taking these drawbacks as a challenge and we are working on this project to overcome these demerits [14, 15].

4 Proposed Techniques

For the we are Fig. 3a giving the inputs ABC as 110, i.e., $A = 1$, $B = 1$, $C_{\text{in}} = 0$. For the XOR circuitry we are giving the inputs A&B as 11 so that both the PMOS transistors P1&P2 will become off and will generate the output as 0(zero). The NMOS transistors N3 and N4 are fed with 1 and 1 so that the transistors are getting on so that the entire input is getting connected with GND so that the output becomes 0 which will store in X. The $X = 0$ is given as input to the N5 transistor, so the final output of XOR circuitry is 0, i.e., XOR = 0 [16]. For the XNOR circuit we are giving 1, 1 as input to the NMOS transistor those are N1&N2 so that the transistors are getting on it will generates the output as 1. A&B is given to the PMOS transistors P3&P4 which become off so that which generates the output as 0 which output is giving as input to the transistor P5. Hence, it is become on. The final output through the XNOR circuitry is 1 [17].

We are giving inputs as 110 through N8, P8 and C_{in} and XNOR so that the transistors become on and will generate the carry as output, i.e., $C_{out} = 1$. For the transistors P9, N9 fed with the inputs as XOR, C_{in}' and XNOR so that both the transistors will become on and which will generate carry as 1. We are giving C_{in}, XOR and XNOR inputs as transistors P6&N6 which will turn off the transistors will generate the output as 0 that is SUM. XOR, XNOR and C_{in} as inputs to the transistors P7&N7 and which turns off the transistors and will generates the SUM as 0. For the design 1 we are giving the inputs ABC as 110, i.e., $A = 1$, $B = 1$, $C_{in} = 0$ [18]. For the XOR circuitry we are giving the inputs A&B as 11 so that both the PMOS transistors P1&P2 will become off and will generate the output as 0(zero). The NMOS transistors N3 and N4 are fed with 1 and 1 so that the transistors are getting on so that the entire input is getting connected with GND so that the output becomes 0 which will store in X [19–21]. The $X = 0$ is given as input to the N5 transistor, so the final output of XOR circuitry is 0, i.e., XOR = 0. For the XNOR

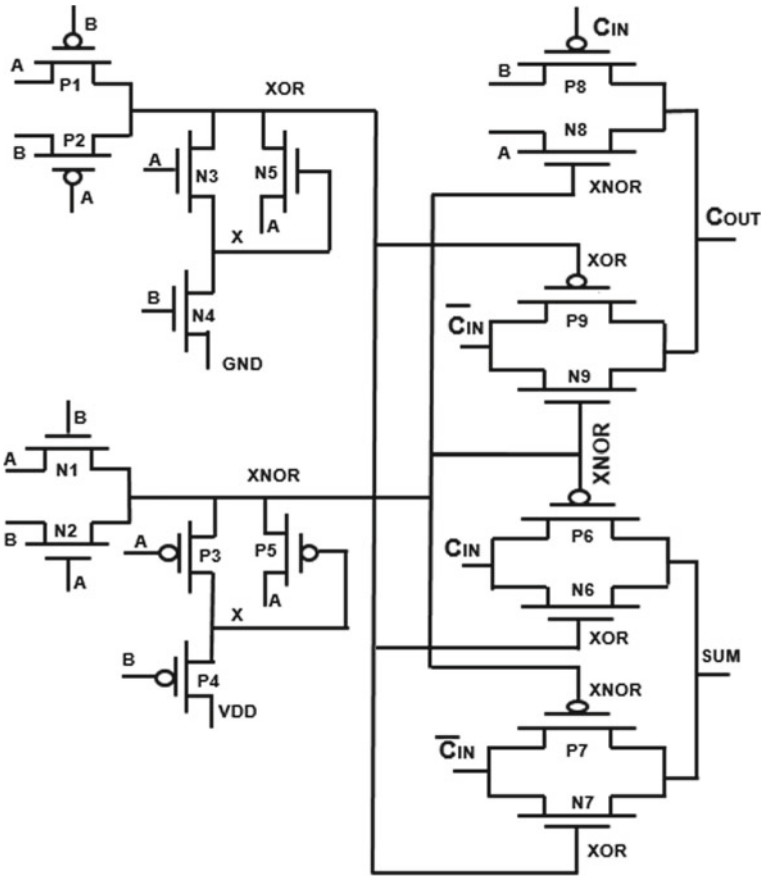

Fig. 2 **a, b** Existed conventional full adder schematic

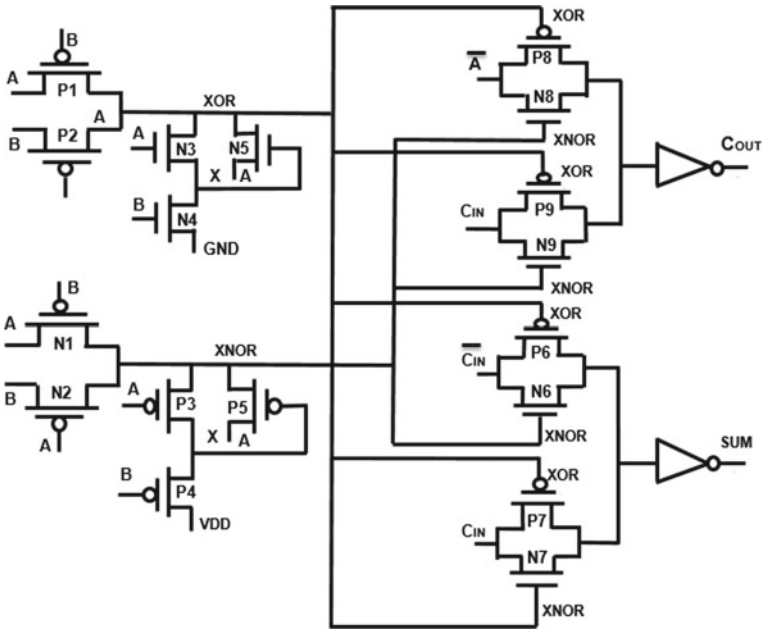

Fig. 2 (continued)

Table 1 Performance of the inputs of a XOR & XNOR circuit in different paths

Inputs *A*, *B*	Path		Path	
	XOR (full swing)	XOR (partial swing)	XNOR (full swing)	XNOR (partial swing)
00	N3	P1, P2	P4, P5	–
01	P2	–	N1	P4, P3
10	P1	N4, N3	N2	–
11	N4, N5	–	P3	N1, N2

circuit we are giving 1, 1 as input to the NMOS transistor those are N1&N2 so that the transistors are getting on it will generates the output as 1. A&B is given to the PMOS transistors P3&P4 which become off so that which generates the output as 0 which output is giving as input to the transistor P5 [21]. Hence, it's become on. The final output through the XNOR circuitry is 1. We are feeding the XOR XNOR circuit results as inputs to the sum and carry circuitry. For the transistors P8&N8 we are giving inputs as *A*', XNOR and XOR so that the transistors become on and will generates the output as 1 and for the transistors P9&N9 as C_{in} and XNOR and XOR so that the transistors become on will generates the output as 1. As a theoretical calculation for the input 110 we need to get carry as 1 so that we are placing the inverter at output of the carry circuit [22]. Hence, we are getting C_{out} as 0. For the

sum circuit we are giving inputs as C_{in}, XNOR, XOR to the transistors P6&N6 so that the transistors become off will generates the output as 0 and C_{in}' and XOR and XNOR to the transistors P7&N7 so that the transistors becomes off so that the sum circuit will generates output as 0.

5 Result

The conventional full adder proposed by the authors was scrutinized and found some drawbacks were taken as a challenge and we overcame those issues. The simulation results of the previous techniques and present techniques was represented in Table 2 for the comparison factors of Power, delay, PDP. In the older IEEE papers the authors was used the 180 nm technology and 90 nm technologies [23]. In this paper we are using 45 nm technology and we are simulating our proposed conventional full adder and we are on the inputs as '110' for this input we are getting effective results. From the comparison table we plotting the graphs for voltage V_s power and Voltage V_s delay and along with Voltage V_s PDP as shown in Figs. 3 and 4.

The output plot of the proposed technology is shown in below simulated Fig. 5.

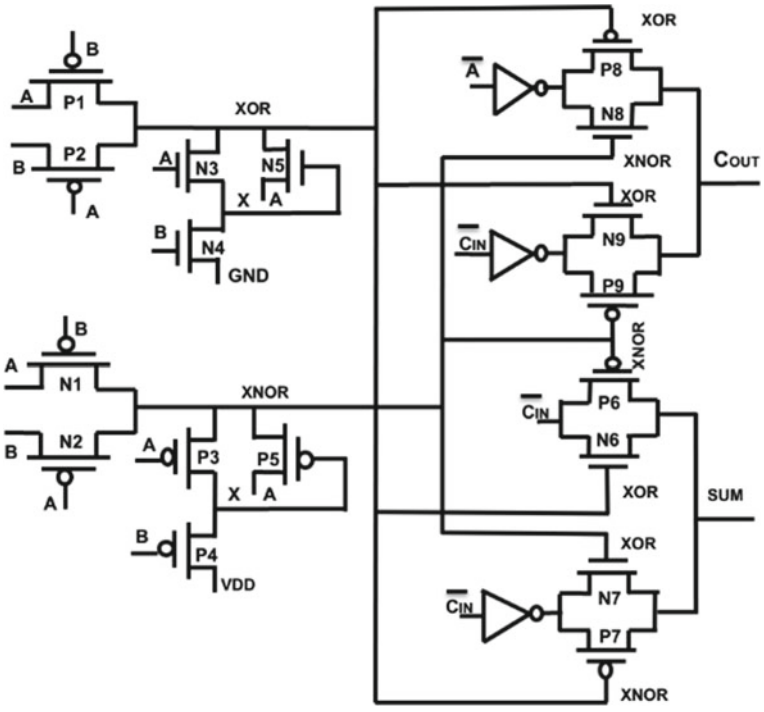

Fig. 3 **a, b** Proposed full adder schematic

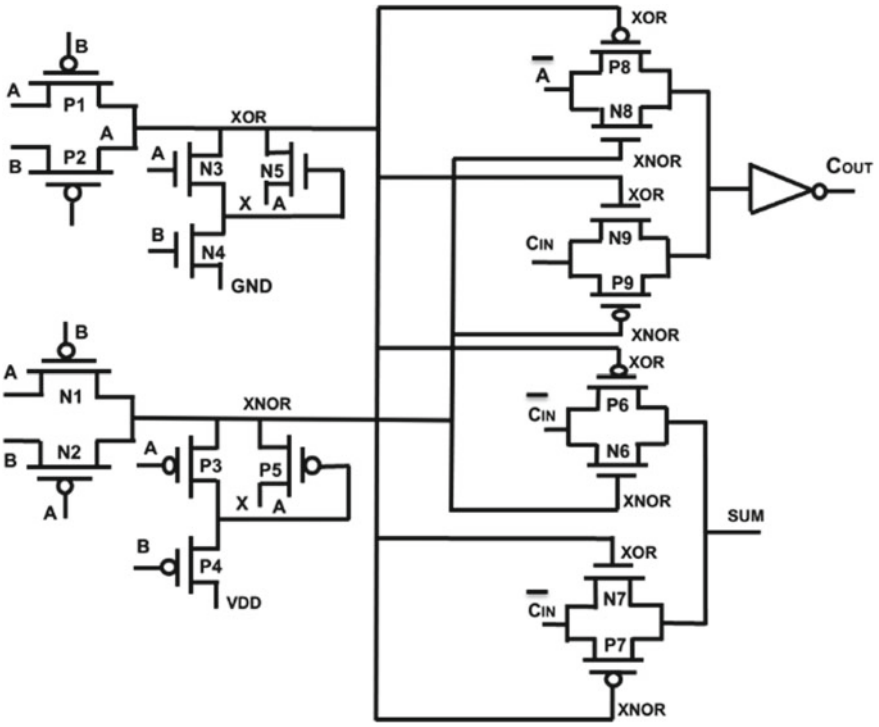

Fig. 3 (continued)

Table 2 Comparison table for existed technology and proposed technology

Conventional full adders	No of transistors	Existed technologies (90 nm)			Proposed technologies (45 nm)		
		Power (uW)	Delay (ps)	PDP (10^{-18})	Power (W)	Delay (ns)	PDP (10^{-18})
ZAVAREI [18]	26	72.3	27	1952.1	72.3	27	1952.1
VALSHANI [17]	18	71.3	25	1782.5	71.3	25	1782.5
BHATTACHARYYA [12]	16	65.59	22.6	1482.33	65.59	22.6	1482.33
H.NASERI [15]	22	55.8	26.7	1489.86	55.8	26.7	1489.86
Schematic-1	20	52.3	27.09	1459.17	9.88	150.02	1482.19
Schematic-2	26	71.8	30.4	2182.72	10.7	149.69	1601.68

6 Conclusion

In this project, a new model conventional multistage adder was established by using XOR XNOR circuit by taking reference from few of previous papers proposed

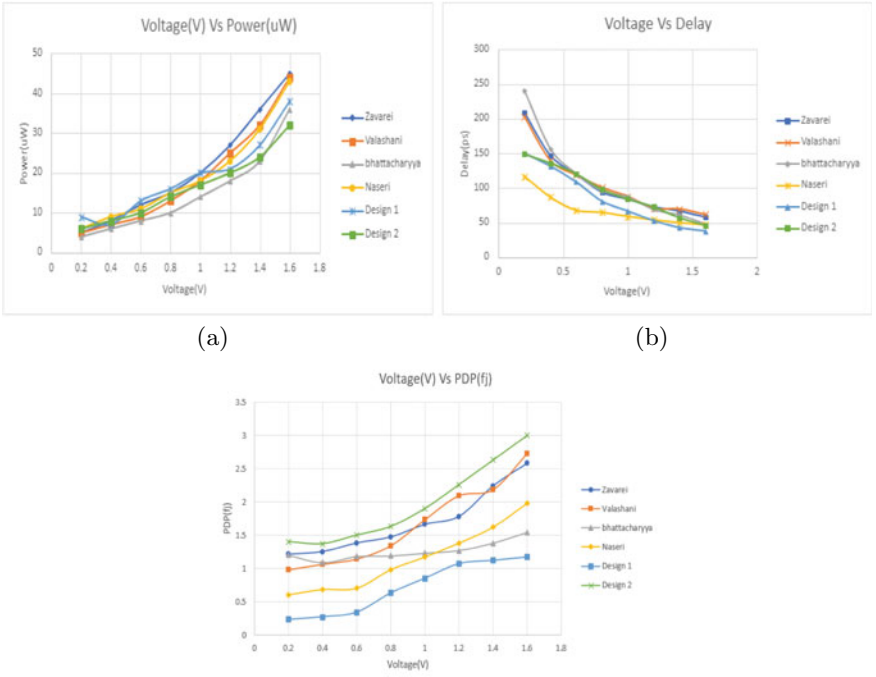

Fig. 4 Proposed design graph **a** voltage versus power, **b** voltage versus delay, **c** voltage versus PDP

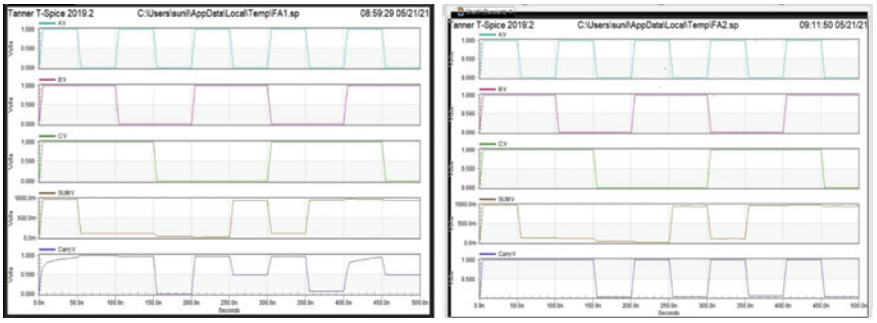

Fig. 5 Simulated output results **a** design 1, **b** design 2

by authors which generates the full swing outputs continuously. By utilizing this proposed XOR–XNOR circuit we designed 2 discrete types of adder circuits with effective outputs. The simulation results of the present XOR XNOR circuitry and the adder circuitry was verified by using mentor graphics 45 nm technology tool.

The present XOR XNOR block represents decrease in words of fluctuations, Delay up to 58%, 60% and power up to 60%, PDP up to 75%, 78.02%, respectively. Then comparing with other models.

References

1. Amini-Valashani M, Ayat M, Mirzakuchaki S (2018) Design and analysis of a novel low-power and energy-efficient 18T hybrid full adder. Microelectron J 74:49–59
2. Naseri H, Timarchi S (2018) Low-power and fast full adder by exploring new XOR and XNOR gates. IEEE Trans Very Large Scale Integr (VLSI) Syst 26(8):1481–1493
3. Nigam A, Singh R (2016) Comparative analysis of 28T full adder with 14T full adder using 180nm. Int J Engg Sci Adv Res 2(1):27–32
4. Valashani MA, Mirzakuchaki S (2016) A novel fast, low-power and high-performance XOR-XNOR cell. In: Proceedings of the IEEE international symposium on circuits and systems (ISCAS), pp 694–697
5. Kumar A, Singh K (2015) A low-power 12 transistor full adder design using 3 transistor XOR gates. Int J Electron Electr Comput Syst 4
6. Bhattacharyya P, Kundu B, Ghosh S, Kumar V, Dandapat A (2015) Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit. IEEE Trans Very Large Scale Integr (VLSI) Syst 23(10):2001–2008
7. Foroutan V, Taheri M, Navi K, Mazraeh AA (2014) Design of two low-power full adder cells using GDI structure and hybrid CMOS logic style. Integration 47(1):48–61
8. Agarwal M, Agrawal N, Alam MA (2014) A new design of low power high speed hybrid CMOS full adder. In: Proceedings of the international conference on signal processing and integrated networks (SPIN), pp 448–452
9. Tung C-K, Shieh S-H, Cheng C-H (2013) Low-power high-speed full adder for portable electronic applications. Electron Lett 49(17):1063–1064
10. Lin J, Hwang Y, Shew M (2012) Low power 10-T full adder design based on degenerate pass transistor logic. ISCAS, IEEE
11. Ramkumar B, Kittur HM (2012) Low-power and area efficient carry select adder. IEEE Trans Very Large Scale Integr (VLSI) Syst 20(2)
12. Kumar M, Arya SK, Pandey S (2012) Low power CMOS full adder design with 12 transistors. Int J Inf Technol Convergence Serv (IJITCS) 2(6)
13. Aguirre-Hernandez M, Linares-Aranda M (2011) CMOS full-adders for energy-efficient arithmetic applications. IEEE Trans Very Large Scale Integr (VLSI) Syst 19(4):718–721
14. Zavarei MJ, Baghban Manesh MR, Kargaran E, Nabovati H, Golmakani A (2011) Design of new full adder cell using hybrid-CMOS logic style. In Proceedings of the 18th IEEE international conference on electronics, circuits, and systems, pp 451–454
15. Goel S, Kumar A, Bayoumi MA (2006) Design of robust, energy efficient full adders for deep-submicrometer design using hybrid-CMOS logic style. IEEE Trans Very Large Scale Integr (VLSI) Syst 14(12):1309–1321
16. Chang C-H, Gu J, Zhang M (2005) A review of 0.18-μm full adder performances for tree structured arithmetic circuits. IEEE Trans Very Large Scale Integr (VLSI) Syst 13(6):686–695
17. Zhang M, Gu J, Chang C-H (2003) A novel hybrid pass logic with static CMOS output drive full-adder cell. In: Proceedings of the international symposium on circuits systems (ISCAS), vol 5. p 5
18. Tien Bui H, Wang Y, Jiang Y (2002) Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates. IEEE Trans Circ Syst II, Analog Digit Signal Process 49(1):25–30
19. Radhakrishnan D (2001) Low-voltage low-power CMOS full adder. IEE Proc-Circ Dev Syst 148(1):19–24

20. Vesterbacka M (1999) A 14-transistor CMOS full adder with full voltage swing nodes. In: Proceedings of the IEEE workshop on signal processing systems. SiPS 99. Design and implementation (SiPS), pp 713–722
21. Zimmermann R, Fichtner W (1997) Low-power logic styles: CMOS versus pass-transistor logic. IEEE J Solid-State Circuits 32(7):1079–1090
22. Chandrakasan AP, Sheng S, Brodersen RW (1992) Low-power CMOS digital design. IEICE Trans Electron 75(4):371–382
23. Zhuang N, Wu H (1992) A new design of the CMOS full adder. IEEE J Solid-State Circuits 27(5):840–844
24. Kandpal J, Tomar A, Agarwal M, Sharma KK (2020) High-speed hybrid-logic full adder using high-performance 10-T XOR–XNOR Cell. IEEE Trans Very Large Scale Integr (VLSI) Syst 28(6):1413–1422. https://doi.org/10.1109/TVLSI.2020.2983850