Implementation and Performance Evaluation of Hybrid SRAM Architectures Using 6T and 7T for Low-Power Applications

M. Parvathi and M. C. Chinnaaiah

Abstract Static random access memory (SRAM) is one of the key components in the growing embedded systems with a demand in its increased capacity. It is necessary to do power analysis at the early stages of the design process for such large sized SRAMs to avoid further complexities that degrade system performance to worst. SRAMs are greatly delved from 6T to 10T with its size against to the read and write stability issues. However, use of 10T alone in the large sized memories is not feasible for the low-power system architectures. In this paper, a unique style of dual-port hybrid SRAM memory architectures is proposed using different combinations of 6T and 7T. The hybrid model using 6T-7T SRAM cell is performing well over traditional 6T-6T and 7T-7T architectures with power reduction improvement of 27.2% and 30.5%, respectively, and with area reduction improvement of 26.1% and 8.15%, respectively.

Keywords SRAM · Low-power designs · Hybrid memories · Embedded systems · 6T to 10T

1 Introduction

The ever growing demand in portable electronic device applications leads to technology evolution in the VLSI design architectures. One of the critical empirical parameters that needs control over the microelectronic technology is power dissipation, especially required in low-power VLSI circuit designs. The trending submicron meter technologies designs for high speed results in increased circuit complexity in addition to power consumption. In the lower technology nodes, one of the traditional methods for power reduction technique follows supply voltage scaling [1]. However, for the circuits like SRAM with large capacity building blocks, the so called power

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V. Bhateja et al. (eds.), *Communication, Software and Networks*, Lecture Notes in Networks and Systems 493, https://doi.org/10.1007/978-981-19-4990-6_22

reduction techniques always cause stability issues. Hence, circuit and system level techniques are needed since the device and voltage level scaling are not feasible methods in providing good results while achieving for low power. Most of the literature suggests supply voltage reduction technique [2] to use as effective and efficient way for leakage power reduction. SRAMs are in general used as primary memory or caches in portable devices due to their inherent faster response. Also, SRAMs are free from periodical refreshing in contrast to its counter memories. However, the predominant limitation of use of SRAM is subthreshold and gate leakage current [3], which are dominant in the large high capacity memory structures.

In multi-core or multiprocessor environment such as high speed computers or and digital signal processors, the use of multiport SRAMs is essential [2, 4–6]. The multiport SRAMs are essential building blocks used as multiport register files in high range modern FPGAs or in multi-core system-on-a-chip (SoC) devices. The advantage multiport over traditional single-port SRAMs is, the multiport memories allow simultaneous access to multiple devices that results in increased throughput. More research is happening in the recent years in the development of various high density, fast multiport memories due to the increased demand for high performance multi-core processors. Few are hybrid memories [7] uses combination of SRAM and DRAM that allow to store multiple bits in each cell. However, to perform read and write operations using this type of hybrid memory, more context switching operations are required, that leads to degradation of system speed. Other hybrid model can be observed using combination of SRAM and CAM [8] for the low-power applications, but its use is specific to applications due to its uniqueness in the design. In this paper, the various dual-port hybrid SRAMs are proposed using the combinations from 6T to 7T. Section 2 presents contemporary design approaches of the SRAM cells using conventional techniques. Design of proposed SRAM cell using hybrid techniques is discussed in Sect. 3. Section 4 presents simulation results and comparative analysis followed by conclusions in Sect. 5.

2 SRAM Cell—Contemporary Design Approaches

Due to poor write stability and read disturbances, the 6T SRAM cell has been reformed to 7T to 10T in the due course of its development for the betterment of signal to noise stability. However, for the present multi-core embedded system, environment needs multiport SRAMs rather than single port. Simple dual-port SRAM cell is shown in Fig. 1. In contrast to single port in which only one port will be used for reading and writing the data, dual-port will have two ports operated as address inputs. In single-port memories, the data lines separated to be used as output and input connections, in addition single address input. This causes either a read or write operation only can be performed as it can be accessed at a time for any operation. This drawback can be overcome using multiports, which consists of many address inputs with corresponding data inputs and outputs. It allows read and write operations in parallel depends on the number of input address line. The minimum sized

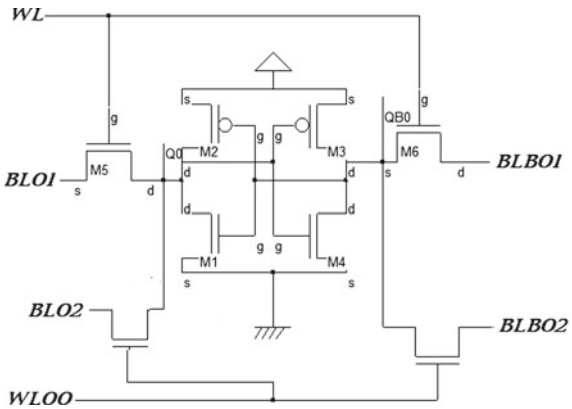

Fig. 1 Dual-port SRAM cell

multiport memory is dual-port memory itself. Though the bit capacity is same, one drawback with multiport memories to its counterpart single-port memory is that, it needs more area due to separate address decoder and data multiplexers to access each port. Hence, it is necessary to identify suitable multiport memory architectures that suits low-power design systems.

When it comes to multi-cell array designs, two types of architectures can be followed such as two cell bit line model and two cell word line model. Two cell bit line model is mere similar to the single-cell model with the additional memory bit cell stacked on the bit lines, whereas a two cell word line model includes two horizontally nested bit cells with two pre-charge and bit line circuits. However, the two cells belong to the same word line, hence, only one word line driver is desirable. The proposed work is based on two cell word line models only due to its importance over single-cell structures.

3 Design of Proposed Dual-Port Hybrid SRAM Cell

This section discusses about various hybrid designs of dual-port memories that uses combination of SRAM circuits with 6T and 7T.

3.1 Two Cell Dual-Port SRAM Architectures

The work on dual-port hybrid SRAM architectures is divided into two sections, one is two cell architecture and other is four cell architecture. In the two cell architecture model, we have considered 6T-6T and 7T-7T SRAM models using traditional CMOS design, then designed the proposed hybrid SRAM using 6T-7T and 7T-6T combination.

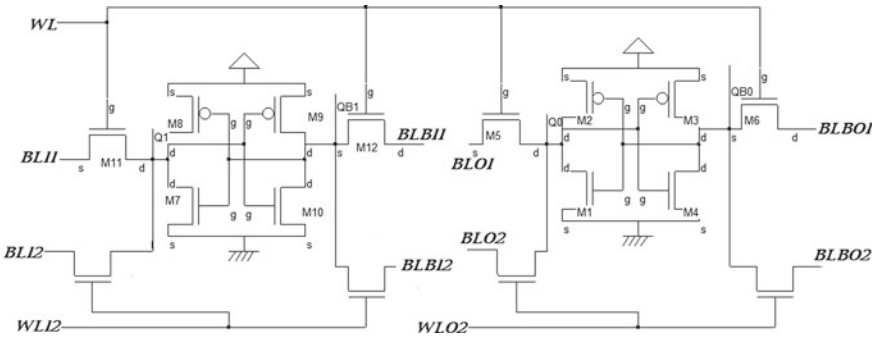

Fig. 2 Dual-port two cell 6T-6T SRAM word line model

3.1.1 Dual-Port 6T-6T SRAM Two Cell Model

At the initial stage, the dual-port SRAM using 6T-6T two cell model is implemented using two cell word line model, as shown in Fig. 2. Write operation can be performed by selecting bit line with data and assert either of the word lines. For write '1' in port 1 operation, assert BL_{11} to logic '1,' and then assert WL_{12} line. Similarly, for write '0,' assert BLB_{11} to '1' (indicates BL_{11} to '0'), then assert WL_{12}. In the same for port 0, but write operation happens through WL_{02} line. For read operation to perform, pre-charge both the bit lines BL_{11} and BLB_{11} to high, then assert corresponding port word line (WL_{11} in this case). As a result, one can observe that the pre-charge value at BLB_{11} gets discharge to '0' through the corresponding nMOS transistor connected to that bit line, while retaining charge on BL_{11} to indicate read '1' operation. If 'WL' is used to write or read operations, then two-port SRAM operation is similar to single-port cell operation. Corresponding simulation results indicates the minimum read delay of 24 ps, with 0.311 mw power consumption by the architecture.

3.1.2 Dual-Port 7T-7T SRAM Two Cell Model

The dual-port 7T-7T SRAM two cell model is implemented to observe the performance variation in terms of minimum read delay, power dissipation along with critical path delay compared to its counter models 6T-6T and hybrid model 6T-7T. The corresponding 7T-7T SRAM cell simulation results indicate 38 ps of minimum read delay with 0.622 mw power dissipation by the architecture.

3.1.3 Hybrid 6T-7T and 7T-6T Dual-Port SRAM Two Cell Model

The dual-port SRAM using 6T-7T two cell model is implemented using two cell word line model, as shown in Fig. 3.

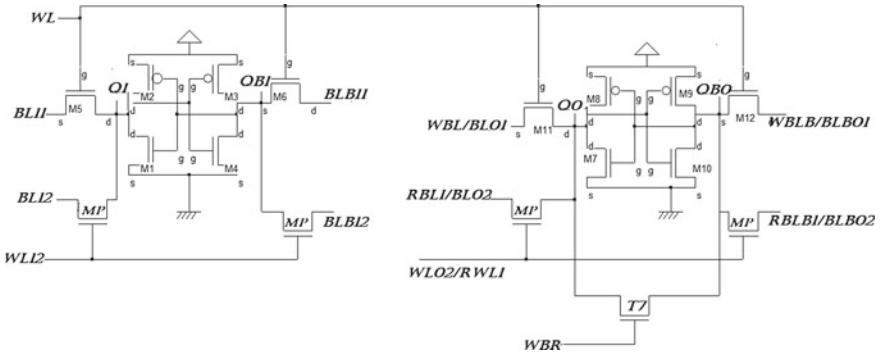

Fig. 3 Two bit dual-port hybrid memory using 6T-7T combination

It uses additional control for write operation in 7T structure with the name WBR using additional 7th transistor compared to its 6T counterpart. Transistors with name 'MP' are used to perform write or read operations in dual-port mode. Using WL line, both 6T and 7T cells get activated simultaneously to write through BL_{11} and WBL (or BL_{01}) into their cells, respectively, for port1. Similarly, for port2, the write operation can be performed using BL_{12} and RBL1 (or BL_{02}). The data will be read by the two cells by the same bit lines in the read mode using prior pre-charge requirement. Additional transistor T7 in 7T is to be maintained in the state 1/0 as per read/write operation.

The simulation results of 6T-7T dual-port hybrid SRAM model are shown in Fig. 4, in which the minimum read delay of 1058 ps, and 0.407 mw of power dissipation are observed. In the similar way, hybrid model using 7T-6T two cell SRAM is designed in which the first cell is taken as 7T followed by 6T. The worth note point in this model is, raise in power dissipation by 16% compared to 6T-7T architecture.

3.2 Four Cell Dual-Port SRAM Architectures

The dual-port SRAM architectures are further studied taking four cell models into consideration. For this, the initial 6T-6T dual-port cell is used twice for obtaining four cell model, then, extended to 7T four cell model. Further, the hybrid four cell models are designed using the combination of 6T and 7T dual-port cells. The four cells can be drawn either column wise or row wise by taking their corresponding read lines or write lines common.

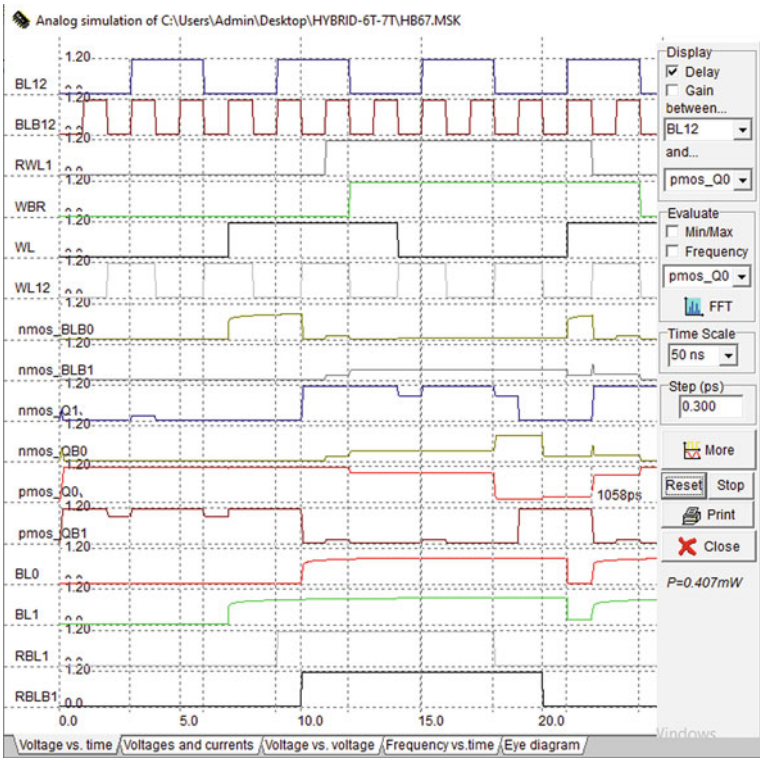

Fig. 4 Simulation results for 6T-7T dual-port hybrid SRAM model

3.2.1 Four Cell Model Using Two 6T-6T Dual-Port SRAM Cells

The dual-port SRAM using 6T-6T four cell model is implemented using four cell—two word line model, as shown in Fig. 5. The two word lines are brought from each pair of 6T-6T dual-port combination and are connected to output of multiplexer. The role of mux is to select the particular word line through which the corresponding dual-port two bit memory will be accessed to perform any operation like write into or to read from it. When the select line given a '0,' the upper two cell combination of memory is ready for the write/read operation. Similarly, when the select line is '1,' the lower two cell combination of memory will get ready for write/read operation.

On every write or read operation, the cell is need to reset to its initial start state. While in the write 1/0 operation, place the value on the corresponding bit lines then access the WL through mux. For example, to write '1' in the upper two cell memory, place the value '1' on bit lines BL_{11}, then assert write line WL_{10}, keeping select line low. On the other hands, to write into lower two cell memory, choose the corresponding lower bit lines BL_{01}, assert corresponding write line WL_{01}, keeping select line high. In the similar way, both the upper and lower memory cells can be

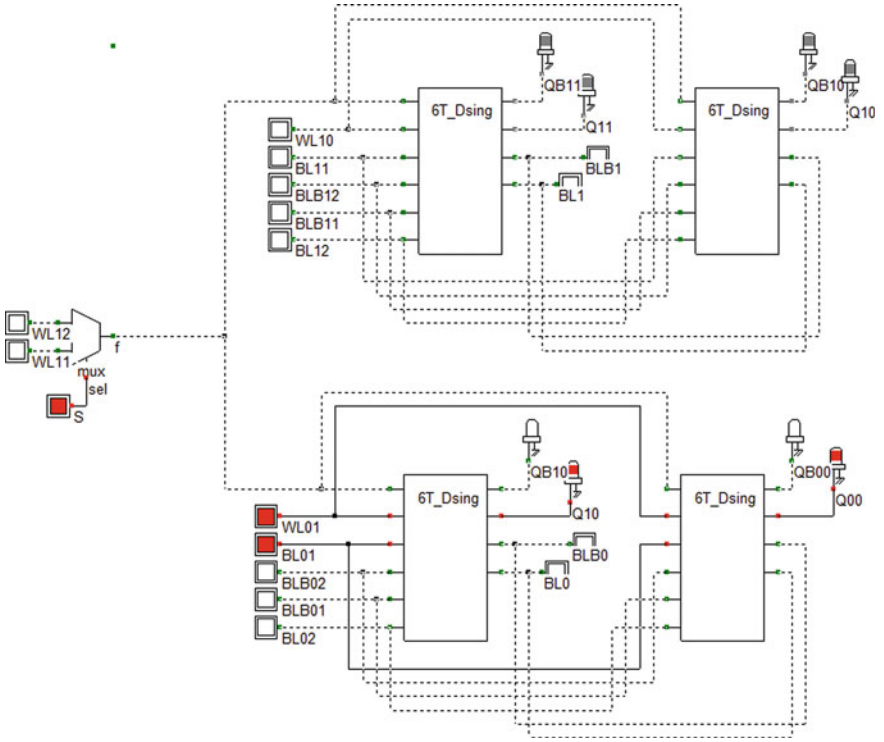

Fig. 5 Two bit four cell dual-port memory using 6T-6T (2 × 2) combination, write '1' in lower two cell memory

accessed for write/read using external write lines through mux. In the similar way, row-based four cell model is also implemented using double the two cell model.

3.2.2 Four Cell Model Using Two 7T-7T Dual-Port SRAM Cells

The dual-port SRAM using 7T-7T four cell model is implemented using both ways, one is in four cell—two word line model (2 × 2), and the other is in row-based model using double the two cell model. The simulation results indicate the 2 × 2 7T-7T model have minimum power dissipation of 0.688 mw compared to its row-based 7T-7T with 1.151 mw. Hence, the power dissipation is reduced by 71.8% in the case of 2 × 2 7T-7T model.

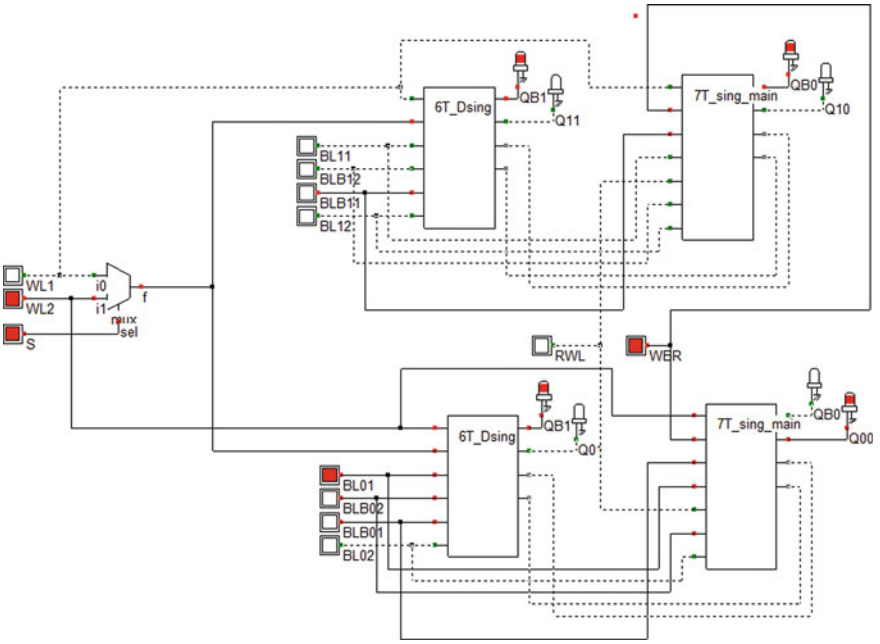

Fig. 6 Two bit four cell dual-port hybrid memory using 6T-7T combination, read '0' in upper memory cell, write '1' in lower memory cell

3.2.3 Dual-Port 6T-7T Hybrid SRAM Four Cell Model (2 × 2 Memory)

The dual-port hybrid SRAM using 6T-7T four cell model is implemented using two cascaded—two cell models as shown in Fig. 6. Due to involvement of 7T SRAM cell, the write or read operations are little different compared to 6T-6T two cell model. Using mux, the cells are activated individually through the select line. When the select line is '0,' upper two cells will be activated to perform data operation. Similarly, when select line is '1,' the lower cell will get activated. While performing write operation the active signal on WBR line causes the two 7T cells to act in dual to each other. Hence, the cell write ability increases using 6T-7T by providing more combinations in writing/reading the data.

4 Results and Comparative Analysis of Hybrid SRAMs

The simulation results for each hybrid model were carried out using microwind tool using 120 nm technology. Each 6T-6T and 7T-6T hybrid model is drawn in dsch tool, observed corresponding critical path delays. The same are extracted into automatic layouts in microwind environment to observe corresponding power consumptions.

The overall comparisons among the proposed hybrid dual-port SRAMs over its traditional counter parts are given in Table 1. One can understand the hybrid model using 7T-6T SRAM cell is performing well over 7T-7T architecture with power reduction improvement of 21.54%, and area reduction improvement of 8.15%.

In the similar way, four cell architectures are compared in Table. 2. For 6T-6T four cell model, the performance is poor in terms of high rage in area, delay and power dissipation including I_{max} compared to other proposed models in this paper. However, row-based four cell model using 6T resulting improved low-power dissipation. While comparing the hybrid models 6T-7T with other architectures under consideration, it results in features like marginal critical path delay of 5.9 ns, with minimum read delay of 16 ps, with low power of 0.799 mw and with low area of 831 μm^2 as observed in Figs. 7, 8, 9, 10 and 11.

Table 1 Comparative analysis of hybrid SRAMs (two cell models)

Type of circuit	# Tr	CPD (ns)	Min. read delay (ps)	Pd (mw)	I_{max} (mA)	Area (μm^2)
6T-6T	16	2.42	24	0.311	1.32	337
7T-7T	**18**	**3.29**	**38**	**0.622**	**1.64**	**401**
6T-7T-H	17	3.29	1058	0.407	1.66	368.3
7T-6T-H	*17*	*3.12*	*1023*	*0.488*	*1.357*	*368.3*

Table 2 Comparative analysis of hybrid SRAMs (four cell models)

Type of circuit	CPD (ns)	Min. read delay	Pd (mw)	I_{max} (mA)	Area (μm^2)
6T-6T (2 × 2)	11.78	14 ns	1.098	2.639	1126
6T-6T-row based	**1.35**	**956 ps**	**0.619**	**1.994**	**859**
7T-7T-row based	1.77	39 ps	1.151	2.461	943.4
7T-7T (2 × 2)	6.79	1030 ps	0.688	1.87	873
6T-7T-H	*5.955*	*16 ps*	*0.799*	*1.789*	*831*

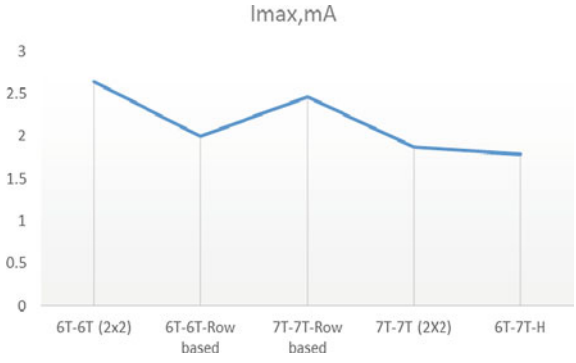

Fig. 7 Comparison of maximum current variation in dual-port four cell models

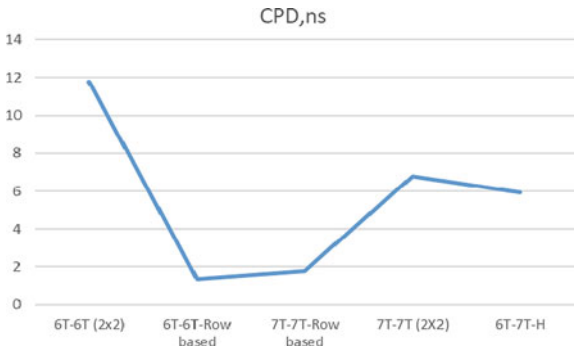

Fig. 8 Comparison of critical path delay in the chosen models

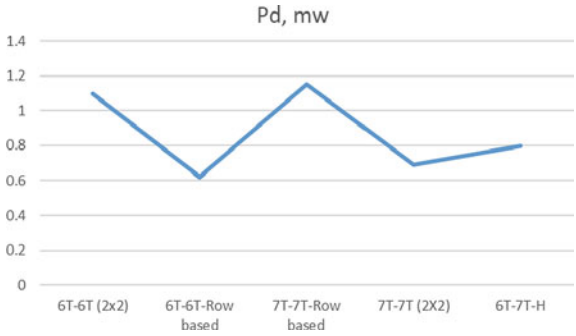

Fig. 9 Comparison of power dissipation variation in dual-port four cell models

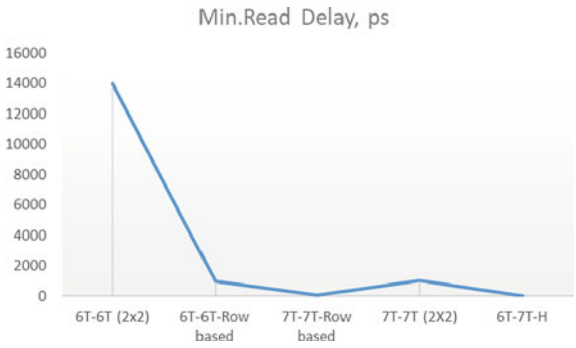

Fig. 10 Comparison of minimum read delay in the chosen models

5 Conclusions

The proposed dual-port hybrid model is implemented using 6T-7T and 7T-6T SRAM cell models observed that 6T-7T is greatly predominant in reducing power consumptions over other models using higher cell architectures under consideration. The power reduction improvement in proposed 6T-7T hybrid four cell is observed with 27.2% and 30.5% over 6T-6T (2×2), and 7T-7T (2×2) four cell traditional models.

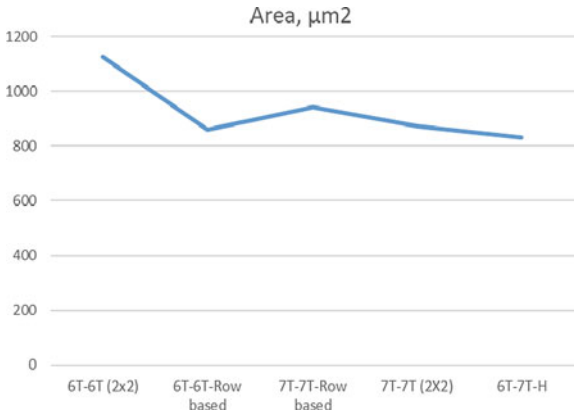

Fig. 11 Comparison of area requirement in chosen dual-port four cell models

Similarly, area reduction improvement in 6T-7T hybrid model observed with 26.1% and 8.15%, respectively, when compared with 6T-6T (2×2) and 7T-7T (2×2) four cell traditional models. Since this proposed model is novel and new, the comparisons are made among the self-dual combinations. This kind of hybrid models is essential under low-power multi-core processor applications.

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