# Design of Low-Power 10T Full Adder Circuit using DG—MOSFET at 180 nm Technology


**Aakrati Agrawal, Pramod Kumar Jain, and D. S. Ajnar**

**Abstract** Keeping the current scenario of digital era in outlook where devices with high portability and performance are in demand, the paper proposes a technique, i.e., double-gate MOSFET (DGFET) which holds well. This technique replaces single-gate transistor logic with double gate results in reducing problems like short channel effects in FETs. The paper includes design of 10T full adder digital logic circuit, parametric analysis such as power consumption and resistance offered. The implementation of design and simulation results has done using Cadence Virtuoso tool at 180 nm technology.

**Keywords** Double-gate FET · Full adder · Single gate · Power consumption · MOSFETs

## 1 Introduction

The most considerate predictions done in the field of microelectronics and VLSI are by Gordon Moore who described a law named Moore's law which states that "the number of transistors in a dense integrated circuit (IC) doubles about every two years." To keep following the law, the dimensions of transistor get reduced by half in a period of every three years. Since transistor is the integral component in microelectronics and VLSI that every feature and parameter is essential to look after. The prime objective of switching technologies from using BJT (bipolar transistor) to FETs (field effect transistor) and MOSFETs is improving performance parameters such as power consumption, increased speed, smaller chip area, cost reduction.

A MOSFET is a semiconductor device which is widely used in electronic devices due to various features it possess like amplification and high switching speed when

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V. Nath and J. K. Mandal (eds.), *Microelectronics, Communication Systems, Machine Learning and Internet of Things*, Lecture Notes in Electrical Engineering 887,
https://doi.org/10.1007/978-981-19-1906-0_8

dealing with electrical signals. It is considered as an ideal switching device which has bidirectional capability and offers low static power dissipation, high scalability, and high packing density in integrated circuits [1–8].

There are two modes of operating MOSFETs:

(1) Depletion mode in FET
(2) Enhancement mode in FET.

There are several types of MOSFETs but here described are two types, i.e., single-gate MOSFET and double-gate MOSFET.

## *1.1 SG—MOSFET*

A single-gate MOSFET is the basic component which has four terminals, i.e., source, gate, drain, and body. In this type of device, all four terminals operate independently and offering different functionality. Single-gate FET operates in both modes of operations, i.e., enhancement mode and depletion mode [1, 9–11].

## *1.2 DG—MOSFET*

The double-gate MOSFET (DGFET) is designed using two single-gate MOSFETs that are placed in such a way the identical terminals of both the components get connected. The symbol now has two gates, i.e., front gate and back gate. These two gates can operate simultaneously also which is termed as symmetrical driven (SDDG). The gates can be operated independently by applying voltage bias to one and switching the other which is known as independent driven (IDDG) [1–5, 8, 11, 12].

Figure 1 shows circuit symbol of p-type and n-type DG-MOSFET.

Transistors and Fig. 2 show modes of operations of double-gate transistor.

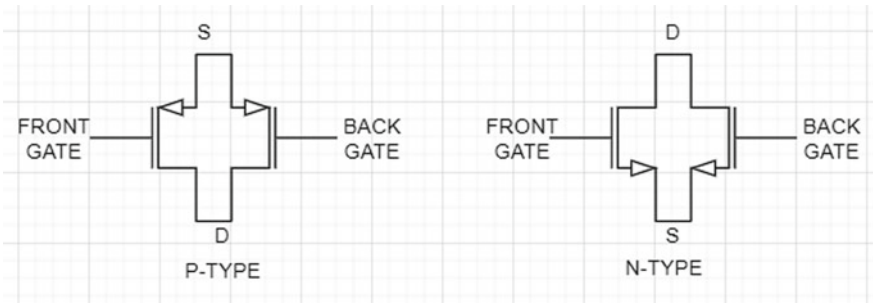


**Fig. 1** Circuit symbols

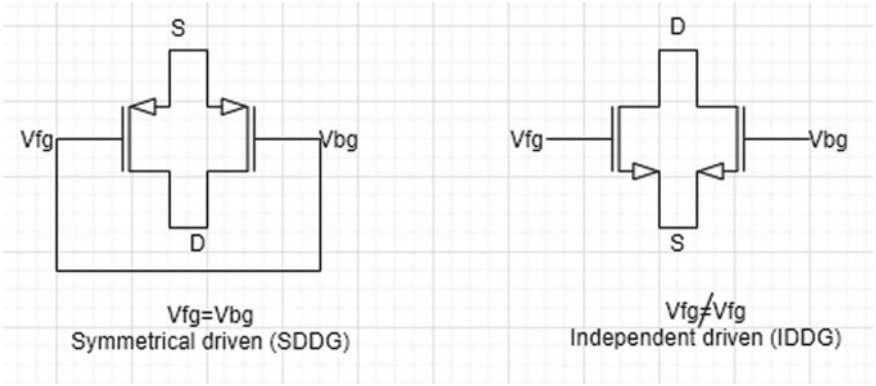


**Fig. 2** Operating modes

## 2 Full Adder

The efficiency of any digital device depends entirely on the internal devices and components used in designing the particular unit. As the market growing and dependency on digital devices is increasing rapidly, there is always a need to improve the performance based on some parameters such as smaller size, cost per unit, durability, and power consumption, these parameters helps a device to be more reliable and portable. Full adder is one integral unit in any digital device, i.e., microcontrollers and microprocessors in its arithmetic logic unit (ALU).

The basic block diagram using logic gates of one bit full adder is shown in Fig. 3.

Figure 3 shows a combinational circuit of full adder that is used to perform arithmetic operations in ALUs. It takes three bits as inputs ($A$, $B$, $C$in), performs the required mathematical operation using the gates and gives two outputs ($S$, $C$out).

The Boolean expression for this logic is described as:

$$S = A \oplus B \oplus C\text{in}$$

$$C\text{out} = AB + AC\text{in} + BC\text{in}$$

For designing of full adder circuit, an additional degenerate module is required, i.e., a 5T XOR-XNOR circuit. This module helps in reducing the number of transistors thus reduces the integration size and also helps in making leakage current less with less static power dissipation.

This module uses combination of p-MOS and n-MOS transistors which takes two inputs ($A$, $B$) and give outputs ($C$, $D$).

The circuit is biased with the input pulses and has a ground pin (gnd, 0 V).

The schematic design of 5T XOR-XNOR module is shown in Fig. 4.

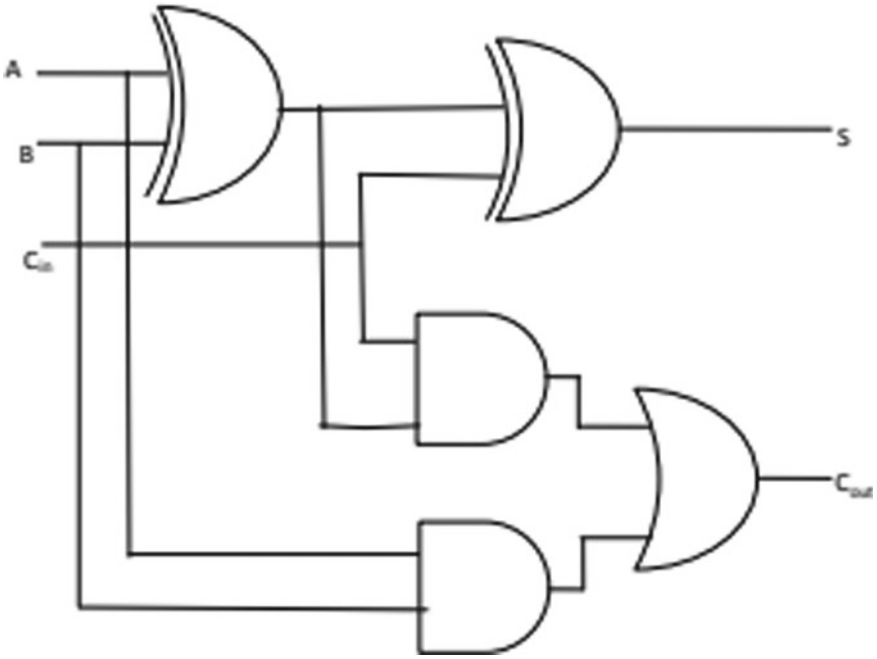


**Fig. 3** One-bit full adder

The module is best suitable even where there is requirement of low-power operations since it excludes the use of voltage.

The circuit performs two operations, i.e., XOR and XNOR on the input pulses taken as *A* and *B*. This operation can be well described through its truth table that is described in Table 1.

The two signals (1−) and (0+) are degraded signals due to threshold voltage loss. In the case where both the inputs are "0," the XNOR output becomes floating which is indicated by the symbol (X). Hence, module is considered logically degenerated.

Combinations of all the inputs are not satisfied this module, but it is sufficient enough to produce the output signals (*C*, *D*) needed for the appropriate functioning of the full adder.

The transient response for the circuit module is recorded at 100 ns shown in Fig. 5.

## 3 Full Adder Design Using Single-Gate Transistor Logic

The designing of full adder using single-gate transistor logic is implemented by using 5T XOR-XNOR module discussed above. The output signals (*C*, *D*) taken from previous module are used as input to the other half module of single-gate full adder design circuit.

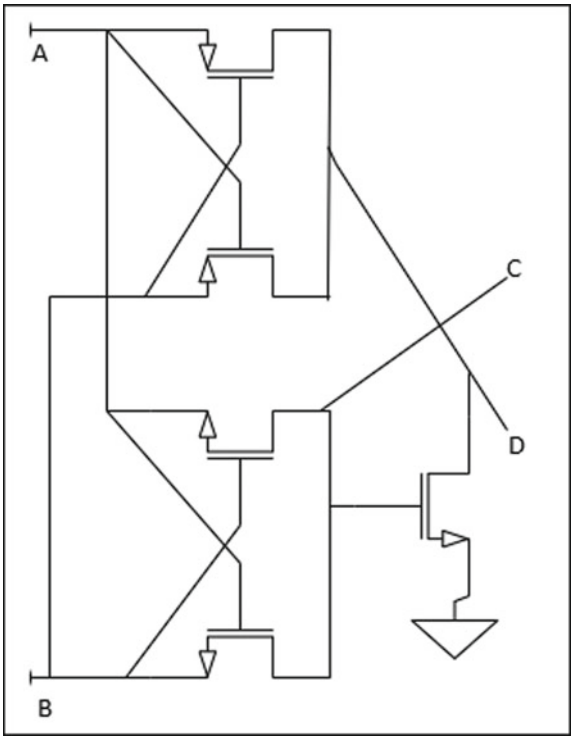


**Fig. 4** 5T XOR-XNOR module

**Table 1** XOR and XNOR operations on the inputs *A* and *B*

| *A* | *B* | $\overline{D}$ (XNOR) | *D* (XOR) |
|---|---|---|---|
| 0 | 0 | X | 0+ |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1− | 0 |

The schematic design of full adder using single-gate transistor logic is shown in Fig. 6.

The Boolean expression for the 5T XOR-XNOR module is described below [13]:

$$S = (\overline{A \oplus B})C + (A \oplus B)\overline{C}$$
$$C\text{out} = (A \oplus B)C + (\overline{A \oplus B})A$$

The Boolean expression for SG-MOSFET-based double adder using the 5T XOR-XNOR module is described below:

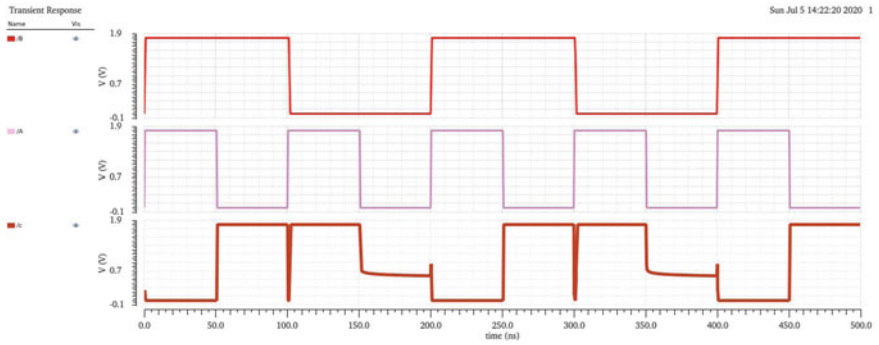


**Fig. 5** Transient response at 100 ns

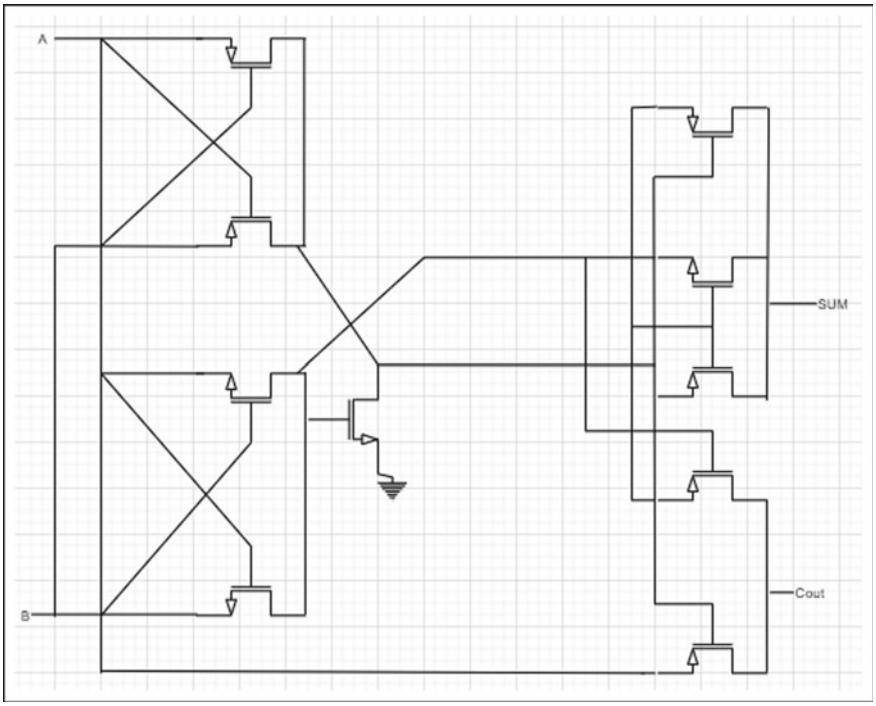


**Fig. 6** Schematic design of full adder using SG transistor

$$\boxed{\begin{aligned} S &= D \oplus C \\ \text{Cout} &= D \oplus C + \overline{D} \oplus A \end{aligned}}$$

The layout design of full adder circuit using single-gate transistor logic is carried out by using Cadence Virtuoso tool at 180 nm technology, which is shown as Fig. 7.

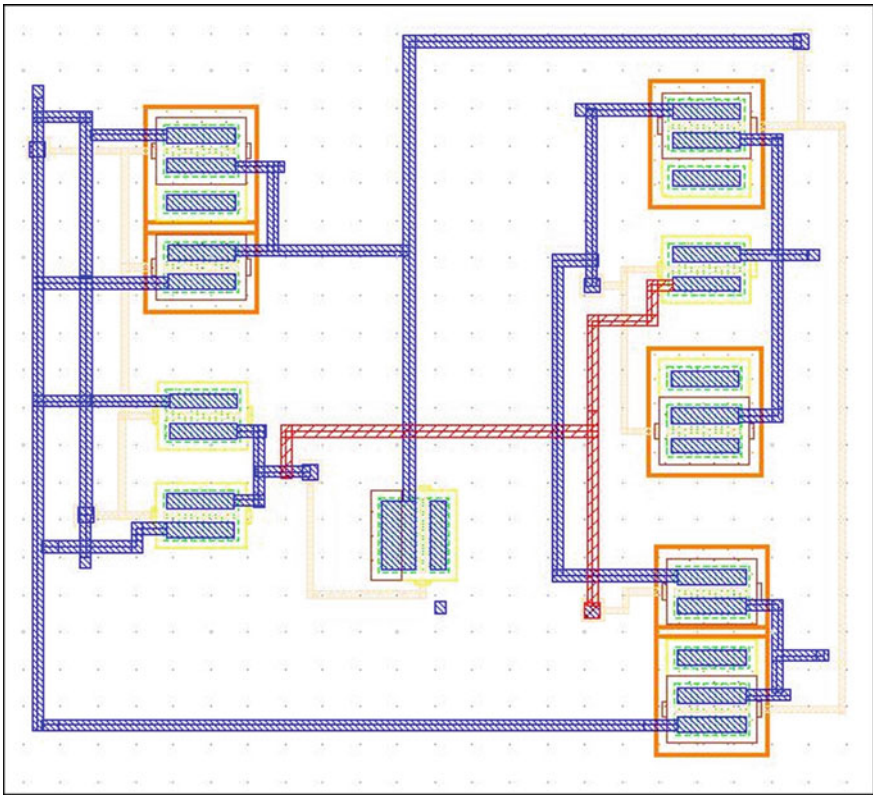

**Fig. 7** Layout design of full adder using SG transistor

All paths in all layers of the layout design are dimensioned in λ units, and subsequently, λ can be allocated an appropriate value compatible with the feature size of the fabrications process. This layout design follows layout design rules, i.e., sub-micron rules such as:

Min poly width ($L$) = 2λ
Min spacing b/w poly = 2λ
Width of contacts = 2λ
Min metal to metal spacing = 3λ
Min metal width = 3λ or 4λ
($w$) Min width of diffusion = 6λ.

To check the correctness of design rules, design rule check (DRC) is done using Assura; it ensures that the layout passes through the rules designed for faultless fabrication followed by LVS (layout vs. schematic) that determines whether a particular circuit layout corresponds to the original schematic of the design.

## 4 Full Adder Design Using Double-Gate Transistor Logic

The designing of full adder using double-gate transistor logic (DG-MOSFET) technique is carried out by using the single-gate transistor logic design in an equivalent way. Each transistor in the circuit is configured and connected in a manner that their source terminal and drain terminal must be connected to each other. The two (front and back) gates of DG-MOSFET logic are electrically coupled which operates in symmetrical mode of operation. This mode of operation establishes connection between the terminals in a way that channel and gates get near to each other which in turn provides good control over conductance of the channel and reduces leakage.

Also, DG-MOSFET technique drastically reduces the short channel effects that occur in basic MOSFET devices which reduces the performance. This technique is preferable more since it possess better scalability even in nanometer range in digital circuits.

The schematic design of double-gate MOSFET-based full adder is shown in Fig. 8.

The transient response of proposed circuit is carried out using an EDA tool, i.e., Cadence Virtuoso tool at 180 nm technology which is shown in Fig. 9.

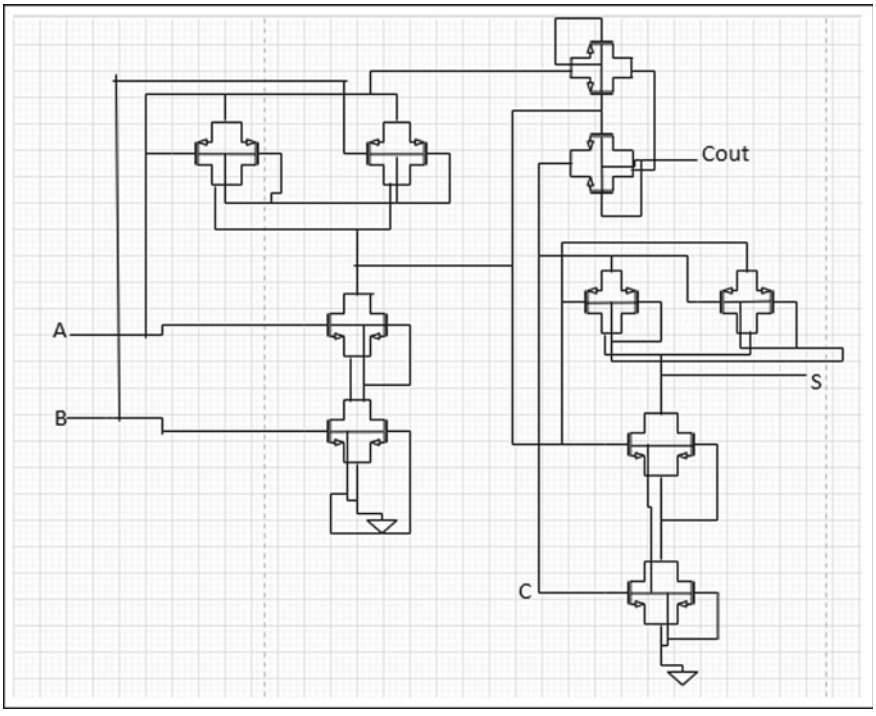


**Fig. 8** Schematic design of full adder using DG-MOSFET

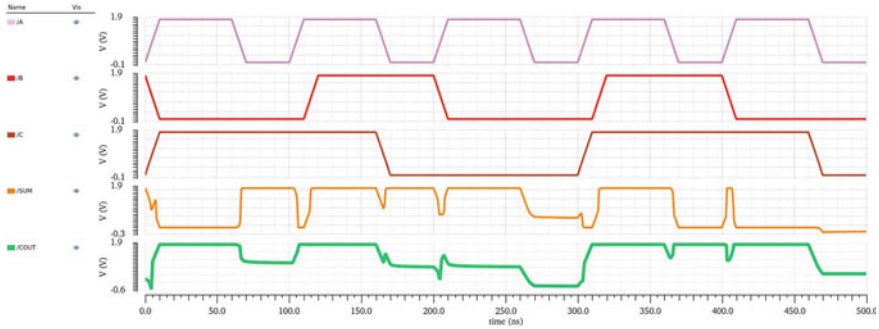


**Fig. 9** Transient response of full adder using DG-MOSFET at 180 nm

## 5 Results and Observations

### *5.1 Average Power Consumption*

The average power consumption for a CMOS circuit is described by the equation [9]:

$$\begin{aligned} P(\text{avg.}) &= P(\text{dynamic}) + P(\text{leak}) + P(\text{short-circuit}) \\ &= \text{CLVddVfclk} + \text{IleakVdd} + \text{IscVdd} \end{aligned}$$

From the above equation, it is clearly visible that the average dissipated depends upon different parameters such as current components (leakage + short-circuit), induced capacitance, and supply voltage. So, to lower the average power consumption, reducing the applied supply voltage will help. This concept will enhance the durability and overall performance of the MOSFET-based full adder circuit.

Figure 10 shows the graphical representation of power consumption against time (ns) taken at different levels of voltage, i.e., at 290, 310, 330, 350, 370 mV for double-gate MOSFET-based full adder circuit.

Figure 11 shows the numerical value of average power consumption in DG-based full adder circuit. This calculation is done using parametric analysis in EDA tool Cadence Virtuoso at 180 nm technology.

The average power consumption of double-gate MOSFET-based full adder calculated above is as follows:

$$P\text{avg (DG)} = 43.38\text{E} - 9$$

And the average power consumption of single-gate MOSFET-based full adder calculated using the same process of parametric analysis is as follows:

$$P\text{avg (SG)} = 1.769\text{E} - 3$$

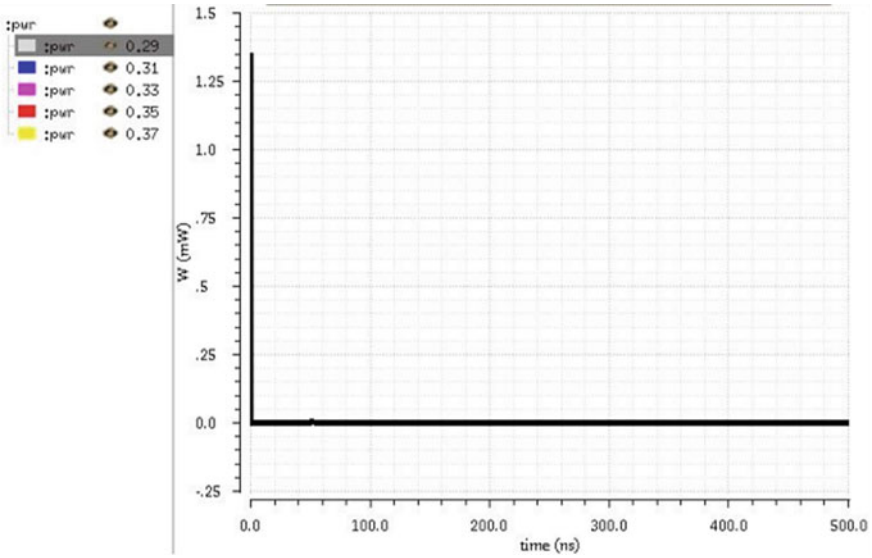


**Fig. 10** Power consumption versus time in ns

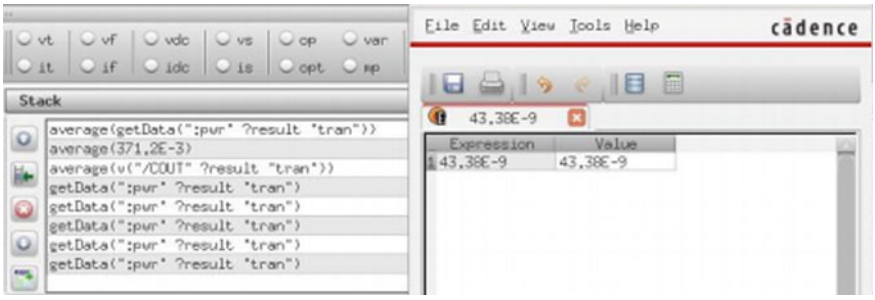


**Fig. 11** Average power consumption

## *5.2 Variation of Power with Voltage*

Figure 12 shows a graph of variation of power consumption with respect to input voltage of both single-gate and double-gate MOSFET-based full adder circuit.

From the graph, the percentage change in power consumption of SG and DG-MOSFET-based full adder circuit, it has been observed that the power consumption gets reduced by 22% in double gate logic circuit.

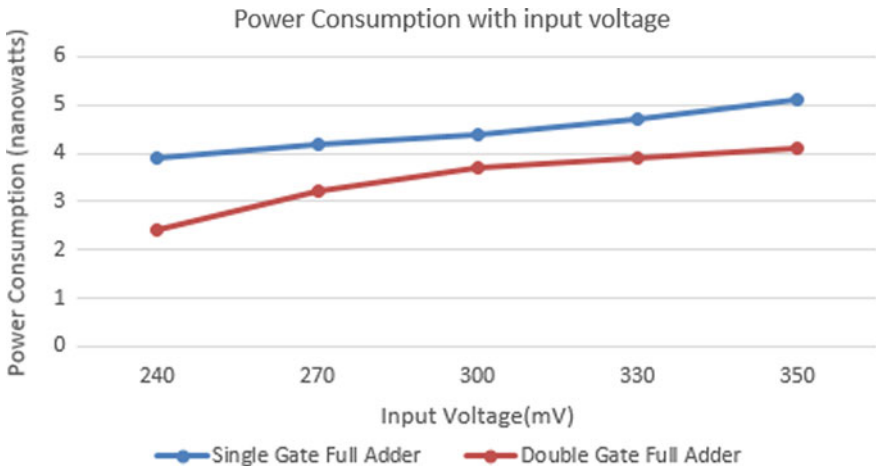


**Fig. 12** Power consumption versus input voltage

## 6 Comparison Results of Parameters

| Parameters | Conventional design | Proposed design |
|---|---|---|
| Power (avg.) | 71.4 μW (14T) | 43.38 nW (10T) |
| Tools and technology | Tanner EDA 13.0 | Cadence Virtuoso (180 nm) |
| Resistance | More | Less |
| Current (*I*ds) (μA) | 0.018 | 0.015 |

## 7 Conclusion

From the above observations and simulation results, it can be easily concluded that double-gate MOSFET-based full adder is way better suitable for the designing of digital devices than single-gate MOSFET based since DG based provides low power consumption, high speed, good scaling at low voltage range. These are most reliable devices that can be used for any microprocessors and other portable digital devices.

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