



Optimization and Comparison of High Performance and Low Power NOR Gate Circuit Using Hybrid Model of Dynamic Voltage Scaling and MTCMOS Technique

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Abstract. The strategy joins VS (Voltage Scaling) and MTCMOS procedure that aids in lessening active and passive power dissemination separately deprived of corrupting the circuit's execution. The anticipated procedure set aside power dispersal by 35% to 85% when contrasted with regular CMOS and other existing procedures and the numbers of transistors is reduced in existing circuit to reduce the overall energy consumption as well as the reduced transistor logic is area efficient and comparison is done with existing design and NMOS structure. A 2-terminal input NOR gate is executed utilizing the VS-MTCMOS procedure in sub-edge district throughout various ranges of temperature at different voltage level. Electronic Design Automation Tool is utilized in the direction of reproduce the planned circuit. As convenience of electronic frameworks requires longer battery life, it is important that they should have instruments in spot to diminish the force utilization. One of the methods used to build power productivity at the framework level is Dynamic Voltage and Frequency Scaling (DVFS). CMOS rationale is broadly utilized in VLSI circuits yet because of scrambling of innovation, limit voltage of the semiconductors utilized in CMOS circuits decline, results in increment in spillage power. Active power utilization, that is relative to source potential difference (V_{DD})² auxiliary combined to general power dispersal. This outcomes in short battery lifespan of cell phones. Transitory is a clever strategy in the direction of shorten mutually unique power dissemination furthermore, spillage power.

Keywords: VS · MTCMOS · NMOS · CMOS · NOR · Power · Efficient · DVFS

1 Introduction

Since past years area, cost, unwavering quality and execution were viewed as the essential worries intended for Very Large-Scale Integration originators despite the fact power utilization is as an optional apprehension [6, 8]. Be that as it may, with the presentation and consistently expanding request of portable electronic gadgets and other remote correspondence frameworks like personal digital assistant and individual correspondents, power utilization be located currently specified equivalent significance cutting-edge contrast with region and execution [1]. It involves power productive Very Large-Scale Integration circuits. Sub-limit rationale circuits have been existing as of late for applications that require super low force utilization [2, 3]. In designed circuits necessitate that the occupied potential difference VDD ought to be not exactly the limit voltages of the semiconductors that are available in the VLSI circuit. The general power feasting utilization i.e., decremented for mentioned circuits. We defined two major sources of power intemperance in any CMOS designed circuit. Primary source is the intemperance of active energy through the exchange of circular motion. In this case, the power of the parasite is amplified and released with a focus between the two levels of sensitivity. Due to current trends through our semiconductors, some of the disturbances of today's scenario after the transformation of electrical energy and heat have now been published [4]. The expansion of this dynamic power corresponds to a doubling of VDD voltage, operating capacity as well as frequency that is provided by $P_{\text{Dyn}} = CV_{\text{DD}}^2 f$. Another power loss source occurs when input is given to the logic gate and output of the logic gate remains unchanged [9]. This also known as static energy dissipation and is caused by scattering of energy transitions, side leaks and door leaks. A subcutaneous fissure indicates the rate of flow from the canal to the eye when the semicircle is closed. This leakage increases significantly when we lower the power limit and calculate the device [7]. The sub-threshold leakage relies upon the boundaries of. This power loss is relational to component supply voltage, the voltage changes of the node, and the average power switching cycle. The voltage change is in maximum circumstances equivalent to the supply voltage, as transition, discharge, is usually different from the square of the supply voltage [5]. In this present study, the technology reduces both energy loss and energy loss by combining voltage technology and MTCMOS technology. In this work the intermediate network of push pull network is eliminated by AOI network in MTCMOS technique and existing structure is optimized MTCMOS NOR circuit with AOI network and compared with existing structure and NOR NMOS logic with MTCMOS.

2 Execution and Simulation of 3T NOR Gate Circuit with MTCMOS

The MTCMOS system is one of the strategies that prevents power failure. The MTCMOS system has two ways of action, a dynamic mode and a backup mode. Typically, an ordinary CMOS circuit merely connects a single-phase transistor (V_T), although the MTCMOS strategy consists of two limiting power transistors. High V_T transistors are known as breaker transistors which help in stopping the current flow and uses low V_T transistors in legal circuits to aid in the starting of circuit. In this circuit energy efficient

an area efficient 2 Input NOR gate is executed with MTCMOS logic. Simulated and executed result is as follows (Figs. 1 and 2):

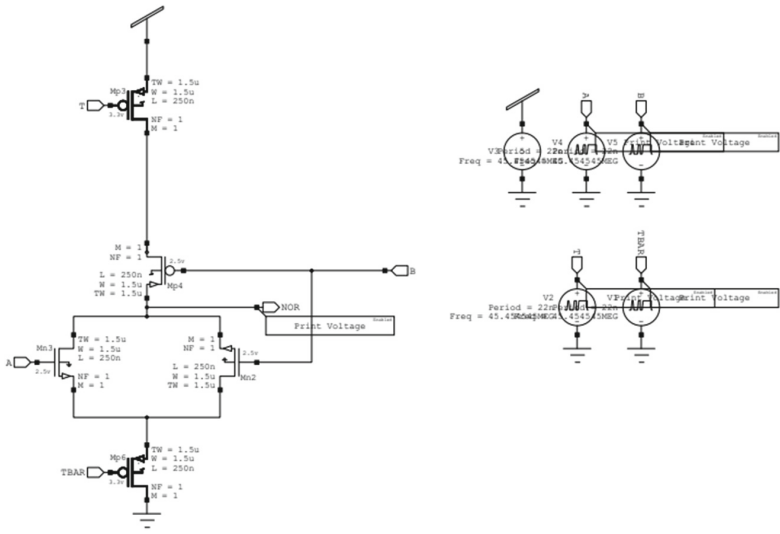


Fig. 1. Schematic of 3T NOR gate with MTCMOS technique

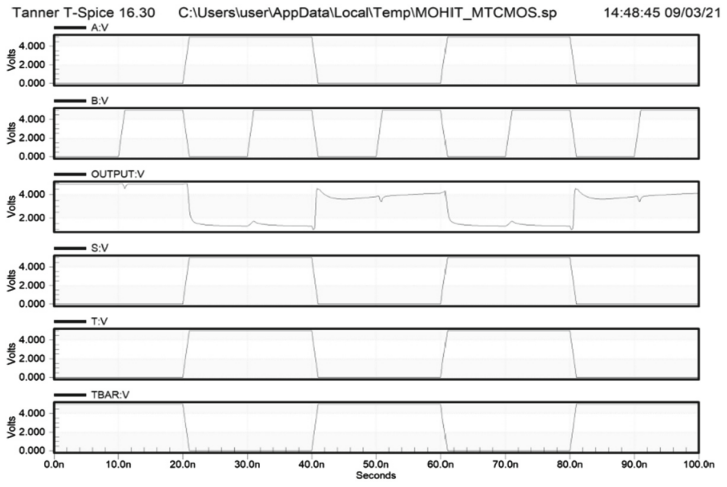


Fig. 2. Output waveform of 3T NOR gate with MTCMOS technique

3 Execution and Simulation of Existing Circuit with VS-MTCMOS Pull Down and Pull Up Network of NOR Gate

The given circuit activates in two ways: dynamic (active) mode and passive mode. During dynamic (dynamic) operation, the electric field is reduced by voltage sharing and sharing process to do justice to the active power loss. The high sleep transistors VT H1 and H2 can use logic of 0 and 1 TBAR of T, which allows them to function as standard transistors. When S is high circuit becomes ordinary CMOS circuit, also turns on to M2, gives out low voltage level of VP. It also switches to M3 and gets full circuit performance. Related products are collected. As S decreases, M1 and M3 decrease by reducing the level of voltage of VS. At that time, the power of Ca and CB share the charge by self-regulation, that will reduce the level of voltage of Vp. When this happens, it will make M3 on or active, which will increase the level of voltage of VS and aid to reduce the massive VS types. The active loss of power is then minimized using the Danab ratio method. In a regression model, in which the input(s) given in the input terminal of logic gate does not change its variable output, the upper semiconductors VT H2 and H1 inside the circuit loop are cleared on giving $T = 1$ and $TBAR = 0$. That will lead to very high level of resistance among two organizations. These lines are delayed due to discrimination of power drop due to the introduction of MTCMOS system of high transistors VT H1 and H2. In the current control loop, the opposite side predicts the power loss of the active power supply and storage system. In this way, generally speaking force is diminished by joining these two methods. This technique is used with pull down and pull up network of NOR gate and output are observed (Figs. 3, 4 and 5).

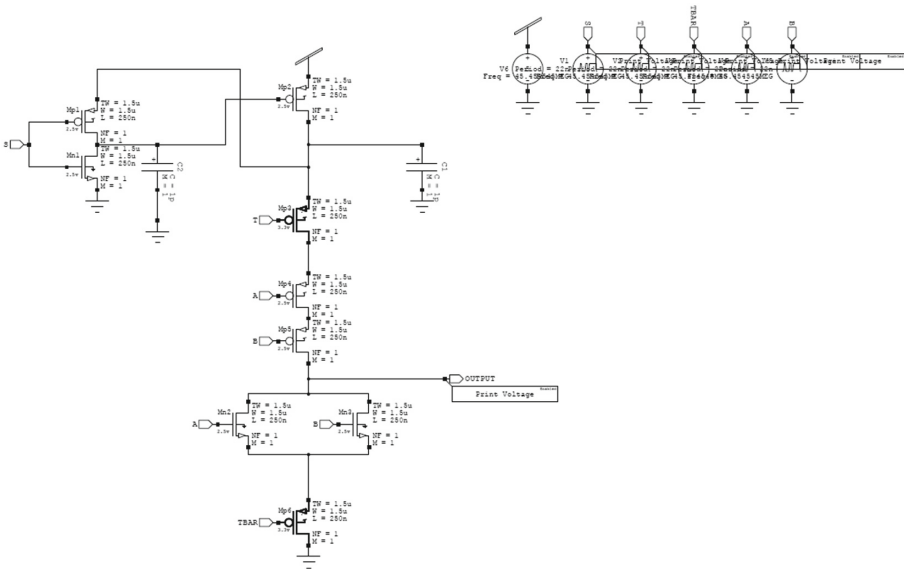


Fig. 3. NOR gate by pull down & pull up network with VS-MTCMOS technique



Fig. 4. Output waveform of NOR gate by pull down & pull up network with VS-MTCMOS technique at various temperature points

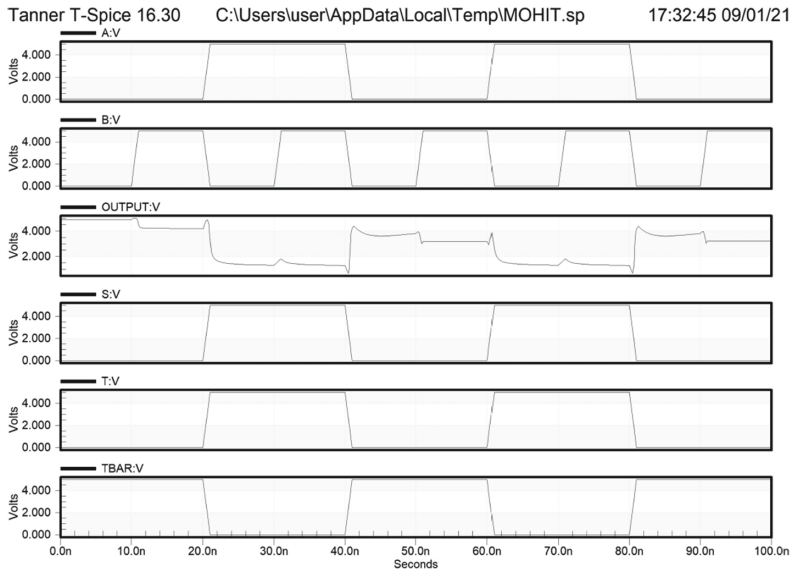


Fig. 5. Output waveform of NOR gate by pull down & pull up network with VS-MTCMOS technique

4 Study and Design of AOI CMOS Logic 3T NOR Gate with VS-MTCMOS

In this circuit the existing VS-MTCMOS technique is used with AOI network instead of pull down and pull up network of NOR gate which reduce the ripples and noise in

the output waveform of circuit as well as reduce the power consumption of the circuit and give out energy efficient and smooth output of NOR gate. The simulation result of AOI or network nor gate is given below and if compared with the output of pull up and pull-down network giver the better waveform with less ripples and deviations and uses less number of transistors that give out area efficient and power efficient output (Figs. 6, 7, 8 and Table 1).

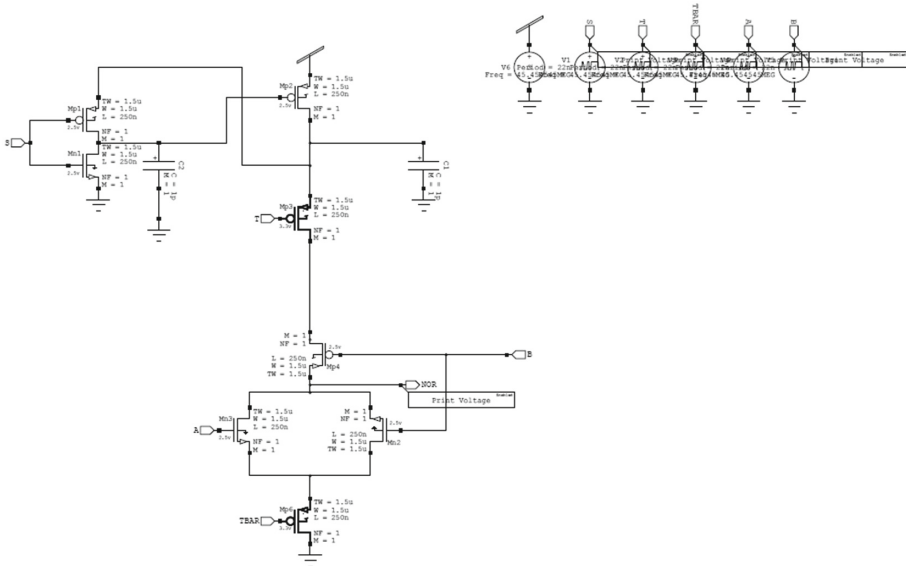


Fig. 6. 3T NOR gate with VS-MTCMOS technique



Fig. 7. Output waveform of 3T NOR gate with VS-MTCMOS technique at various temperature points

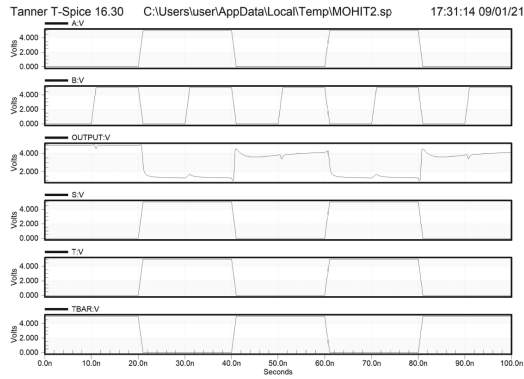


Fig. 8. Output waveform of 3T NOR gate with VS-MTCMOS technique

Table 1. Power consumption of 3T NOR gate by CMOS with VS-MTCMOS technique

Modified design of 2-Input NOR gate using hybrid voltage scaling and MTCMOS in CMOS logic

VDD (V)	Average power consumed	Max power consumed	Min power consumed
0.6	1.779E-007	3.057E-005	0.0032E+000
0.5	1.046E-007	2.467E-005	0.0022E+000
0.4	6.0297E-007	0.273E004	0.0020E+000
0.3	4.005E-007	0.010E-004	0.0028E+000

5 Study and Design of VS-MTCMOS NOR Gate with AOI NMOS Logic

In this circuit VS-MTCMOS is used on 2 input NOR gate using NMOS and the analysis of output in terms of power consumption output deviation is noted and compared with other circuits which used CMOS AOI logic network and CMOS pull down and pull up network (Figs. 9, 10, 11 and Table 2).

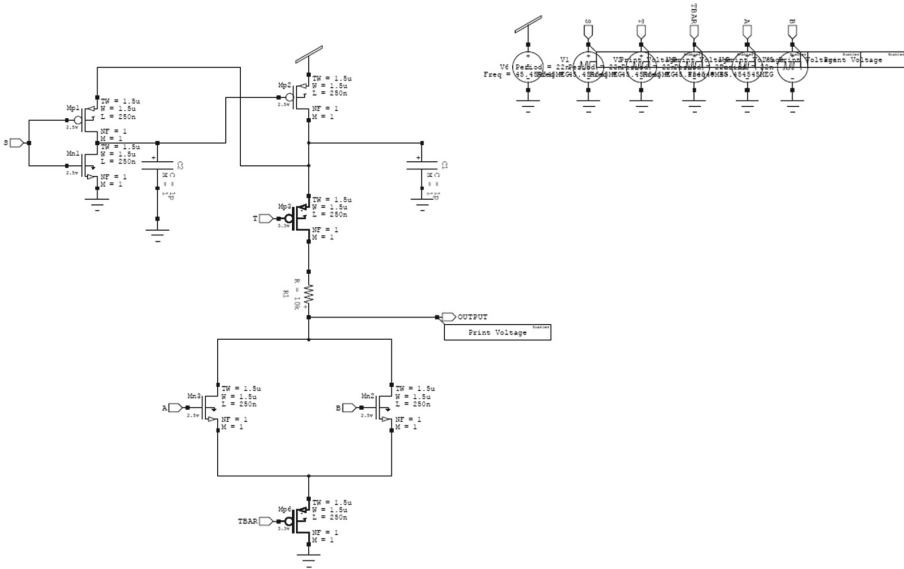


Fig. 9. The 2T NOR gate by NMOS logic with VS-MTCMOS technique

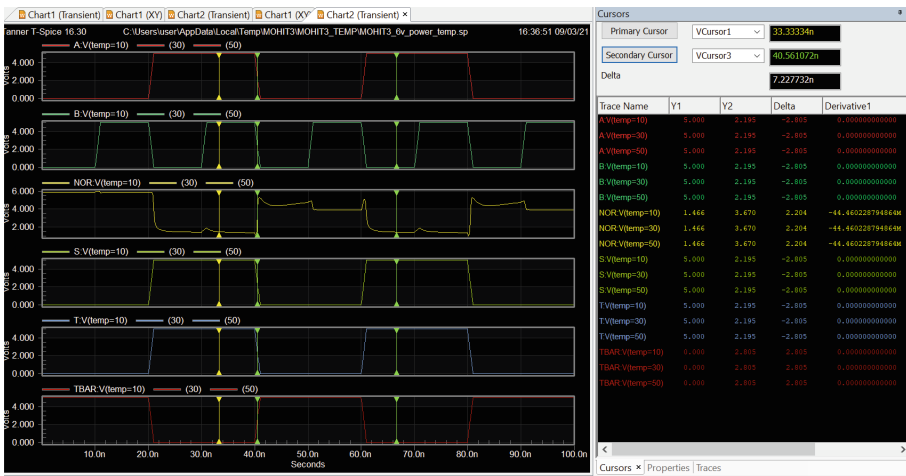


Fig. 10. Output waveform of 2T NOR gate by NMOS logic with VS-MTCMOS technique at various temperature points

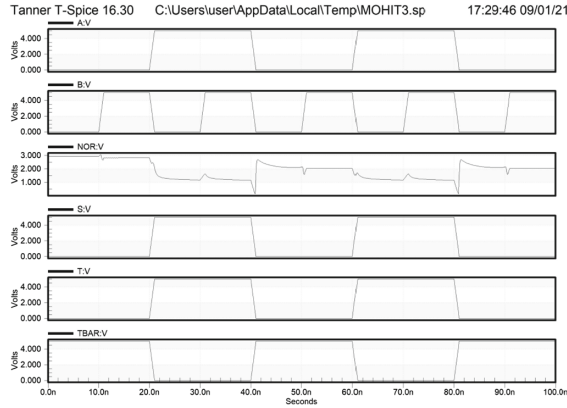


Fig. 11. Output waveform of 2T NOR gate by NMOS LOGIC with VS-MTCMOS technique

Table 2. Power consumption of 2T NOR gate by NMOS LOGOIC with VS-MTCMOS technique

Modified design of 2-input nor gate using hybrid voltage scaling and MTCMOS in NMOS logic

VDD (V)	Average power consumed	Max power consumed	Min power consumed
0.6	2.510E-001	1.513E-004	0.001E+000
0.5	1.233E-007	2.411E-004	0.0011E+000
0.4	3.670E-007	3.29E-004	0.001E+000
0.3	2.815E-007	3.202E-004	0.023E+000

6 Comparison of Power Consumption of 3 Different Designed Circuit with Using Hybrid VS-MTCMOS Techniques at Different Voltage Ranges

Power consumption of 2 input NOR gate of obtained of Hybrid Voltage Scaling and MTCMOS technique is compared with Standard CMOS, Voltage scaling and simple MTCMOS techniques and keeping the value of VDD slightly above the value of threshold value. Testing is done at different values of the voltage from 0.3 V to 0.6 V (Table 3).

Table 3. Comparison of power consumption of various designed NOR gates with MTCMOS AND VS-MTCMOS technique

VDD (V) [10]	Standard CMOS [10]	2-terminal input NOR circuit using voltage scaling [10]	2-terminal input NOR circuit using MTCMOS [10]	2-terminal input NOR circuit with hybrid VS-MTCMOS [10]	Modified design of 2-input NOR circuit with hybrid VS and MTCMOS in NMOS logic	Modified design of 2-terminal input NOR circuit with hybrid voltage scaling and MTCMOS in CMOS logic
0.6	7.067E-8	6.460E-8	5.895E-8	2.832E-004	2.510E-001	1.779E-007
0.5	4.588E-8	3.281E-9	3.812E-8	1.060E-9	1.233E-007	1.046E-007
0.4	2.734E-8	1.997E-9	2.247E-8	8.047E-10	3.670E-007	6.0297E-007
0.3	1.405E-8	9.382E-10	1.126E-8	6.451E-10	2.815E-007	4.005E-007

7 Conclusion

In this paper, MTCMOS electrical technology and techniques are implemented and implemented in various NOR circuits using AOI CMOS, PULL UP and PULL-DOWN networks. The current system combines voltage measurement and multiple CMOS technology (MTCMOS), which minimizes electrodynamic or static losses without compromising circuit performance. By this technique power consumption can be saved by 35% to 85% as compared to traditional CMOS and other current technologies. In the subfield a variety of 2-door NOR gates were developed using VS-MTCMOS technology and using MTCMOS technology to create the circuits intended to simulate, compared to using Tanner's EDA equipment was used.

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