A 12T SRAM of 16 nm CMOS Technology Using One Sided Schmitt Trigger Inverter and Read Port

Komaladitya Challa(✉) and Vinay Kumar Pamula

Department of ECE, University College of Engineering Kakinada, JNTUK, Kakinada, Andhra Pradesh, India
Komaladitya.challa@gmail.com

Abstract. This work describes a one-sided Schmitt-triggered with data independent read and write operation from a 9T Static Random-Access Memory (SRAM) cell that consume less power and has excellent read and write stability. The existing approaches are performed with data leakage problem, huge area, expensive energy per access read data bits. To solve this problem, the proposed work will introduce three duplications of Static RAM cells with read ports to arise ST 12T SRAM, with the goal of greatly reducing data based read port leakage to improve the read quality and minimize area and power. The proposed methodology of Schmitt-trigger based 12T SRAM memory cell achieves excellent read robustness in a one-sided Schmitt-triggered inverter with a three different single bit arrangement, while the write ability improves by power gating in Schmitt-trigger-inverter with support of control and trip voltage. This article's proposed approach 12T SRAM memory cell will be designed at the single bit level, utilizing 16 nm and 22 nm CMOS Technology, and demonstrate the area, latency and power consumption using Tanner EDA Tool.

Keywords: Low power · Near threshold · Schmitt-trigger · Read port leakage

1 Introduction

Memory is significant in data processing application devices for storing and retrieving data, especially when it comes to storing confidential and sensitive information with extremely protective encryption methods, such as AES, DES, SEA, etc. Static RAM is vital in System-on-Chip (SOC) and a notable commitment to the SOC's maximum force usage and space. Because area is important concern when designing circuits, memory configuration researchers seek to place as many cells as possible per segment for the sharing of edge hardware [1]. Ordinary 6T SRAM, 8T SRAM and other cells are greatly constrained by their lack of ability to perform in longer segments. This happens to owe the negative impacts of information overflow, distorted I_{ON}/I_{OFF} ratios, and read bit line swing when more cells are packed on one section. Various approaches have attempted to face this matter in question by working on the I_{ON}/I_{OFF} proportion to empower up to thousand cells per segment [4]. Even though these procedures have been beneficial,

© The Author(s), under exclusive license to Springer Nature Singapore Pte Ltd. 2022
S. Mekhilef et al. (Eds.): ICEEE 2022, LNEE 893, pp. 383–391, 2022.
https://doi.org/10.1007/978-981-19-1742-4_32

they continue to endure from the negative impact of vast region or moving information execution. Some also fail to stipulate the base energy point in Static RAMs, resulting in vast amount of energy in each access at extremely low voltages [2]. The greatest method to heavily reduce energy consumptions is reducing power by lowering the supply voltage (V_{DD}). Power decreases in quadratic function with the decrease in V_{DD} [3]. In any event, when V_{DD} decreases, deferral and soft error rates (SER) rises, while functional yields fall. In the sub-threshold voltage (sub-V_{th}) region, where V_{DD} is lower than V_{th}, the delay increments dramatically [2]. In the same way, the energy utilization is explained essentially in expanded static energy utilization, even though exceptionally low force is accomplished. When set side by side to ultra-scale operation, operating in near-V_{th} zone, where V_{DD} is slightly greater than V_{th}, can accomplish a vast power reduction and a good improvement in latency over sub-V_{th} operation. Therefore, by optimizing both delay and power in near-V_{th} area, energy consumption may be reduced [3]. The Sensitive miscalculation caused by α-particles becomes a problem in near V_{th} action. This happens when, the SER is increased by the contracted basic charge in near V_{th} activity. A multi-bit error can appear in single work in the non-bit interleaving structure, where components of a word are constantly stored away. This happens when a sensitive error occurs leading to bit error in cells that are nearby to one another. Multi-bit error correction must be implemented which involves the error correction code (ECC) circuit to attain an extremely large area and energy usage. Since, bits of a word are spatially interleaved in a bit-interleaving structure, single bit mistake occurs in every word [4]. A basic ECC circuit can be casted to rectify these errors. So, to resolve the increasing SER in the near V_{th} area, the bit-interleaving structure was used [9].

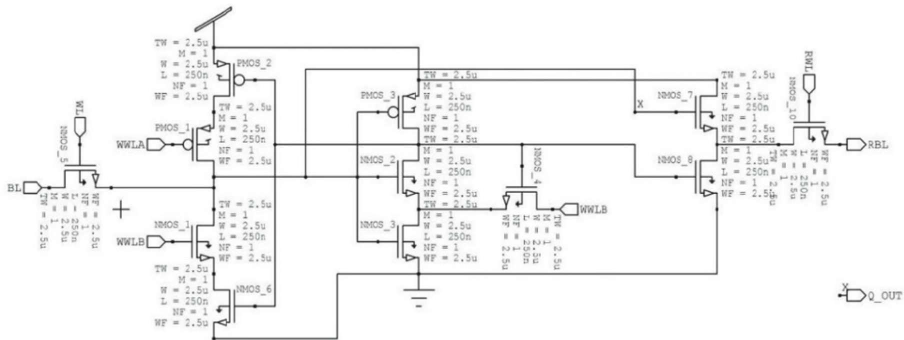
2 Previous SRAM Cell Designs

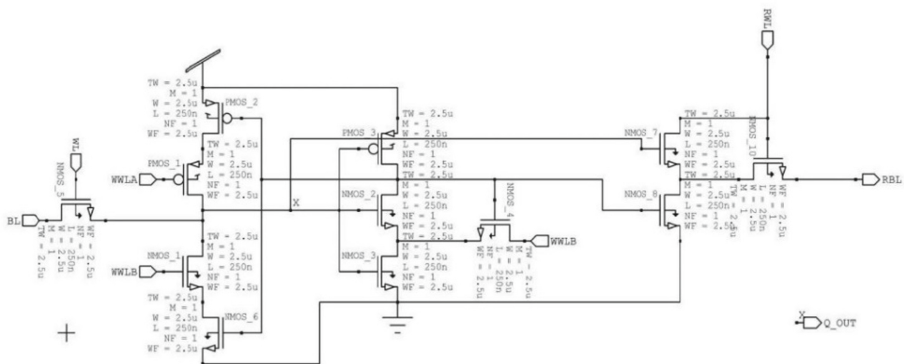
Many SRAM cells are introduced in near Vth operation. Cross coupled standard inverters formed traditional 6T [6] and 8T [7], WRE 9T, MH's 9T, Chang's 10T Static RAM cells, whereas cross coupled ST inverters are introduced in ST 10T, 11T SRAM cells [9]. In addition, depending on whether the storage node experiences read disturbance, these cells will be categorized as read disturbance and read disturbance free cells. Because read disturbance from BL or BLB can flip the stored data, the ordinary 6T and ST 10T Static RAM cells can be differentiated as a read disturbance cell. A read buffer is added to the standard 8T and WRE 9T, Chang's 10T, MH's 9T Static RAM cells to overcome the problem of read disturbance. These cells have the same read and hold stability since the read buffer decouples the storage node from the read BL. As a result, Static RAM cells provide enough read stability. By adopting power gating, the WRE 9T SRAM cell enhances the read buffer's leakage current as well as its write capabilities [7]. All the cells use bit interleaving structure, which helps in reducing SER, except the 6T SRAM cell. Since 8T and WRE 9T SRAM cell experience read disturbance from differential BL. Write back scheme is applied along with bit interleaving structure causing high energy consumption and area. So, to apply bit interleaving without write back Chang's 10T, ST 10T, MH's 9T and ST 11T SRAM cells are proposed. But they all have area and energy overheads due to number of transistors, control signals and differential BL structure.

So, a new ST 9T SRAM is introduced to reduce area and energy consumption with sufficient read, write, and hold stability [9]. A cross coupled arrangement of a normal inverter with stacked transistor (PUL1, PUL2, PDL1, PDL2), a ST inverter (PUR, PDR1, PDR2, NF), and one nMOS PG makes up the proposed cell. Write word line A (WWLA) and write word line B (WWLB) are column-based signals, whereas word line (WL) is a row-based signal. The gates of PG and PUL2 are connected to WL and WWLA, respectively. PDL1 gate and NF source are both connected to WWLB. The presented Schmitt-trigger based 9T cell employs a bit interleaving structure without a write-back scheme and consumes less energy than current cells while maintaining appropriate read stability and write ability in the near-Vth region by combining the following features: (1) a reduction in energy consumption and area by using a single bit line (BL) structure, (2) an improvement in read stability and write ability by using a selective power gating technique with the ST inverter write assist technique [9].

3 Proposed SRAM Cell Design

The proposed SRAM Cell describes three duplications of SRAM bit cells with nMOS only read ports. Figure 1 depicts a schematic of the proposed 12T SRAM cells. Each one has two access transistors and two cross coupled inverters. Each cell's read port is made up of three nMOS transistors. Figure 1(a) shows a read port with reduced data based read bit line leakage and a high-performance goal. The read ports in Fig. 1(b) and 1(c) have no data based read bit line leakage and are designed for extremely low power and high density, respectively. The I_{ON}/I_{OFF} is drastically deteriorated while working in the near and sub threshold area, making it increasingly difficult to implement a larger number of cells on a single column. The cumulative pass gate leakage grown equivalent to the read current as the number of cells increases, making it difficult for the sense amplifier to accurately evaluate the read bit voltage level. Furthermore, the read bit line leakage is affected by the data stored in the cell, causing the off state read bit line leakage current to fluctuate greatly. At ultra-low voltages, this is compounded by the worst-case data pattern, which might cause the RBL voltage level of 'zero' to exceed the RBL voltage level of 'one'. Although, as shown in Fig. 1, the suggested 12T-S1 cell has a lower data reliance than the 12T-S2 cell, it is still essentially incapable of executing a read operation at ultra-low voltages. However, as seen in the proposed work at ultra-low voltages increases the energy per access, where operating at the near threshold point is the most energy efficient. As a result, the ST 12T cell is operated in the near-threshold area for the best energy efficiency and performance. The read bit line swing is concern for the 12T-S1 cell at near threshold and super threshold voltages. The following proposed work goes deep into the RBL swing of each cell in relation to data pattern and supply voltage.





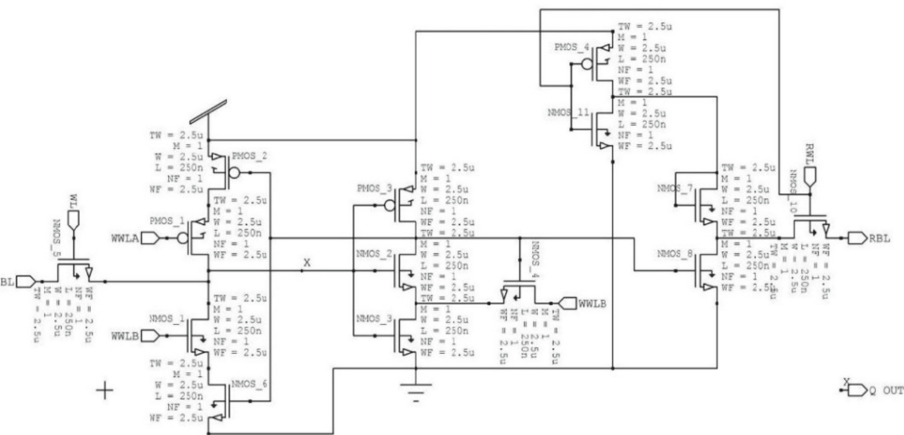


Fig. 1. Schematic of the proposed (a) 12T-S1 (b) 12T-S2 (c) 12T-S3 SRAM cells.

3.1 Main Contribution of This Work

This paper describes three duplications of SRAM cells with nMOS only read ports that aim to greatly reduce read port leakage based on data, improve read performance, and reduce area and minimum power consumption over ST 9T cell to enable thousand cells per column. The original ST 9T cell has single bit line structure to be pre-charged for both read and write operations causing increased delay between operations of cell resulting in higher static power consumption. The Proposed SRAM has RBL (Read-Bit line) in read port which carries out read operation ensuring to separate the write operation carried out by BL (Bit line). The ST 12T improves the read stability over ST 9T by implementing the path for read operation independent of storage node. Since, RWL is source to fill the RBL and storage node is a conducting voltage rather than storage node being the source to fill BL in ST 9T greatly reduces the possibility of read disturbance. Partially pre-charging bit lines to reduce the strength of access transistor can also help in further reducing read disturbance. The ST 12T also enables thousand cells per column by adding read buffer RBL which is independent of storage node, read disturbance free and avoiding read bit line swing issues for better sense amplifier evaluation of read bit line voltages. The SRAM cell usually perform more read operation than the write operation because write operation is performed only when a change is needed in cache. Therefore, power consumption is based on frequency of operation and switching activity. The ST 9T has more switching activity in both read and write operation due to WWLA, WWLB, and WL constantly changing voltage levels from '0' to '1' and '1' to '0', whereas in ST 12T during read operation only RWL is switching from '0' to '1' making it to consume less power while performing read operation than ST 9T. The sense amplifier can be adjusted with reduced voltage differentiation at RBL for improved read performance as it is independent of BL for read operation. The technology used is a 16 nm CMOS technology over the 22 nm CMOS technology which greatly reduces the area and power of SRAM cell. We achieve increased read access performance, low energy per access and low area using a unique architecture in each of the three read port cells, therefore expanding the design and application gamut for memory designers in low powered devices.

4 Results and CMOS Implementation

Utilizing side channel analysis and power control transistors where this work is implemented in Back-End ASCII technique of 16 nm and 22 nm CMOS technology of low power and highly secure data information will be executed with the goal of reducing power consumption and increasing security on memory control operation. The output of comparisons of one-sided Schmitt-Trigger based 9T SRAM cell for near threshold operation given in Table.1, and comparisons analysis chart given in Fig. 2. The output comparison of proposed work in data independent read port with one sided Schmitt-trigger based 12T SRAM cell are given in Table 2, and comparisons analysis chart is given in Fig. 3. The Output waveforms are given in Fig. 4(a), (b), (c).

Table 1. Comparison of one-sided Schmitt-trigger based 9T SRAM cell for near threshold operation

	One-sided Schmitt-trigger based 9T SRAM cell for near-threshold operation			
	Single bit 9T SRAM		8-Bit 9T SRAM	
	22 nm	16 nm	22 nm	16 nm
MOSFETs	9	9	72	72
Area (nm)	192	144	1584	1152
Power (μW)	21.401	0.325	169.93	2.476
Delay (ns)	21.384	20.14	9.085	0.104
Input voltage (V)	0.8	0.6	0.8	0.6

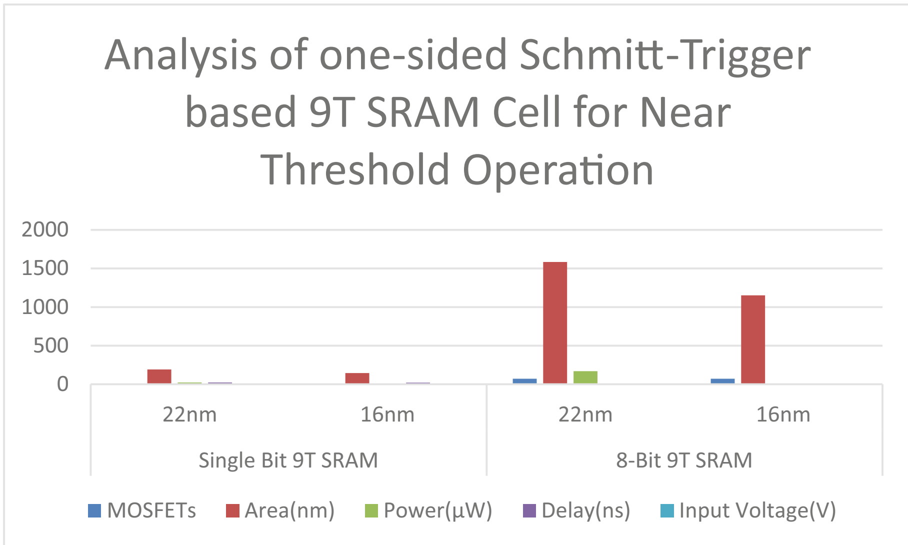


Fig. 2. Analysis of one-sided Schmitt-trigger based 9T SRAM cell for near threshold operation

Table 2. Comparison of one-sided Schmitt-trigger based 9T SRAM and 12T SRAM cells.

	Comparison of ST 12T SRAM cells with ST 9T SRAM cell							
	ST 9T SRAM		ST 12T SRAM-S1		ST 12T SRAM-S2		ST 12T SRAM-S3	
	22 nm	16 nm	22 nm	16 nm	22 nm	16 nm	22 nm	16 nm
MOSFETs	9	9	12	12	12	12	14	14
Input voltage (V)	0.8	0.6	0.8	0.6	0.8	0.6	0.8	0.6
Area (μm)	0.198	0.144	0.286	0.208	0.286	0.206	0.330	0.240
Min. power (μW)	46.02	0.42	1.13	0.13	0.80	0.12	10.12	0.56
Delay (ns)	9.14	6.17	40.53	40.17	40.52	40.10	40.59	40.15

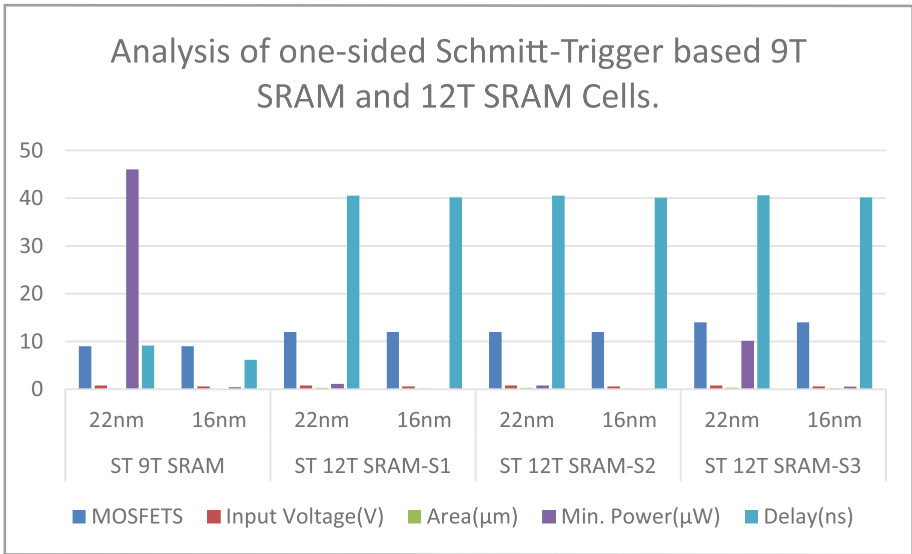
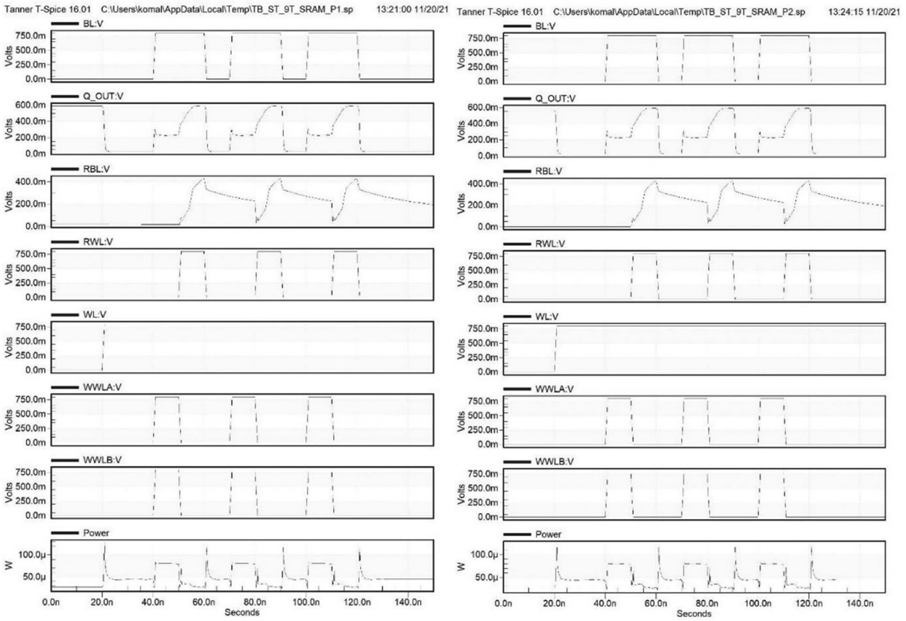
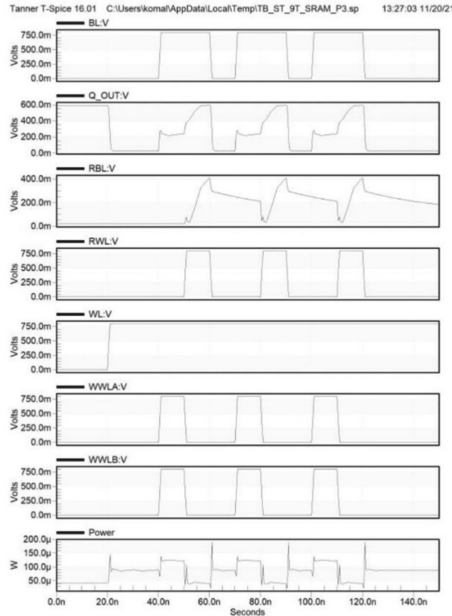


Fig. 3. Analysis of one-sided Schmitt-trigger based 9T SRAM and 12T SRAM cells.



(a) (b)



(c)

Fig. 4. Output waveforms of (a) 12T-S1, (b) 12T-S2, (c) 12T-S3 SRAM cells.

5 Conclusion

In this work, we suggest three area of expertise read ports for SRAM cell with improved data independent read port leakage identified as high performance, low power, and low area. Since none of the intended read ports had any PMOS, the NMOS size was reduced, resulting in lower vertical sizing and shorter bit lines in thin form architectures. This decreased the amount of area per cell and the amount of energy used in each access of read and write operations. Each cell with the intended read ports increased the effective read operation with reduced dynamic power per read bit line, and its allowing for significant area savings through the sharing of peripheral hardware. As a result, the proposed ST 12T SRAM cell consumes less power, energy, and delay.

References

1. Calhoun, B., Chandrakasan, A.: Static noise margin variation for sub-threshold SRAM in 65-nm CMOS. IEEE J. Solid-State Circ. **41**(7), 1673–1679 (2006)
2. Calhoun, B.H., Chandrakasan, A.P.: A 256-kb 65-nm sub-threshold SRAM design for ultra-low-voltage operation. IEEE J. Solid-State Circ. **42**(3), 680–688 (2007)
3. Dreslinski, R.G., Wieckowski, M., Blaauw, D., Sylvester, D., Mudge, T.: Near-threshold computing: reclaiming Moore's law through energy efficient integrated circuits. Proc. IEEE **98**(2), 253–266 (2010)
4. Kim, T.-H., Liu, J., Keane, J., Kim, C.H.: A 0.2 V, 480 kb subthreshold SRAM with 1 k cells per bitline for ultra-low-voltage computing. IEEE J. Solid-State Circ. **43**(2), 518–529 (2008)
5. Pasandi, G., Fakhraie, S.M.: A 256-kb 9T near-threshold SRAM with 1 k cells per bitline and enhanced write and read operations, IEEE Trans. Very Large Scale Integr. (VLSI) Syst., **23**(11), 2438–2446 (2015)
6. Hu, V.P.-H., Fan, M.-L., Su, P., Chuang, C.-T.: Analysis of GeOI FinFET 6T SRAM cells with variation-tolerant WLUD read-assist and TVC write-assist. IEEE Trans. Electr. Devices **62**(6), 1710–1715 (2015)
7. Yabuuchi, M., Nii, K., Tsukamoto, Y., Ohbayashi, S., Nakase, Y., Shinohara, H.: A 45 nm 0.6 V cross-point 8T SRAM with negative biased read/write assist. In: Proceedings of the IEEE Symposium on VLSI Circuits, pp. 158–159, June 2009
8. Gupta, S., Gupta, K., Calhoun, B.H., Pandey, N.: Low-power near-threshold 10T SRAM bit cells with enhanced data-independent read port leakage for array augmentation in 32-nm CMOS. IEEE Trans. Circ. Syst.-I Regul. Papers **66**(3), 978–988 (2019)
9. Cho, K., Park, J., Oh, T.W., Jung, S.-O.: One-sided Schmitt-trigger-based 9T SRAM cell for near-threshold operation. IEEE Trans. Circ. Syst.-I Regul. Papers **67**(5), 1551–1561 (2020)