Design and Analysis of All-Optical Universal Logic Gates Using 2D Silicon Photonic Crystal Structures

Anushka Lucas, R. Narayanan, and Nikhil Deep Gupta

Abstract With the continuous increase in the demand for higher computational speeds, photonics-based Integrated Circuits (ICs) are becoming more vital for future computational technologies. For designing Photonic ICs there is a requirement to have logic gates that can work in all-optical domain. The proposed work presents the design and numerical analysis of All-Optical universal logic gates including NAND, NOR, and NOT gates that are realized using 2-D Silicon periodic nanophotonic structures through light beam interference-effect. 2D Photonic crystals through photonic bandgap optimization, make it possible to reduce the losses incorporated during the propagation of light. The structures are designed to operate at 1.55 μm. The present work demonstrates an unpretentious but effective approach for designing the all-optical universal logic gates. The design has shown good transmission efficiency for all the input combinations of the logic gates and thus can be used to design other forms of logic gates and circuits, further.

Keywords Photonic crystals · Optical logic gates · Silicon photonics · Universal logic gates

1 Introduction

Conventionally, from past several decades, electrons are the preferred choice to make information flow from one place to another through semiconductor transistor-based devices, but as they are reaching the pinnacle of their performances in terms of limitations such as power dissipation, input power requirement, and delay, one has to look for the alternatives. To overcome the mentioned limitations, photonics-based designs can come to the rescue. There are a lot of concentrated efforts going on

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M. Tiwari et al. (eds.), *Optical and Wireless Technologies*, Lecture Notes in Electrical Engineering 892, https://doi.org/10.1007/978-981-19-1645-8_1

all around the globe to design all-optical Photonic Integrated Devices and circuits [1]. In that regard, all-optical logic gates (AOLGs) have to compulsorily evolve and required to make its mark for the development of futuristic technologies like optical computers, optical networks etc.

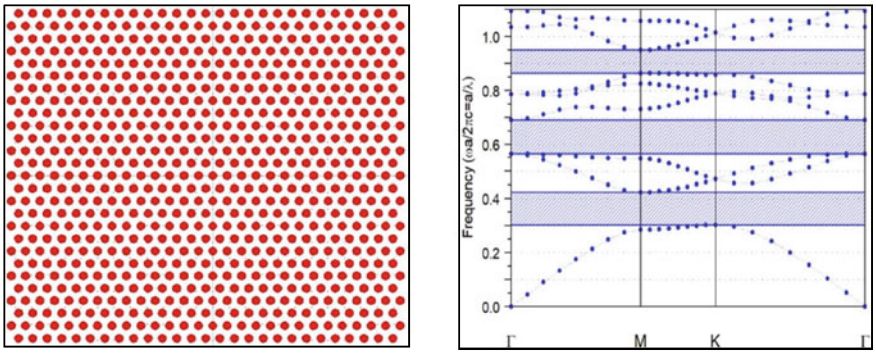
On the other hand, Photonic crystal (PhC), a periodic dielectric nanophotonic sub-wavelength structure, in the past decade or so has shown its immense potential to manipulate light beyond fundamental principles [2]. PhC structures are also known as semiconductors of light as they can control the propagation of light. 3D PhCs can allow full control over the photons transmission in all directions. PhC structure has a periodic arrangement of two different materials of a particular refractive index. Due to the periodic arrangement, they lead to the generation of photonic band gaps that implies that the device does not allow a certain range of wavelengths to travel through it [3]. Many insects such as butterflies and peacock's feathers have naturally occurring PhC structures due to which we can see beautiful colours in their wings and feathers.

The PhC-based AOLGs have numerous advantages [4–9]. Because of their remarkable ability to manipulate the density of states for photons at particular wavelengths, these structures give the freedom to open photonic bandgaps as per the requirement of application and can be a perfect ingredient for the realization of integrated all-optical devices. AOLGs based on these periodic sub-wavelength structures are thus realistically promising for practical on-chip applications.

In the present paper, we are presenting the design and analysis of a 2-D Silicon PhC based Universal AOLGs i.e. NAND, NOR and NOT gate based on light beam interference-effect. The devices are designed on the Si platform to make it compatible with Si photonic integrated circuits. The design has been realized with Si based PhC waveguide having optimized defects created in it that make these AOLGs simple and at the same time easy to design practically. The results have demonstrated the good transmission efficiency for all the input combinations and thus it is predicted that it can be a good option to fit in with the Si-based photonic integrated circuits. It has also been observed that for the operation of these AOLGs, high power excitation is not required.

2 Structure Design and Numerical Analysis

In the projected design, All-optical Universal Logic Gates i.e. NAND, NOR and NOT gates are realised based on waveguide defects created by light beam interference effect [7]. The 2D PhC are preferred over 3D designs because of the owning to the bigger chances of their replication for mass productions. The schematic structure of the proposed 2-D PhC is shown in Fig. 1(a). The structure is composed of hexagonal lattice arrays of cylindrical Si rods considered to be placed in the air as a background medium. The structure is optimized on the premise of the band diagram as given in Fig. 1(b).



(a) (b)

Fig. 1 **a** Schematic diagram of 2-D PhC taken as a base for the proposed AOLGs designs; **b** Photonic band diagram for the structure shown in 1(a)

The optimized lattice constant for the structure is then taken as 0.875 um and the Si rods radius is considered as 0.2475 um as it suits the design requirement to work at 1550 nm. The area of PhC calculated is 1.4051 μm^2. As the design is set to work at 1550 nm, the Si relative permittivity is set at 11.56 [7]. A continuous-wave (CW) light source at a wavelength of 1550 nm is used as an input. The parameters of the optimized structure are listed in Table 1.

There are various numerical modelling techniques that has been used over the years for the modelling of photonic devices such as Finite-Difference Time-Domain (FDTD) Method, Plane Wave Expansion (PWE) Method, Beam Propagation Method, Finite-Element Method, etc. [10]. Although, all the different techniques are having their own advantages, out of them few techniques have shown more adaptability on account of their applicability for numbers of applications and those techniques involved FDTD and PWE method [9]. In the present work, FDTD and PWE methods are getting used for the optimization of the design and its analysis. During this research work, commercially available Synopsys Rsoft CAD tools has been used, which are supported by the concepts of FDTD and PWE algorithms [11].

The PWE technique is commonly used to obtain dispersion relation and mode profiles for PhC structures. PWE is traceable to analytical formulations and is useful in calculating Maxwell's modal alternatives over an inhomogeneous or regular geometry, it is a technique of the frequency domain in which Bloch principle is employed

Table 1 Parameters used for the design of proposed basic 2-D Si PhC platform for the design of AOLGs

S. no	Parameters	Value
1	Background medium index	1 (Air)
2	Rod index at 1550 nm	11.56 (Si)
3	Lattice constant or period	875 nm
4	Radius of rods	247.5 nm

to deal with the issues of its own value and answers are acquired as a plane wave superposition. The FDTD method, which is one of the most reliable and rigorous method to provides a solution to Maxwell's equations, has been used in the present case as it does not have any approximations or theoretical restrictions and is reliable being used throughout the optics and photonics research community.

3 Design Procedure and Optimization

The section discusses about the design aspects specific for the particular logic gate. The universal optical gates that we are going to discuss, are NOT, NAND and NOR gates. The input source is taken as continuous wave (CW) source at 1550 nm with input launch power of 1 W for all the cases. Defects are created in the structure shown in Fig. 1(a) to create a Y-shape junction, which is in the proposed logic gate designs taken as a basic building block and modified to get different operations. The Y-shaped structure is shown in Fig. 2.

3.1 NOT Gate

The study and analysis of an optical NOT logic gate is realized by modifying the Y-shape junction such that the reference light (RC) waveguide would become longer than the input waveguide (AC) as shown in Fig. 3. A CW reference light of 1550-nm wavelength is given at into the port R to travel through waveguide RC, whereas the input is applied at port A.

At first, when there is no input signal at port A, this allows the reference beam introduced through port R to propagate through RC and the output, then, produced

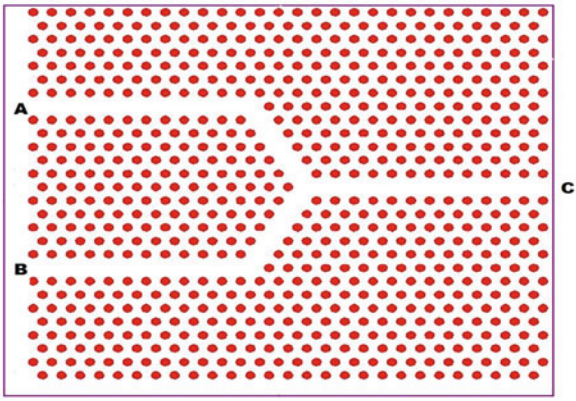


Fig. 2 Schematic diagram of basic Y-shaped junction waveguide used to design AOLGs

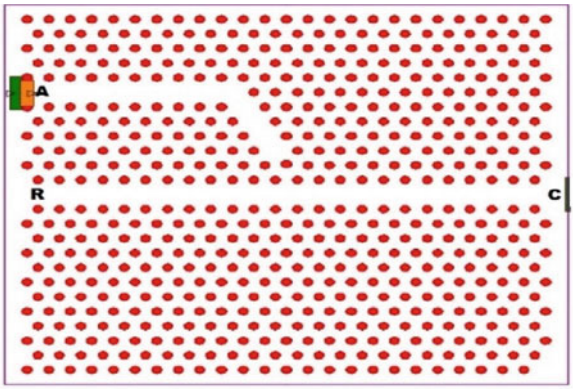


Fig. 3 Schematic diagram of proposed NOT gate

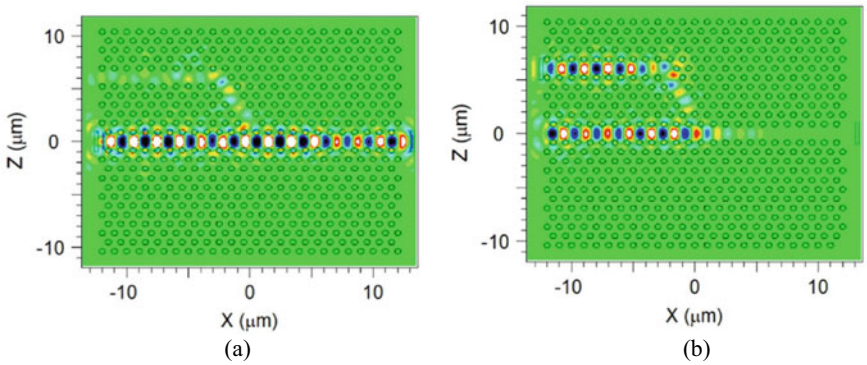


Fig. 4 Observed field distributions for the proposed NOT AOLG at steady state, **a** when no signal applied at port A, **b** when the input beam injected into port A

at port C, as shown in Fig. 4(a), corresponds to the logical operation of "0 NOT = 1". The transmission percentage observed at port C is around 85%. The transmission percentage has been calculated as the percentage of input received as compared to the input launch. Next, when an input signal is fed to port A, leads to destructive interference between the signals given at port A and port R that occurs due to the as such designing of the structure, as they travel toward the output port across defect waveguide. There is, then, no signal received at the output port that can be seen from Fig. 4(b) and corresponds to the logical operation "1 NOT = 0". From the two operations mentioned above, it can be said that the proposed design can work reasonably well as NOT AOLG. The transmission percentage calculated at output port for low logic is only 0.11%. The truth table with transmission ratio for the proposed NOT AOLG is given in Table 2.

Table 2 Truth table for realized NOT AOLG with transmission percentage

Input (A)	Output (C)	Transmission %
0	1	85
1	0	0.11

3.2 NAND Gate

To design and study the 2 input NAND AOLG function, the path length for the input optical signal in waveguide AC is made larger than that in RC, whereas the signal in waveguide BC is made to travel less than that in RC by one lattice constant (period of PhC structure). The design is used to make sure that there are sufficient constructive and destructive interferences to take place to achieve required logic operations. In this case too, A CW at 1550-nm wavelength is fed into the reference port R to travel through RC. The reference beam fed to port R has double the power as that of the input signals fed at port A and B, separately. The proposed schematic of the NAND AOLG is shown in Fig. 5.

When there is no input given at ports A and B, then the reference signal fed at port R can propagate across RC and the output signals are observed at port C, as shown in the Fig. 6(a) that resembles the logical operation "0 NAND 0 = 1". Very small back reflections are observed at port A and B. The transmission percentage calculated for the corresponding logic operation at output is 85%. Now, when the optical signal is fed at input port A with no signal at port B (A = 1 and B = 0), then input signal while propagating through the waveguide lead to the destructive interference when interacts with reference beam. However, as the reference signal given at port R has double the power as that of signal, the output signal with sufficient transmission percentage is observed at port C, as shown in Fig. 6(b). This process is equivalent to the logical operation "1 NAND 0 = 1". The transmission percentage calculated for the corresponding logical operations is 86%.

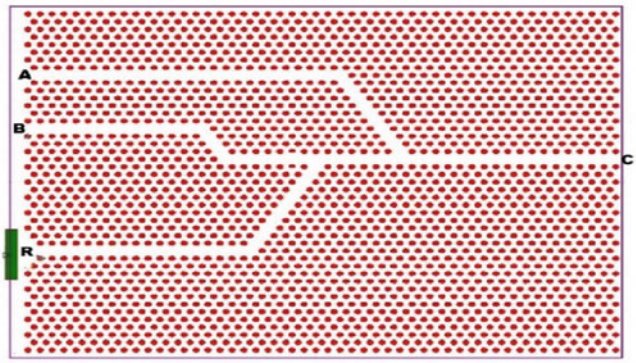


Fig. 5 Schematic diagram of proposed NAND Gate

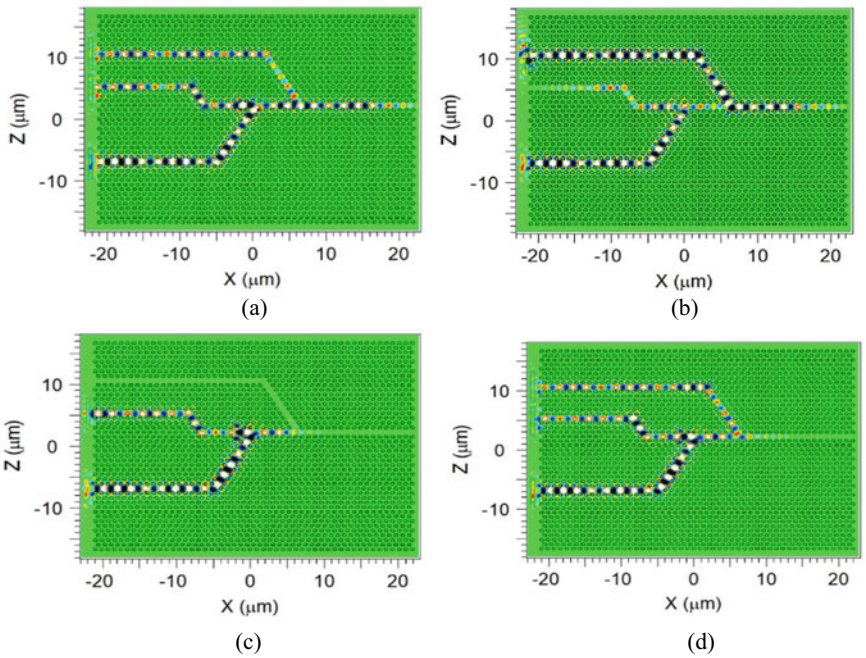


Fig. 6 Observed field distributions for the proposed NAND AOLG at steady state, **a** when both A = B = 0; **b** when A = 1 and B = 0; **c** When, A = 0 and B = 1; **d** When, A = 1 and B = 1

Now, for the case, when B = 1 and there is no signal at port A. In that case, destructive interference takes place between the signal fed at port B and reference fed at port R as they interact with each other during forward propagation, as discussed above.

However, as the feed at port R has double the power that of the input at port B, the high output is observed at port C, as observed in Fig. 6(c), which is equivalent to the logical operation "0 NAND 1 = 1". The transmission percentage calculated is 86%. Lastly, for the case when signal is applied at both port A and B, then the three signals (two input and one reference) when interact with each other during forward propagation undergo destructive interference due to the as such design of the device. However, in this case, as the reference beam power is equal to the summation of the power of two input signals, there's no output observed at port C, as observed in Fig. 6(d). The entire process resembles to the logical operation of "1 NAND 1 = 0". The truth table for the proposed NAND AOLG with transmission values are given in Table 3.

Table 3 Truth table for realized NAND AOLG with transmission percentage

Input A	Input B	Output C	Transmission %
0	0	1	85
1	0	1	86
0	1	1	86
1	1	0	0.1

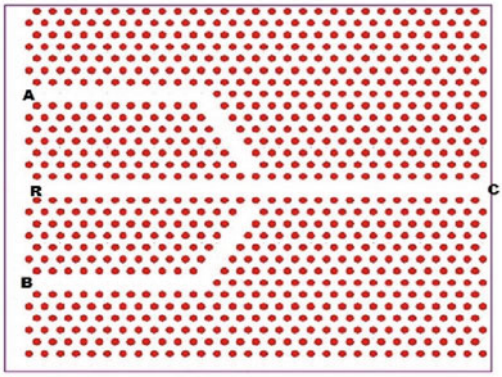


Fig. 7 The proposed schematic diagram of the NOR AOLG

3.3 NOR Gate

A 2 input NOR AOLG is realized by modifying the Y-shape junction (Fig. 2) such that the reference light waveguide (RC) is longer than the input waveguides (AC, BC). Here also, 1550-nm CW is used as the reference signal that is fed at port R. The reference signal fed at port C is fed with double the power than the signal fed at port A and B, separately. The proposed NOT AOLG schematic is shown in Fig. 7.

When there is no input signal at port A and B (A = 0 and B = 0), the reference fed at port R can propagate through waveguide RC and output is observed at port C, as shown in the Fig. 8(a), which resembles the logical operation "0 NOR 0 = 1". Now, when the light is fed at port A only (A = 1 and B = 0), without any signal at port R, the output signal received is approximately negligible, as shown in Fig. 8(b). The process is equivalent to the logical operation "1 NOR 0 = 0". The transmission percentage calculated for the corresponding logic operations is 0.11% only. Next, when there is signal applied at input port B without any input at port A and R. Again, the output signal observed is negligible, as observed in Fig. 8(c), and matches with the logical operation "0 NOR 1 = 0". The transmission percentage in this case is also only around 0.11%. Finally, when signals are fed at both the input ports together with signal at port R, destructive interference is observed among the signals in the output waveguide and as a result there is no significant signal output observed at port C, as can be seen from Fig. 8(d) that matched with the logical operation "1 NOR

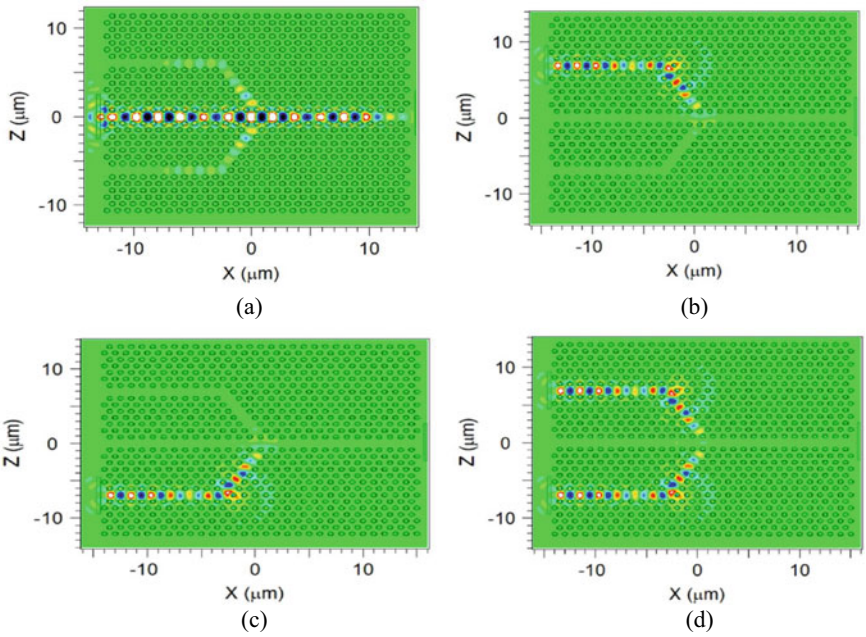


Fig. 8 Observed field distributions for the proposed NOR AOLG at steady state. **a** When both A = B = 0; **b** When A = 1 and B = 0; **c** When, A = 0 and B = 1; **d** When, A = 1 and B = 1

Table 4 Truth Table for realized NOR AOLG with transmission percentage

Input A	Input B	Output C	Transmission %
0	0	1	80
1	0	0	0.1
0	1	0	0.1
1	1	0	0.1

1 = 0". The proposed design can perform all the required operations for the NOR gate using light, thus can be termed as NOR AOLG. The transmission percentage calculated for the corresponding logic operations in this case is also less than 0.2%. The truth table for the proposed 2-input NOR AOGL operation is given in Table 4.

4 Conclusion

The presented work has demonstrated a simple but effective design for a universal all-optical gate including NAND, NOR, and NOT gates. The transmission losses are controlled through the incorporation of the subwavelength structures designed with 2D PhC structures. The numerical simulation studies are done for the different input

signals and the transmission percentage is calculated. For all the three logic gates operations, the observed transmission percentages have shown good contrasts for the logic high and low output. For 'OFF' or '0', the output transmission percentage observed is less than even 1% and for 'ON' or '1' it is in all the cased is more than 80%. The used 2D PhC structures in the proposed designs are supposed to be done over the Si platform and therefore, has a realistic potential for Si photonics-based on-chip applications, that can be designed with current microfabrication techniques, including electron-beam lithography processes etc.

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