A Comparative Study of GaN and Si-Based SOI FinFET

Abhishek Saha, Rudra Sankar Dhar, and Subhro Ghosal

Abstract Over the last decade, the continuous strife for miniaturization has led to an exponential increase in the power density of semiconductor electronics. The average operating temperature of devices has sharply increased due to the combined effects of high frequency switching and lower surface area per device. A possible way out is the introduction of with high bandgap materials or alloys as an alternative to silicon electronics. Of the different options, GaN with its high bandgap and mobility has emerged as one of the most promising materials. However, use of GaN has primarily been restricted to applications in HEMT and optoelectronic devices. In this paper, a comparative simulation study of GaN and Si field effect device has been presented using SOI FinFET as the device of choice. It has been shown that besides a higher ON current GaN shows a reduced sensitivity of I_{ON}/I_{OFF} ratio to variations in operating temperature justifying its choice in high-power density devices. Effect of an LDD profile has been studied. Moreover, this work reports a higher susceptibility of threshold voltage of GaN-based devices to variations in dielectric. This has promising implications with respect to its use as a bio-detector.

Keywords TG-FinFET · *GaN* channel · Bio-detector

1 Introduction

Over the past couple of decades, silicon technology has dominated the semiconductor industry and the major factors responsible for it, besides easy availability, and excellent oxide properties have been the scalability of Si devices. However, the

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aggressive demands on device and circuits parameters which are being set by the wireless communication sector in the microwave and RF region will soon appear to be out of reach of Si-based devices whose parameters are close to their theoretical maxima. Moreover, relatively lower values saturation velocity besides a low carrier mobility precludes silicon as the material of choice for modern high speed switching applications. Over the last decade, the continuous strife for miniaturization has led to an exponential increase in the power density of semiconductor electronics. Besides the obvious bottlenecks due to short-channel effects and leakage current due to tunneling, the average operating temperature of devices has sharply increased due to the combined effects of high frequency switching and lower surface area per device. However, it is very much problematic to use silicon electronics device as a power device because of its temperature constraint. Hence, the focus of device scientists on new compound semiconductors which include group III–V materials, silicon–carbide, and silicon–germanium. In the last two-decade, group III-nitride semiconductors and in particular gallium nitride (GaN), and its associated alloys, have emerged as the most promising nitride semiconductor for commercial applications, especially in the field of optoelectronic and high-power devices due to its inherent material properties. Indeed, GaN has a larger breakdown field (20 MV/cm) [1] than GaAs (4 MV/cm) and Si (3 MV/cm) and also high peak electron velocity [2] of 3 $\times$ 107 cm/s as compared to GaAs (2 $\times$ 107 cm/s) and Si. The acceptability of GaN technology to the stringent military as well as commercial sector owes itself the superior electron transport properties of GaN. However, widespread acceptability cannot be achieved unless some bottlenecks such as drain current collapse and other reliability problems [3–5] are overcome.

As we move further into the DSM regime, effective control of channel is an area of concern. As per the roadmap provided by ITRS, the effects associated with short channel together with the stringent leakage requirements for devices beyond 32 nm technology node will seriously impede further developments using planar devices. Multigate devices like tri-gate transistor or fin-shaped field effect transistor appear to be one of the most promising devices below the 20 nm technology node, as the effective increase in the inversion layer owing to multiple gates leads to a better channel control. The gate-all-around architecture provided by FinFET suppresses the short-channel effects (SCE) while achieving high trans conductance value and lower subthreshold swing [6–8]. Miniaturization of the components and low energy consumption makes it possible to use them as switching power supplies, amplifiers, frequency converters in electronic equipment [9, 10], sensors [11–13], as well as high frequency switching generators and modulators in medical surgical devices for high frequency and ultrasonic welding of biological tissues.

In this study, the proposed structure is simulated with two different channel materials, i.e., GaN and Si. An LDD doping profile has been chosen. The parameters varied are temperature and gate material, and different figures of merit of relevance, namely I_{ON}/I_{OFF} ratio, threshold voltage, leakage current, saturation current, and subthreshold slope have been calculated from the simulation data.

This paper is organized as follows. In Sect. 2, the simulation model is described. The simulated results of GaN-based n-channel TG-FinFET are analyzed and discussed in Sect. 3, and Sect. 4 discusses the significance of the study.

2 Materials and Methods

2.1 FinFET

In this work, a model of GaN-based FinFET structure is considered for the simulated study by Atlas of Silvaco_TCAD device simulator. An SOI FinFET is the chosen structure for simulation. While the larger gate area leads to a better control, the SOI structure helps in the elimination of parasitic capacitance leading to a better high-frequency response. Moreover, due to BOX layer, there is no unwanted leakage paths which are far from the gate and lesser effect of back-gate leading to lower power consumption. A major drawback of SOI structure is self-heating as the silicon oxide substrate prevents heat dissipation. However, the better thermal properties of the chosen material GaN make this structure better suited for it than Si.

The simulated device structure of the n-channel TG (Tri gate) FinFET, used in this study, is shown in Fig. 1. A buried oxide thickness (TBOX) of 50 nm has been used.

The device consists of a Si fin of rectangular cross-sectional wrapped around the channel which terminates in the source and drain regions at both ends. The inversion current is controlled by the polarization charge on gate oxide which forms the interface between the channel and the fin. Thus, the output drain current is a function of gate and drain bias voltages.

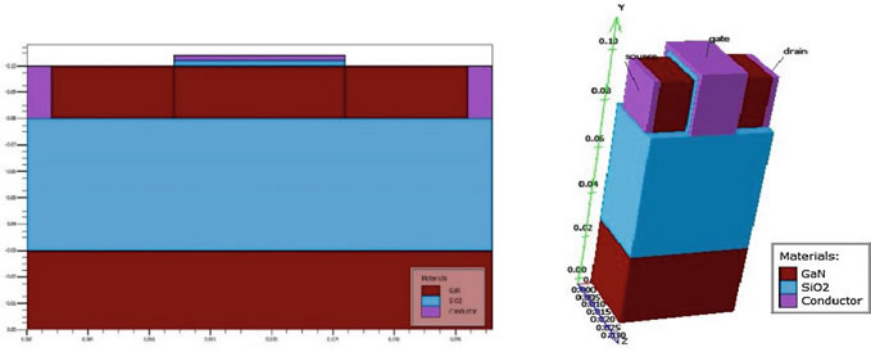

Fig. 1 TG-FinFET structure (2D and 3D view)

2.2 Simulation Method

All simulations of this work have been carried out using ATLAS SILVACO TCAD, 3D simulation. Basic parameters of this n-channel TG-FinFET structure are presented in Table 1.

A Gaussian doping profile has been used for the channel region. In this entire simulation procedure, work function of gate electrode is assumed as 4.6 eV. Solution method applied is Gummel Newton. For carrier statistics, instead of the default Boltzmann statistics, we have used Fermi to account for reduced carrier concentrations in heavily doped regions. As this study considers the effects of high temperature, the energy exchange with the surrounding lattice environment through carrier heating and through generation-recombination processes need to be taken into account. To take account of the recombination effects, the leakage currents that owe their origin to thermal generation are simulated by the Shockley–Read–Hall (SRH) model while consrh accounts for concentration dependent lifetimes. Auger is used to account for recombination at high current densities and high-level injection effects. The Auger recombination rate is reduced at higher values of carrier density as the inter-carrier interactions become more significant. Experimental work has shown that in heavy doped regions SOI MOSFET starts behaving like a bipolar transistor as the pn product becomes doping dependent, and bandgap narrowing occurs; BGN accounts for this effect. The quantum mechanical effect of carrier confinement at the gate oxide interface in MOSFETs is accounted for by the correction given by Hansch (Model HANSCHQM).

3 Simulation and Results

In this section, the simulated results of n-channel TG-FinFET with different channel materials, various dielectric materials, different types of channel doping, and temperature variations are analyzed and discussed in detail.

Table 1 Basic parameters used for SOI TG-FinFET

Device parameter	Value	Unit
Length of source and drain	10	Nm
Gate length	14	Nm
Source/drain height	20	Nm
Source/drain width	20	Nm
Doping of source and drain	1×10^{18} (n-type)	Atoms/cc
Doping of substrate and channel	1×10^{15} (p-type)	Atoms/cc
T_{BOX}	50	Nm
T_{sub}	30	Nm
T_{OX}	2	Nm

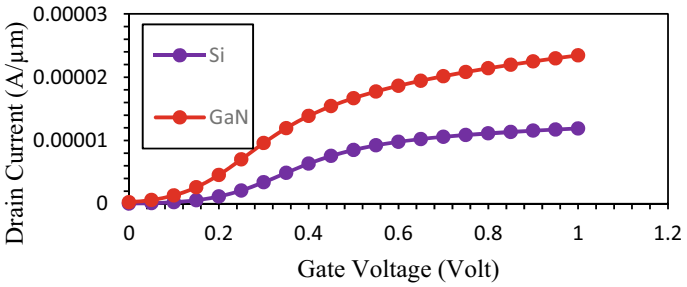

Fig. 2 I_D–V_G curve for n-channel TG-FinFET (uniform doping) with different channel materials

3.1 Variation in Channel Material

Figure 2 shows the variation of drain current with the increment of gate voltage for silicon (Si) and gallium nitride (GaN) channel TG-FinFET. Here, the DC voltage is applied to the gate terminal which is varied from 0 to 1 V with the drain bias fixed at $V_{DS} = 1$ V.

The transfer characteristics show that the higher mobility of GaN translates to a higher ON current than Si. This makes such GaN-based field effect devices a better choice for power-electronics circuits where a higher drive current is required.

3.2 Variation in Drain Doping Profile

Various works have been done on the effects of gradation of doping of field effect devices in the channel region [14–17]. The gradation may be deliberate or an undesired consequence of the implantation process. However, in this study, it was observed that replacement of a uniform doping profile with a Gaussian one in the channel region led to an insignificant change. This could be a consequence of the light doping and tight control of the channel region by the surrounding gate structure. However, the source and drain regions are highly doped, and FinFET devices with LDD implantation have been reported [15] to exhibit better electrostatic characteristics resulting in reduced values of subthreshold slope and DIBL. In this study, also, the effect of an LDD doping profile (Fig. 3) was studied, and the transfer characteristics show a notable improvement for GaN though the effect is less pronounced for the Si channel device (Fig. 4).

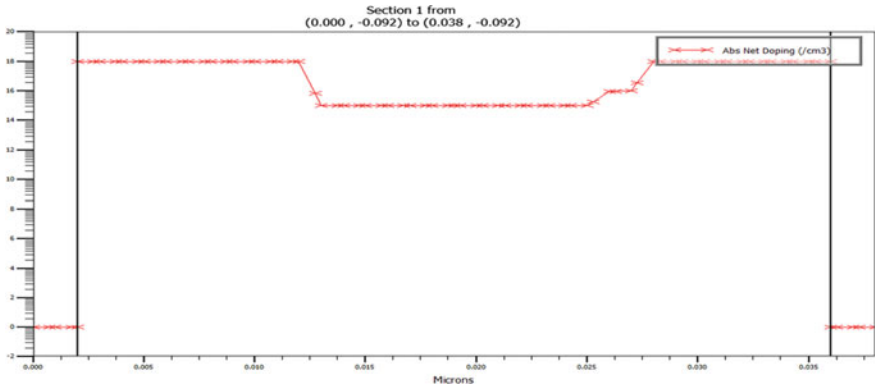

Fig. 3 Doping profile of LDD region

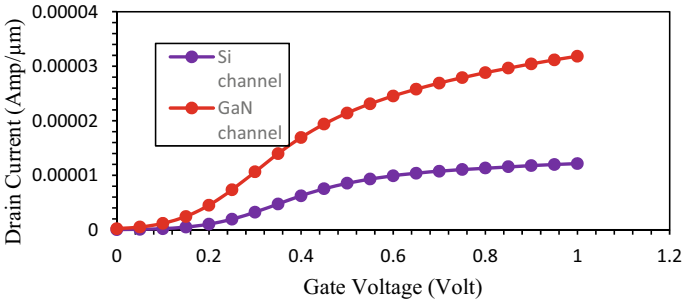

Fig. 4 I_D–V_G curve for n-channel TG-FinFET with LDD region

3.3 Dielectric Material Variation

Simulations were done to study the outcome of gate dielectric material on the output of both GaN and Si-channel devices. It can be seen that in both the cases GaN channel-based field effect device produces more current than silicon channel-based device and significantly reduction in threshold voltage also. The different dielectric materials used were aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), silicon nitride (Si_3N_4), and zirconium dioxide (ZrO_2) in contrast with the silicon dioxide (SiO_2). Figure 5 shows the simulated result.

Extracted parameters from the simulations are given in Table 2. From the comparison shown in the Table 2, it can be noted that with the decreasing value of dielectric constant of different dielectric material the value of the threshold voltage is decreased. The value of maximum saturation drain current I_{DSmax} is also decreased, whereas the value of leakage current is increased. Furthermore, it is observed that the value of threshold voltage for all kind of dielectric material used in GaN channel-based

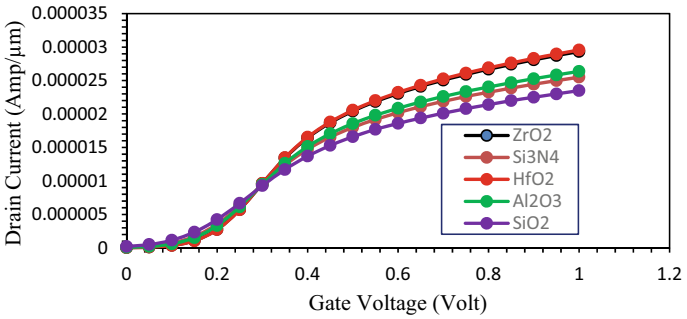

Fig. 5 I_D–V_G characteristics (GaN channel TG-FinFET) for different dielectric materials

Table 2 Extracted parameter value for n-channel TG-FinFET

Channel material	Dielectric material (dielectric constant value)	V_t V	I_{DSmax} ($\times 10^{-6}$) A	Leakage current ($\times 10^{-9}$) A	Sub V_t mV/decade
GaN	HfO_2 (25)	0.127	29.6	29.85	91.29
	ZrO_2 (23)	0.126	29.3	31.36	91.91
	Al_2O_3 (9)	0.108	26.4	68.85	103.31
	Si_3N_4 (7)	0.101	25.5	92.20	108.58
	SiO_2 (3.9)	0.073	23.5	207.2	127.79
Si	HfO_2 (25)	0.204	14.0	2.52	88.74
	ZrO_2 (23)	0.203	13.9	2.69	89.37
	Al_2O_3 (9)	0.181	13.0	7.97	100.77
	Si_3N_4 (7)	0.172	12.8	11.87	105.88
	SiO_2 (3.9)	0.144	12.2	35.4	124.03

TG-FinFET is lower than that of the Si channel-based TG-FinFET. The sensitivity to dielectric material [17] can be explained as follows:

The drain current in the subthreshold region has an exponential dependence of the form exp $\left({}^{v_{gs}}/_{nVT}\right)$ which results a relation for subthreshold voltage

$$S = nVT\ln(10) \text{ where } n = \left(1 + \frac{C_b}{C_g}\right),\ C_b = {}^{\int Si}/_{w_d},\ C_g = {}^{\int ox}\Big/_{t_{ox}}$$

Now, as HfO_2 has the higher dielectric constant, there will be an increment in oxide capacitance which translates to a lower value of n. Thus, a higher value dielectric constant of gate oxide helps the subthreshold slope to approach its ideal value. The lower leakage current can be accounted for by the decrease in threshold voltage.

A very significant observation is given in Table 3. Table 3 provides the data for percentage change in threshold voltage with variable dielectric material, in this case

Table 3 Percentage change in threshold voltage with dielectric

Channel material	Dielectric material	Percentage change in threshold voltage
GaN	HfO_2 (25)	73.97
	ZrO_2 (23)	72.6
	Al_2O_3 (9)	47.94
	Si_3N_4 (7)	38.36
Si	HfO_2 (25)	41.66
	ZrO_2 (23)	40.97
	Al_2O_3 (9)	25.69
	Si_3N_4 (7)	19.44

GaN taken as the primary material for this study, whereas silicon data are used as a comparison. The percentage change in threshold voltage with dielectric constant is much more for GaN than Si. Over the past decade, a significant amount of work [18–22] has been done on the use of field effect devices as a biosensor. The increased sensitivity of GaN-based device to dielectric variation makes it a promising candidate for use as a detector of biologically relevant substances.

3.4 Temperature Variation

Applicability of group III-nitride-based devices for high-frequency, power, and temperature applications is well documented [22–25]. Therefore, for device optimization, self-heating effect and ambient temperature effect of a device are such a thing that can be studied to establish its suitability as a power electronic device. In this work, the transfer characteristics of GaN FINFET have been studied for temperatures ranging from 300 to 600 °K. From the result plotted in Fig. 6 it can be concluded that

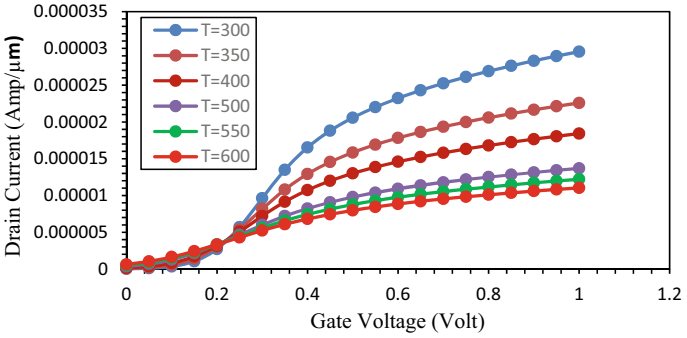

Fig. 6 Temperature variation in transfer characteristics for n-channel (GaN) TG-FinFET

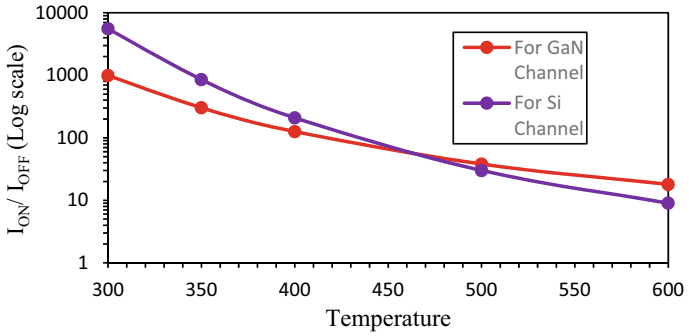

Fig. 7 Variation in I_{ON}/I_{OFF} ratio with temperature for different channel material

with the variation of the temperature the saturation drain current decreases with the increasing temperature. Furthermore, if the ratio of I_{on}/I_{off} is considered, significant phenomena is being noticed. With the increasing temperature, the ratio of I_{on}/I_{off} decreases more sharply in case of silicon channel device compared to GaN channel device. This comparison is plotted in Fig. 7. It may be observed that the sensitivity of I_{on}/I_{off} ratio to temperature is much lower for GaN as compared to Si over the measured temperature range. This indicates the issue of degradation of performance with temperature is much lower for GaN making it a promising candidate for devices with high-power density.

4 Conclusion

A survey of existing scientific reports shows that the existing work on GaN has been limited to HEMT-based devices. The wafer technology of GaN is not mature that coupled with the technologically challenging HEMT structure does not encourage its acceptance as a mass-scale replacement for Si. The objective of this study was to show its suitability as simple field effect device vis-à-vis silicon without taking into consideration the piezoelectric advantage associated with the AlGaN/GaN heterostructure. The SOI n-channel TG-FinFET structure is successfully designed and simulated by the influence of different channel material, lightly doped drain profile, and temperature variation. It has been shown that the GaN channel devices provide a higher ON current and lower threshold voltage though its leakage current and subthreshold performance lag behind silicon. Moreover, the temperature sensitivity of GaN is much lower than Si FinFET indicating its suitability for high-power density devices. Perhaps, the most interesting outcome of this study has been the observation of a significantly enhanced sensitivity of threshold voltage of GaN FINFET to dielectric variation as compared to Si. This has promising implications by way of application as a biosensor. In future, this work will be extended to study the switching performance of such devices as well its sensitivity to variations in structural parameters.

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