A High-Speed CMOS Frontend Readout ASIC for Multi-Channel Muon Detectors

Menka Sukhwani, Vinay B. Chandratre, Megha Thomas, and K. Hari Prasad

Abstract A prototype high-speed frontend readout ASIC, designed in 180 nm CMOS process for tracking and precision time-tagging applications in high energy physics experiments, is presented. This ASIC comprises four readout channels, each consisting of a three-stage voltage amplifier, an on-chip analog cable driver and a comparator with LVDS driver. The amplifier and comparator are AC coupled externally. In this ASIC, potential distribution method (PDM) is used to design the high-speed amplifier, cable driver, and comparator stages. This method has proven to be an efficient way of optimizing the target specifications trade-offs. The ASIC exhibited a total voltage gain of ~ 71 and maximum output swing of ~ 600 mV across 50 Ω load for both the input polarities with power consumption of ~ 20 mW/channel. The timing precision of the overall FEE channel is measured to be ~ 530 ps RMS with comparator overdrive of around three times the threshold voltage.

Keywords Frontend electronics · Resistive plate chamber detector · Potential distribution method

1 Introduction

In high energy physics experiments, large area multi-channel detectors, like resistive plate chamber (RPC) and drift tube detectors, are used for muon trigger generation through event tracking and precision time-tagging. These detectors are also suitable for neutrino studies and muon tomography systems. The Iron Calorimeter (ICAL) experiment of the India-based Neutrino Observatory (INO) will also use ~ 28,800

M. Sukhwani (✉) · V. B. Chandratre · K. Hari Prasad
Bhabha Atomic Research Centre, Mumbai 400085, India
e-mail: menkat@barc.gov.in

Homi Bhabha National Institute, Mumbai 400094, India

M. Thomas
Electronics Corporation of India Limited, Mumbai 400028, India
e-mail: meghathomas@ecil.co.in

J. K. Mandal et al. (eds.), *Topical Drifts in Intelligent Computing*, Lecture Notes in Networks and Systems 426, https://doi.org/10.1007/978-981-19-0745-6_20

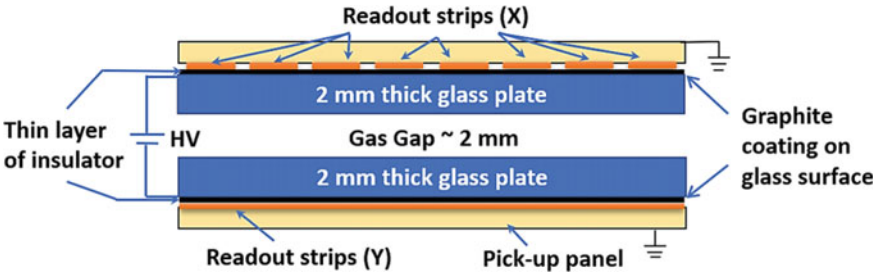

Fig. 1 Schematic representation of the RPC detector

single-gap RPC detectors to study atmospheric muon neutrinos [1]. In this experiment, each RPC detector is of size 2 m × 2 m with 64 X and 64 Y orthogonal readout strips on both sides of the detector, as shown in Fig. 1. Each readout strip exhibits ~ 120 pF capacitance and acts as a strip-line with ~ 50 Ω characteristic impedance.

When a muon particle passes through the gas gap of the RPC detector, it produces charge carriers which move in presence of the applied high electric field. This movement of charge carriers inside the gas gap induces a current signal on the X and Y pick-up strips in opposite polarity. The typical signal of an RPC detector, being operated in the avalanche mode as in the INO-ICAL experiment, has a rise time of ~ 1 − 2 ns with total signal charge in the range of ~ 0.1 pC to a few pC. The measurement requirements of the INO-ICAL experiment involve hit-pattern latching for muon tracking and precision time-tagging of the valid events to identify the direction of incident neutrino.

These detectors require a high-speed, low power, multi-channel amplifier, and leading-edge comparator-based frontend electronics (FEE) to meet the measurement requirements. Furthermore, in the INO-ICAL experiment, access to the amplified detector channels is also required for detector health monitoring, which is not provided in previously reported single-gap RPC FEE solutions [2, 3].

A prototype quad voltage amplifier and leading-edge comparator ASIC is developed in 180 nm CMOS process to meet the novel readout requirements of the single-gap avalanche mode RPC detectors of the INO-ICAL experiment. This FEE ASIC provides an indigenous, low-cost, and low-power solution to cater to the long-term requirements of the experiment. The potential distribution method (PDM) [4, 5] is used for design of the amplifier, cable driver, and comparator stages in this ASIC, which has efficiently allowed optimization of design trade-offs. The detail design aspects and lab test results of the quad FEE ASIC are presented in the following sections.

2 Design of Quad FEE ASIC

The prototype quad FEE ASIC comprises four channels of high-speed amplifier and leading-edge comparator that can be used either individually as stand-alone amplifier and comparator or can be coupled externally to form a complete FEE channel. The external coupling through a bypass capacitor allows a stable overdrive at the comparator input in presence of random DC offset at the amplifier output due to process variations and device mismatch. A single channel configuration of the ASIC is shown in Fig. 2 with details given below.

2.1 High-Speed Amplifier Channel

The amplifier channel is built with three stages of single-ended, closed loop voltage amplifiers with DC offset adjustment provided in the first two stages. These amplifier stages are followed by an on-chip analog 50 Ω cable driver.

The critical design aspect of this FEE ASIC was to obtain the overall amplifier bandwidth of ~ 350 MHz, as required to match the minimum detector signal rise time of ~ 1 ns, while achieving the required gain with minimum power consumption (< 30 mW/FEE channel). In the previous versions of INO-ICAL RPC FEE ASIC [6, 7], designed in 0.35 μm CMOS process, single stage transimpedance, and voltage amplifiers were used to build the amplifier channels. However, in this FEE ASIC, owing to the lower intrinsic transistor gain in 180 nm CMOS process [8], a rail-to-rail two-stage amplifier with class AB output buffer [9], as shown in Fig. 3, is used to implement all the amplifier stages and analog cable driver. The design approach followed for optimum and efficient design of these rail-to-rail amplifier stages is described below.

Design Methodology

Initial design using PDM in open loop DC analysis: In short channel CMOS technologies, the g_m/I_D design methodology is typically followed to optimize the analog

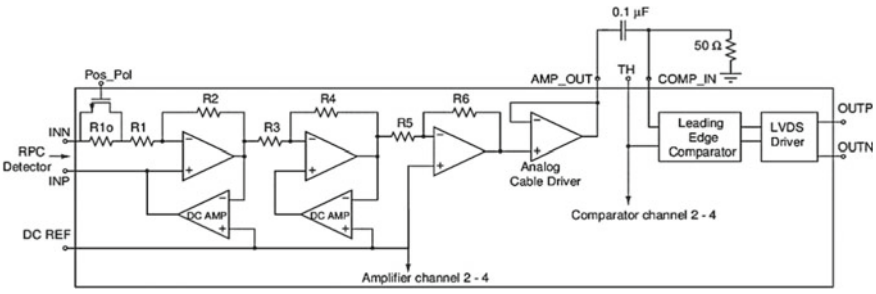

Fig. 2 Single channel schematic of the quad FEE ASIC

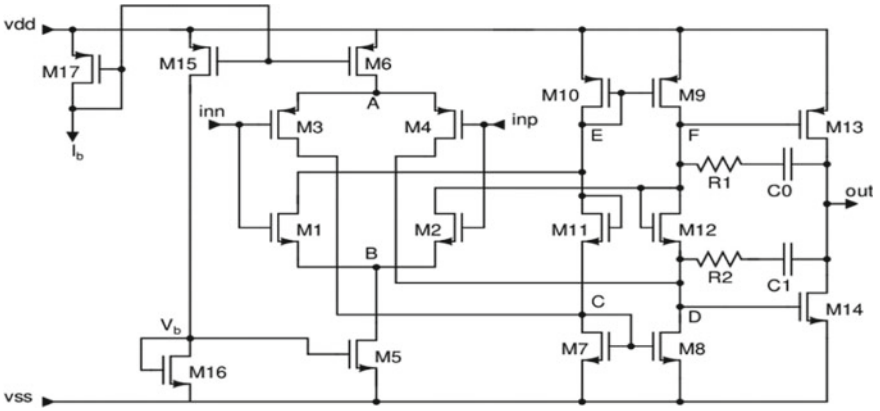

Fig. 3 Schematic of the wide swing amplifier with class AB output stage

designs. However, it was observed that the potential distribution method (PDM) quickly yields the preliminary design through open loop DC analysis and final design can be obtained through minimal optimization iterations. In this method, DC voltage biases at all the amplifier nodes were first estimated based upon following considerations,

(a) Input and output nodes were fixed at $V_{\text{cm}} = \frac{(Vdd-Vss)}{2}$. The bulk of all the transistors were connected to their respective supplies. Further, an overdrive of 5% of (Vdd − Vss), i.e., ~ 90 mV, was considered for all the transistors as in [4, 5], except for output transistors (M13, M14). For these transistors, an additional overdrive of ~ 200 mV was taken to ensure linearity at larger swings.

(b) Gate voltages of the bias transistors (NMOS: M5, M16 and PMOS: M6, M15, M17) were fixed as $V_{GN-\text{Bias}} = Vss + V_{\text{thn}} + 0.05 * (Vdd - Vss)$ and $V_{GP-\text{Bias}} = Vdd - V_{\text{thp}} - 0.05 * (Vdd - Vss)$, respectively.

(c) The common source nodes (A and B) of the input differential pairs were estimated at $V_{SN-\text{Diff}} = V_{\text{cm}} - V'_{\text{thn}} - 0.05 * (Vdd - Vss)$ and $V_{SP-\text{Diff}} = V_{\text{cm}} + V'_{\text{thp}} + 0.05 * (Vdd - Vss)$. Here, V'_{thn} and V'_{thp} represent the threshold voltages of NMOS and PMOS input devices with the given body bias.

(d) The gate and drain nodes (C and E) of diode connected loads were assumed to be at same potential as the output nodes (D and F), respectively, of the input differential pairs. As these nodes (D and F) also form the gate bias of output stage, these were kept at, $V_E = V_F \approx Vdd - V_{\text{thp}} - 0.05 * (Vdd - Vss) - 0.2$ and $V_C = V_D \approx Vss + V_{\text{thn}} + 0.05 * (Vdd - Vss) + 0.2$.

The voltage biases on all the nodes of the amplifier design as determined through above considerations, with Vdd = 0.9 V and Vss = −0.9 V, are given in Table 1.

The bias currents in the input differential pair and output branch can only be finalized based upon the required closed loop 3-dB bandwidth (that determines the amplifier rise time) and stability margins, respectively, in presence of circuit parasitic

Table 1 Node voltages (in V) of amplifier design in Fig. 2 based on PDM

Devices	V_{th}	V_G	V_S	V_D	Devices	V_{th}	V_G	V_S	V_D
M1, M2	0.54	0	0.63	0.1	M3, M4	0.58	0	0.67	−0.13
M5	0.48	−0.33	−0.9	−0.63	M6	0.51	0.3	0.9	0.67
M7, M8	0.48	−0.13	−0.9	−0.13	M9, M10	0.51	0.1	0.9	0.1
M11, M12	0.54	0.1	0.1	−0.13	M13	0.51	0.1	0.9	0
M14	0.48	−0.13	−0.9	0	M15	0.51	0.3	0.9	−0.33
M16	0.48	0.33	0.9	0.63	M17	0.51	0.3	0.9	0.3

while minimizing the power consumption. Initially, these currents were estimated at ~ 100 μA. Then, widths of all the transistors (with L = 0.18 μm) were obtained through DC sweep simulation of single transistor circuit [5] keeping voltage biases at all the terminals as decided previously. Here, a testbench was developed to directly provide the width of the transistor for the given drain current without any graphical analysis, allowing easy iterations. Back annotation of these MOS widths in the amplifier design yielded the designed voltage biases at all the nodes along with the branch currents. The values of miller compensation capacitor and lead compensation resistance were estimated in open loop AC analysis to yield a single-pole response. This base amplifier design exhibited an open loop DC gain of ~ 55 dB with unity gain bandwidth of ~ 2.44 GHz. In the open loop design, the trade-off between the amplifier bandwidth and power consumption can be optimized by careful choice of the bias current.

Design optimization of the closed loop, cascaded amplifiers: Three base amplifiers were DC coupled in closed loop configuration to achieve overall channel gain of ~ 70, as shown in Fig. 2. Now, in order to achieve a rise time of ~ 1 ns, a 3-dB bandwidth of ~ 350 MHz [10] would be required for overall channel. Therefore, closed loop 3-dB bandwidth of each amplifier stage (assuming similar values for all the stages) in the N-stage channel can be estimated as [10],

$$f_{\text{amp}} = \sqrt{N} \times f_{\text{channel}} \tag{1}$$

In this FEE ASIC, the amplifier channel comprises four stages including the analog cable driver, therefore, individual amplifier should have a 3-dB bandwidth of greater than 700 MHz to safely accommodate the post layout parasitic load also. Furthermore, a minimum phase margin of 65° needs to be ensured in closed loop configuration with expected load from the subsequent stages. Therefore, the values of the bias currents, miller compensation capacitors, and lead compensation resistors for each amplifier stage were required to be optimized simultaneously in the closed loop, cascaded configuration to achieve the required stability margins, overall bandwidth, and power consumption. The simulated AC response of all the four stages is shown in Fig. 4.

Analog cable driver: In this FEE design, the analog cable driver consumes the maximum power as it is required to provide a maximum voltage swing of ~ 600 mV

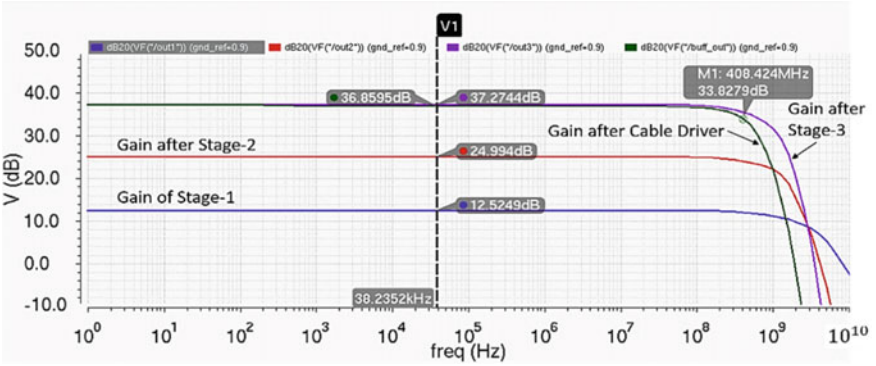

Fig. 4 Simulated AC response of four stages of the amplifier channel

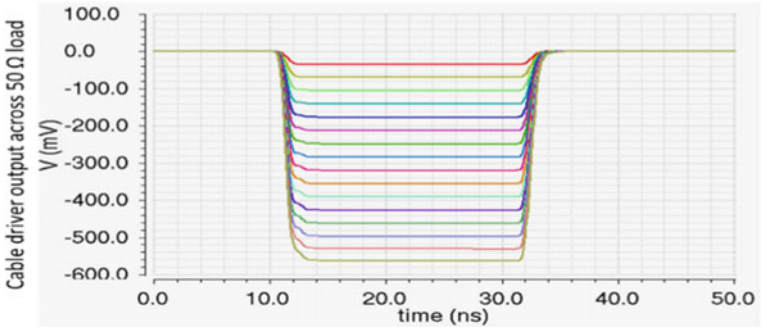

Fig. 5 Simulated transient response of the amplifier channel through analog cable driver across 50 Ω load for input range of 0.5 mV to 8 mV

across external 50 Ω load, as shown in Fig. 5, maintaining the amplifier rise time in presence of parasitic load from two I/O pads and bond wires (amplifier output and comparator input I/Os). Therefore, it was designed to provide only sinking current, i.e., only negative output through NMOS output device leading to lower quiescent power consumption.

However, as the detector provides single-ended complementary outputs from the top and bottom readout channels, the opposite polarity output would require an inversion to obtain negative only output for both the input polarities. A gain trimming option is, therefore, provided in the first amplifier stage in order to equalize the total channel gain in both inverting and non-inverting configurations, as shown in Fig. 2. The analog cable driver was also designed using PDM. The final design details of the amplifier and cable driver stages are given in Table 2.

Table 2 Design details of the amplifier and cable driver stages of the FEE ASIC (L = 0.18 μm)

Devices	Size	Quiescent current	Devices	Size	Quiescent current
M1, M2	5.81 μm	80 μA	M3, M4	18.53 μm	80 μA
M5	16.2 μm	160 μA	M6	50.6 μm	160 μA
M7, M8	1.3 μm	80 μA	M9, M10	3.9 μm	80 μA
M11	0.5 μm	0	M12	0.5 μm	0
M13: Amplifier M13: Cable driver	9.5 μm 20 μm	220 μA 1142 μA	M14: Amplifier M14: Cable driver	3 μm 100 μm	220 μA 1142 μA
M15	17.42 μm	80 μA	M16	7.31 μm	80 μA
M17	21.6 μm	80 μA	C1, C2: Amplifier	45 fF	
R1, R2: Amplifier R1, R2: Driver	5 kΩ 3 kΩ		C1, C2: Driver	120 fF	

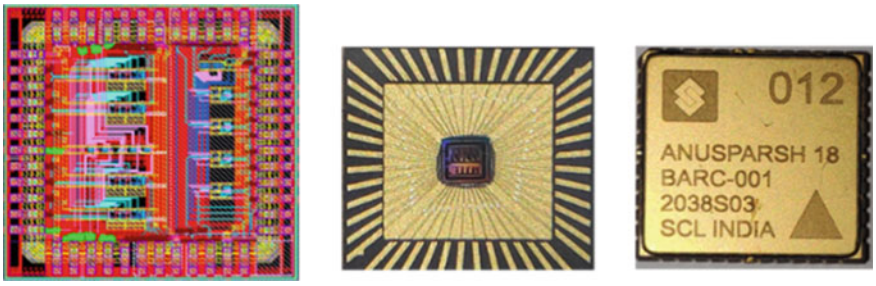

Fig. 6 Die picture of the quad FEE ASIC and packaged ASIC in CLCC-48 package

2.2 Comparator and Layout Design

The design of leading-edge comparator [11] was ported to 180 nm CMOS process using PDM. It comprised a pre-amplifier followed by cross-coupled latch and output buffer. An on-chip LVDS driver [12] provided the comparator output on external 100 Ω load. The layout of the FEE ASIC was designed in full custom manner, occupying an area of 2 mm × 2 mm. The ASIC is packaged in CLCC-48 package, as shown in Fig. 6.

3 Experimental Results

The quad FEE ASIC is tested in the laboratory for amplifier gain and linearity along with LVDS output compatibility with the standard receiver and timing precision. The amplifier output, for an input voltage pulse of amplitude ~ 5 mV and rise time ~2.2 ns, is shown in Fig. 7a. The voltage gain of the amplifier channel was measured

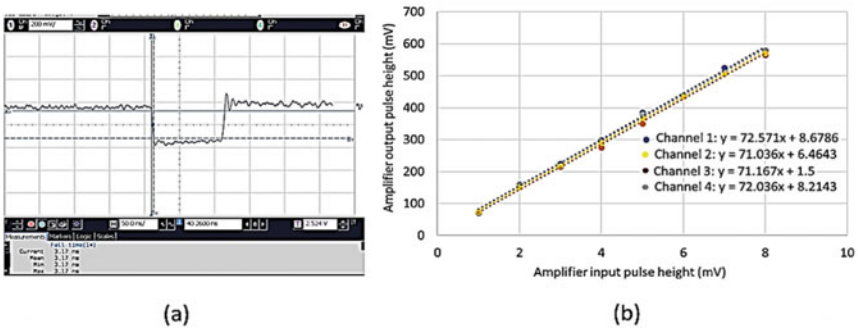

Fig. 7 Experimental results **a** amplifier output profile, **b** transfer characteristics of the four amplifier channels

to be ~ 71, as obtained from its transfer characteristics shown in Fig. 7b. The values of the miller compensation capacitors and lead compensation resistors that were finalized in the closed loop, cascaded configuration considering the actual on-board parasitic, were found to be optimum as amplifier output exhibited good transient stability without significant overshoots and ringing.

The comparator LVDS output was acquired by an FPGA TDC-based data acquisition module, and timing precision was measured by plotting the LVDS width spectrum for comparator overdrive of around three times the threshold voltage (~ 50 mV). The comparator exhibited an intrinsic time precision of ~ 50 ps RMS and time precision of the entire FEE channel, including the amplifier and comparator, was measured to be ~ 530 ps RMS, as shown in Fig. 8a and b, respectively. The power consumption of the FEE ASIC was measured to be ~ 20 mW/channel.

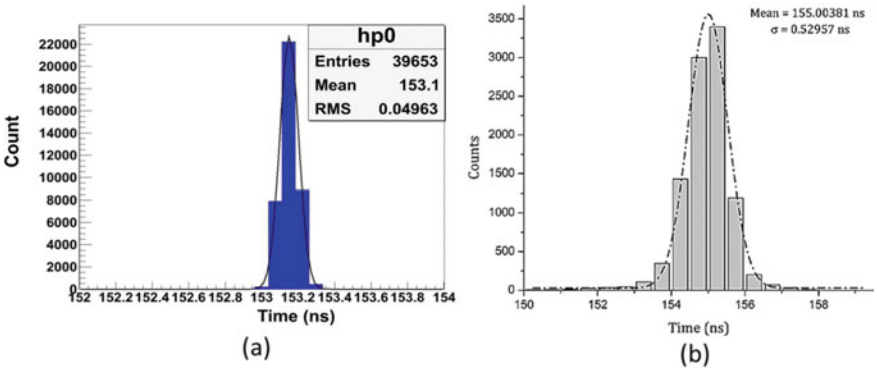

Fig. 8 LVDS pulse width spectrum for **a** intrinsic time precision of the comparator, **b** for time precision measurement of the overall FEE channel including amplifier and comparator

4 Conclusion

A prototype quad FEE ASIC is developed, in 180 nm CMOS process, for readout of large area, multi-channel muon detectors like RPC and drift tube detectors. The ASIC comprises four independent channels of high-speed amplifiers and comparators that are coupled externally. The amplifier and comparator stages were efficiently designed using potential distribution method (PDM). This method quickly leads to an initial design and allows easy iterations of the bias currents and respective MOS aspect ratios to achieve the required specifications. The FEE ASIC has achieved the desired specifications with amplifier channel voltage gain of ~ 71 and overall timing precision of ~ 530 ps RMS with power consumption of ~ 20 mW/channel.

References

1. Kumar A et al (2017) Physics potential of the ICAL detector at the India-based Neutrino observatory (INO). Pramana—J Phys 88:79
2. Manen S, et al (2013) FEERIC, a very-front-end ASIC for the ALICE muon trigger resistive plate chambers. In IEEE nuclear science symposium and medical imaging conference. Seoul, pp 1–4
3. Abbrescia M et al (2000) New developments on front-end electronics for the CMS resistive plate chambers. Nucl Instr Meth A 456:143–149
4. Todani R, Mal AK (2012) Design of CMOS opamp using potential distribution method. In: 2012 IEEE international conference on circuits and systems (ICCAS). Kuala Lumpur, Malaysia, pp 184–189
5. Ghosh NN, Todani R, Chaudhuri C, Mal AK (2013) Simplified design method for fully differential gain-boosted folded cascade OTA. In: 2013 IEEE conference on information and communication technologies. Thuckalay, India, pp 943–948
6. Sukhwani M et al (2013) Regulated cascode preamplifier-based front-end readout ASIC "ANUSPARSH" for resistive plate chamber detector. In: Proceedings of international conference on VLSI, communication, advanced devices, signals and systems and networking (VCASAN-2013). Bangalore, India, pp 71–77
7. Chandratre VB, et al (2015) ANUSPARSH-II frontend ASIC for avalanche mode of RPC detector using regulated cascode trans-impedance amplifier. In: Proceedings of the DAE-BRNS symposium on nuclear physics 60. Mumbai, India, pp 928–929
8. Murmann B, Boser BE (2004) Digitally assisted pipeline ADCs: theory and implementation. Springer, US
9. Atkin EV, Vinogradov SM (2017) Approach to the design of monitoring buffer for read-out ASICs. J Phys: Conf Ser 798
10. Hollister AL (2007) Wideband amplifier design. SciTech Publishing Inc
11. Sukhwani M et al (2020) A high speed BiCMOS comparator ASIC with voltage adjustable hysteresis. Nuclear Inst Methods Phys Res A 980:164503
12. Tajalli YA (2009) A power-efficient LVDS driver circuit in 0.18um CMOS technology. IEEE J Solid-State Circ 44(2):538–548