# Memristor Emulator Circuits an Emerging Technology with Applications



Jyoti Garg, Aishita Verma, and Subodh Wairya

Abstract In this paper, the fourth fundamental passive circuit element called memristor has been discussed along with models, emulator circuits, characteristics, and applications in different engineering areas. Memristors are able to hold the information about net amount of charge gone through it. Memristors are also compatible with the CMOS fabrication process and enable hybrid CMOS/Nanodevices integration, which imports that this device can be used in various applications. Memristor has a wide application in memory logic design, where memristor acts as a building block. Other applications of memristor include Nanocomputing, Neuromorphic circuits, and digital computation, which includes implication logic. This review imitates a compendious elucidation of memristor, in addition to future scope in a proper manner.

**Keywords** Memristor model · Characteristics · Emulator circuits · Engineering application

# 1 Introduction

In 1971, Prof. Leon Chua perceived that existed no entity relating magnetic flux and electric charge [1]. The resistor capacitor and inductor are passive elements as they need no internal power source to operate, and as their behavior cannot be mimicked by other basic passive elements. Prof. Leon Chua realized that out of six relations only five had been recognized. Based on these simple symmetry arguments, the Prof. proposed the memristor to complete the missing link. Therefore, a prediction was made based on criteria of symmetry that there should be another element of circuit and named this hypothetical element, "memristor." Till 1971, circuit theory was ruled

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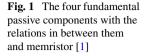
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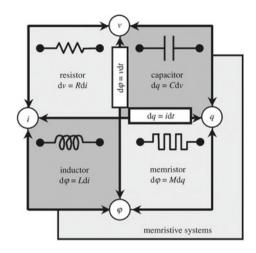
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by three fundamental circuit elements, resistor which relates Voltage and Current (dv = R.di) where R is the Resistance, Capacitor-Relates Voltage and Charge (dq = R.di)(C.dv) where C is the Capacitance, and Inductor-Relates Current and Magnetic Flux  $(d\Phi = L.di)$  where L is the Inductance. Memristor relates Charge and Magnetic flux  $(d\Phi = M dO)$  where M is the memristance. Figure 1 shows the fourth fundamental passive element with resistor, inductor, and capacitor. Memristors have important characteristics, which are current voltage, flux charge, etc. A memristor represents an increasing or decreasing function of monotonic nature as shown in Fig. 3a-c. The tangent of the  $\Phi - O$  curve grants memristance of a memristor. On increasing the frequency pinched hysteresis loop shrinks and at very large input frequencies, the linear resistance behavior of the device is observed. If the hysteresis curve is pinched, then it is a memristor; if the curve is not pinched, then it is not a memristor. Characteristic curve is shown in Fig. 2. If flux and charge is defined in terms of charge, then term is coined as charge-controlled memristor and when in expressed as function of function flux it is a flux-controlled memristor. It is known as charge-controlled flux, and  $\varphi$  is expressed as a function of the charge,

$$\varphi = f(q) \tag{1}$$

The voltage across the charge-controlled memristor is expressed as

$$v(t) = M(q(t)).i(t)$$
<sup>(2)</sup>

M is called as the memristance/resistance of the memristor.

It is called as flux or voltage-controlled if the charge (q) can be expressed as a single valued function of the flux  $(\varphi)$ , i.e.,

$$q = f(\varphi) \tag{3}$$

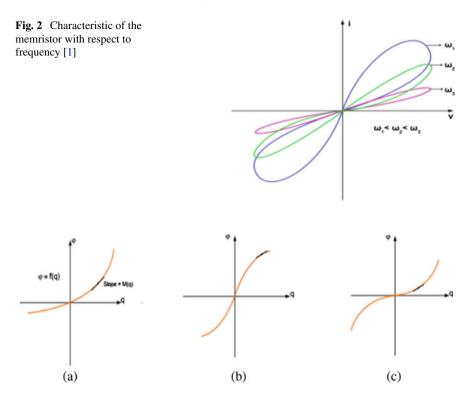


Fig. 3 a-c are monotonically increasing charge-flux characteristics of memristor [2]

Similarly, current across the flux or voltage-controlled is given as:

$$i(t) = W(\varphi(t)).v(t) \tag{4}$$

$$W(\varphi(t)) = \frac{\mathrm{d}q(\varphi)}{\mathrm{d}\varphi} \tag{5}$$

The unit of memristance of the memristor is the same as the resistance unit, and memconductance unit is the same as the conductance unit. In particular, a description of the first memristor, manufactured at HP Laboratories, is presented in memristor model. This paper is explained in detail followed by the respective sections. Section 2 gives a brief description of memristor emulator circuit and memristor models. Section 3 gives the research review of memristor emulator circuits, Section 4 gives the brief of Memristor Applications, and Conclusion and Future scope are discussed in Sect. 5, respectively.

The dissipation of power by the memristor is given by Eq. 6, and since  $M(q) \ge 0$ , the power has a positive value (Fig. 3).

$$P(i) = M(q)i((t))^{2}$$
(6)

## 2 Memristor Emulator Circuit and Memristor Models

The memristors are commercially inaccessible, few circuit which perform as memristors are obligatory to develop application circuits and these must have some important characteristics like memristors. The memristance should be capable of being programmed, devoid of volatility, and connected to different circuit elements [3]. The memristor emulator circuit response is always limited to first and third quadrants, which indicate that the device is passive. The response always crosses the origin, which means that once the input signal is removed from the device, the output always falls to zero. In order to obtain, analyze, and simulate memristor-based circuits, appropriate model is mandatory. The HP Lab for the first time presented a brief on memristor implementation, and also models for various applications were been discussed. Figure 4 shows the HP memristor and its implementation where there is a doped and undoped side and a TiO<sub>2</sub> layer between two platinum electrodes. The voltage has been applied at the platinum contacts, respectively, and the characteristics are obtained. Other models of memristors are discussed in detail.

#### 2.1 Linear Ion Drift Model

This model was presented by HP, based on the physical dimensions of the device. It is presumed that the physical device of width D had a couple of regions where one side is doped with oxygen ions having a positive charge and the other side is not doped. The modeling of the regions has been done using a resistor. The region which is doped has width w resulting in lower resistance and is more conductive, and the region that is not doped retains resistance of higher value. Figure 5 shows the HP memristor model. This model's advantages are its simplicity and easy to analyze, but the demerit of this model is the lowest accuracy.

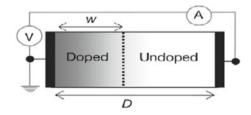
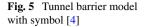
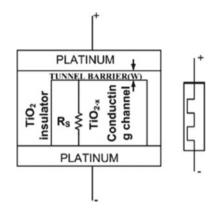


Fig. 4 HP memristor [2]





#### 2.2 Nonlinear Ion Drift Model

A memristor that is voltage controlled is presumed in the nonlinear ion drift model, which has nonlinear dependency interjacent the voltage and internal state derivative [4]. The linear drift model has the lowest accuracy; hence, another model called nonlinear ion drift model was developed. It was noted that the comportment of memristors were nonlinear, and the linear ion drift model had lower accuracy, so there was a need to develop this model. For some of the significant applications, nonlinear characteristics are needed, which can be achieved by this model.

## 2.3 Simmons Tunnel Barrier Model

Pickett et al. presented an exact model of the memristor. This model worked as a substitute of two resistors in series, and a resistor is in series with an electron tunnel barrier, as shown in Fig. 5. It has been insisted that it is the more definite model of memristor; however, in terms of complexity, this model is more intricate as compared to other existing models, and this model also consists of complex equations to study the memristor characteristics. This model is not pertinent to different types of memristors and only fits a specific type of memristor [5]. Figure 5 is the schematic of the memristor model with its symbol. The titanium dioxide TiO<sub>2</sub> is in between two platinum (Pt) electrodes, and a tunnel barrier is placed along withTiO<sub>2-X</sub>, which is a conductant.

#### 2.4 Threshold Adaptive Memristor Model (TEAM)

The TEAM model, proposed by Kvatinsky et al., is the elementary model. This model has simple expressions to study the memristor characteristics. The model could be fitted to any of the actual memristor models, such as the linear ion drift model [6]. The above model can be pertained to different memristor models and also to the above-discussed memristor model. The TEAM model is precise enough with a mean error of 0.2% and improved simulation by approximately 47.5%. It justifies sufficient efficiency needed for simulation engines and also essentials for the memristor-based applications.

## 3 Research Review

The Concept of Memristor by L. O. Chua, "Memristor-The Missing Circuit Element" hypothesized based on relations among the four prominent circuit elements and symmetry, there should be another circuit element to complete missing link, whose resistance was not constant it can depend on one or more basic differential equations. In fact, a symbol was presented along with three fundamental circuit realizations [1]. In 2012, memristor emulator for memristor circuit applications was proposed which shows the behavior of a TiO memristor and also this emulator can be connected in serial, in parallel, or in hybrid. The most significant drawback is the memristive behavior [2] was only seen at some particular frequencies 100 Hz and also more number of component were used which increased chip area. In [3], another memristor emulator circuit was proposed with simple dimensionless expression models double-loop behavior, and this memristor emulator circuit was proposed couple of current conveyor (CCII) devices, voltage multiplier, and noninverting or inverting buffer (using Op-amp). Simultaneously, they also proposed two emulator circuits, for the current-controlled memristor and for the voltagecontrolled memristor, but more number of active elements were used, which resulted in increased power dissipation and the device area [7]. A memristor emulator circuit comprising DDCC (differential difference current conveyor) based on CMOS was presented, this emulator was quite less complex as comparable to the other designed emulator circuits and it consisted 1-DDCC, 2-resistors, 1-capacitor, and 1-multiplier circuit, but the single DDCC circuit consists of a high number of transistors and also this emulator cannot be controlled tuned electronically. The authors in research article [8] have addressed an emulator circuit consisting of 2-CCII+s, 1-multiplier, 2-resistors, 1-capacitor, and a switch. A behavioral model of the emulator circuit has been analyzed in this work. It was concluded that this emulator was much more improved over the existing emulator, but this circuit requires more passive elements [9]. The emulator circuit comprises three operational transconductance amplifiers (OTA) and four second-generation current conveyors (CCII), six resistors, and one capacitor element for the emulator circuit. Since this circuit consists

of OTA, which has low output impedance, so the gain was less [10]. In this, the emulator circuit was designed with CCII+, a four-quadrant analog multiplier, capacitor, resistor, and two DC voltage sources, and also the derivation of memductance of the proposed memristor emulator circuit was done with the equations but since this design consisted of more active elements, there was much power dissipation. Hence, an emulator circuit with less transistors counts should be designed to reduce its chip area and power dissipation [11]. Memristor emulator consists of only four MOS transistors. This circuit is convenient both for emulating the fabricated memristor and also for some applications of memristor. This circuit did not consist of a circuit block as multiplier or an active element to obtain memristive characteristics. The analysis was done at a different temperature and also on different voltages. The chip area was also reduced since this design consisted of a significantly less number of MOS transistors, the layout area was also reduced as compared to other existing emulator circuits, also this design did not consist of active elements and the power dissipation was also less as compared to other circuits of memristor emulator. However, [12] proposed meminductor models that can be used in wide applications consist of only two active voltage differencing transconductance amplifier (VDTA) and grounded capacitors. The meminductor emulator circuit depicts broad operating frequency range clarity, and also, this circuit was congruent for memristor applications [13]. This memristor emulator circuit consists of a second-generation current conveyor CCII and OTA as active elements besides few passive elements. This circuit is compatible with both CMOS realizations and breadboard implementations. The circuit resembles a comprehensible design of an ideal memristor and also functional verification of circuit is realized with 0.18- $\mu$ m CMOS technology and voltage of  $\pm 1.2$  V. In [4], emulator circuits presented could be used for the implementation of several analog circuits, as it can operate to the 26.3-MHz frequency in which designing was done with CMOS technology and consisted of a single resistor and capacitor as passive elements. In addition to this, the designing of the emulator circuit [14] was done from BJT-based ICs and performed up to 1.7 MHz and can be used in many applications efficiently.

# 4 Applications of Memristor

Memristor has wide applications in digital and analog designing [15]. Their division is based on how the memristance of the device is utilized. In digital applications, only a discrete number of resistance states is used, while in analog applications, the complete resistance changes between the minimum and the maximum values. Memristor has several applications in different discipline of engineering, including neuromorphic application, chaos circuits, image processing, neural networks, memories, etc. Apart this, hybrid memory circuit can be designed as can see in Fig. 6. Some significant memristor applications are discussed in detail in following section.

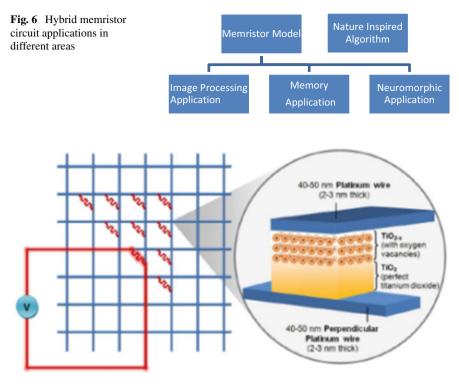


Fig. 7 Crossbar structure [17]

# 4.1 Crossbar

Crossbar structures are versatile nanostructures that consist of many switches in nanoscale. These are scalable as well as flexible. Crossbar grids can be used in many applications such as digital circuits and memories [16]. These switches have a grid of nanowires consisting of vertical wires which are intersected, which is a memristor switch. Junction size is about 2–3 nm. Nanoimprint lithography (NIL) is a method for fabricating nanowires. The fabrication method used for crossbar nanowires is simpler, is cheaper, and has a higher resolution. Figure 7 shows the memristor's crossbar structure, and Fig. 8 shows the mapping of the NOR gate.

# 4.2 Hybrid Chip

The hybrid chip consists of an amalgamation of transistors and memristors [19]. It has a single layer of transistors to operate memristor layers effectively. This entire structure is power-efficient and intakes less energy, resulting in less heat generation.

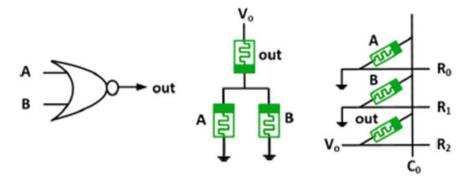


Fig. 8 Mapping NOR gate to crossbar column [18]

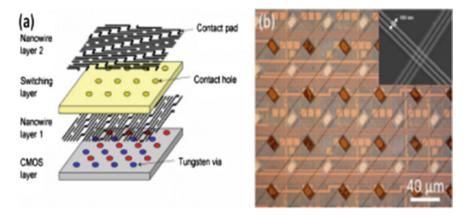


Fig. 9 Memristor reconfigurable hybrid chip

There is a CMOS Layer at the bottom, and above the CMOS layer, there is nanolayer1, and the switching layer exists in between the nanolayer1 and nanolayer2 as shown in Fig. 9.

## 4.3 IMPLY Logic Gate and Memristor-Aided Logic (MAGIC)

A cluster of memristors can be used to realize Boolean logic because memristors are passive elements. Some of these approaches are Wired AND logic and implication logic [20]. The best approach is implication logic which uses the implication operator because it can implement all the Boolean functions [21]. IMPLY function is one of the elementary 2 input Boolean functions. The schematic of the memristor-based IMPLY is shown in Fig. 10. The IMPLY logic gate is based on one resistor  $R_G$  connected to two memristors from memory crossbar array p and q. The resistance of

**Fig. 10** Memristor-based IMPLY gate [14]

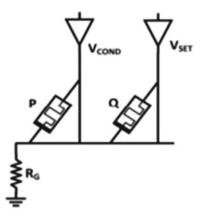
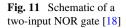
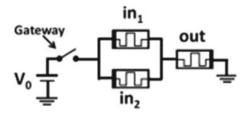


Table 1         Truth table of           IMPLY function [18]	р	q	pIMPq
	0	0	1
	0	1	1
	1	0	0
	1	1	1

 $R_{\rm G}$  has a value between the minimum and maximum resistances of memristor  $R_{\rm on}$ and  $R_{\rm off}$ , and the memristor p and q are the input of logic gate, the memristor q is also the output of logic gate as its initial value is the input of logic gate, and its value after computation is the output of the logic gate. The essential operation is to apply two different voltages,  $V_{\rm SET}$  and  $V_{\rm COND}$ , to the memristors where the magnitude of voltage  $V_{\rm SET}$  is higher than the magnitude of voltage  $V_{\rm COND}$ . Table 1 illustrates the IMPLY function, and a schematic of memristor-based IMPLY is shown in Fig. 10.

Implementing NAND gate with the IMPLY logic requires three computational steps, so three clock cycles will be required but if a more complex function e.g., a 1-bit full adder is to be implemented with IMPLY logic, then with Naive approach it will require 89 computation steps but with the parallel approach it will require only 5 computational steps. There is a need for refresh because of drift in IMPLY logic, whereas MAGIC-Memristor-Aided LOGIC consists of one applied voltage  $V_G$  in the gateway of logic gate and the separate input and output memristors, unlike IMPLY logic gate. The NOR schematics are shown in Fig. 11. It contains two inputs with separate outputs. In the first phase, there is a need to commence the output memristors to logical 1, and applied voltage causes current to flow from left to right. MAGIC NOR is good for logic inside memory and is easy and intuitive.





#### 4.4 Neuromorphic Computing

In the analog domain, memristors can be used to enable new unconventional applications, and the most exciting applications are large-scale Neuromophic circuits [22]. Artificial neural networks are implemented in the hardware mimicking functionalities of the human brain. The synapse in our brain initiates the learning, and it dictates how strong the connection in the middle of two neurons is and how a signal propagates from neuron one to two. Depending how frequently neuron1 sends signal to neuron2 to readjust its weight is according to nonlinear function. Memristor is placed in the middle of the pre-neuron and post-neuron, and synaptic weight crossbar of the memristor is created. Figure 12 depicts an illustration of two neurons and their connection.

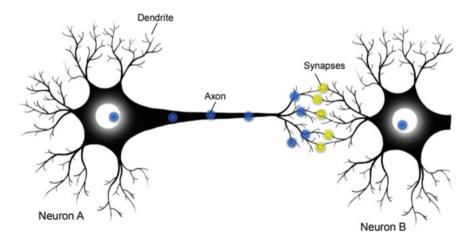


Fig. 12 An illustration of two neurons and their connection [22]

	Traditional memory			Emerging technology		
	DRAM	SRAM	Flash	FeRAM	MRAM	Memristor
Cell element	ITIC	6 T	1 T	1T1C	1T1R	1D1T1R
Feature size (nm)	36–45	45	22	180	65	20
Read time (ns)	2-10	0.2	100	45	35	<50
Write time (ns)	2-10	0.2	106	65	35	0.3
Retention time	4–64 ms	NA	10 yr	10 yr	>10 yr	>10 yr

 Table 2
 Comparison of memristor with other memory

## 4.5 Non-Volatile Memory

Memristor device has many advantages: compatibility with CMOS, low power consumption, no leakage current, high scalability, nonvolatility, fast access time, high retention time, and high switching speed. Due to these properties, it has a wide application in memory circuit designing, low power designing. The memristor device has a unique feature that its memristance can be varied in a very effective controlled way by only changing biasing. Memristor has been compared with other memories, as can see in Table 2 [23].

## 5 Conclusion

The literature review of memristors, characteristics, various models, and emulator circuits have been discussed. Different emulator circuits are feasible for several applications such as digital circuits, analog circuits, neural networks, and neuromorphic computing. Future works include memristor modeling and neuromorphic applications, pattern recognition, and ternary logic gates; hence, there is a requirement of a definite model for circuit analysis and simulation to suggest more radical applications of memristors. Memristors can offer promising higher capacities when used in applications of memory or hybrid memory circuits. The expedience of memristors over other memories is the non-volatile property of memristors which can be used effectively in memories; hence, more research is being conducted. Finally, it can be concluded the need to develop memristor emulator circuits in order to discover many more application areas with fast computation and less power dissipation.

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