Chapter 21
SiP Simulation and Verification

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21.1 Overview of SiP Simulation and Verification

With the rapid development of SiP and Advanced Packaging technology, the complexity of design is increasing. The main manifestation is that there are more and more layers of the substrate, and more and more chips and passive components are integrated on the substrate. The bare IC chips are becoming more and more complex, the number of pins is increasing, and the working frequency is also improving. At the same time, the density of routing on substrate is also increasing, and the signal frequency transmitted is also enhancing rapidly. In addition, the use of multiple substrates within a package is becoming more common.

With the improvement of chip performance and design complexity, the problem of high-speed circuit becomes more and more prominent, which directly affects the performance and reliability of SiP system. Without simulation, directly designed systems usually do not meet the design requirements. For example, the designed SiP can only work at lower clock frequencies than specifications. Strict screening of the chip is required for system to work properly, sometimes even rework the design several times.

To solve these problems, advanced SiP design platforms are needed, strict SiP design processes and specifications are formulated, and the experience of engineers is relied on for circuit design and problem investigation.

At present, the experience of engineers in SiP and Advanced Packaging design is far from comparable to that in PCB design. Because PCB design technology has been relatively mature for many years, SiP and Advanced Packaging design have only become popular in recent years. The lack of design experience requires designers to learn more from various simulation tools to ensure the success of the design.

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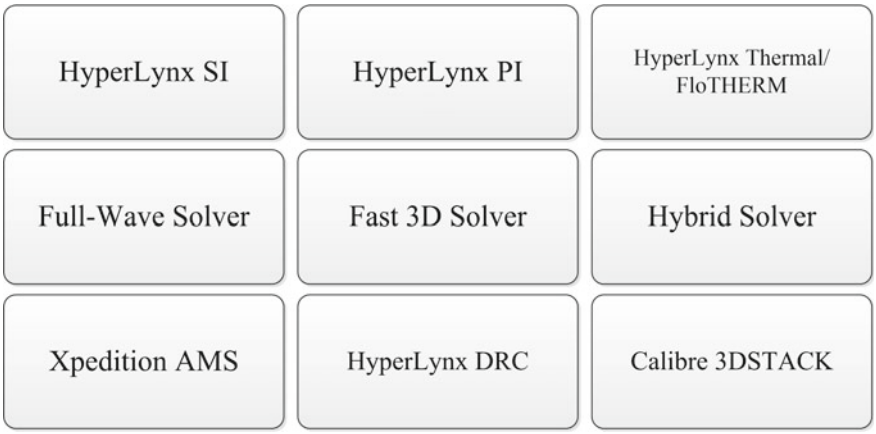

Fig. 21.1 SiP and advanced packaging simulation and verification tools

Therefore, after a SiP design is completed, simulation is an essential means to ensure that the design version is as successful as possible. The simulation ensures that the product has good signal integrity, power integrity, good heat dissipation, and meets various requirements of electromagnetic compatibility.

In Chap. 6 of this book, we have known that the simulation tools provided by Siemens EDA (Mentor) cover three aspects: Electromagnetic, Thermal and Force. Among them, the electromagnetic and thermal aspects are more comprehensive, and the force simulation needs to be further improved. Here we will focus on the electromagnetic and thermal simulation. In addition, Siemens EDA also provides electrical verification and Advanced Packaging physical verification tools, which we will describe accordingly. Figure 21.1 provides the SiP simulation and verification tools.

For SiP simulation needs, Siemens EDA offers HyperLynx SI for signal integrity simulation, HyperLynx PI for power integrity simulation, HyperLynx Thermal and FloTHERM for SiP thermal analysis. Because SiP differs from PCB in that it is integrated in a variety of ways (see Chaps. 4 and 6 for more details), there are different requirements for simulation tools. For non-planar integration, a 3D solver is required to analyze the nets and extract the corresponding parameters. Siemens EDA provides advanced 3D solvers, including Full-Wave Solver, Fast 3D Solver, Hybrid Solver, which can solve these problems. In the schematic design phase, Siemens EDA provides Xpedition AMS for digital-analog hybrid circuit simulation, which can be directly emulated in the schematic environment based on Designer. In addition to simulation tools, Siemens EDA also provides validation tools, including HyperLynx DRC, an electrical verification tool, and Calibre 3DSTACK, an Advanced Packaging physical verification tool.

Limited to length, some tools are described in more detail, and their simulation methods are illustrated with examples. Some tools are only briefly described their functions.

21.2 Signal Integrity Simulation

Signal integrity refers to the waveform quality of the signal at the receiver, sender and transmission path, which is mainly manifested in such aspects as delay, reflection, crosstalk, time sequence, oscillation, etc.

With the increasing frequency of signal, the problem of signal integrity becomes more prominent. The frequency and characteristics of bare chip, the physical parameters of the substrate, the layout of the chip on the substrate, and the routing of high-speed signals all probably cause the signal integrity problems, which lead to the instability of the system operation and ultimately the system design failure. Taking full account of signal integrity factors and taking effective control measures will effectively improve the signal integrity problems in SiP design.

21.2.1 Introduction to HyperLynx SI

HyperLynx SI is a widely used simulation tool for signal integrity of high-speed circuits. Including pre-simulation environment (LineSim), post-simulation environment (BoardSim) and multi-layout analysis functions, embedded DDRx and SerDes analysis wizard, can help designers to simulate signal integrity, crosstalk, DDRx and SerDes analysis and validation, eliminate design hazards, and improve the success rate of design.

HyperLynx SI is widely compatible with layout design files from many manufacturers, such as Siemens EDA, Cadence, etc. From net topology planning, impedance design, high-speed rule definition and optimization at the beginning of the design, to final layout validation can be completed in HyperLynx SI. Figure 21.2 show the HyperLynx SI simulation screenshot.

(1) Pre-simulation LineSim

Pre-simulation LineSim can analyze the "What-If" hypothesis of the high-speed signal in the schematic diagram before layout and routing, inspect the signal transmission effect under the virtual layer stackup and routing parameters, and help the designer optimize a set of layout layer stackup, routing impedance and high-speed design rules suitable for the current design.

LineSim can automatically connect with the schematic design tool Designer and import the topological structure model of the key nets in the schematic diagram. By investigating the overimpulse/underimpulse, delay, crosstalk and other indicators, it can verify whether the assumptions in the process of SiP product design are reasonable. A set of constraints, such as layer stackup, topology and routing parameters, suitable for such critical nets is obtained by simulation debugging. These constraints can be passed back by LineSim to Designer to form routing rules, which can be transferred to the Xpedition layout design environment to implement rule-driven routing.

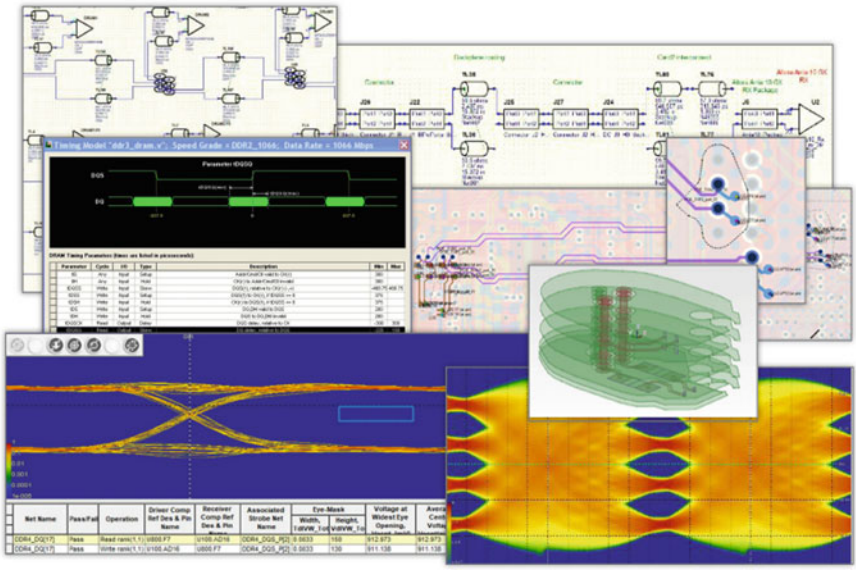

Fig. 21.2 HyperLynx SI simulation screenshot

(2) Post-simulation BoardSim

Post-simulation BoardSim can import Xpedition layout design files, extract layer stackup and physical parameters, calculate transmission line characteristic impedance, and conduct signal integrity, crosstalk and electromagnetic compatibility analysis.

BoardSim can perform interactive simulation analysis on a single net to output accurate signal transmission waveforms or signal eye maps. Designers can modify various matching, passive element parameters and other information of the net in BoardSim.

BoardSim also has Batch Simulation capabilities to quickly scan all nets in the layout, discover nets with overshoots, delays, crosstalk and EMI radiation that exceed design requirements, and give detailed analysis reports.

(3) Multi-Layout Analysis Function

The multi-layout analysis function can analyze the signal integrity of a system consisting of multiple SiP layouts, as well as provide practical solutions to the more popular Advanced Packaging systems that contain multiple substrates in a single SiP (such as Interposer + Substrate). The multi-layout analysis function is also applicable for the user to place the designed SiP in the PCB system for co-simulation. Through multi-layout analysis, the transmission effect of key nets on multiple layouts is examined to help designers quantify the impact of cross-substrate transmission on signal working status.

(4) DDRx and SerDes simulation capabilities

The DDRx wizard guides designers through step-by-step analysis of the signal integrity and timing of the entire DDR interface, supporting a variety of DDR, LPDDR, and NV-DDR technologies. Designers can use parameter scan analysis to determine the best ODT settings, support JEDEC standard parameterized modeling of DRAM controllers, and output reports provide simulation results such as design margins, eye maps, and measured waveforms.

The SerDes wizard supports over thirty different standard protocols, including Ethernet, OIF-CEI, PCIe, Fiber Channel, USB, and JESD based technologies, a built-in COM/JCOM analysis engine, full support for IBIS-AMI models, integration of dedicated 3D EM solvers, and the creation of parameterized 3D via models and PCB cross-section models of any structure.

(5) Model Output Function

HyperLynx SI supports S-Parameter, SPICE model output function, which outputs the nets on the layout, including vias, transmission lines, IC pins, matching circuits, etc., to S-Parameters or SPICE format simulation models.

HyperLynx SI is compatible with simulation models of many formats, such as IBIS, SPICE, S-Parameter, etc. HyperLynx SI provides powerful IBIS model library support for high-speed simulation, including IC models for standard processes such as CMOS/TTL, CPU/DSP, and IBIS models for devices such as FPGA/CPLD.In addition to the powerful model library support, HyperLynx provides a model creation wizard. Designers can create simple MOD simulation models or IBIS models in standard format by simply entering information such as switch time, parasitic parameters, process type of component pins.

21.2.2 Signal Integrity Simulation Example

The following is a brief introduction to the HyperLynx SI simulation process with a SiP design example.

1. Design Data Transfer

Figure 21.3 show a 3D screenshot of a Dual-SoC SiP layout consisting of two SoCs designed in Xpedition. From the Xpedition menu, select Analysis_Export to HyperLynx SI/PI/Thermal, and the system automatically transfers data to the HyperLynx SI/PI/Thermal environment and opens HyperLynx.

In HyperLynx SI, Dual-SoC SiP designs can be automatically imported as shown in Fig. 21.4.

2. SI Simulation of Key Signals

First, the SI simulation of key signals is performed. Click the Select Nets button  in the toolbar of the HyperLynx SI simulation window, and in the Select Net by Name window that pops up, select the key signal that needs to be simulated. HyperLynx supports simultaneous simulation of multiple critical signal nets. The software has

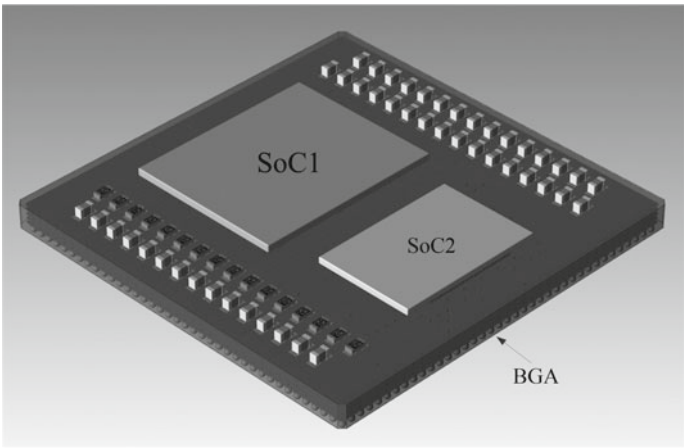

Fig. 21.3 3D screenshot of SiP layout design in Xpedition

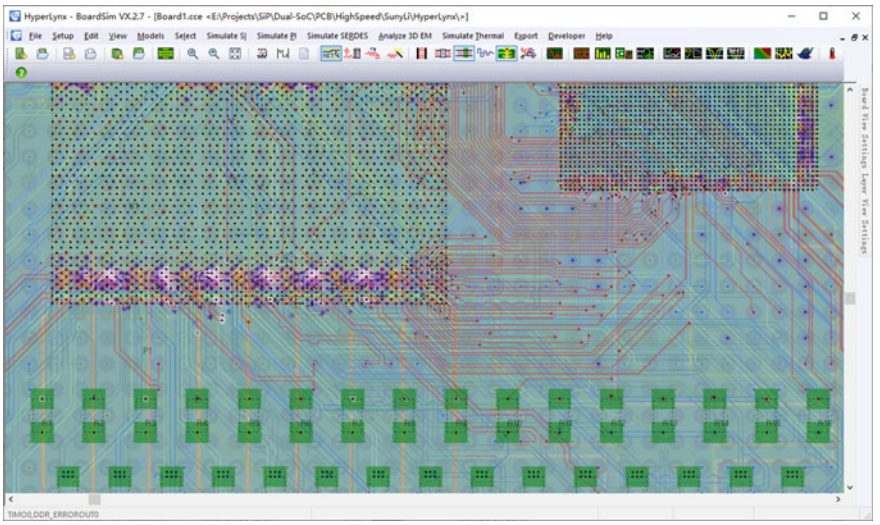

Fig. 21.4 SiP design imported into HyperLynx

no limit on the number of simultaneous simulation nets, but choosing too many nets will affect the simulation speed. In this example, we choose HSPEED_IO4 ~ HSPEED_IO7 four nets, as shown in Fig. 21.5.

After selecting the net, except HSPEED_IO4~HSPEED_Outside IO7 net, other nets are faded. Then click the Assign Models button in the toolbar, click the Select button in the pop-up model specifying window, and pop-up the Select IC model window to select the model for the chip. Note that before choosing a model,

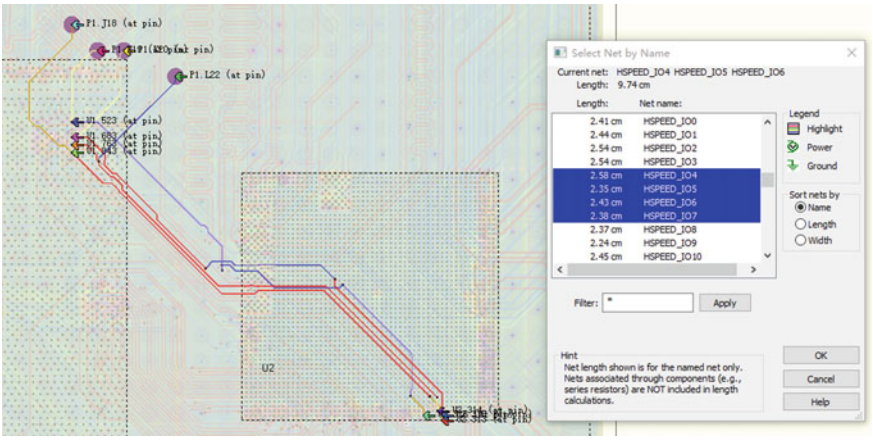

Fig. 21.5 Select the critical signal nets to simulate

if you download it from the website yourself, you can add the model path to the Directories list through the Models → Edit Model Library Paths.

Select Model SiP_SoC1.ibs for U1, and select the corresponding Signal D3\D4\D5\D6 one by one. Select Model SiP_SoC2.ibs for U2, and select the corresponding Signal DATA3\DATA4\DATA5\DATA6. As shown in Fig. 21.6.

In the Buffer Settings bar, set the four pins of U2 as Output, the four pins of U1 as Input, and for P1 (BGA package pins), we don't set them first, as Fig. 21.7 shows.

When the setup is complete, close the model specifying window, then click the menu to select Simulate SI → Run Interactive Simulation, or click the icon button to start the digital oscilloscope and simulate, the settings as shown in Fig. 21.8.

After the simulation, the simulated waveforms can be seen in the oscilloscope window. The waveforms of all detection points are shown on Fig. 21.8a, and the waveforms of the receiver side are shown on Fig. 21.8b. It can be seen that the signal

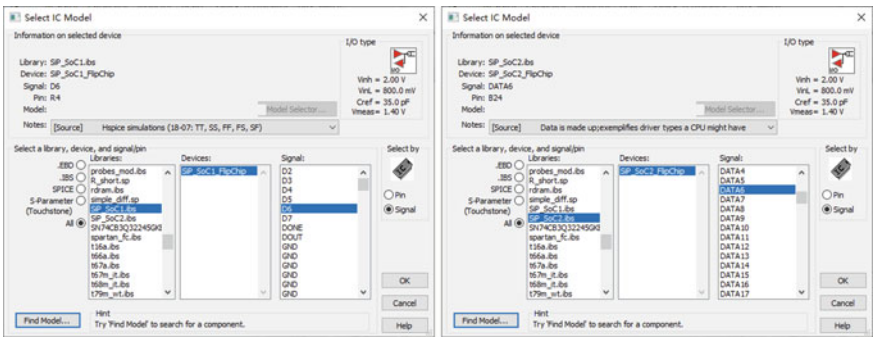

Fig. 21.6 Specify models for SoC1 and SoC2

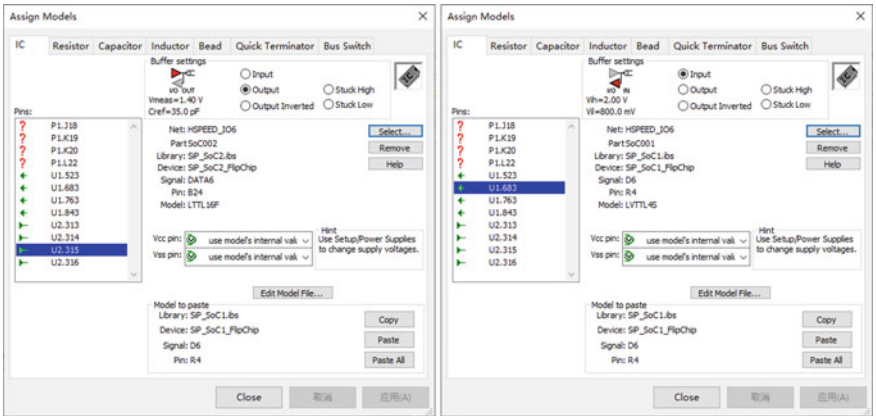

Fig. 21.7 Specify input and output types for simulation models

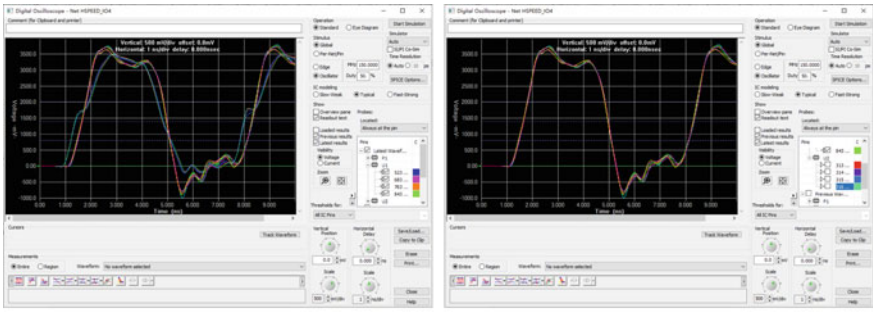

Fig. 21.8 Digital oscilloscope display simulation results

quality of the receiver side is not very good, and there are obvious oscillations and overshoots.

To improve the signal quality, several methods can be used, such as changing the signal drive strength, changing the design of layer stackup, rerouting and terminal matching. Here, we try the last method.

Select Simulate SI → Optimize Termination from the menu or click the Tool button to launch the Terminator Wizard, which automatically analyzes the net and gives the analysis results. As shown on the left side of Fig. 21.9a, the software recommends selecting series resistance matching and giving a recommended resistance value of 25.4 Ω. As recommended by the software, we set Quick Terminator in Assign Model to R Series of 25.0 Ω (which allows some tolerances), as shown on the Fig. 21.9b.

Rerun the simulation to get the results, the waveforms of the receiver shown on Fig. 21.10a. To compare the results of two simulations in the same window, select

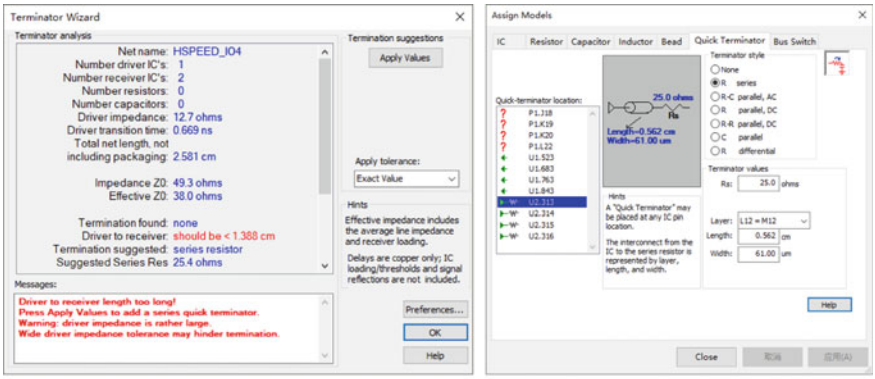

Fig. 21.9 Use terminator wizard to add series resistor

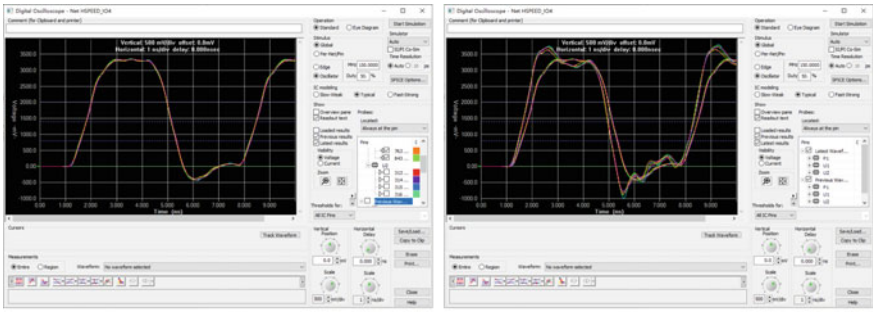

Fig. 21.10 Significant improvement of signal quality after adding matching resistor

the Previous Waveforms check box, as shown on Fig. 21.10b. By comparing the two simulations, we can see that after adding a match series Resistor, the rise and fall edges are reduced, the overshoot and oscillation are suppressed, and the signal quality is improved significantly.

3. Exploration of Package Pin Model

In above simulation, we have no settings for P1 (BGA package pins) model, how to deal with such problems in the actual project? First, in the above simulation, there are already signal output pins (four pins of U2), so the BGA package pins can only be input type. In HyperLynx SI simulation, the input pins can have no model, which is equivalent to when the SiP is welded to the PCB, these nets are not connected to other devices, as shown in Fig. 21.11a.

Another scenario is that when SiP is welded to PCB, the nets are connected to other devices on PCB, as shown in Fig. 21.11b. At this time, the simulation needs to consider the effects of routing and other devices on PCB, as well as the connection

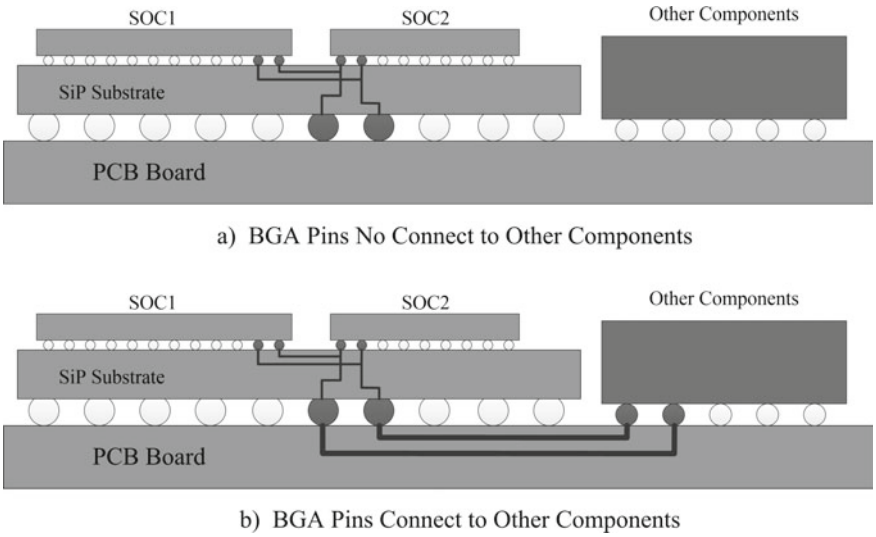

Fig. 21.11 Two scenarios of nets on SiP connected through BGA

of SiP Substrate and PCB Board using multi-layout simulation. Due to the size of the text, the discussion will not continue in this chapter and the readers can try by themselves.

4. Transmission Path Model Extraction

For SiP or Package designers, it is important to extract model parameters for signal transmission paths that indicate the impact of SiP or Package substrate routing on the signal.

Select Export → Net to → S-parameter model from the menu. In the pop-up Extract S-parameter model window, click the button Map Auto, and the S-port will automatically correspond to the component pins in the net. As shown in Fig. 21.12a, it can be seen that The three ports of HSPEED_IO4 are mapped as 1, 2 and 3; The three ports of HSPEED_IO4 are mapped to 4, 5 and 6; The three ports of HSPEED_IO6 are mapped as 7, 8 and 9; The three ports of HSPEED_ IO7 are mapped to 10, 11, and 12.

Then enter the frequency range in the modeling parameters field, such as 0.1–10000 MHz. In frequency Sweeping Type, select adaptive, and check the option of automatically display results. After setting, click the button Create Model in the lower left corner of the window and enter the name of the model to be created, such as HSPEED_IO4-7.s12p in the pop-up window, and then click Save to generate the S-parameter model. As shown in Fig. 21.12b.

The software automatically opens the HyperLynx Touchstone Viewer, where you can view S-Parameters for different channels, as shown in Fig. 21.13, which can be used in subsequent simulations.

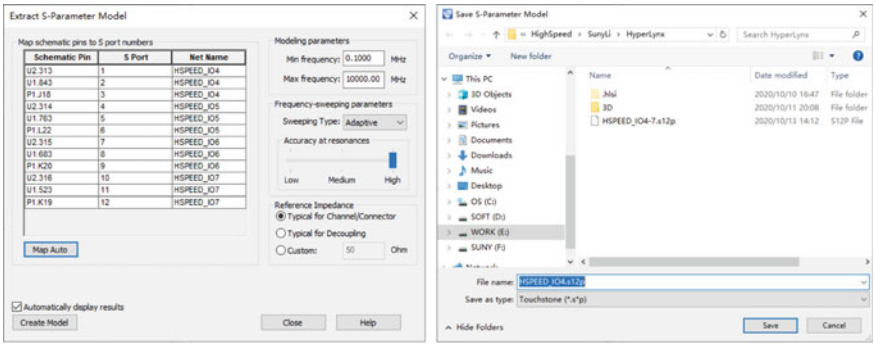

Fig. 21.12 Output S-parameter model setting

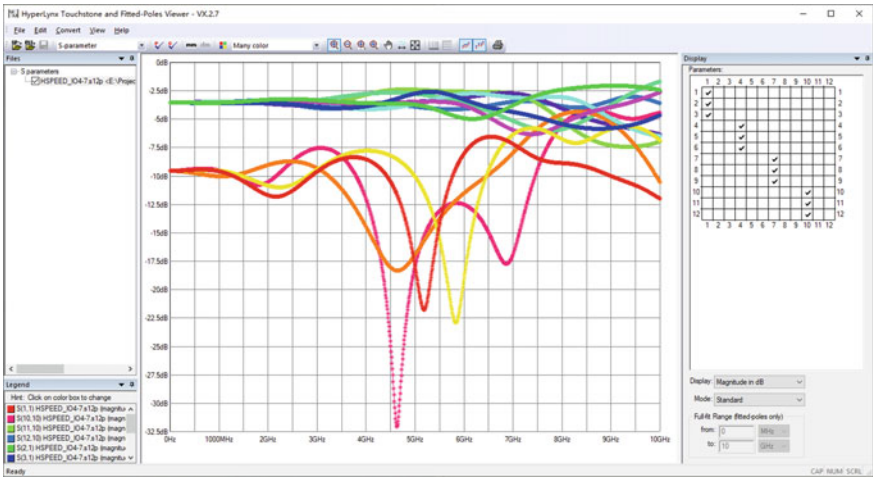

Fig. 21.13 View S-parameter in touchstone viewer

In addition, you can choose Export_Net To_Free-Form Schematic from the menu to output the selected net to the pre-simulation tool LineSim, as shown in Fig. 21.14.

LineSim can modify and edit various parameters of the nets to facilitate various hypothetical analysis and quickly obtain the best design solution.

21.3 Power Integrity Simulation

With the continuous pursuit of system performance, the design complexity is gradually increasing, and the signal frequency is also increasing. In addition to the analysis

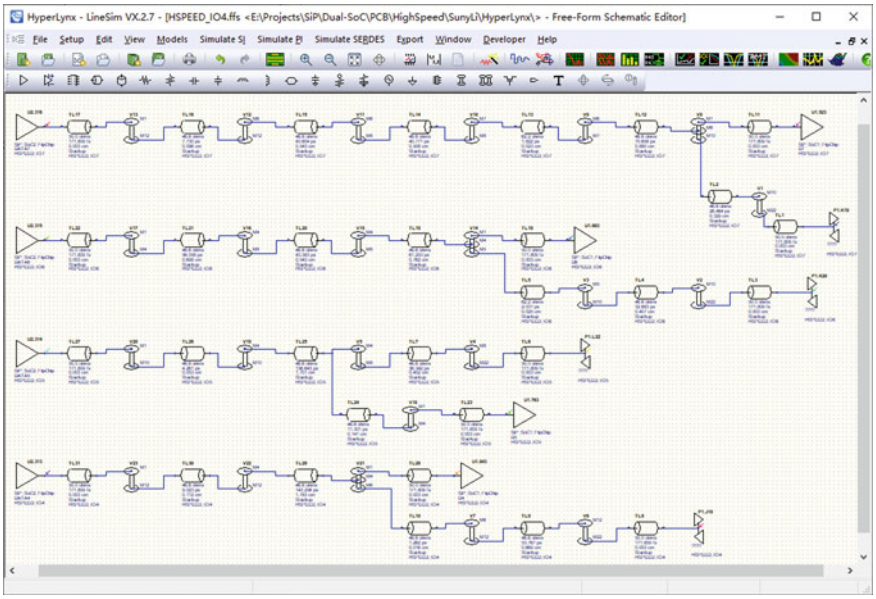

Fig. 21.14 Output selected nets to LineSim

of signal integrity, such as reflection and crosstalk, stable and reliable power supply has become an important research direction for high-speed SiP design.

As the number of chips increases, the core voltage decreases, and the type of power supply increases, more and more power sources are needed to share the same plane layer. Power fluctuation often has a serious impact on system, so the concept of Power Integrity, referred to as PI, has been proposed.

In fact, PI and SI are closely related, but the previous simulation tools generally assume that the power supply is in a stable state when performing signal integrity analysis. However, as the system design requirements for simulation accuracy continue to increase, this assumption is obviously becoming unacceptable, so the research and analysis of PI arises. In a sense, PI belongs to the scope of SI research, and Signal Integrity simulation must be based on reliable power integrity.

Although power integrity mainly discusses the stability of power supply, how to reduce noise on the ground is often discussed as part of power integrity because the ground level and the power plane are always inseparable in practical systems.

21.3.1 Introduction to HyperLynx PI

With the increase of IC power supply types, power consumption, less noise margin and increasing frequency, it is very difficult to design power supply system rationally. Power integrity analysis becomes an essential part of electronic design.

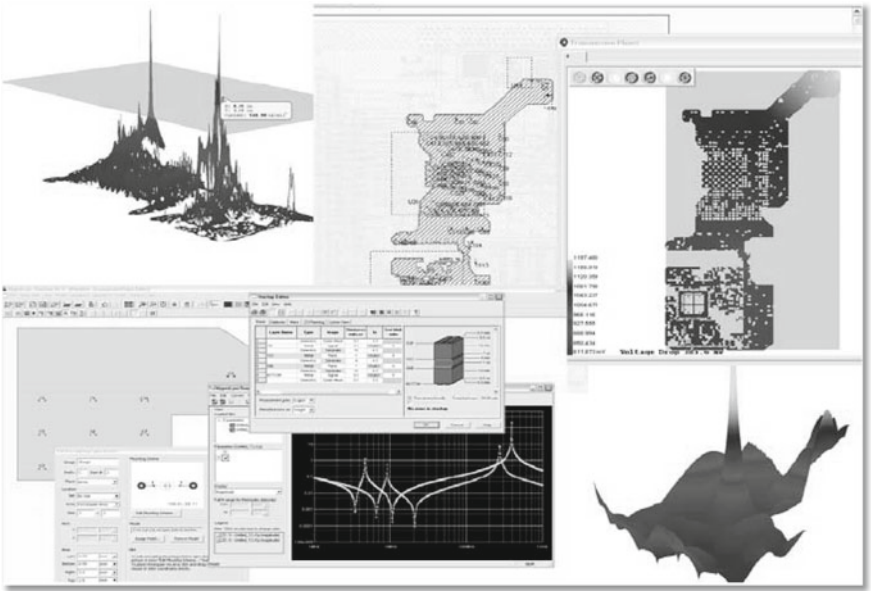

Fig. 21.15 HyperLynx PI simulation screenshot

With the HyperLynx PI, power distribution problems can be identified early in the design, problems that are difficult to locate in laboratory tests can be found early in design stage, and solutions can be detected immediately in an easy-to-use "What-if" environment. After Layout is completed, the design can be validated by post-simulation to ensure that all the requirements of the design are met.

Figure 21.15 show the HyperLynx PI simulation screenshot.

(1) Analysis of DC drop and current density

HyperLynx PI identifies potential DC power distribution problems. For example, excessive voltage drop will result in IC not working properly due to insufficient power supply voltage. High-density current or excessive via current may generate excessive heat, which can cause interruption of connection or damage to the entire circuit board. The results of simulation can be viewed graphically or the results of simulation can be generated, which can help to quickly find and locate DC power distribution problems.

(2) PDN impedance optimization

HyperLynx PI can help designers optimize the impedance of power distribution net (PDN), help designers determine the optimal decoupling capacitance distribution, including the number of capacitors, installation location, installation method, and obtain the impedance curve of power plane under different capacitor distribution to determine the optimal capacitor distribution.

On this basis, HyperLynx PI can also help designers to analyze the effect of planar impedance on the propagation of noise on the power plane, and show the propagation of noise on the planar layer through the 3D waveform.

(3) Model Extraction

In areas above GHz, a reasonable parameterized via is very important for the SerDes bus. In HyperLynx PI, high-precision via models can be generated, including decoupling net of the entire substrate, all capacitor and the effect of the vias and plane-to-plane resonance. HyperLynx PI allows extraction of PDN models and can be easily applied in subsequent simulations.

21.3.2 Power Integrity Simulation Example

Following is a brief introduction to the HyperLynx PI simulation process using the Dual-SoC SiP layout design example.

Since HyperLynx PI and HyperLynx SI are in the same simulation environment, there is no need to re-import the design data.

1. DC Voltage Drop Simulation

Select Simulate PI → Run DC Drop Simulation from the menu or click on the toolbar icon to pop up the DC Drop Analysis window. The power nets in the design are listed. Click on different power nets to see a preview of power plane shape. Select different metal layers and the selected layers will be highlighted, as shown in Fig. 21.16.

Next, we take VCCINT and VDD as examples for analysis, in which VCCINT = 2.5 V, maximum current 8A, VDD = 1.5 V, maximum current 10A.

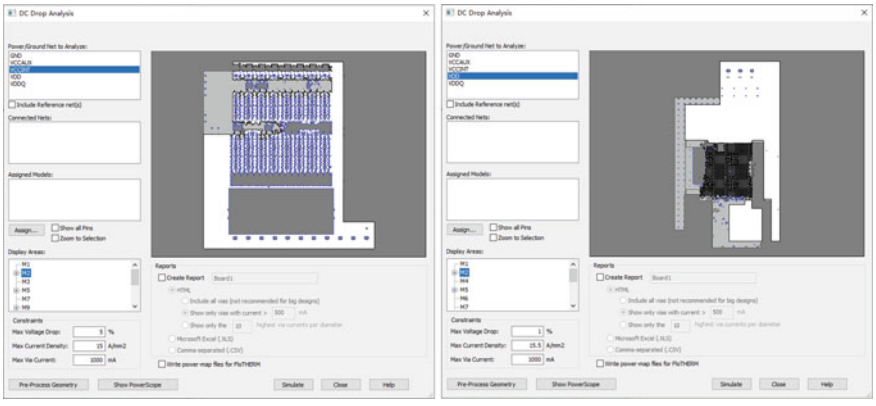

Fig. 21.16 DC Drop analysis interface

First, select VCCINT and click the assign button Assign... in the DC Drop Analysis window to set VRM model and DC sink model in the pop-up window. As shown in Fig. 21.17. In this example, P1 is the power supply device VRM and U1 is DC sink.

Press and hold the shift key, select all pins of U1, click the assign button under DC sink model to pop up the window shown in Fig. 21.18a, input the following parameters, then click the assign button under reference net, select reference net as GND, as shown in Fig. 21.18b, and then click OK.

Then click VRM manager under VRM model, click New in the pop-up window to open Add/Edit VRM window, input the following parameters, click in power pins, select browse, select all pins of P1 belonging to VCCINT in the pop-up dialog window, and then click OK to return to add/edit VRM window, set ref net to GND, click OK to return to VRM Manager window, and the whole setting process is shown in Fig. 21.19.

After the model is specified, in DC drop analysis window, click simulate button to simulate. According to the complexity of the design, the simulation time will

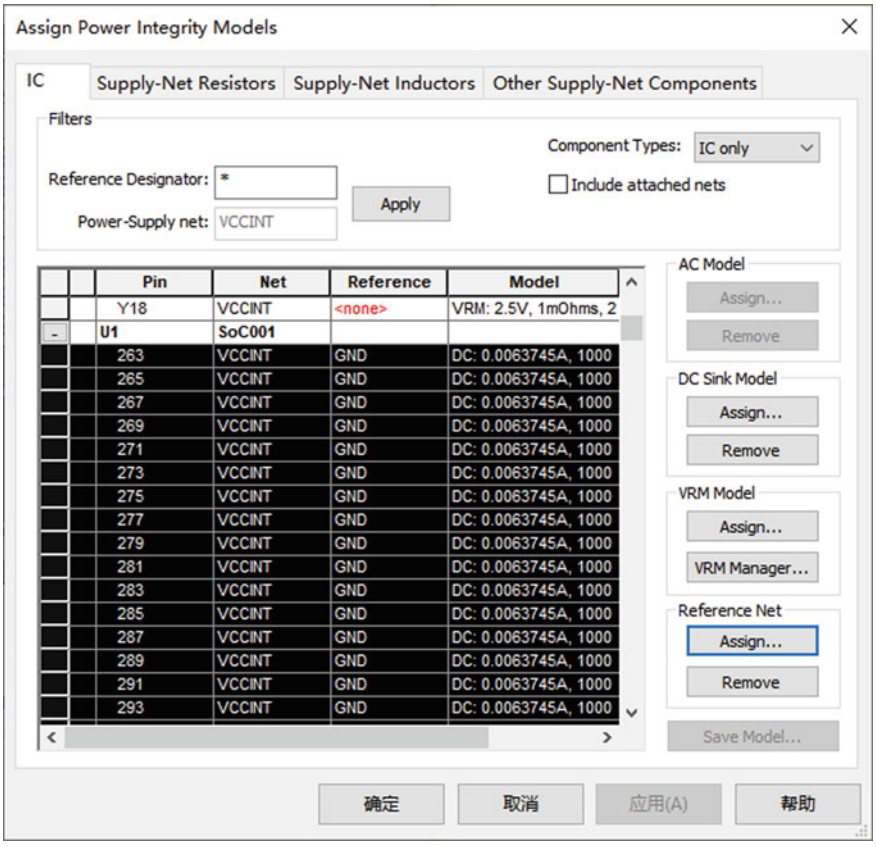

Fig. 21.17 Assign power integrity models for VCCINT

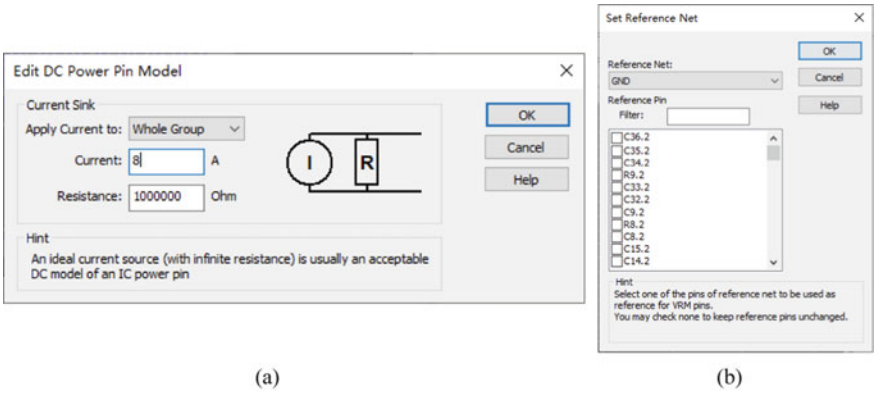

Fig. 21.18 Setting DC sink model and reference net

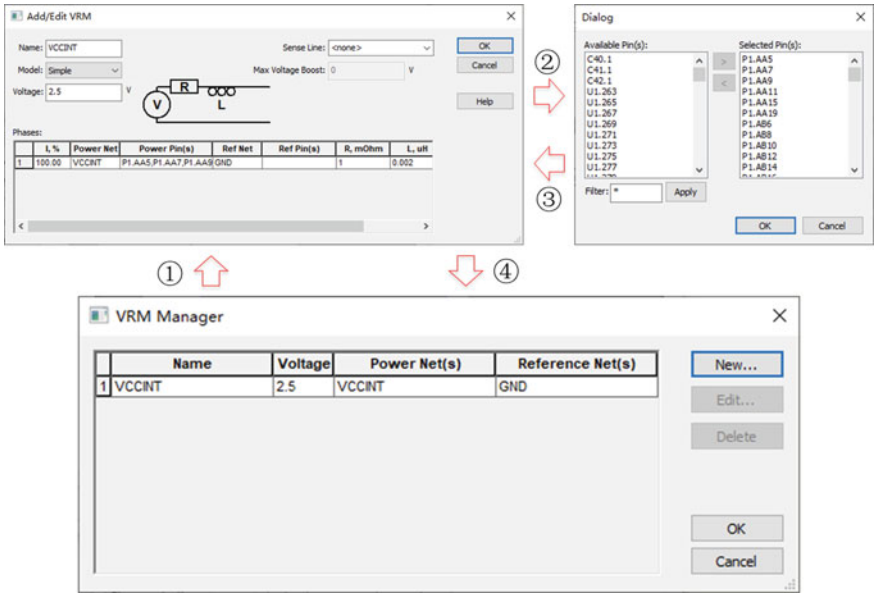

Fig. 21.19 Setting VRM model and reference net

be different. After the simulation is completed, two windows can be obtained: 3D graphics display window and report window. The 3D graphics display window is shown in Fig. 21.20.

From 3D graphics window, we can see VCCINT is distributed in many metal layers, and the voltage on each layer has slight changes. The maximum voltage drop of VCCINT is 1.1mv, which meets the design requirements.

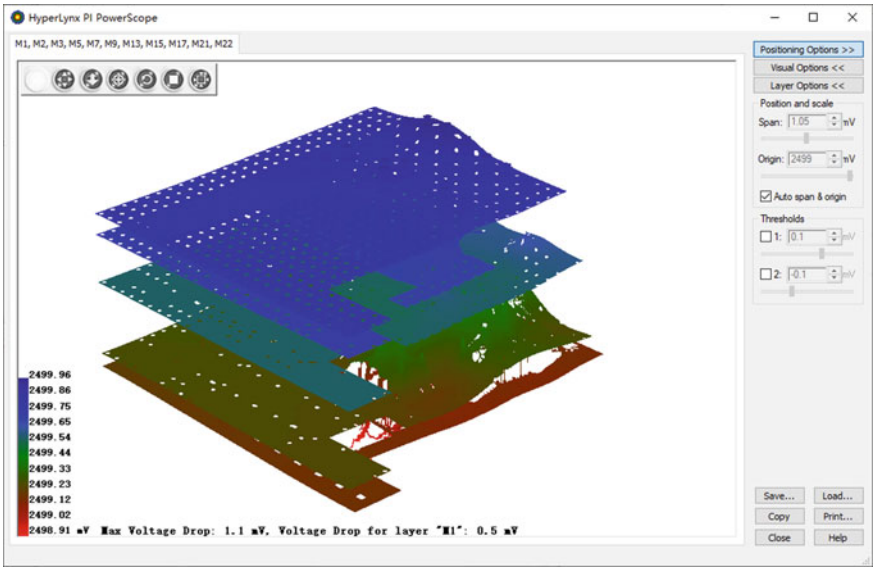

Fig. 21.20 Simulation results of DC drop of VCCINT

The report window lists the voltage and current values of all pins, via and trace, and all coordinate points are dynamically linked with the DC drop analysis window. After clicking the option of pin column in the report window, the mouse will automatically jump to the corresponding coordinate points in the graphics window, as shown in Fig. 21.21.

Using the same method to simulate the DC voltage drop of VDD, the following simulation results of DC drop can be obtained. From the 3D graphics window, it can

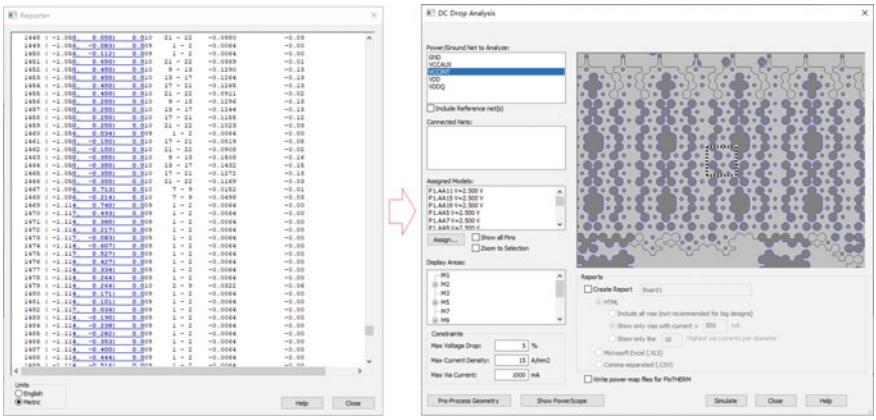

Fig. 21.21 The report window is associated with the graphics window

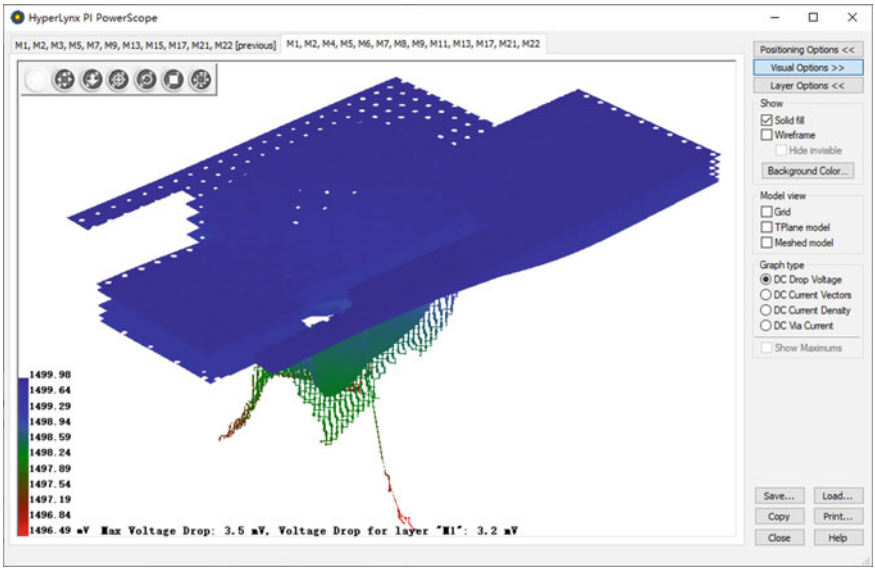

Fig. 21.22 Simulation results of DC drop of VDD

be seen that VDD is distributed in multiple metal layers, and the voltage on each layer changes slightly. The maximum voltage drop of VDD is 3.5mv, which meets the design requirements, as shown in Fig. 21.22.

2. Current Density Simulation

After setting the parameters, in one simulation, not only the simulation results of DC drop, but also the simulation results of current density and via current can be obtained.

From the 3D graphics window, select switch graph type to DC current density to view the current density simulation results. The maximum current density of VCCINT is 44.0 A/mm^2, as shown in Fig. 21.23.

Select switch graph type to DC via current from 3D graphics window to view the simulation results of via current. The maximum via current of VCCINT is 0.192a, as shown in Fig. 21.24.

For VDD net, use the same method, switch graph type to DC current density to view the current density simulation results, and the maximum current density of VDD is 75.6 A/mm^2, as shown in Fig. 21.25.

Switch graph type to DC via current to view the simulation results of via current. The maximum via current of VDD is 0.5A, as shown in Fig. 21.26.

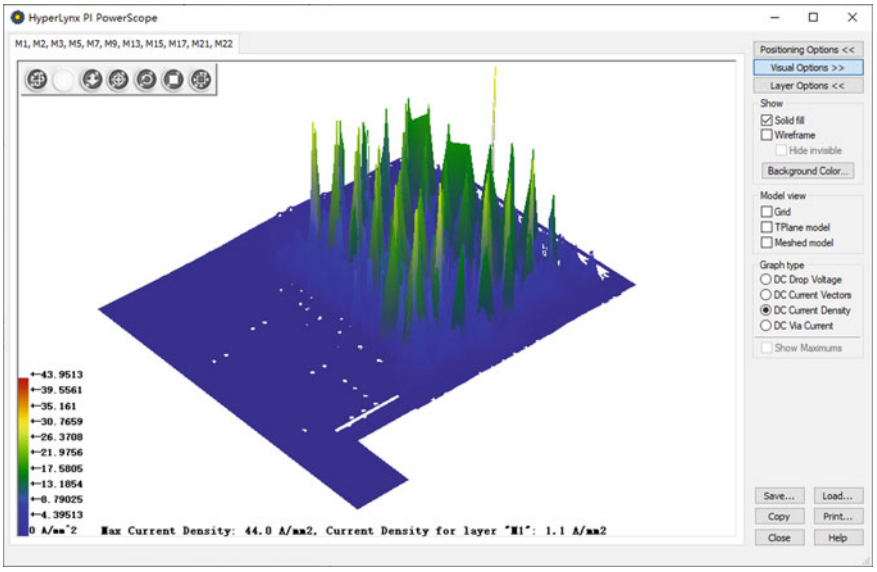

Fig. 21.23 Simulation results of VCCINT current density

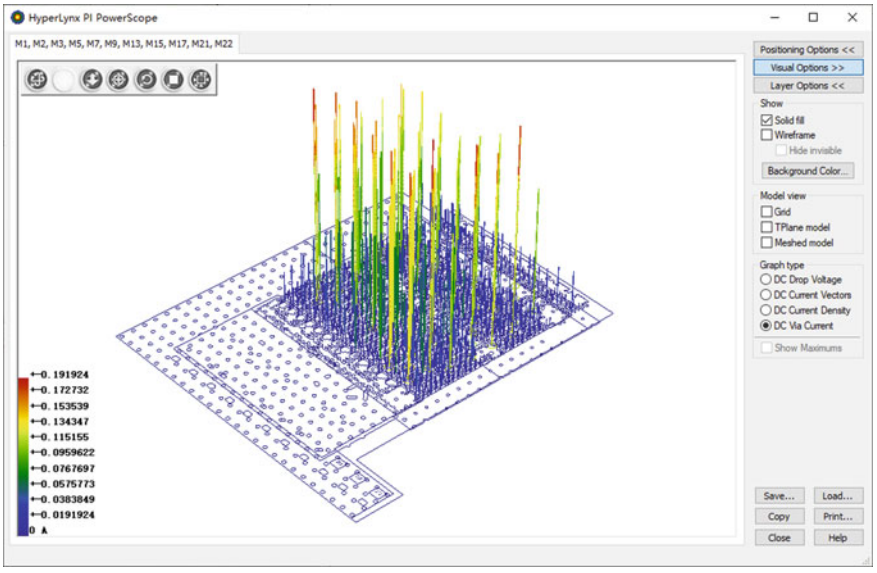

Fig. 21.24 Simulation results of VCCINT via current

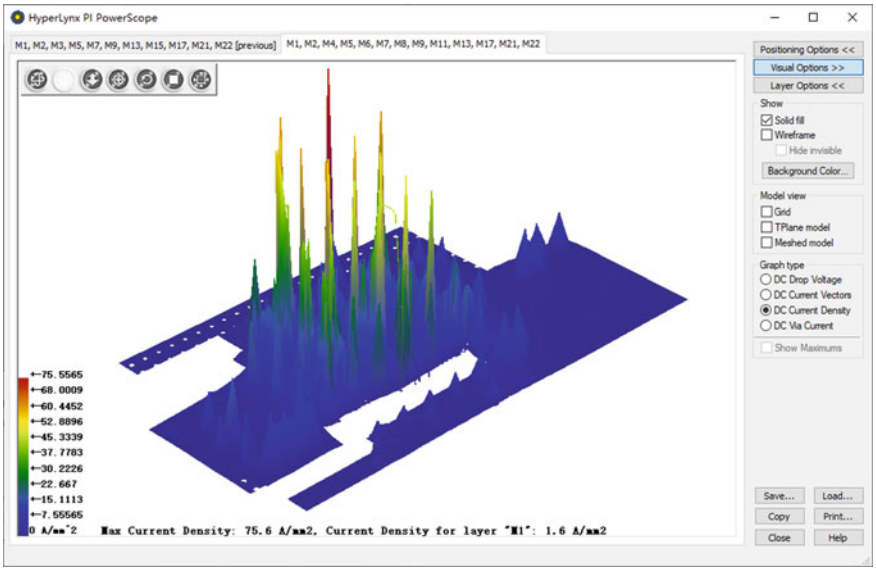

Fig. 21.25 Simulation results of VDD current density

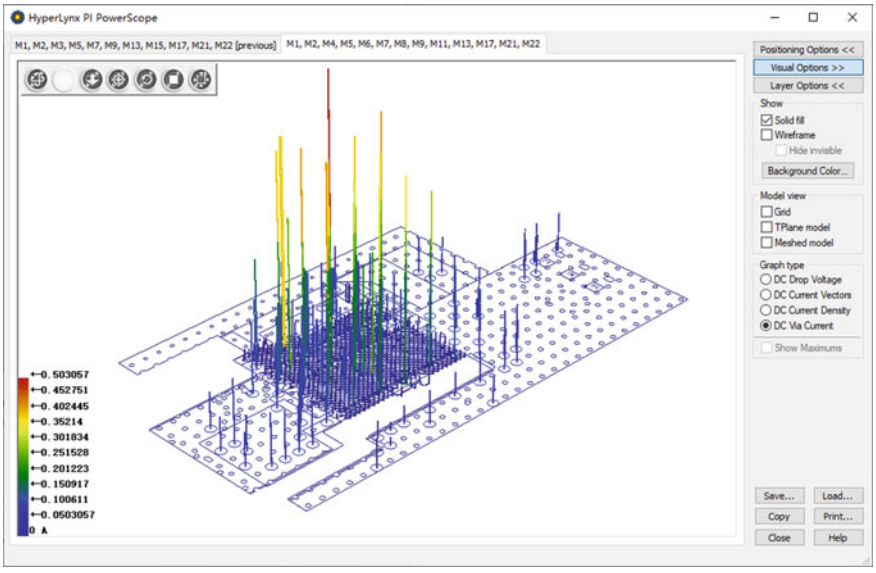

Fig. 21.26 Simulation results of VDD via current

21.4 Thermal Simulation

SiP consumes more power in the same area than ordinary packages or PCBs because of its small size, many chips concentrate in a smaller space. SiP consumes a lot of power in small area, so thermal simulation of SiP becomes very important.

21.4.1 Introduction to HyperLynx Thermal

HyperLynx Thermal uses a locally variable step finite differential algorithm, which is faster than the traditional finite element algorithm. It can be used for heat conduction, convection and radiation. It also considers whether heat sinks are installed on the device, whether heat conduction holes and heat conduction tubes are installed on the substrate.

HyperLynx Thermal can analyze multilayer and irregularly shaped substrates, hybrid or subcircuit boards. The substrate can be cooled by edges in an enclosed space or by forced convection in an open system. The flow of gas can also be natural or forced convection, or the enclosed system can be cooled by a heat exchanger.

HyperLynx Thermal models can take into account the effects of gravity, gas pressure and direction of gas flow, anisotropic trace, and the influence of copper on heat transfer. By determining the temperature and temperature gradient of SiP substrate and the temperature of the chip, the designer can easily identify potential thermal and reliability problems in the design.

(1) Component Library

HyperLynx Thermal provides two component libraries (Working library and Master library), which contain a large amount of component information. The Master library contains more than 2000 defined components and allows users to expand. Devices built in the working library can be conveniently stored in Master library, and the heating simulation design can be reused.

(2) Component temperature

The objective of thermal analysis is to obtain the temperature of IC devices and their junctions. HyperLynx Thermal calculates the average temperature of IC devices, calculates the junction temperature of IC devices, and displays the temperature of IC devices with color cloud maps. It is easy to quickly find components with higher temperatures, and the temperature values can also be output through a numerical table.

(3) Temperature Cloud Map

The temperature cloud map of HyperLynx Thermal reveals heat conduction on the SiP substrate. Because the thermal expansion is proportional to the temperature, the high temperature area in the work may expand and warp, which causes the connection to

be detached. The hot spots on the circuit board can be quickly identified by simulation during the design phase.

(4) Temperature gradient cloud map

HyperLynx Thermal outputs a temperature gradient cloud map over the entire SiP substrate. Because of thermal expansion, high gradient areas cause high thermal stress, which is often where cracks and warps occur on printed circuit boards. Temperature gradient cloud maps can help designers find potential problems.

When the parameters are set correctly, the simulation results of HyperLynx Thermal are compared with the measured results and with the results of infrared scanning. The simulation accuracy is more than 90%.

21.4.2 Thermal Simulation Example

Following is a brief introduction to the HyperLynx Thermal simulation process using the Dual-SoC SiP layout design. Since HyperLynx Thermal and HyperLynx SI are in the same simulation environment, there is no need to re-import design data.

1. Thermal analysis simulation

By selecting Simulate Thermal → Run Thermal Simulation from the menu, the thermal analysis process can be started and the initial simulation results (simulated with the default parameters of the system) can be obtained, as shown in Fig. 21.27.

In HyperLynx Thermal, you can switch between different layers by clicking View the next side/layer button , or through a drop-down window on the right side of the toolbar, as shown in Fig. 21.28, where the dark color represents copper or metal trace.

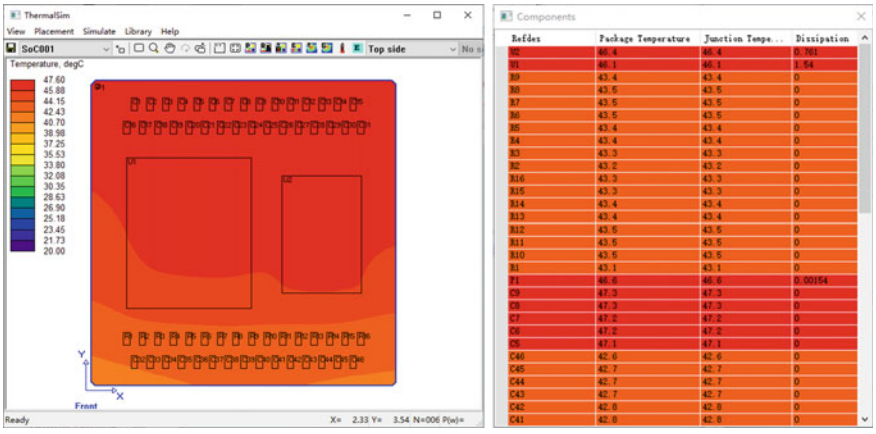

Fig. 21.27 HyperLynx thermal initial simulation results

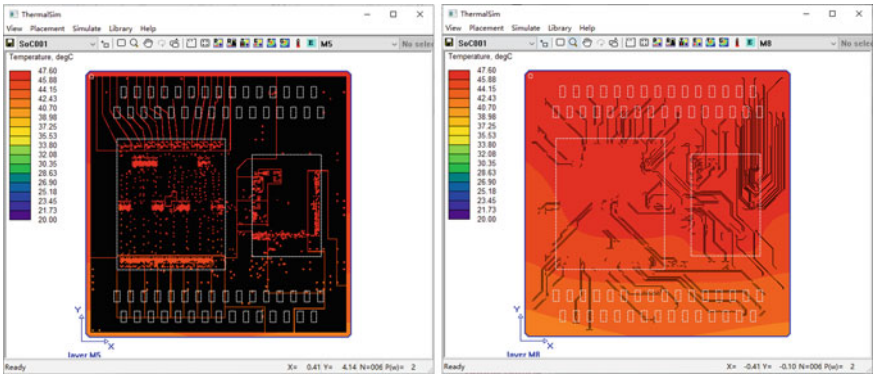

Fig. 21.28 View the metal distribution of different layers in HyperLynx thermal

These data are important for the heat transfer of the substrate, because the heat transfer coefficients of the two materials metal and dielectric in the substrate are very different, the precise distribution of the metals in each layer, and the proportion of the metals in the substrate have a great impact on the accuracy of thermal analysis.

(1) Setup of Environment Parameters

Click on the tool icon **E** to set environmental parameters, such as air temperature, air pressure, gravity, humidity ratio, incoming air velocity, and so on. And the Casing related parameters are set, as shown in Fig. 21.29.

(2) Setup of Component Properties

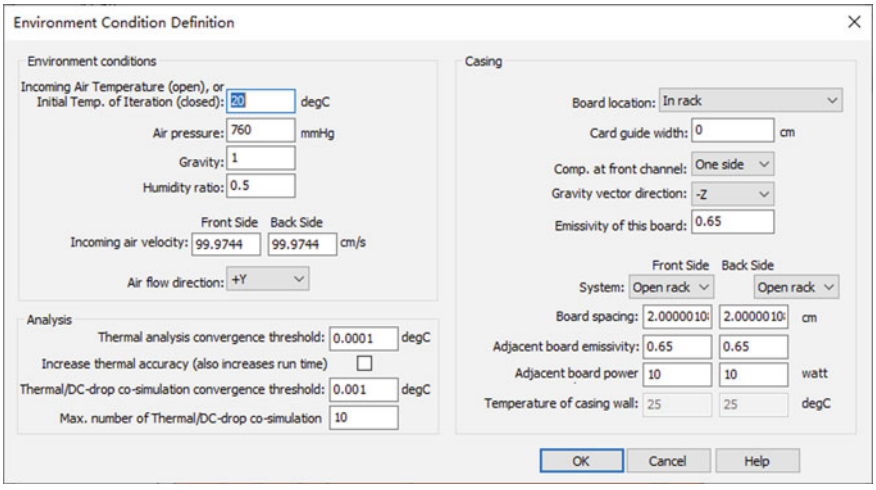

Fig. 21.29 Environment parameters setting

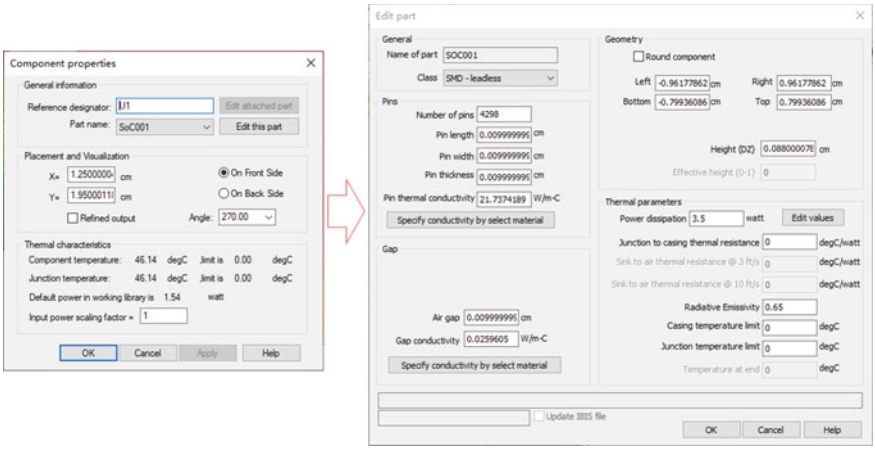

Fig. 21.30 Component properties setting

After setting the environment parameters, set the component properties, mainly setting the name, location, power scaling factor (ratio of actual work power consumption to maximum power consumption), etc.

Double-click the left mouse button on any component and pop up the Component Properties window. The properties in this window are basically inherited from Xpedition. The designer needs to input the power factor in the Input Power Scaling factor according to the ratio of the actual power consumption to the maximum power consumption of the component. Then click the Edit this Part button to set up the components in more detail in the pop-up Edit Part window. In the Edit Part window, pin parameters, air gap between the components and the substrate, gap thermal conductivity, power dissipation of the components can be set. Here, the power dissipation of U1 is modified to 3.5 W, U2 is modified to 2.5 W, and P1 is modified to 0 W. The default power consumption is estimated by the software based on the area of the device. Others remain default, as shown in Fig. 21.30.

(3) Setup of Substrate Parameters

After the component properties setting, click Stackup Editor button  under the HyperLynx environment to set the parameters of the substrate, such as the number of substrate layers, thickness and heat conductivity. These parameters are inherited from the Xpedition design. If the correct settings are made in the Xpedition, there is no need to modify, just check them, as shown in Fig. 21.31.

After setting all the parameters, click the Run Analysis button  to rerun the thermal analysis, the maximum temperature of the substrate is 92.9 °C and the maximum temperature gradient is 35.9 °C/mm, as shown in Fig. 21.32.

If the temperature does not meet the design requirements at this time, other auxiliary cooling methods can be used to reduce the temperature of the substrate and components, such as by adding boundary conditions, heat sink, heat pipe or heat

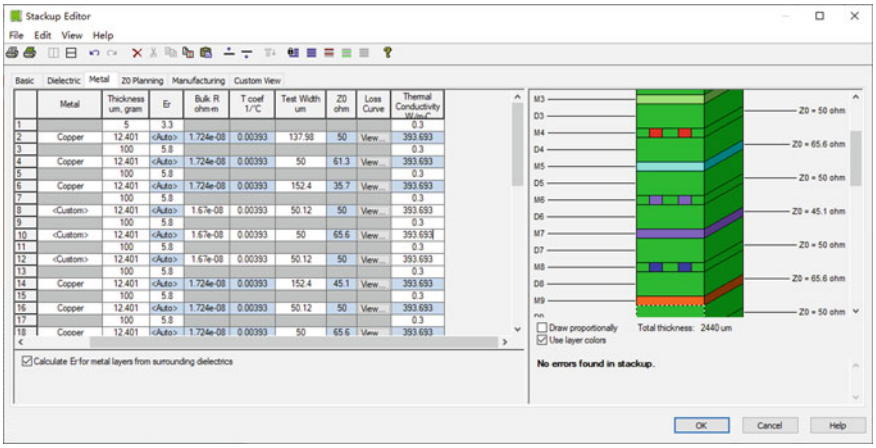

Fig. 21.31 Substrate parameter setting

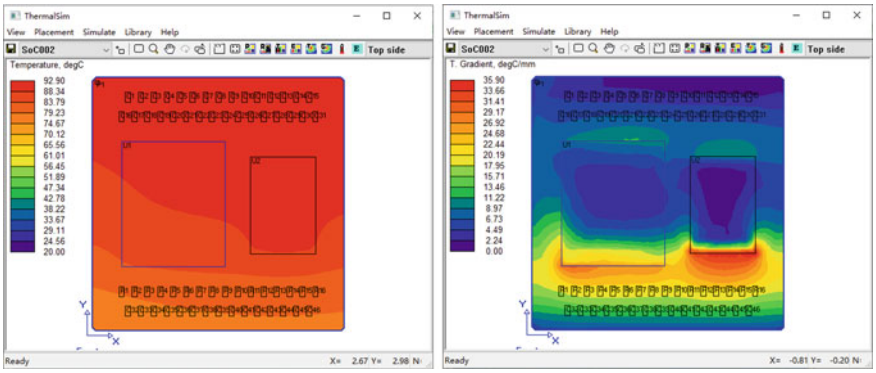

Fig. 21.32 Rerun the simulation to get temperature and gradient cloud maps

screw, and verify its feasibility. Due to the size of the text, this is not to be repeated here, and readers can analyze it by practice.

2. Electrothermal co-simulation

In addition to the device itself, the high current in the traces on the substrate will also heat up. Considering the heat of this part in the simulation will increase the accuracy of thermal simulation, so the electro-thermal co-simulation is required.

Menu selection Simulate Thermal → Run PI/Thermal Co-Simulation, in the pop-up Batch DC Drop Simulation window, select the net to be emulated, and set its maximum limit. For example, the maximum voltage drop is 5%, the maximum current density is 100A/mm^2, and the maximum via current is 1A, as shown in Fig. 21.33.

Because the electrothermal co-simulation needs many iterations, the simulation time is relatively long. After the simulation is completed, we can get the following

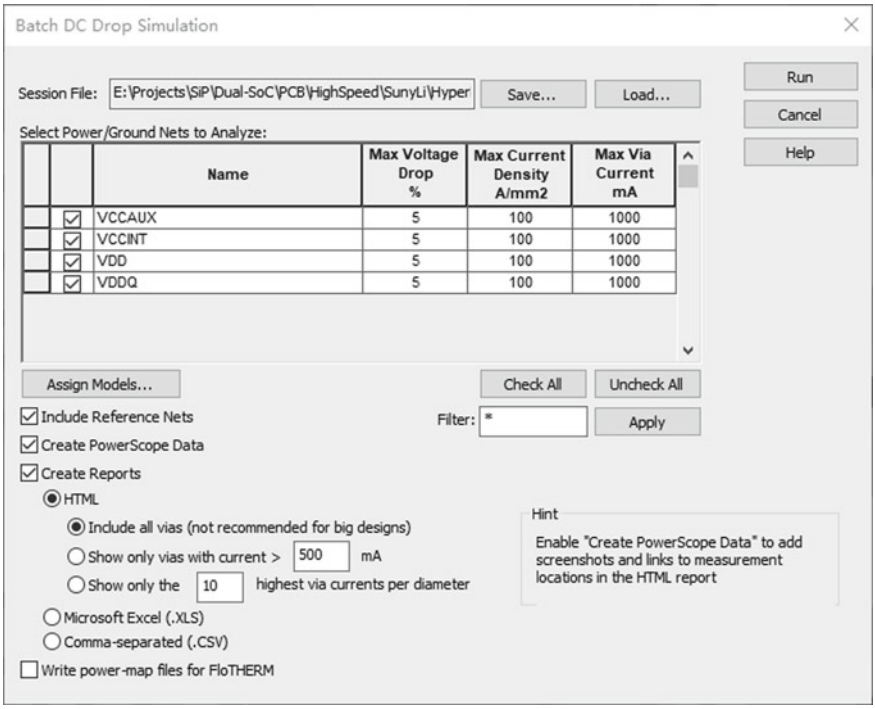

Fig. 21.33 Setup interface for electrothermal co-simulation

results. Refer to Fig. 21.34, the maximum temperature and maximum temperature gradient are reduced to some extent. The simulation results here are different from what we expected, perhaps due to the change of algorithm or external conditions,

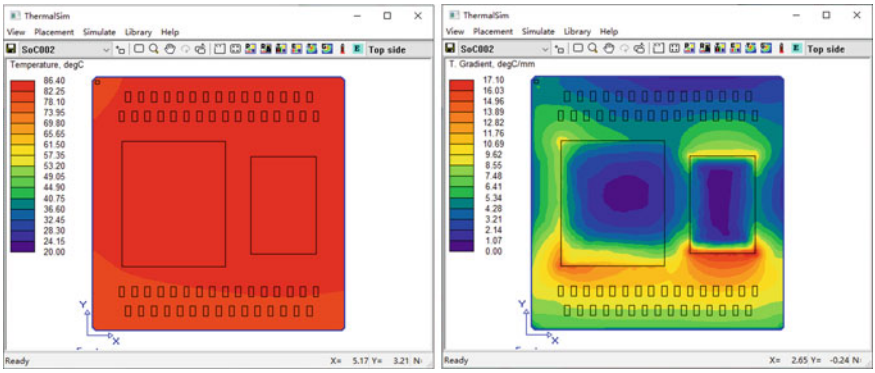

Fig. 21.34 Simulation results of electrothermal co-simulation

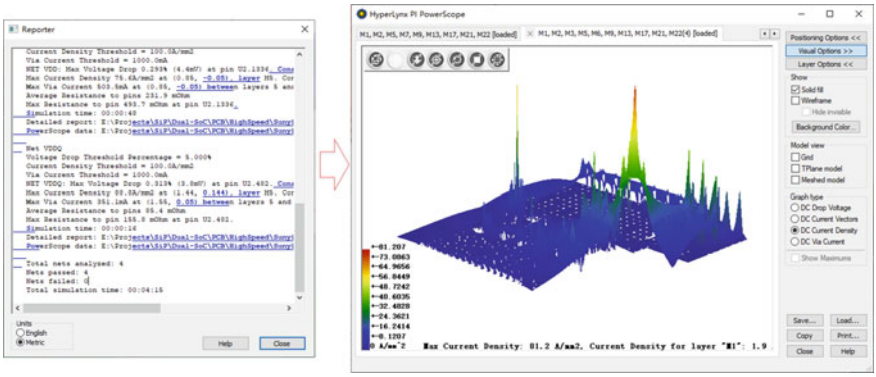

Fig. 21.35 Report and waveform of electrothermal co-simulation

limited to space. The reason is not discussed here and left for the reader to think about.

In addition to graphically displaying the simulation results, we can also get a simulation report, which lists the simulation results of the power net. Click on the link text inside the report to view the detailed report and the simulation waveforms of the power net, as shown in Fig. 21.35.

21.4.3 Introduction to FloTHERM Software

From above thermal analysis, we can see that HyperLynx Thermal is easy to use and can quickly get the simulation results, but there are some limitations, such as simple condition settings, not suitable for complex design, etc. Below we introduce a more specialized thermal analysis tool, FloTHERM.

FloTHERM is a powerful three-dimensional Computational Fluid Dynamics (CFD) software that accurately predicts air flow and heat transfer, including the combined effects of conduction, convection and radiation, inside and around electronic components.

FloTHERM can be used to quantitatively analyze the heat loss, temperature field and internal fluid movement of the system at different levels.

FloTHERM uses an advanced finite volume solver to comprehensively analyze the thermal radiation, heat conduction, heat convection, fluid temperature, fluid pressure, fluid velocity and motion vectors of an electronic system in a three-dimensional structure model.

FloTHERM has both steady-state and transient analysis capabilities. It can analyze not only the normal working conditions of electronic equipment, but also the thermal reliability of changing working conditions or sudden failures. It can also analyze the thermal analysis of heat sink systems containing a variety of cooling media, such as electronic equipment or cooling plates with both liquid and air cooling (Fig. 21.36).

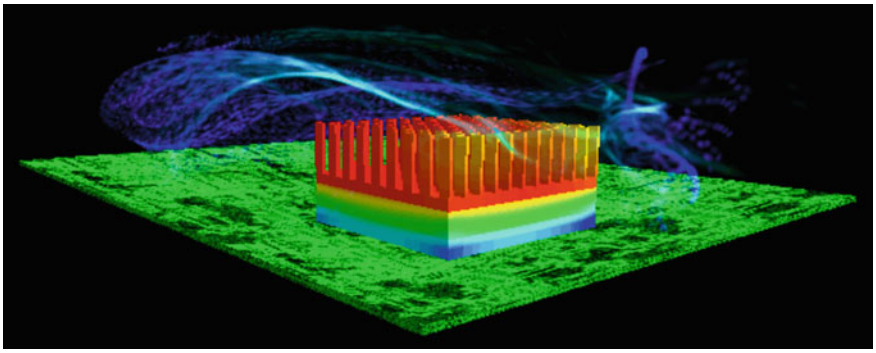

Fig. 21.36 Package thermal analysis using FloTHERM

The post-processing module of FloTHERM can visually and conveniently display the calculated temperature field, velocity field, pressure field and other data in the form of plane cloud, isopotential map, surface temperature distribution map, and three-dimensional animation of fluid motion. Flexible multilayer embedded localized grid technology can greatly improve computational efficiency and handle complex structures while ensuring computational accuracy.

Perfect thermal analysis model library, intelligent CAD and EDA interface, full compatibility with common CAD and EDA software, and can be imported and exported through STEP, SAT, IGES, STL, IDF and other standard formats.

The application scope of FloTHERM software includes:

- Packaging Level and Chips Level thermal analysis
- PCB board and module level thermal analysis
- System level thermal analysis
- Environmental level thermal analysis.

21.4.4 Introduction to T3Ster

To get accurate results in thermal simulation, the accuracy of device model is very important. How to obtain an accurate thermal model of the device? Usually requires testing. Let's take a look at the T3Ster thermal test equipment.

T3Ster (Thermal Transient Tester) is advanced thermal characteristics tester used for semiconductor devices, and for testing thermal characteristics of IC, SoC, SiP, radiator, heat sink, etc.

T3Ster, which combines static mode and dynamic mode defined by JESD51-1, can collect device transient temperature response curves (including temperature rise and cooling curves) in real time, with sampling rate as high as 1 microsecond, test delay as short as 1 microsecond, and junction temperature resolution as high as 0.01 °C.

T3Ster can test both steady-state and transient thermal resistance.

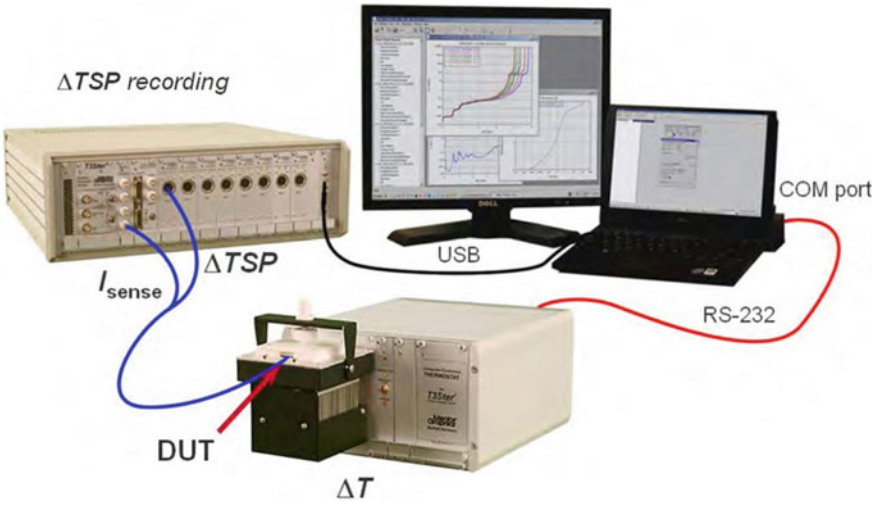

Fig. 21.37 T3Ster minimum test environment

T3Ster is the developer of JEDEC's latest test standard for thermal resistance of Junction-case (θjc) (JESD51-14). T3Ster has developed the world's first international standard JESD51-51 for testing LEDs, as well as the LED photothermal co-test standard JESD51-52. Figure 21.37 are the minimum test environments for T3Ster, including the T3Ster host, thermostat, test computer and test software installed on the computer. The DUT (device under test) are generally placed in the thermostat or in a temperature-controlled environment.

T3Ster's original Structural Function analysis method, which can analyze the thermal performance (thermal resistance and thermal capacity parameters) of each layer structure on the device's thermal conduction path, and construct the equivalent thermal model of the device, is a powerful tool to support the packaging process, reliability test, material thermal characteristics and contact thermal resistance of the device. Therefore, it is known as "X-ray" in thermal testing equipment.

T3Ster can seamlessly link with professional thermal analysis software such as FloTHERM to import the thermal parameters of the device from the actual test into the thermal simulation software for subsequent simulation and optimization (Fig. 21.38).

The functions of T3Ster include:

- Chip junction temperature testing, without destroying the chip structure, directly test and obtain the chip junction temperature.
  Chip surface temperature testing which is measured by thermocouple.
- Material Thermal Resistance Measurement
  θjc (Thermal Resistance from junction to case)
  θja (Thermal Resistance from junction to air).
- The chip structure and defect analysis can be done through the structure function

Fig. 21.38 Data transfer between T3Ster and FloTHERM

Internal structure analysis, process defect analysis, reliability testing, contact thermal resistance evaluation.

21.5 Advanced 3D Solver

21.5.1 Introduction to HyperLynx Full-Wave Solver

HyperLynx Full-wave Solver is a powerful 3D full-wave electromagnetic field solver.

Using proprietary accelerated boundary element technology to achieve unprecedented solution speed and capacity while maintaining simulation accuracy. Solvers use multi-core and hybrid architecture technology to enable designers to get results faster and solve the most challenging problems quickly. In a unified environment, designers can solve complex problems such as signal integrity, power integrity and EMI, all of which use broadband full-wave electromagnetic field simulation technology.

HyperLynx Full-Wave Solver supports three-dimensional full-wave electromagnetic field simulation, boundary element technology, broadband material and loss modeling, accuracy and frequency-dependent loss, inductance, skin effects, radiation effects, etc. Supports current and voltage sources, as well as a variety of planar wave excitation sources.

It supports layout editing and creation, automatic EM analysis, automatic generation of net lists, flexible model clipping options, automatic port settings, adaptive fast frequency scanning capabilities and etc.

It can output S, Y, Z parameters, near and far field graphs, noise spectrum graphs, current density graphs, etc. it supports a variety of standard EDA file formats (Fig. 21.39).

HyperLynx Full-wave Solver contains Hybrid Signal and Power Integrity Analysis to provide accelerated power-aware signal results. Maxwell's accuracy is guaranteed through a powerful multi-solver hybrid technology. Designers can analyze crosstalk, loss, characteristic impedance in signal integrity from the frequency domain, as well as current density, decoupling design, and AC analysis in power integrity.

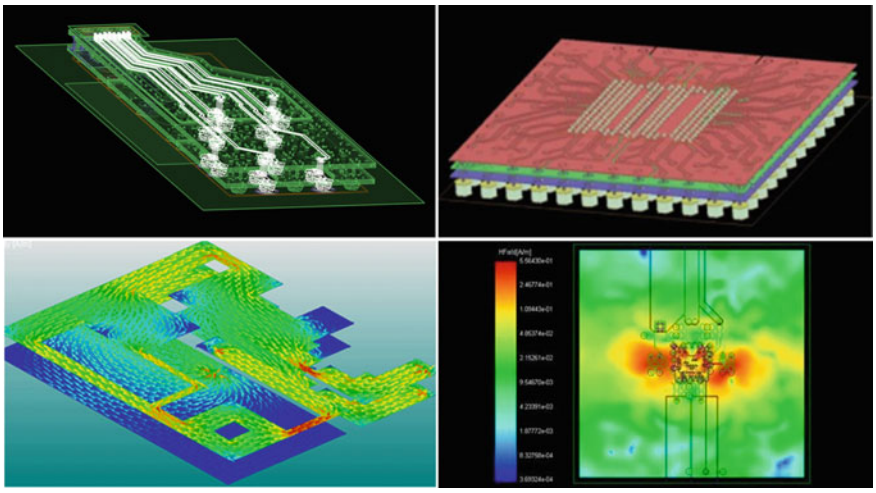

Fig. 21.39 HyperLynx Full-wave Solver simulation screenshot

Designers can not only optimize the design to improve performance, but also reduce design costs from chips, packaging to PCB.

21.5.2 Introduction to HyperLynx Fast 3D Solver

HyperLynx Fast 3D Solver enables the creation and processing of SiP models suitable for power integrity, low frequency SSN/SSO, and full system SPICE model generation, taking into account the skin effect on resistors and inductors.

Fast 3D Solver has a quasi-static extractor that solves power integrity, signal integrity, and synchronous switch noise. With its powerful 3D capabilities, automatic extraction includes the ability to process power and signal nets. Users can select a variety of extractions, including impedance, resistance, conductance, capacitance, inductance, and a complete SPICE net. Skin effect can be considered. Fast 3D Solver supports SiP, MCM, PoP and other types of design to extract accurate RLGC models (Fig. 21.40).

21.6 Simulation of Digital-Analog Mixed Circuit

In schematic design phase, Siemens EDA provides a hybrid circuit emulation tool Xpedition AMS based on Designer, which can simulate and analyze circuit functions to ensure “design is correct” from the beginning of the design.

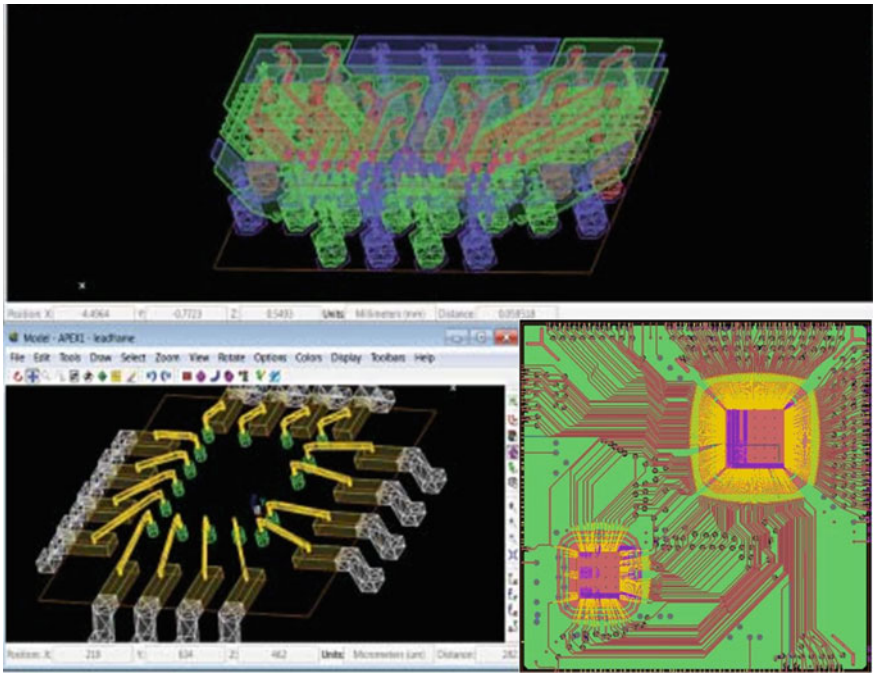

Fig. 21.40 Simulation screenshot of HyperLynx fast 3D solver

Xpedition AMS is based on the Designer environment. If the correct model is attached to the components in the schematic diagram designed in Designer, the Xpedition AMS can be directly started for simulation.

Xpedition AMS supports mixed simulation of multilingual models, which is embedded in a hybrid simulation engine based on ADMS and can support multiple languages, including industrial standard Eldo/SPICE, Verilog, VHDL, and the latest standard mixed simulation languages Verilog-AMS, VHDL-AMS and C. Xpedition AMS has a unique hybrid emulation function. For analog circuits, it can use SPICE model. For digital circuits, it can also use languages such as VHDL directly without any model conversion, which makes the digital/analog hybrid emulation function easy to implement.

Xpedition AMS has a variety of analytical tools, such as AC analysis, DC analysis, Transient analysis, frequency-domain analysis, time-domain analysis, etc. It can be extended to advanced simulation including Parametric Sweep, Temperature Sweep, Monte Carlo analysis, Worst-Case analysis, etc. to ensure design quality and design stability. It can fully take into account the discrete situation of circuit and components, and ensure the reliability of the product.

Xpedition AMS supports multi-tool co-simulation, connecting multiple tools in an integrated simulation environment to give full play to their respective advantages. Figure 21.41 are shown. Xpedition AMS and other analysis tools, such as Simulink

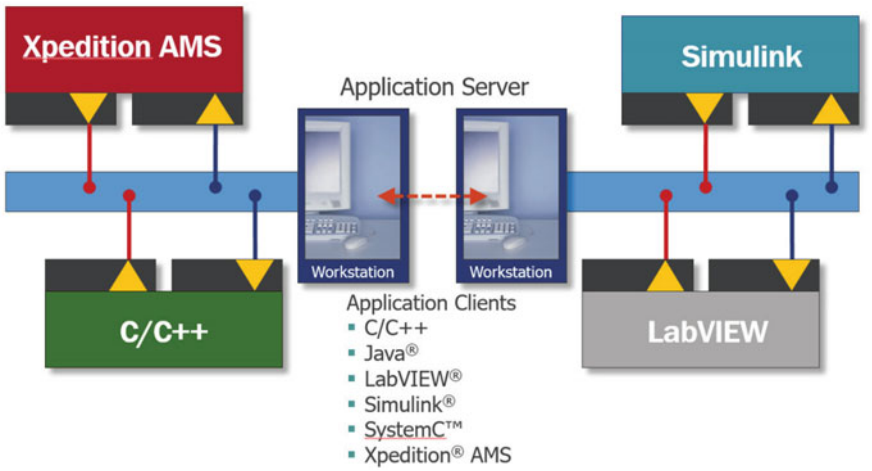

Fig. 21.41 Xpedition AMS supports multi-tool co-simulation

and LabVIEW link and process with languages such as C/C++, java, and SysteemC, are particularly effective for analyzing complex systems by connecting design teams from the beginning to the end of the development process.

21.7 Electrical Rules Verification

Electrical rule verification is to check and validate the electrical rules of the whole design after the layout design is completed. It is an effective guarantee for the design quality. Especially for complex electrical rules that are not easy to emulate, such as traveling across planar divisions, vertical reference plane changes, and rule checks for SI, PI, EMI/EMC, to help designers complete the design quickly, efficiently and with high quality.

21.7.1 Introduction to HyperLynx DRC

HyperLynx DRC is a powerful and fast electrical design rule checking and verification tool that helps designers perform electrical rule checking through an automated verification process.

Unlike the physical rule-based DRCs built into the design tools, HyperLynx DRC is mainly for electrical rules, which contain five categories of 82 rules, and will be

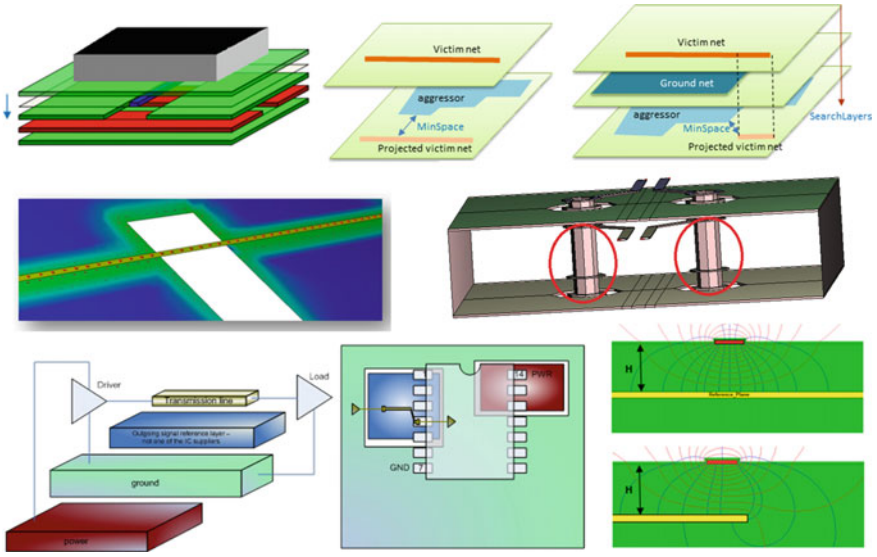

Fig. 21.42 HyperLynx DRC integrates multiple types of electrical rules

enriched with software upgrades. In addition, HyperLynx DRC allows users to incorporate their own design experience rules and allows designers to conduct electrical design rule checks on SiP substrate designs using different electrical standards.

The rules embedded in the current version of HyperLynx DRC include 43 SI rules for signal integrity, 10 PI rules for power integrity, 18 EMI/EMC rules for electromagnetic compatibility, 3 Analog rules for analog circuits, and 8 rules for safety, which cover all possible problems in electronic design.

The Developer can write custom rules in JavaScript or VBScript.

In addition to its rich and extensible rules, HyperLynx DRC provides designers with a powerful checking method that enables software to not only locate errors in a highlighted way, but also report the causes of problems and solutions that can be referenced. Figure 21.42 show examples of several types of electrical rules integrated in HyperLynx DRC.

21.7.2 Examples of Electrical Verification

Here, we use an example of an 8-chip stacked SiP design to briefly introduce the HyperLynx DRC electrical verification process.

The design consists of eight chips stacked on a ceramic substrate, which contains a cavity. The chips are stacked in cavity, and the chips are connected to the substrate by bond wires. The substrate has six layers, two of which are ground layer and the

other four layers are routing layers. The screenshots designed in Xpedition are shown in Fig. 21.43, with 2D view on the left and 3D view on the right.

In Xpedition, select Analysis → Export to HyperLynx DRC from the menu, the system automatically passes the data and opens HyperLynx DRC. First enter the Project Setup Wizard, as shown in Fig. 21.44.

Then click the next button Next below the window and proceed step by step as prompted. The entries we need to set and the settings values in this example are listed in Table 21.1.

After setting, click Finish button Finish to import design data and related parameters into HyperLynx DRC, including layers, components, electrical nets, physical nets, net classes and other design elements, which can be accurately transferred to HyperLynx DRC. As shown in Fig. 21.45.

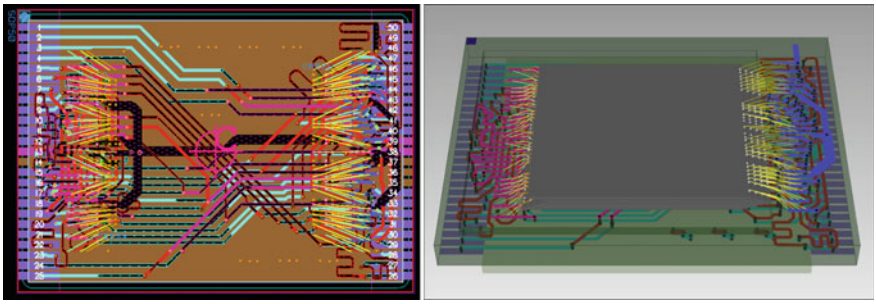

Fig. 21.43 Xpedition design screenshot

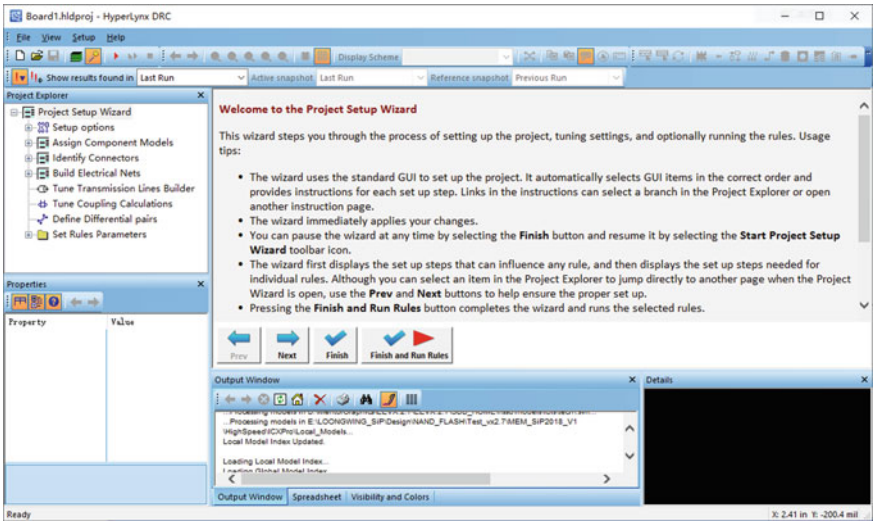

Fig. 21.44 HyperLynx DRC project setup wizard

Table 21.1 HyperLynx DRC parameter settings table

	Setup entries	Set location	Reference value	Note
1	Set project units	Setup → Options → Units	Metric, micron	Others keep the default value
2	Set default values	Setup → Options → Default values	Stackup(); Component(); Electrical Net(50 M, 2 ns, 100 mA, 3.3 V); Physical Net	It mainly sets electrical net parameters, and other parameters can be kept as default
3	Set project paths	Setup → Options → Paths	Local Model Directory = E:\Project\Sim_Models	Related path settings
4	Assign component models	Setup → Options → Models	Assign by part name	Model specific settings
5	Identify connector	/	/	This design does not include
6	Build electric nets	Project Explorer	Frequency (50 M) Voltage (3.3 V)	Mainly set the net frequency and voltage
7	Identify constant nets	Project Explorer	VCC, VSS	Constant net
8	Identify series components	/	/	This design does not include
9	Tune transmission lines builder	Setup → Options → Transmission line	Ground search distance on (100 um), Minimum TLine length (50 um)	Set the distance from normal and minimum transmission line size
10	Tune coupling calculations	Setup → Options → Coupling	Coupling distance (150 um)	Others keep the default value
11	Define differential pairs	/	/	This design does not include
12	Set rule parameters	Project explorer	No change	Keep default

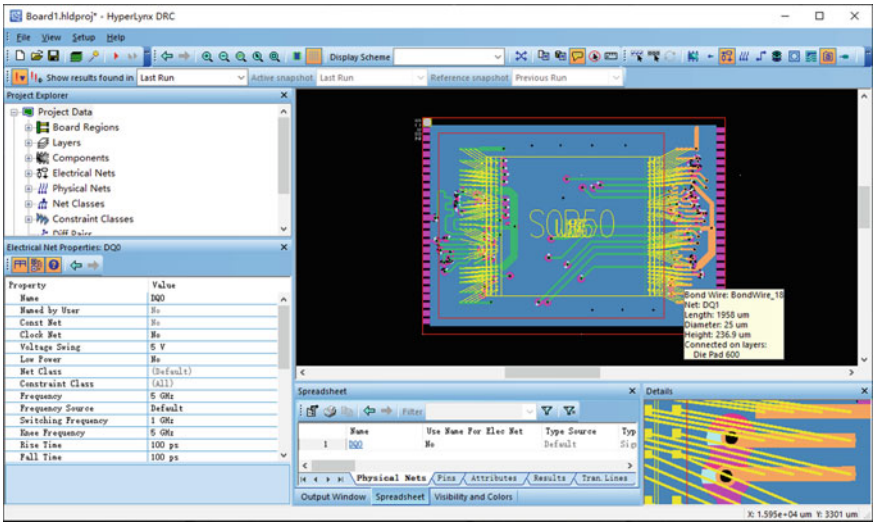

Fig. 21.45 Design is imported to HyperLynx DRC

The current version of HyperLynx DRC contains five categories, a total of 82 rules, which need to be selected according to the characteristics of the design for different complex situations.

Because this design is a digital circuit, we can ignore the Analog rule and choose among SI, PI, EMI and Safety. In this case, we select the following 11 items as examples to check, see Table 21.2. Designers can choose appropriate checks based on the actual situation of their own projects.

When setup is complete, click the Execute Rules button to run rule checking and validation. When the check is complete, expand the Rules rule and we can see that some of the colors of the Check box change to red and some to green, red indicates that the Rules failed the DRC rule check, and green indicates that the rule passed the DRC rule check.

Below, we will elaborate on the checks in Table 21.2.

(1) In the SI category, we select three check items.

The termination check and trace shielding checks passed, and many vias checks failed. There was an error because the number of vias in some nets exceeded the set value. Expand the inspection results in Project Explorer and select the corresponding entries. The selected net will be highlighted. In the spreadsheet below the window, we can view the number of vias of the net, as shown in Fig. 21.46.

The solutions to this problem are as follows: ① Modify the problem net in Xpedition to reduce the number of vias. ② If the net is not a high-speed net, check conditions can be relaxed, such as changing the maximum allowable number of vias in the net to 10, such nets can pass check. Readers can choose based on the actual situation of their own projects.

Table 21.2 Check item status in this example

Check categories	Check items	Pass or not	Problem analysis	Resolvent
SI	Termination check	Pass	/	/
	Trace shielding	Pass	/	/
	Many vias	Error	The number of holes exceeded the set value	Modify design/change settings
PI	Power/Ground width	Warning	Part of the line width is less than the set value	Allowable
	Ground layer	Pass	/	/
	PDN via count	Pass	/	/
EMI	Net crossing gaps	Pass	/	/
	Return path	Pass	/	/
	Via sub length	Pass	/	/
Safety	Multi-layers creepage distance	Setup error	The design is recognized as Rigid Flex and cannot be checked for	Skip check
	Same-layer creepage distance	Setup error	The same as above	Skip check

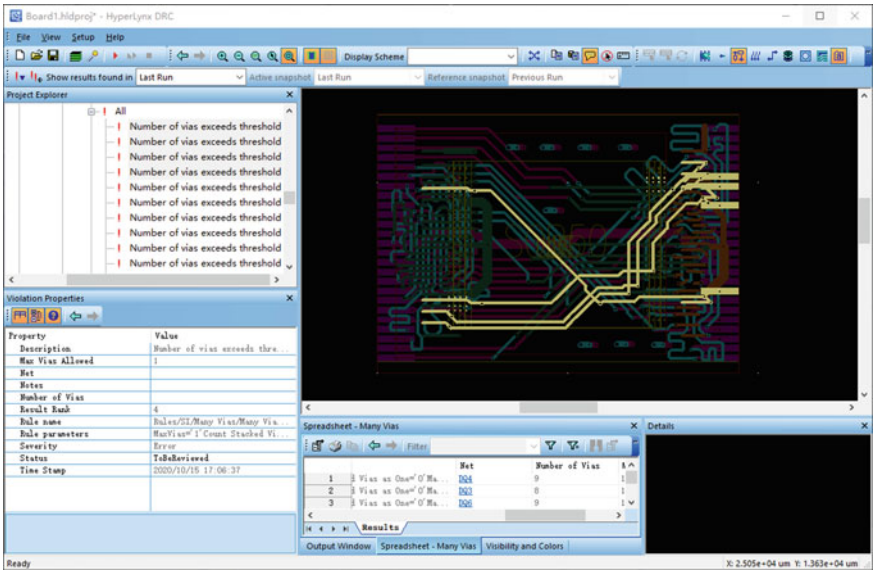

Fig. 21.46 Rules violation net highlighting

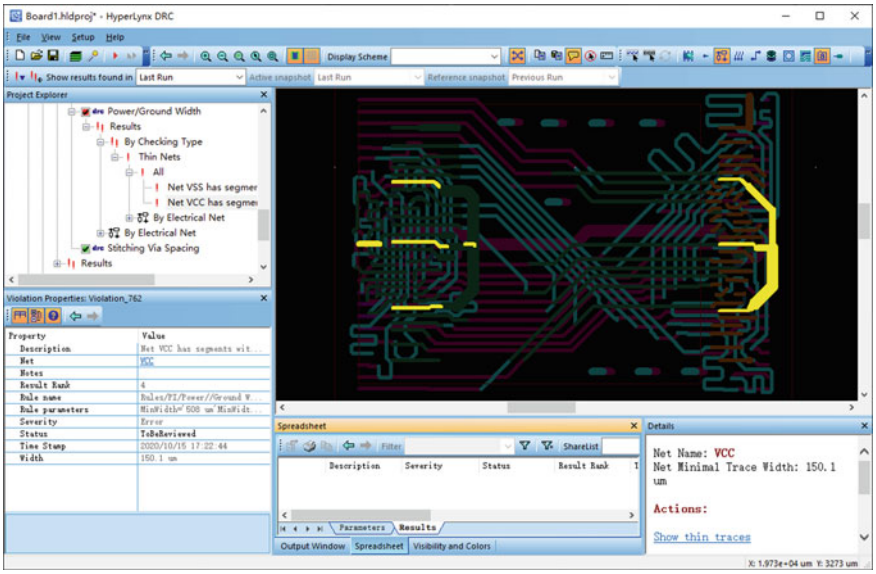

Fig. 21.47 Net VCC segment width warning

(2) In the PI category, we selected three checks.

The Ground Layer and PDN Via Count checks passed, the Power/Ground Width checks failed, and there was a warning because some trace widths of the VCC and VSS were smaller than the set values.

Expand the results of the check in Project Explorer and select the appropriate entry, and the selected net will be highlighted. The parts of the VCC net widths below the set values shown in Fig. 21.47 are highlighted.

This problem is usually caused by local inconsistencies between rule settings and actual conditions. For example, for power and ground nets, designers want to increase the widths as much as possible, so in rule settings, widths are set as wide as possible, which is acceptable in most areas, but in some areas of higher density, even in some Bond Finger or where the width of the pad itself is less than the set value, the widths need to be reduced manually. Because these areas are usually smaller and such segments are shorter, they do not affect the design and are generally allowed.

By clicking the Enable Crossprobing button in the HyperLynx DRC window, HyperLynx DRC can perform design interaction checks with Xpedition. Selecting any net in HyperLynx DRC will also be selected and highlighted in Xpedition, which increases the convenience of interactive checking and facilitates timely modification of the problem net in Xpedition, as shown in Fig. 21.48.

(3) In the EMI category, we selected three checks, Net Crossing Gaps, Return Path, and Via Sub Length, all pass.

(4) In the Safety category, we selected two checks, Multi-layers Creepage Distance and Same-layer Creepage Distance, which failed because the design type

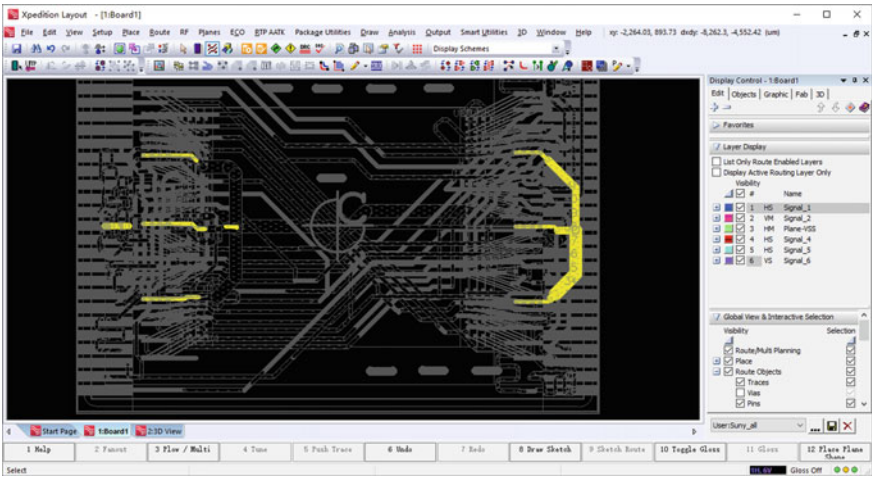

Fig. 21.48 Design interactive check in Xpedition

was not appropriate. Considering that the design voltage is relatively low, the problem of violating the rules will not occur in general, so the Safety category can be ignored in this case.

Let's conclude:

(1) HyperLynx DRC contains five broad classes and 82 rules, which will be enriched with software upgrades and allow users to customize rules. Because the actual designs vary widely, HyperLynx DRC has a rich set of rules to provide a more comprehensive coverage of all situations. Not all rules are appropriate for a specific project. Designers need to choose the appropriate inspection items, and understand the purpose of the inspection items and set the parameters correctly.

(2) Whether all selected checks should pass the checks, this is a specific problem to be analyzed, and the problems that affect the performance and reliability of the product must be modified before re-checking. For some warnings or errors due to setup reasons, we can modify the parameters of the check and re-check until it passes. In addition, some warnings that have little impact on the design can be accepted or ignored, and be noticed in the next design and promoted gradually.

21.8 HDAP Physical Verification

Before HDAP physical verification for high density Advanced Packaging, many people will have a question. After the design is completed, we have already done DRC

checking in the packaging design tool. The rules I set can also meet the requirements of the process. Why do I need to do physical verification specifically?

This is actually closely related to the characteristics of HDAP. In layout design tool Layout301and XPD, the embedded DRC checking tools are sufficient to assist designers in checking and validating for traditional package.

For the 3D and 2.5D of HDAP, due to the use of silicon technology, its density and complexity are increasing, and its production process and IC process also have a gradual trend of integration. Traditional DRC tools have been difficult to meet their physical verification needs, and special verification tools are needed. These tools are usually derived and reconfigured from IC Verification tools, such as Calibre 3DSTACK provided by Siemens EDA.

21.8.1 Introduction to Calibre 3DSTACK

Calibre is the industry's most influential IC layout verification tool, because of the integration of IC design and HDAP design, and the need for 3D and 2.5D integration on silicon materials for RDL and TSV. Therefore, Calibre 3D STACK has been developed specifically for 3D and 2.5D integrated design.

Calibre 3DSTACK extends physical verification at the Calibre chip level to allow full verification of various 2.5D and 3D stacked chips. With Calibre 3DSTACK, designers can perform DRC and LVS checks on a complete multichip system at any process node without disrupting the current tool flow or requiring new data formats, thus greatly reducing the time required for production output. Since 3D STACK uses standard Calibre DRC, Calibre LVS, and Calibre Design Rev features, no new license is required.

Although standard Calibre supports wafer factory certified design rule checking (DRC) and comparing the layout of individual chips to the schematic (LVS), Calibre 3DSTACK extends Calibre's chip-level signature verification capabilities to allow full design verification of stacked chip components. Calibre 3DSTACK can be used to validate stacked chip components such as 3D stacked memory, stacked sensor arrays, 2.5D structure, or WLP wafer-level packaging.

Calibre 3DSTACK performs all DRC and LVS checks based on the package information in the rule set (stacking order, x/y position, rotation, direction, etc.) for the interface geometry between chip designs, including bumps, BGA solder balls, TSV, or copper-to-copper bonding, and supports chips with different process flows.

Traditional DRC and LVS validation tools assume that layers are coplanar, that is, polygons on the same GDSII layer are on the same vertical plane. The 2.5D and 3D integrated structures contain multiple chips, which may be graphics on the same GDSII layer, but represent completely different geometries at different vertical depths. When validating 2.5D and 3D designs with traditional tools, layer conflicts may occur between multiple chips with the same GDSII layer.

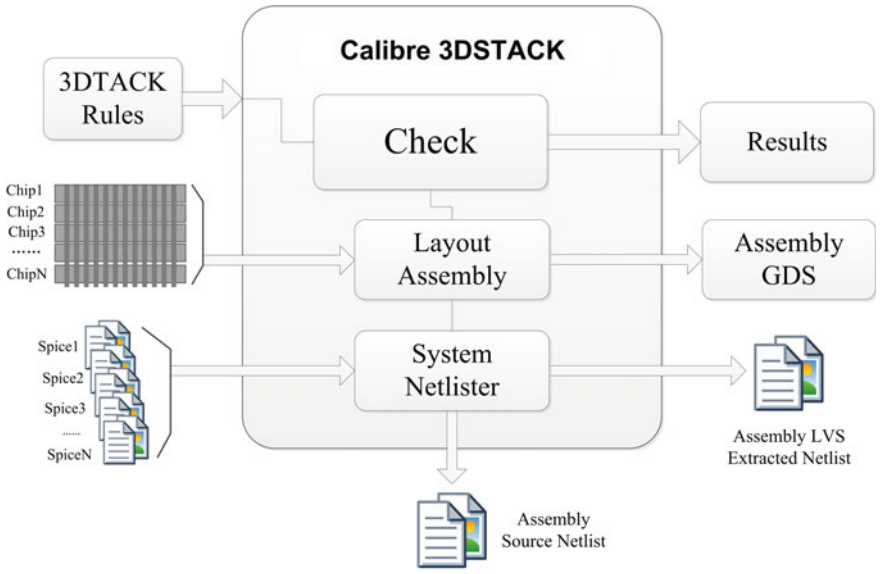

Fig. 21.49 Calibre 3DSTACK function block diagram

Calibre 3DSTACK uniquely identifies the geometry of each chip placement layer in the component, allowing precise inspection between the chips. By supporting flexible stacking configurations for multiple chips, Calibre 3DSTACK minimizes interference with existing validation processes, while providing maximum flexibility for designers across process nodes and stacking configurations (2.5D and 3D). Calibre 3dstack can distinguish the layers placed on each chip, so that designers can verify the physical properties of each chip (offset, scaling, rotation, etc.), and track the connection between interposer or chip to chip interface. Calibre 3DSTACK provides scalability to integrate new extraction and validation solutions in the future.

The function block of Calibre 3DSTACK is shown in Fig. 21.49.

21.8.2 HDAP Physical Verification Example

Next, we use HDAP design example to briefly introduce Calibre 3DSTACK physical verification process.

First, it is important to note that Calibre 3DSTACK can only run in UNIX or Linux environments at present. In order to work with XSI or XPD, it is better to install XSI and XPD in Linux environment with Calibre 3DSTACK, or install XSI or XPD in Windows environment, and install Calibre 3DSTACK in Linux environment to solve this problem.

Next, the author introduces the process of HDAP physical verification in RHEL7 virtual machine environment together with windows environment. If windows environment can support we operate in windows, otherwise it can be operated in RHEL7 Linux environment.

1. Configure Calibre 3DSTACK Wizard

First, we use the HBM-HDAP designed in Chap. 19 of this book as an example to configure Calibre 3DSTACK, which includes two floorplan, interposer and substrate, and the interposer Floorplan is shown in Fig. 21.50.

In XSI, select package utilities → Calibre 3DSTACK wizard from the menu, and the window as shown in Fig. 21.51 will pop up.

In XSI Calibre 3DSTACK wizard window, select tools → property manager from the menu, and the window as shown in Fig. 21.52 will pop up. Select interposer and select 3DSTACK → design… from the menu in this window. Add the following properties and values to the interposer.

Then, in property manager, select substrate and select 3DSTACK → Design → Exclude → Yes from the menu. This function is to exclude substrate from this verification. Select the interposer and choose 3DSTACK → Design → Exclude → No from the menu to include the interposer in this verification. Then, close the property manager and return to the XSI Calibre 3DSTACK wizard window.

2. Generate Calibre 3DSTACK file

First, we start with assembly connection, including chip assembly file, interposer assembly file and chip TCL file. In 3DSTACK wizard, select assembly connection TAB, select the Die Assembly option, and then click generate to get the file shown in the box on the right side of the figure below, as shown in Fig. 21.53.

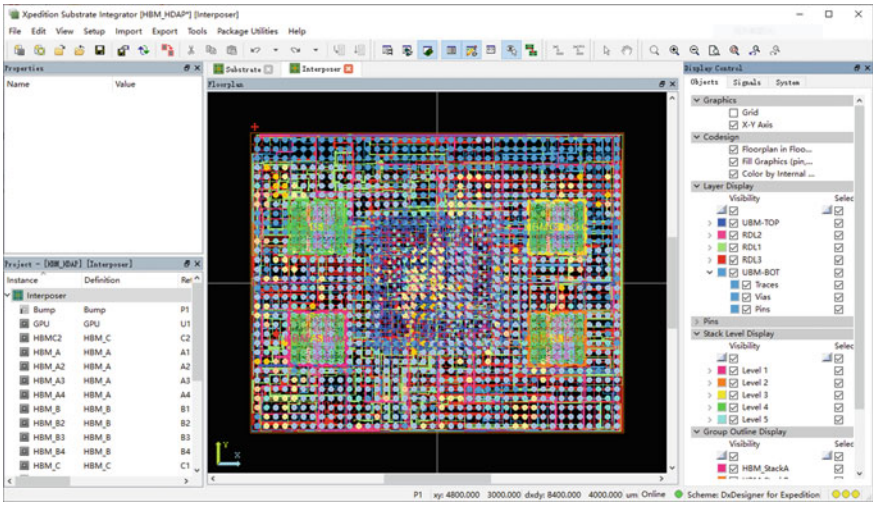

Fig. 21.50 Interposer floorplan in XSI

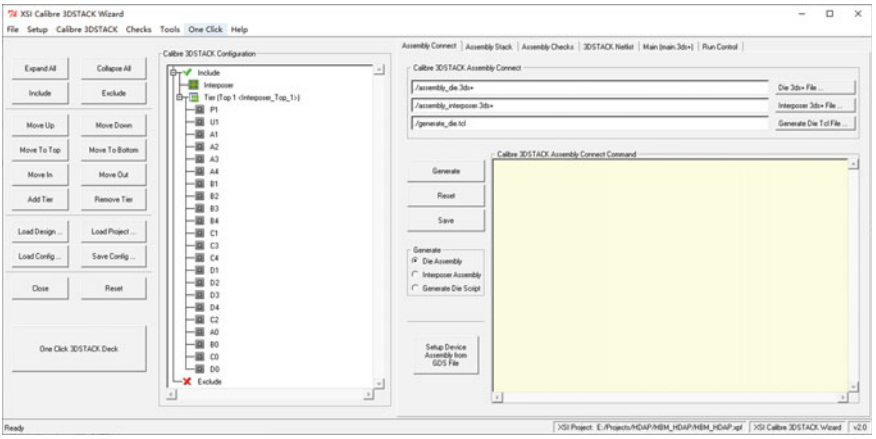

Fig. 21.51 Startup XSI Calibre 3DSTACK wizard

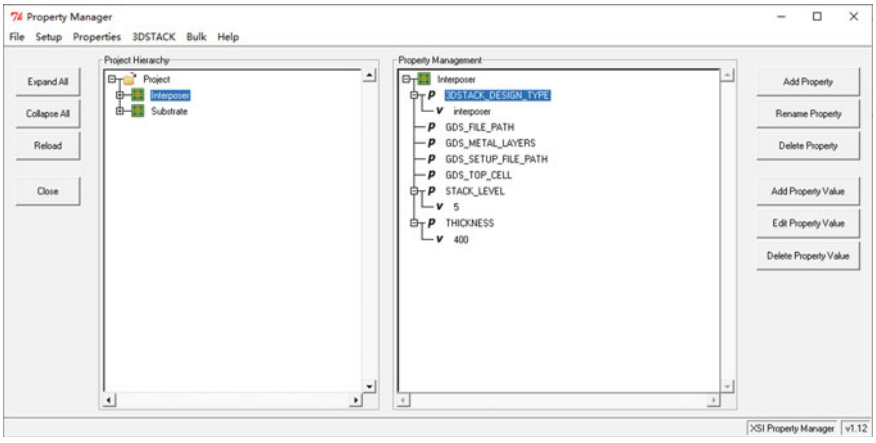

Fig. 21.52 Add properties and values to interposer

Then, select Interposer Assembly and generate Die Script Options respectively, and then click the generate button to get two files as shown in Fig. 21.54.

In the same way, switch to the Assembly Stack TAB and Assembly Checks TAB, and generate the corresponding file through the Generate button, as shown in Fig. 21.55.

Then, switch to the 3DSTACK Netlist TAB, generate Calibre 3DSTACK Netlist file, which is saved in the 3DSTACK directory under the design, as shown in Fig. 21.56.

Then, switch to main (main.3ds+) TAB, select all 3ds+ files, generate Main.3ds+ File and save it with the Save button, as shown in Fig. 21.57.

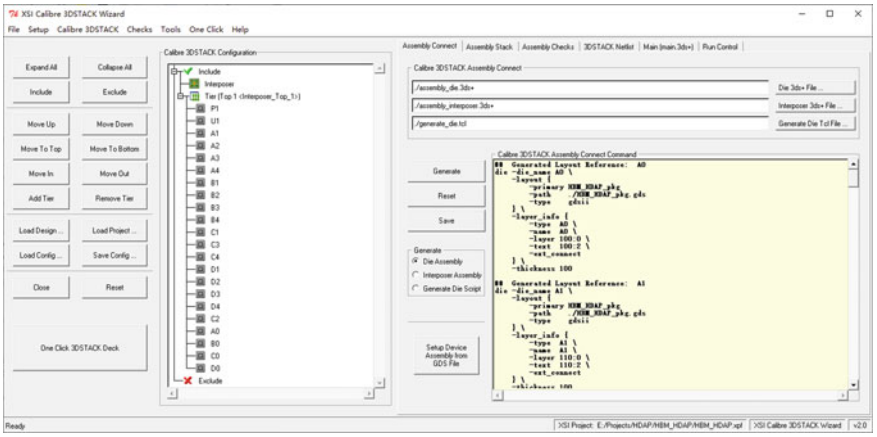

Fig. 21.53 Generate die assembly file

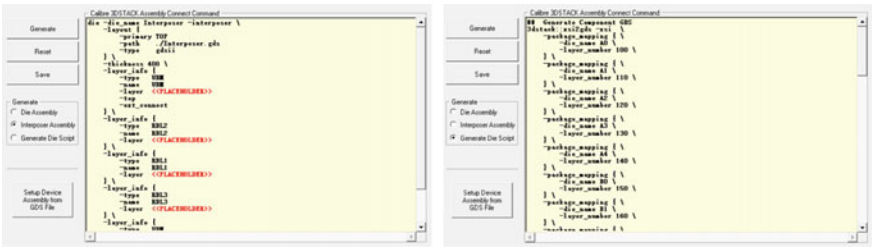

Fig. 21.54 Generate interposer assembly and die script files

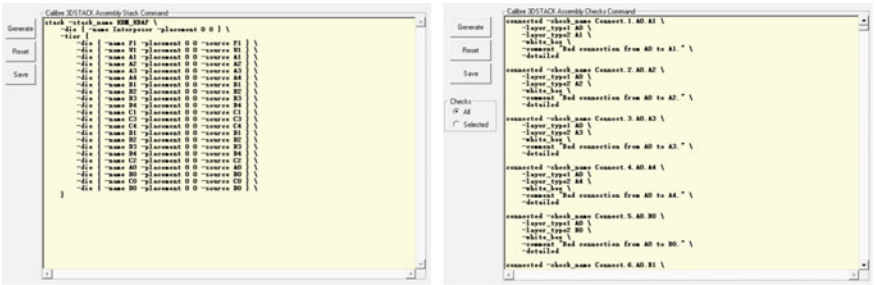

Fig. 21.55 Generate assembly stack and assembly checks files

Then, switch to Run Control TAB and generate run.sh, clean.sh, specs.svrf file, and save it by the Save button, as shown in Fig. 21.58.

Hereto, all the required files have been generated and saved in the 3DSTACK folder, as shown in Fig. 21.59.

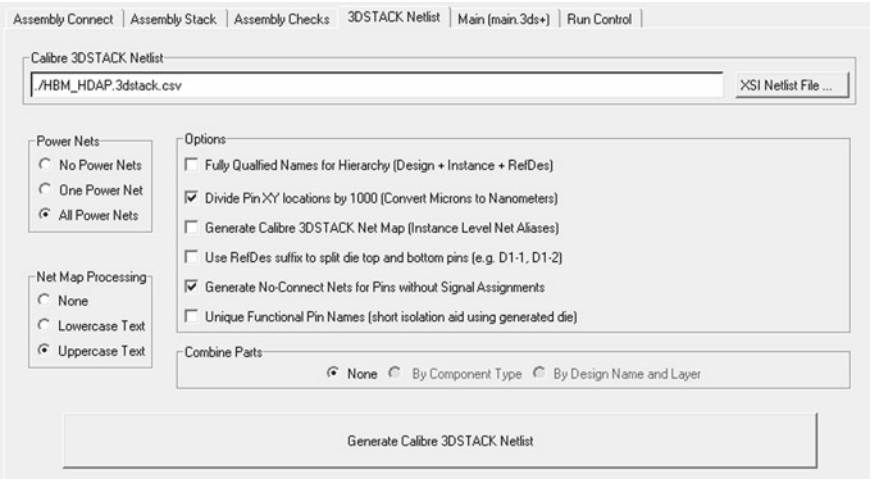

Fig. 21.56 Generate Calibre 3DSTACK netlist files

Fig. 21.57 Generate Main.3ds+ file

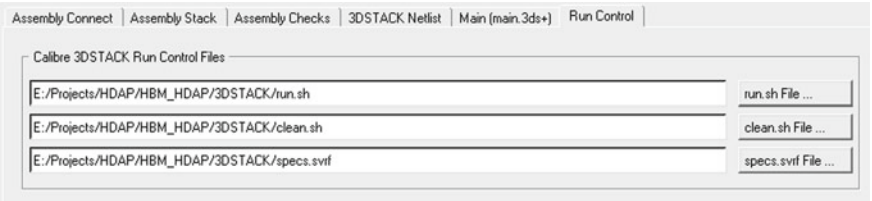

Fig. 21.58 Generate run.sh, clean.sh, specs.svrf file

All the above files are generated manually. After the designer is familiar with the function and process of each file, he can also generate all the files by pressing the "One Click 3DSTACK Deck" button at the bottom left of the window.

In addition to the above generated files, GDS files need to be generated in the design for Calibre inspection and verification. For the generation of GDS file, please refer to Chap. 20. After all the required files are generated, the next step is to physically verify the design through Calibre 3DSTACK.

3. Use Calibre 3DSTACK for Physical Verification

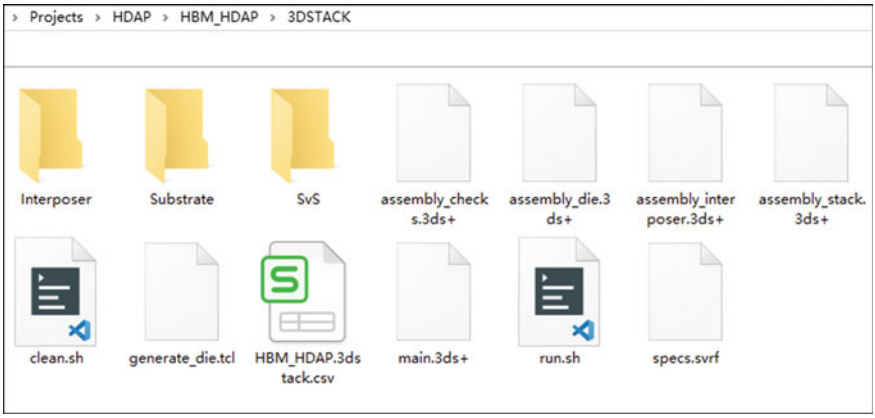

Fig. 21.59 The generated files are saved in the 3DSTACK folder

Copy the entire design folder to the Linux environment, start terminal and switch to the 3DSTACK folder under the design, and start Calibre 3DSTACK by calling./run.sh the script file.

The system automatically checks and validates the design, and Calibre DESIGNrev and RVE (Results Viewing Environment) environments start after verification is complete. View the design in Calibre DESIGNrev, as shown in Fig. 21.60.

Look at 3dstack.rdb and 3DSTACK Report in CalibreRVE, and 3dstack.rdb checks pass in this design. As shown in Fig. 21.61a, the 3D STACK Report is correct, as shown in of Fig. 21.61b.

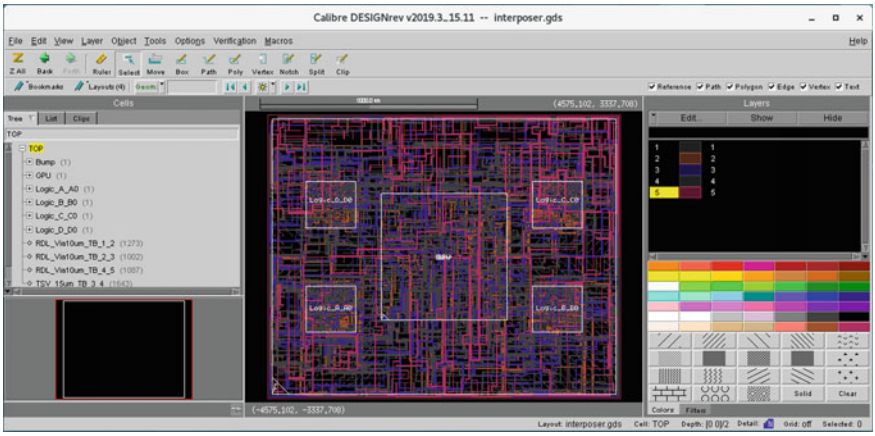

Fig. 21.60 Verify interposer design in Calibre DESIGNrev

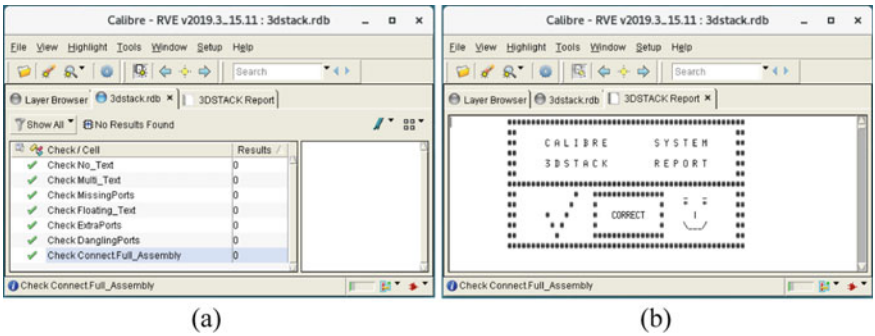

Fig. 21.61 View inspection report in Calibre RVE

In addition to verification for a single layout, we can also validate multiple layouts at the same time. For example, the design includes two layouts, Interposer and Substrate. When generating a 3DSTACK file, both layouts need to be included.

In Property Manager, select Interposer and menu select 3DSTACK → Design → Exclude → No, then select Substrate and menu select 3DSTACK → Design → Exclude → No, to include both Substrate and Interposer in verification.

Close the Property Manager, return to the XSI Calibre 3DSTACK Wizard window, and generate all files with "One Click 3DSTACK Deck" button, then perform a similar check above.

In the 3DSTACK folder, start Calibre 3DSTACK by calling the script file./run.sh.

The system automatically checks and validates the design, and the Calibre DESIGNrev and Calibre RVE environments start after the validation is complete. View the design in Calibre DESIGNrev, as shown in Fig. 21.62. Then, look at 3dstack.rdb and 3DSTACK Report in Calibre RVE.

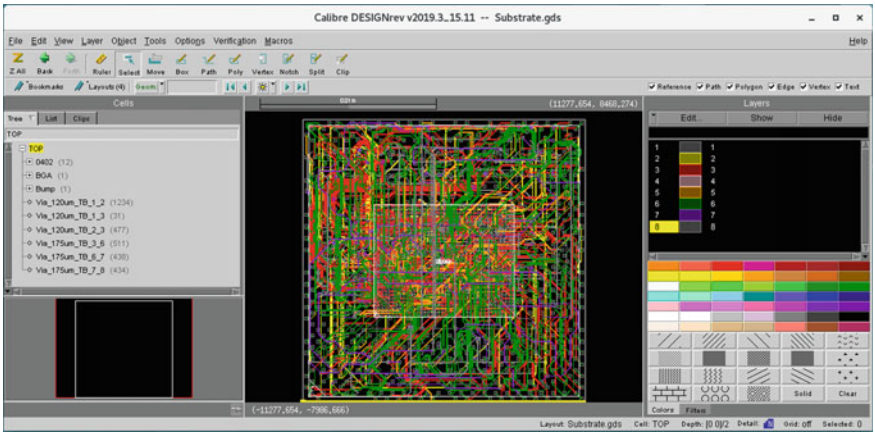

Fig. 21.62 Verify the overall design in Calibre

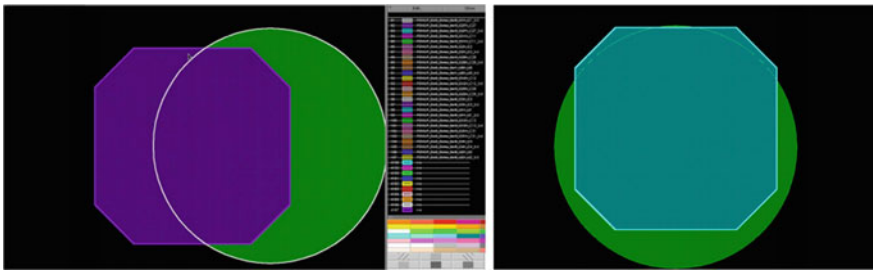

Fig. 21.63 Perform pad overlap check in Calibre

In addition to the above checks and verifications, there are many checks that can be performed in Calibre, such as routing sharp angle checks, routing density checks, connectivity checks, Pad center alignment checks, Pad overlap checks, and so on.

Due to the size of the chapter, we do not cover each of them. Readers can refer to the user guide of Calibre software.

Figure 21.63 show a report screenshot of dislocation of upper and lower pads in a chip stack during Calibre Pad overlap check in a project. By this kind of check, we can find out the upper and lower misalignment caused by library building among the devices in chip stack in 3D design or avoid the misalignment between the pin of the chip and the Interposer pad in 2.5D design.

With the complete physical verification function of Calibre 3DSTACK, we can effectively ensure the correctness and reliability of the design output data, thus improving the one-time success rate of product development.