AVP Control Method for an Improved Phase Shifted Full Bridge Soft Switching DC-DC Converter

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Abstract. This paper proposes an adaptive voltage position (AVP) control method for the improved phase shift full bridge (PSFB) soft switching DC-DC converter. For the improved topology, clamping diodes and resonant inductor are added. All power Mosfets can achieve soft switching at full load conditions and since clamping di-odes are utilized, the voltage oscillation of the output rectifier diodes can be de-creased. In order to improve the output voltage response ability of the converter in the process of load conversion, An AVP control method based on output cur-rent feedback regulation is proposed. Working principle of the topology and control method are introduced. Small signal model and controller design process are analyzed. Performance of the proposed control method and topology are verified by a 500W simulation model.

Keywords: AVP control · Improved PSFB · ZVS · DC-DC converter · Output current feedback regulation

1 Introduction

With the development of industrial facilities, military equipment, microprocessors and industrial server more and more equipment or devices show the characteristics of load mutation [1–4]. In addition, there are a lot of pulse loads in the application of communication power supply, vehicle power supply and ship power supply system. The power required by the pulse load is constantly changing, the current change rate di/dt is very high, and the change of load current has a certain periodic characteristics. When the pulse load is running, the output voltage of power supply system should be stable enough, and the voltage overshoot caused by load current mutation should be within the allowable working voltage range of load. Thus these applications put forward higher requirements for the performance of switching power supply. It is necessary to design better DC/DC converter to meet the increasing dynamic response requirements of the output load.

In order to reduce the output voltage overshoot or drop, the traditional method of increasing the output filter capacitor will not only increase the cost, but the power density is reduced. In order to improve the dynamic response without additional output capacitance, many control methods and circuit structures are proposed. In [5, 6], hysteresis

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control is proposed, in [7, 8] V2 control is analysed and in [9] interleaving technology is introduced.

Among all kinds of technologies, the method of improving dynamic performance by optimizing control strategy is widely concerned, such as AVP control. AVP control strategy is often utilized to reduce the output voltage fluctuation in the process of load conversion without adding output filter capacitance [10–12]. Figure 1 depicts the waveforms of the output voltages of the converter which applied with and without AVP control method.

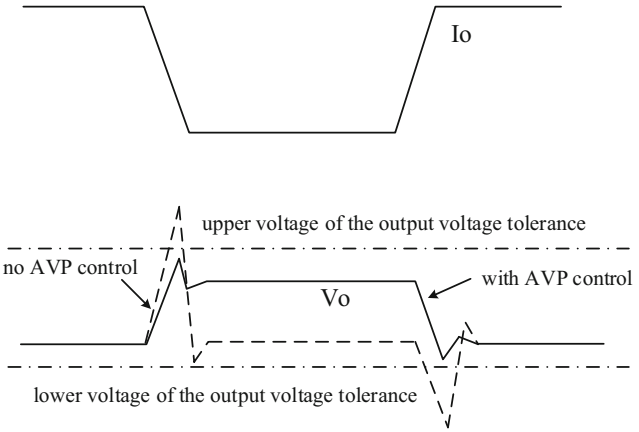


Fig. 1. Output current and output voltage of the converter with/without AVP control

At present, the research of the AVP control method is mainly based on Buck topology [10–12]. Thus, the AVP control algorithm applied to other circuit topologies needs to be studied. In low voltage and high current applications, in order to achieve electrical isolation between input and output side of the converter, phase shifted full bridge circuit topology is often used, as shown in Fig. 2.

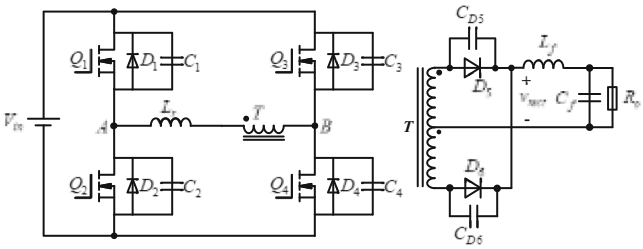


Fig. 2. Phase shifted full bridge circuit topology

As shown in Fig. 2, through reasonable design of L_r, the power switches can achieve ZVS at rated load conditions. However, in this topology, the lagging lag has narrow soft

switching range, and voltage oscillation across rectifier diodes are not reduced. In order to broaden the soft switching range, an resonance network is added in [13]. However the voltage spikes of the diodes still not be solved. To reduce voltage spikes, snubbed circuits [14, 15] have been utilized. However the circuit topology is complex.

In this paper, a phase shift full bridge soft switching DC-DC converter based on clamping diodes is introduced. The AVP control method based on output current feedback regulation which applied on DC-DC converter is proposed and studied. The working principle of the topology and the control method are analysed. The small signal model and the controller design process are presented. And the performance of the new control system is verified by 500W simulated prototype.

2 System Configuration

Figure 3 shows the improved topology and the AVP control method. As it shown, T is the transformer of the topology. On the primary side of topology, v_{in} is the input voltage, v_o and i_o is the output voltage and output current, respectively; Q_1–Q_4 are the power switches of the converter; D_1–D_4 and C_1–C_4 are the parasitic diode and junction capacitance of Q_1–Q_4, respectively; L_r is the resonant inductor and D_7–D_8 is the clamping diodes. On the second side of topology, D_5, D_6 are the rectifier diode and C_{d5}, C_{d6} are the absorption capacitance of the diodes. L_f and C_f is the output filter inductance and capacitor; R_o is the output load.

For the control circuit, Z_2 is sampling coefficient of output feedback voltage; i_r is the output current adjustment feedback reference; v_{dr} is output voltage droop adjustment signal; v_{ref} is the output voltage given signal; Z_f is compensation coefficient of output voltage control loop; v_c is the output signal of the control loop; PSR is phase shift regulating circuit and d_1–d_4 are the duty cycle adjustment signal.

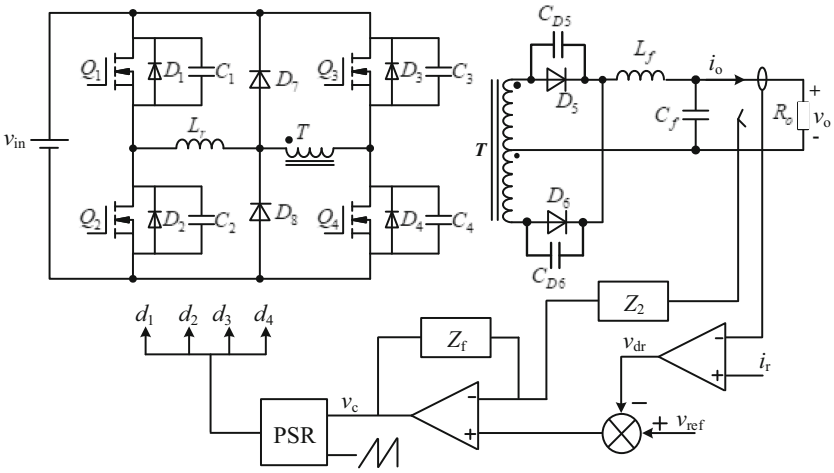


Fig. 3. The proposed system configuration

3 Introduction

3.1 DC/DC Topology Operation Principle

There are 18 operating modes in each cycle. Compared with the traditional phase shifted full bridge converter, it mainly increases the conduction modes of the two clamping diodes. Since the principle of other modes is basically the same as that of traditional converter, this paper only analyses the working principle of the two clamping diodes conduction modes. The equivalent circuit of each mode are shown in the following Fig. 4.

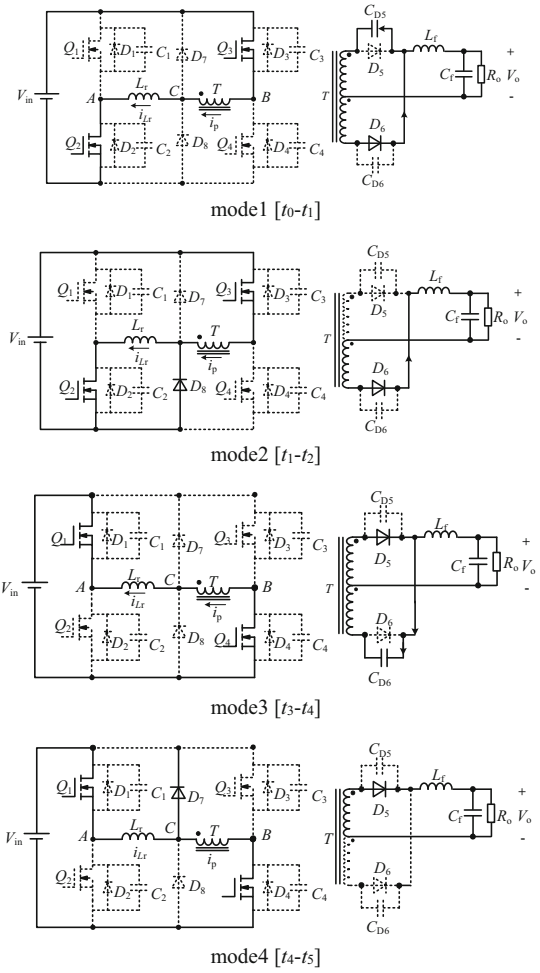


Fig. 4. Equivalent circuit diagram of clamping diode switching process

In the analysis, assume that: rectifier diode is regarded as the ideal diode; other devices, such as inductors and capacitors, are ideal components, and the leakage inductance of transformer is ignored; $L_f \gg L_r/N^2$, where N is the turn ratio of the primary and secondary sides of the transformer;

At t_0, D_5 turns off and D_6 turns on. L_r resonates with C_{D5} and C_{D5} is charged. i_p and i_{Lr} continue to increase in the opposite direction.

During the period of [t_0-t_1], the potential of point B is always equal to the input voltage v_{in}. Due to the continuous accumulation of electric charge of C_{D5}, v_{BC} increases. Thus the potential at point C decreases continuously. At t_1, the voltage across C_{D5} is charged to $2v_{in}/N$. At this point, the potential of point C drops to zero, D_8 is clamped, and v_{BC} is clamped to v_{in}.

At t_1, D_8 turns on and provides current channel. The primary current i_p of transformer is reduced to the value of which i_{Lf} converted to the primary side. After that, i_p begins to increase in negative direction, while the resonant inductor current i_{Lr} remains constant. And the current difference between i_p and i_{Lr} flows through the clamping diode D_8 during this period. At t_2, the primary current i_p of the transformer increases to value of the resonant inductor current i_{Lr}, and at this moment D_8 turns off.

During the period of [t_3–t_4], the potential of point B is equal to zero. Due to the continuous accumulation of electric charge of C_{D6}, v_{CB} increases. Thus the potential at point C rises continuously. At t_4, the voltage across C_{D6} is charged to $2v_{in}/N$. At this point, the potential of point C rises to v_{in}, D_7 turns on, and v_{CB} is clamped to v_{in}.

At t_4, D_7 turns on and provides current channel. The primary current i_p of transformer is reduced to the value of which i_{Lf} converted to the primary side. After that, i_p begins to increase in positive direction, while the resonant inductor current i_{Lr} remains constant. And the current difference between i_p and i_{Lr} flows through the clamping diode D_7 during this period. At t_5, the primary current i_p of the transformer increases to value of the resonant inductor current i_{Lr}, and at this moment D_7 turns off.

It can be seen from the above analysis that the clamping diodes D_7 and D_8 only conduct once in a switching cycle.

3.2 AVP Control Method Operation Principle

As shown in Fig. 5, when $i_o > i_r$, it indicates that it is a heavy load. At this moment, through comparator, adjust the output voltage droop signal value to zero. When $i_o < i_r$, it indicates that it is a light load. At this moment, through comparator, adjust the output voltage droop signal value v_{dr} to negative direction. Then the output voltage droop signal value v_{dr} is overlaid to the output voltage given value to form a new output voltage given signal v_{ref_H}. The output voltage controller makes the output voltage v_o of the converter follow the given signal to realize AVP control.

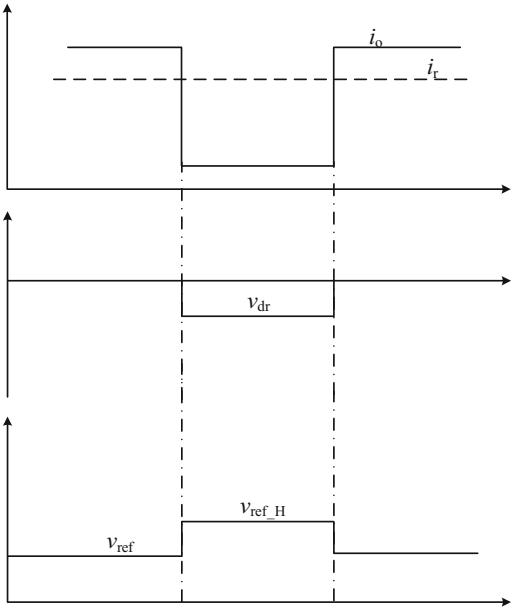


Fig. 5. Operation principle of AVP control

4 Control Design Process

4.1 Small Signal Model

The phase shifted full bridge ZVS PWM converter is a buck type converter. So its small signal model is similar to buck circuit. The difference is that the phase-shifting full bridge ZVS PWM converter causes the loss of duty cycle when soft switch is realized.

The small signal model of buck converter is depicted as follows.

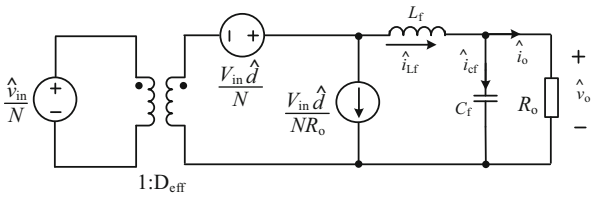


Fig. 6. Operation principle of AVP control

In Fig. 6, $\hat{v}_{in}$ is the small signal disturbance value of input voltage; $\hat{d}$ is the small signal disturbance value of duty cycle; $\hat{i}_{Lf}$ is the small signal disturbance value of inductance current; $\hat{i}_{Cf}$ is the small signal disturbance of charge/discharge current of C_f; $\hat{i}_o$, $\hat{v}_o$ is the small signal disturbance value of output current and voltage; D_{eff} is equivalent duty cycle of converter.

The equivalent duty cycle of PSFB converter is as follows.

$$D_{\text{eff}} = D - \frac{2L_r}{NV_{\text{in}}T}\left[2I_{\text{Lf}} - \frac{V_{\text{o}}}{L_{\text{f}}}(1-D)\frac{T}{2}\right] \tag{1}$$

As can be seen from (1), the factors that affect D_{eff} are as follows: Duty cycle D of original buck topology; input voltage v_{in} and the output filter inductor average current i_{Lf}.

The above formula is disturbed,

$$\begin{cases} \hat{d}_{\text{d}} = \left(1 - \frac{L_{\text{r}}}{N^2 L_{\text{f}}} D_{\text{eff}}\right)\hat{d} \approx \hat{d} \\ \hat{d}_{\text{v}} = \frac{4L_{\text{r}}f_{\text{s}}I_{\text{Lf}}}{NV_{\text{in}}^2}\hat{v}_{\text{i1}} \\ \hat{d}_{\text{i}} = -\frac{4L_{\text{r}}f_{\text{s}}}{NV_{\text{in}}}\hat{i}_{\text{Lf}} \end{cases} \tag{2}$$

Thus, the small signal model of phase shifted full bridge soft switching PWM converter can be obtained, as shown in Fig. 7.

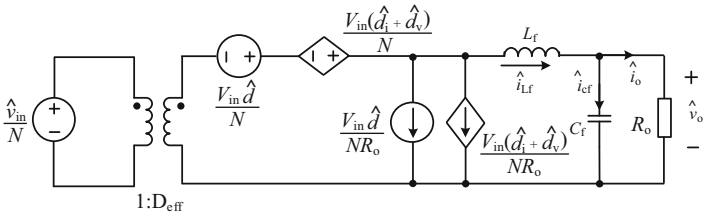


Fig. 7. Phase shifted full bridge soft switching small signal model

4.2 Control Design Process

According to the small signal model, the circuit topology related transfer functions are calculated as follows.

Transfer function $G_{\text{vd}}(\text{s})$ of duty cycle $\hat{d}(s)$ to output voltage $\hat{v}_o(s)$ is shown as follows.

$$G_{\text{vd}}(s) = \frac{V_{\text{in}}/N}{s^2 L_{\text{f}}C_{\text{f}} + s\left(\frac{L_{\text{f}}}{R_{\text{o}}} + R_{\text{s}}C_{\text{f}}\right) + \frac{R_{\text{s}}}{R_{\text{o}}} + 1} \tag{3}$$

where, $R_{\text{s}} = 2L_{\text{r}}f_{\text{r}}/N^2, f_{\text{r}} = 2/T_{\text{s}}$.

Transfer function $\text{G}_{\text{id}}(\text{s})$ of duty cycle $\hat{d}(s)$ to output current $\hat{i}_o(s)$ is shown as follows.

$$G_{\mathrm{id}}(s) = \frac{\left[s^2 L_{\mathrm{f}} C_{\mathrm{f}} + s\left(\frac{L_{\mathrm{f}}}{R_{\mathrm{o}}} + R_{\mathrm{o}} C_{\mathrm{f}}\right) + 1\right] V_{\mathrm{in}}/NR_{\mathrm{o}}}{s^2 L_{\mathrm{f}} C_{\mathrm{f}} + s\left(\frac{L_{\mathrm{f}}}{R_{\mathrm{o}}} + R_{\mathrm{s}} C_{\mathrm{f}}\right) + \frac{R_{\mathrm{s}}}{R_{\mathrm{o}}} + 1} \tag{4}$$

According to the small signal model and the related transfer function, the control loop diagram of the proposed control system is shown in Fig. 8.

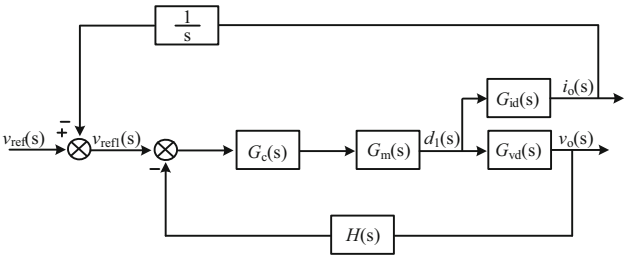


Fig. 8. Control loop diagram

As shown in Fig. 8, $G_{\mathrm{c}}(s)$ is the Transfer function of compensation controller; $G_{\mathrm{m}}(s)$ is the transfer function of pulse width modulator; $H(s)$ is the output voltage feedback sampling coefficient.

According to the control loop diagram, the open loop transfer function is deducted as follows.

$$G(s) = G_{\mathrm{c}}(s) G_{\mathrm{m}}(s) G_{\mathrm{vd}}(s) H_1(s) \tag{5}$$

where $G_{\mathrm{m}} = 1/V_{\mathrm{m}}$, V_{m} is the peak value of the saw tooth wave.

According to the compensation principle of the feedback controller, the cut-off frequency is 1/5–1/10 of the switching frequency, and the phase angle margin is 30°–60°. Based on the zero pole compensation principle, the PI controller is designed. The amplitude frequency and phase frequency characteristics of the system after correction are shown in Fig. 9.

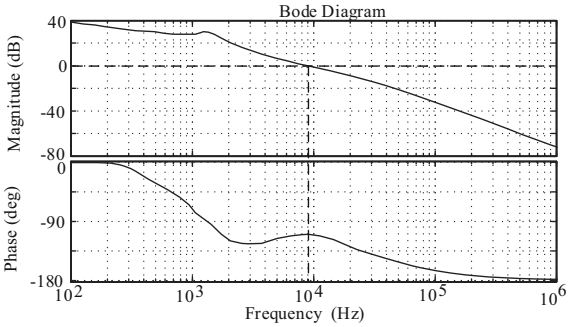
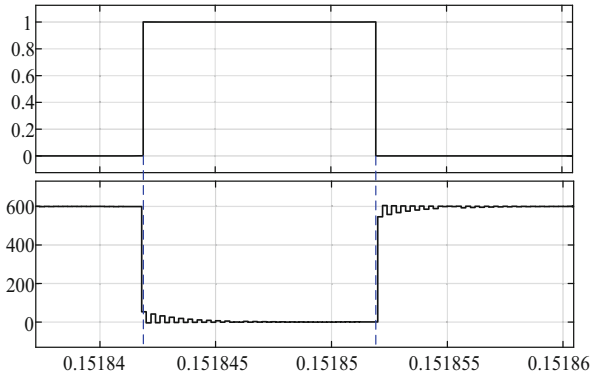


Fig. 9. Bode diagram after compensation

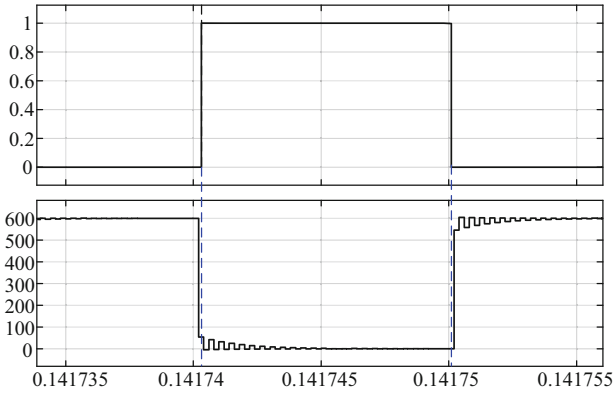
5 Simulation Results

On the basis of the above design, a simulation module was built. The simulation design parameters are as follows: $v_{in} = 600V$. $v_o = 48V$. Under light load condition, the output current is 5A and under heavy load condition, the output current is 10A.

Figure 10 shows the soft switching conditions of the main power switch in AVP control mode under heavy load condition.



(a) driving and voltage waveform of lead leg switch



(b) driving and voltage waveform of lagging leg switch

Fig. 10. The soft switching conditions of the main power switch

As shown in Fig. 10, under the condition of heavy load, zero voltage switching (ZVS) can be realized in both lead leg and lag leg.

The simulation waveform of voltage across the rectifier diodes on second side of the converter is shown in Fig. 11.

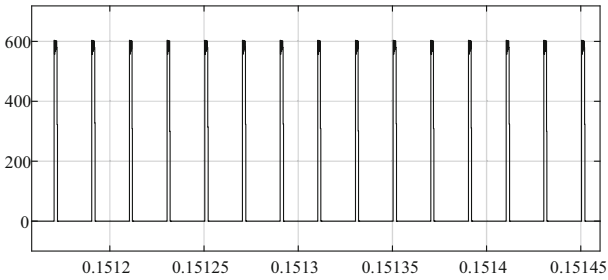


Fig. 11. The soft switching conditions of the main power switch

According to the above simulation waveform, the voltage spike across the rectifier diodes is reduced and clamped to input voltage.

In Fig. 12, the current of clamp diode is simulated. The simulation waveform shows that each diode only turns on once during each cycle.

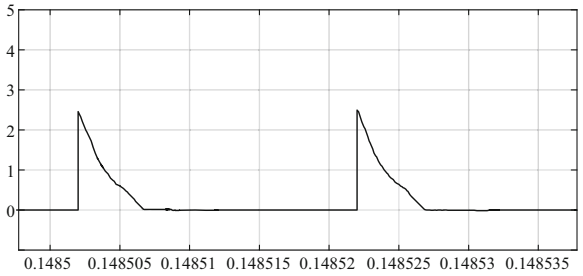


Fig. 12. The current of clamp diode simulation waveform

Designing the load of the converter is switched from light load to heavy load in 0.1 s, and then from heavy load to light load at 0.2 s. The simulation waveforms of the output voltage and current of the converter with/without AVP control mode are shown in Fig. 13.

As shown in Fig. 13, In AVP control mode, the fluctuation of output voltage and the recovery time of dynamic response are reduced effectively in the process of heavy/light load converting.

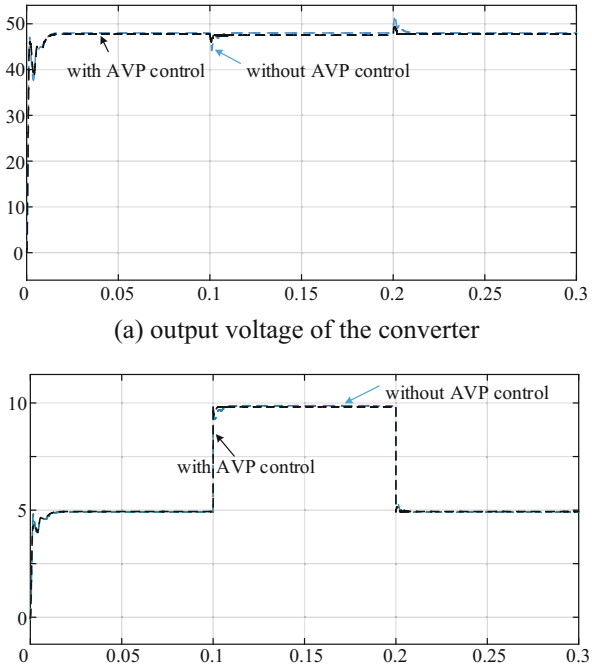


Fig. 13. Simulation waveforms of the output voltage and current of the converter

6 Conclution

In this paper an AVP control method is applied to the improved phase shift full bridge soft switching DC-DC converter. By combining the AVP control method with the topology, not only the output voltage response ability to the load converting can be improved, but also the soft switching of the converter switches can be achieved. In the proposed converter, the AVP control method is based on output current feedback regulation. This can simplify the design complexity of the controller while improving the dynamic response capability to the output load. Meanwhile, the PSFB circuit topology with clamping diode can not only realize soft switching, but also the peak voltage oscillation across the rectifier diode is clamped. At the same time, the clamping diode only turns on once in a switching cycle, which improves the efficiency of the converter.

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