Transformerless Three-Phase Solar Photovoltaic Power Conversion Systems

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Abstract Solar photovoltaic (SPV) energy is one of the promising and dominant renewable energy sources for clean and sustainable electricity production. Typically, a power conditioning unit (PCU) along with a low-frequency transformer on the AC side is utilized to integrate the photovoltaic (PV) source with the grid. However, they offer low efficiency, high cost, and low power density. Transformerless inverters gained more attention in grid-connected PV systems due to demands of power density, high efficiency, reliability, and low cost. However, leakage current is produced through the stray capacitances between the PV array and the ground. It is generated due to the fluctuation of common-mode voltages between PV neutral and grid. Also, it enhances DC injection into the grid due to the absence of galvanic isolation. Consequently, it causes fundamental safety problems and the degradation of the system's performance. This chapter aims to study and compare leakage current minimization approaches through converter topology modifications and pulse width modulation schemes in transformerless PV systems. The key performance of each inverter topology in terms of leakage current is holistically evaluated through simulation studies in MATLAB software. Finally, the merits and demerits of each power converter topology for transformerless solar systems are summarized in this chapter.

Keywords Common-mode voltage · Inverters · Leakage current · Modulation schemes · And solar power conversion systems

List of Symbols

P	Power (W)
D	Diode

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S	Switching device
L	Inductor (mH)
I_{PV}	PV array output current (A)
V_{PV}	PV array output voltage (V)
C_{pv}	Stray capacitance of PV panel (μF)
V_{dc}	Input DC voltage (V)
V_{an}, V_{bn}, V_{cn}	Phase voltages of converter (V)
n	Neutral point
a, b, c	Terminals of a 3-phase system
V_0 *to* V_7	State vectors
$I_{leakage}$	Leakage current (A)
V_{CM}	Common-mode voltage (V)
R_g	Ground resistance (Ω

List of Acronyms

PV	Photovoltaic
PCU	Power conditioning unit
PVS	Photovoltaic systems
IEA	International Energy Agency
PVES	Photovoltaic energy systems
Hz	Hertz
LFT	Low-frequency transformer
HFT	High-frequency transformer
kWh	Kilowatt hour
THDs	Total harmonic distortions
EMI	Electromagnetic interference
CMV	Common-mode voltage
DC	Direct current
MPPT	Maximum power point tracking
CI	Central inverter
SI	String inverter
PWM	Pulse width modulation
UPS	Uninterrupted power supply
RMS	Root mean square
AC	Alternating current
kHz	Kilo Hertz
IGBTs	Insulated gate bipolar transistors
V	Volt
kW	Kilo watt
GW	Giga watt
VSI	Voltage source inverter
CSI	Current source inverter

MPPT	Maximum power point tracker
MPP	Maximum power point
I-V	Current versus voltage
P-V	Power versus voltage
A	Ampere
s	Seconds
MOSFET	Metal oxide semiconductor field-effect transistor
W	Watt
LC	Inductor-capacitor
SPWM	Sine pulse width modulation
SVM	Space vector modulation
NSPWM	Near-state PWM
AZPWM	Active zero state PWM
RSPWM	Remote state PWM
MSVPWM	Multilevel space vector pulse width modulation

1 Introduction

The generation of electricity from photovoltaic systems (PVS) is growing rapidly and has become one of the prominent among the distributed generation systems. International Energy Agency (IEA) has reported that more than least 627 GW of PV are installed worldwide, as 115 GW of PV were installed in 2019 [1]. The PVs are the third-most energy resource after hydro and wind energy in terms of cumulated installed capacity. Currently, strategic incentives and tariff schemes by federal governments in many countries are contributing to the widespread adoption of PVS. Last decade, the cost of PVS has dropped by 59% due to cutting-edge advances in materials, power electronics, and digital technologies along with the escalated manufacturing facilities by the industries. The power conditioning units (PCUs) are a part of PVS, which comprise of power electronic converters and their digital control mainly contribute to enhancing the energy yield from the sun and minimizing the cost, thereby offering convenient access to solar energy and cost-effective. Also, a smaller footprint, enhanced power quality, grid codes compliance, and improved reliability can be achieved through power electronic converters and their control [2].

PVS is mainly classified into grid-connected and off-grid (standalone) systems. The energy produced by grid-tied PVS is growing significantly, which feed power to the grid with sinusoidal currents and local loads. The standalone PVS are utilized in remote and rural areas where the grid connection is not available, complicated, and expensive. The local loads are fed by PVES with constant voltage and frequency in off-grid applications. Energy storage is employed with standalone systems, to supply continuous power supply in such a way that harvested PV power charges energy storage and gets utilized for supplying to the local loads [3]. However, grid-connected

PVS are preferred due to the existence of short-lived, costly, and bulky batteries in standalone applications. The PCU employing the voltage source converters with output filters is used for grid-connected and standalone systems. The output current and load voltage are regulated in on-grid and off-grid PVS, respectively. The main challenge associated with all PVS is the extraction of maximum power as the PV characteristic curve varies changes with environmental conditions, such as solar irradiation and core temperature [4].

To integrate solar PV with grid or AC loads, a PCU which converts the energy produced by PV panels from DC to AC while extracting maximum power from the solar PV system and is responsible to generate the required voltage and frequency for grid synchronization. This connection is achieved in two possible ways with and without galvanic isolation, as depicted in Fig. 1. Galvanic isolation between the PV source and grid is provided by using a transformer with an inverter connection. The most traditional way is the connection of the inverter along with a low-frequency transformer (LFT) on the AC side (Fig. 1a) or a high-frequency transformer (HFT) on the DC side (Fig. 1b). With the galvanic isolation, PVS is protected from hazardous voltages and avoids DC current injection into the grid [5]. However, LFTs (Fig. 1a) generates power loss in the windings, thereby reducing the system efficiency. Also, they are bulky, heavy, and expensive. One of the possible ways to enhance the power

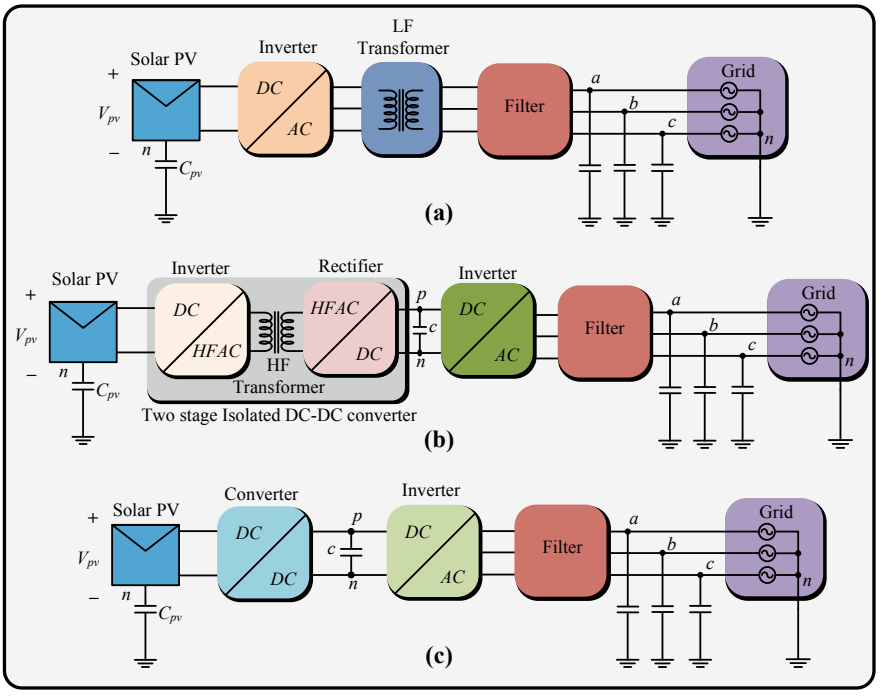

Fig. 1 Classification of grid-connected PVS: **a** LFT-based PCU, **b** HFT-based PCU, and **c** transformerless based PCU

density is the adoption of HFT, and their configuration is shown in Fig. 1b. However, the system efficiency is comparatively low due to multiple conversion stages.

Alternatively, transformerless PV grid-tied inverters (Fig. 1c) is introduced which can reach their efficiencies up to 97–98% with the high power density and low cost. However, several concerns such as safety issues, malfunction of sensors, and corrosion in underground equipment under the effects of the leakage current due to the absence of galvanic isolation between PV sources and the grid [6]. Also, the existence of the leakage current escalates the total harmonic distortion (THD), electromagnetic interference (EMI), and system losses.

Typically, the PV panels frame will be grounded (Fig. 2) to limit the leakage current as described in European and USA standards [7]. The intensity of leakage currents can be determined by the value of PV panel parasitic capacitance, converter topology, control technique, and switching frequency of converter operation [8]. Among them, inverter topologies and control strategies (pulse width modulation schemes) are proven to be the most dominant factors in determining the leakage current that flows from the PV source to the grid through parasitic capacitors formed between them. The intensity of these currents highly depends on the amplitude and frequency content of common-mode voltage (CMV) and parasitic capacitances [9]. Therefore, it is essential to understand the phenomenon of leakage current generation and methods to mitigate the generation of this phenomenon. Over the past years, sincere attempts have been made by the researchers to minimize the leakage current in the transformerless grid-tied PV inverters through advanced modulation techniques and power converter topology modifications. A holistic comparison among transformerless two-level converter topologies in terms of CMV and leakage current is also missing in the literature. This chapter mainly focuses on a review of transformerless inverter topologies, switching techniques, and control schemes are presented to limit the leakage current in PV systems.

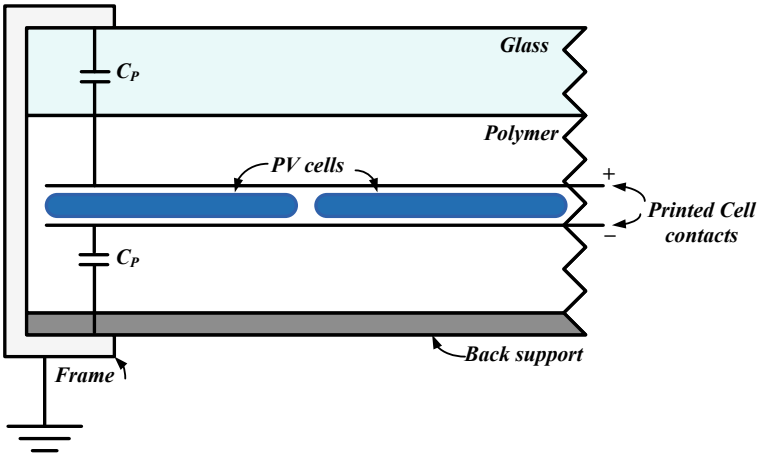

Fig. 2 Parasitic capacitance view of the solar PV panel

This chapter is organized as follows:

- The overview of power interface systems and their classification for grid-connected PV systems are presented in Sect. 2.
- The fundamental details of grid-tied inverters regarding leakage current generation and its minimization through control schemes are discussed in Sect. 3.
- The overview of transformerless three-phase grid-tied inverters and their operation principles are presented in Sect. 4.
- Comparison of various transformerless three-phase grid-tied inverters through simulation studies is illustrated in Sect. 5.
- Section 6 provides the concluding remarks of this chapter

2 Classification of Power Interface Systems

PV panel output is continuously varied concerning the irradiation and atmospheric temperature. Also, the partial shading and module age are considerable effects of PV system performance [10]. This mismatch of output leads to a reduction in output energy and the lifetime of the PV modules. Various maximum power point tracking (MPPT) techniques are proposed to extract the maximum energy from the PVS. The PCU extracts the maximum output from PVS and plays a vital role in maintaining the output at desired standards of load (for a standalone system) or grid (voltage and frequency) [11]. Based on the range of the output power, PVS are categorized under three regions [12, 13].

- Small-scale PVS (power rating <10 kW)
- Medium-scale PVS (power rating typically 10 kW–1 MW)
- Utility-scale PVS (typical power rating of 1–10 MW)

Based on the conversion stages, PVS can be interfaced with grid or load in two-stage or single-stage conversion. In two-stage, two sets of power conversion stage i.e. DC–DC and DC–AC conversion. The front-end DC–DC converter is accountable for yielding maximum power from PVS, whereas the DC–AC converter converts the DC power to AC with maintaining the grid standards. Two-stage conversion systems are mostly used for high power applications due to the maturity of the topological structures and their simplicity in control. However, conversion losses are more in the two-stage conversion. In single-stage conversion, both are maintained by the inverter alone and by the conversion losses are less as compared to the two-stage. However, the control of the system becomes complex.

Recently, the medium- and large-scale PV plants have gained great attention due to low maintenance and zero-emission. In general, the inverter is connected to the grid through the low-frequency transformer (LFT) to provide isolation, step-up operation, and minimize the leakage current. Because of the weight and size constraints of the LFT, the PV inverter system can be expensive and complex for installation and maintenance. To overcome the aforementioned short comes, transformerless inverter

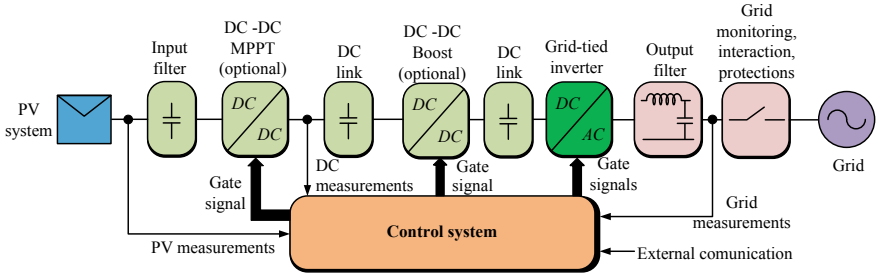

Fig. 3 A typical overview of grid-connected PVS

topologies are presented in this chapter. The block diagram of transformerless grid-connected PVS is illustrated in Fig. 3, which consists of several conversion stages and is followed by the filters [13]. PVS is connected through the DC/DC converter-1 and followed by one more DC/DC converter. The front-end DC/DC converters are placed to extract the maximum power from the PVS and a secondary DC/DC converter provides step-up or step-down based on the requirement. Usually, for grid-connected PVS step-up converter is equipped to deliver power to the medium voltage (MV) grids without using any step-up transformer and these DC/DC converters are optional. Finally, the inverter is placed at the output end to deliver AC power from the secondary DC/DC converter to the MV grid and in between filters are placed to suppress the voltage/current ripples.

The control system is shown in Fig. 3 monitor and controls all converters to extract maximum power from the PVS and to deliver power to the grid with the following predefined standards (Table 1). This block also controls the circuit breakers to make or break the PVS from the grid. During night-time, faulty condition or standalone operation control systems disconnects the PVS from the grid.

Grid interfaced solar PVs are categorized into four different (Fig. 4) types based on the configuration [2]. Central inverter (CI) based PV configuration illustrated in Fig. 4a is mostly adaptive configuration due to simple structure. CI configuration consists of a minimal component count for PCU, and one low-frequency transformer is sufficient to provide galvanic isolation. Therefore, the cost and the losses associated

Table 1 Standards associated with grid integration of PVS [12, 14, 15]

Standard	Voltage fluctuation	Power factor	DC current injection	Frequency tolerance (Hz)
IEEE 1547	5%	>0.9	<0.5%	59.3–60.5
IEEE929	–	>0.85	<0.5%	59.3–60.5
IEC 61,727	–	–	<1%	59–61
RULE 21	5%	>0.9	<0.5%	59.3–60.5
VDE-AR-4105	3%	>0.9	<1A	47.5–51.5
AS 4777	–	>0.5	<1%	45–55

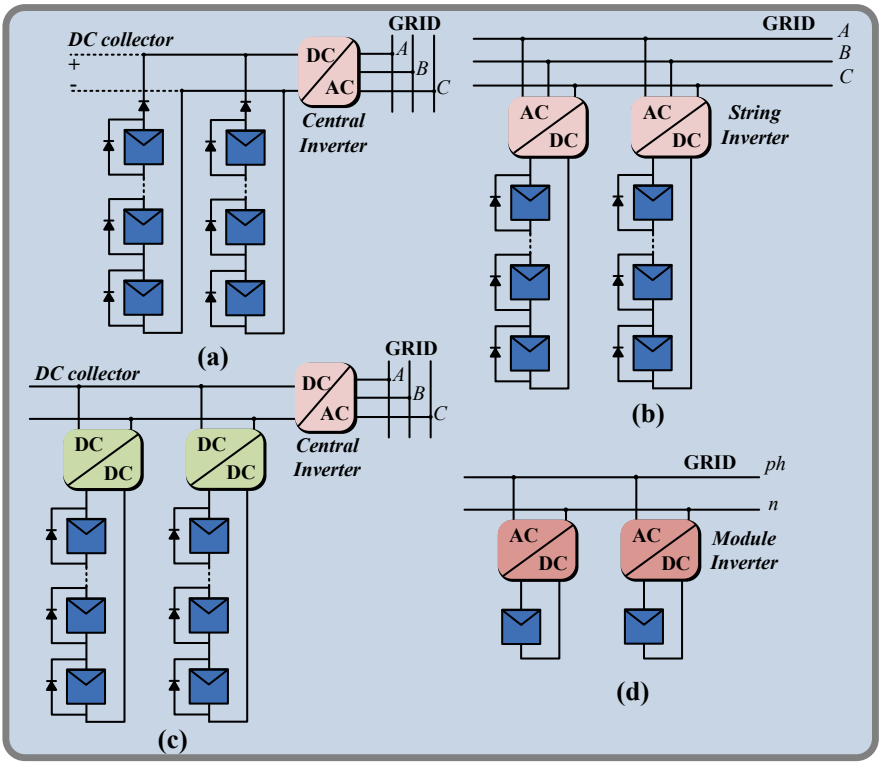

Fig. 4 Grid-tied PVS configurations, **a** central inverter configuration, **b** string inverter configuration, **c** multi-string inverter configuration, **d** module inverter configuration

with CI configurations are very less. Usually, these configurations are having an efficiency of typically 95–98% [16]. Because of the aforementioned benefits and ease of control, this configuration is more suitable for large-scale PVS. Apart from the benefits, CI configuration has poor MPPT tracking due to a single inverter for multiple strings. Multilevel inverter topologies are more suitable for CI-based PV systems. Over the past years, researchers have proposed various multilevel inverter topologies for transformerless grid interfaced PVS and which are consolidated in [17–21].

String inverter (SI) configuration illustrated in Fig. 4b consists of individual inverters for each string to improve MPPT (power yielding capability is increased by 1–3%) [22]. SI configuration consists of more conversion stages compared to the aforementioned configuration and also each string requires an individual LF transformer, which results in 60% expensive than CI configuration and increases the losses. Due to that SI configuration is preferable for medium-scale PVS.

The multi-string configuration in Fig. 4c combines the benefits of the CI configuration as well as the SI configuration. DC–DC converter yields the maximum output

from individual strings similar to SIs and forms DC bus and followed by CI to interface with the grid results reduction in transformer count to one. Therefore, improved efficiency and lower cost are achieved due to the reduction in the number of the transformers as compared to SI configuration, [2, 22]. Figure 4d shows the module inverter configuration; each module consists of individual inverter results increase in the power yielding capability. Due to a large number of component counts, these are suitable for small-scale applications [23].

Overall, transformerless inverters especially in string configuration have gained more attention due to demands of high efficiency, power density, and low cost. However, it causes fundamental safety problems and PV system degradation due to the existence of leakage current and DC injection into the grid. Therefore, this chapter mainly deals with the transformerless string inverter topological configurations to mitigate the leakage current to interconnect the PV plant with a grid.

3 Grid-Tied Inverters and Control Schemes

The inverter is used to convert the fixed DC voltage to the desired alternating voltage with the required frequency. These are used to interface the renewable energy sources with the grid or DC sources to the AC loads, and the block diagram of the inverter is shown in Fig. 5. Here, the DC input voltage is maybe from PVS (single-stage conversion) or the output terminals of DC–DC converter (two-stage conversion), and the output may be a single-phase or a three-phase based on the inverter topological configuration. Usually, inverters are used for various power controlling applications like speed control of motors, induction heating, uninterrupted power supply (UPS) for sophisticated loads.

Inverters are broadly classified into voltage source inverters (VSIs) and current source inverters (CSI) based on the input source. VSI converts the fixed DC voltage to the variable frequency AC voltage; its output voltage is independent of the load, and the current is depends on the impedance of the load. CSI converts the fixed DC voltage to the variable frequency AC current, the output current of the CSI is independent of the load but the voltage is dependent on the impudence of the load [9]. Based on a number of phases at output inverters are categorized into single-phase

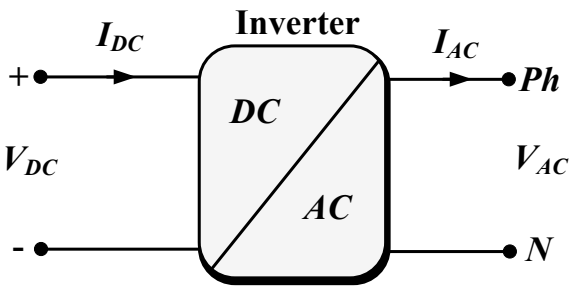

Fig. 5 Block diagram of the inverter

and three-phase inverters. Single-phase inverters are restricted to low power output and these inverters are popular for the UPS.

3.1 Three-Phase Inverter

Three-phase inverters are pretty popular in most applications due to their high power handling capabilities. The basic three-phase inverter is a six-switch inverter (H6 inverter), illustrated in Fig. 6. It consists of three arms with having two switches on each arm. These switches are operated in several states to obtain desired voltage and frequency at the output terminals, and this process of symmetrical switching is known as modulation [24]. The basic modulation techniques are 180° mode and 120° mode. During the 180° mode of operation, each switch operates for half of the period over a cycle, and switches corresponding to the same arm are operated in a complementary manner to avoid a dead short circuit of source terminals. The switching pattern of the 180° mode of operation is shown in Table 2. Due to the non-ideality of the switches, the outgoing switch goes to turn off slowly and leads to a dead short circuit of source terminals [25].

To eliminate the aforementioned problem, dead time is provided between the transitions of pole voltages. To achieve that 120° mode of operation is proposed. In this, each switch conducts for 120° over a period and 60° delay is provided in between the switching of the switches (Table 2) in the same leg but the major drawback with the 120° mode is output voltage decreases.

The output phase voltages of the VSI corresponding to the 180^0 mode of conduction are shown in Fig. 7. Irrespective of the load impudence the voltage remains

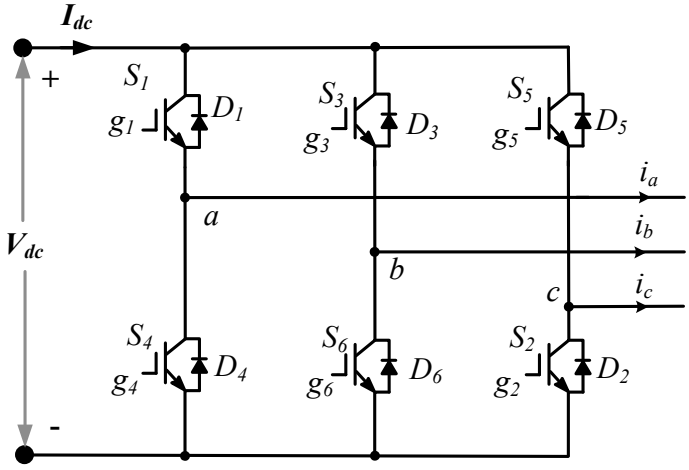

Fig. 6 Three-phase H6 inverter

Table 2 Switching pattern of VSI

Switching pattern for 180° mode of operation					
0–60°	60°–120°	120°–180°	180°–240°	240°–300°	300°–360°
S_1			S_4		
S_6		S_3			S_6
S_5	S_2			S_5	
Switching pattern for 120° mode of operation					
0–60°	60°–120°	120°–180°	180°–240°	240°–300°	300°–360°
S_1			S_4		
S_6		S_3			S_6
	S_2			S_5	

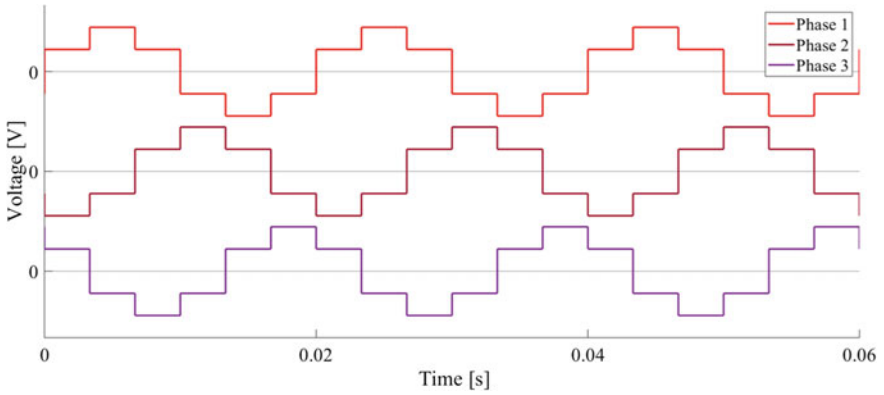

Fig. 7 The output voltage of three-phase H6 VSI in 180° operating mode

constant at 4 levels ($2*V_{dc}/3$, $V_{dc}/3$, $-V_{dc}/3$, $-2*V_{dc}/3$) with a 31% total harmonic distortion (THD).

3.2 Leakage Current and Common-Mode Voltage (CMV)

The CMV and the parasitic capacitance of the solar PV (Fig. 2) cause the leakage current. CMV can be determined by taking the mean of the pole voltages of the inverter (Eq. 1) [26]. Figure 8 shows the model diagram of the H6 inverter, where $V_a(t)$, $V_b(t)$, $V_c(t)$ are the instantaneous pole voltages and the V_{CM} is the common-mode voltage that appears in between the neutral point of the load and the source *–ve*, and C_{pv} is the stray capacitance of the solar PV panel.

$$V_{CM} = (V_a + V_b + V_c)/3 \tag{1}$$

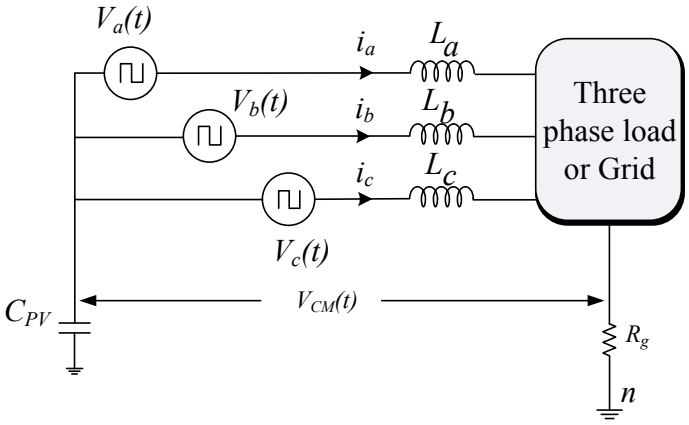

Fig. 8 CMV model of H6 inverter

$$I_{\text{leakage}} = C_{pv} * \mathrm{d}(V_{CM})/\mathrm{d}t \tag{2}$$

$$I_{\text{leakage}} \propto \mathrm{d}(V_{CM})/\mathrm{d}t \tag{3}$$

Therefore, the leakage current of the inverter can be minimized by suppressing the change in CMV (Eq. 3), and this must be within the standard limits of VDE-AR-N-4105 mentioned in Table 1 [27]. In this chapter, various modulation schemes and the inverter topologies are presented to minimize the leakage current by reducing the change in CMV.

3.3 Modulation Techniques to Minimize CMV

Change in CMV affects the leakage current of the inverter. This variation (peak-to-peak) can be minimized with the help of various modulation techniques. Peak-to-peak CMV of the H6 inverter in 180° conduction mode is V_{dc}, which results in more leakage currents, and in the following sub-sections, several modulation schemes are presented to minimize the CMV without changing the topological configuration.

3.3.1 Space *V*ector *M*odulation (SVM)

SVM is the most adopted modulation technique for controlling of H6 inverter to use the maximum DC bus of 91% without injecting any third harmonic component [28]. H6 inverter with the SVM technique forms 8 distinct states without causing any dead

Table 3 CMV at various states in SVM

S_1	S_3	S_5	Vector	CMV
0	0	0	V_0	0
1	0	0	V_1	$V_{dc}/3$
1	1	0	V_2	$2 * V_{dc}/3$
0	1	0	V_3	$V_{dc}/3$
0	1	1	V_4	$2 * V_{dc}/3$
0	0	1	V_5	$V_{dc}/3$
1	0	1	V_6	$2 * V_{dc}/3$
1	1	1	V_7	V_{dc}

Table 4 CMV at various states in NSPWM

S_1	S_3	S_5	Vector	CMV
1	0	0	V_1	$V_{dc}/3$
1	1	0	V_2	$2 * V_{dc}/3$
0	1	0	V_3	$V_{dc}/3$
0	1	1	V_4	$2 * V_{dc}/3$
0	0	1	V_5	$V_{dc}/3$
1	0	1	V_6	$2 * V_{dc}/3$

short circuit of DC source terminals. Each state is having different CMVs and are listed in Table 3.

From Table 3, it can be observed that with the SVM technique the variation of common-mode voltage is very high i.e. 0 to $V_{dc,}$ and results in a large leakage current.

3.3.2 Near *State* PWM (NSPWM)

The near-state pulse width modulation (NSPWM) method is similar to the SVM only. In this method, any output voltage vector is modelled with the neighbour three vectors of the reference voltage. Therefore, only the six active vectors (V_1 to V_6) are utilized to model any reference voltage [29]. From Table 4, it can be observed that the peak-to-peak voltage variation of the CMV is $V_{dc}/3$ i.e. from $V_{dc}/3$ to $2 * V_{dc}/3$. With the NSPWM method CMV variation is reduced to $V_{dc}/3$, and it minimizes the leakage current of the inverter.

3.3.3 Active *Zero State* PWM (AZPWM)

Extreme values of the CMVs are $0 * V_{dc}$ and V_{dc} occur at the time of zero vector instants. In the AZPWM scheme, a zero vector is produced by operating the two

Table 5 Switching pattern for AZPWM schemes

Modulation technique	Sector 1		Sector 2		Sector3	
SVPWM	7-2-1-0-1-2-7		7-2-3-0-3-2-7		7-4-3-0-3-4-7	
NSPWM	2-1-6-1-2		3-2-1-2-3		4-3-2-3-4	
AZPWM1	3-2-1-6-1-2-3		1-2-3-4-3-2-1		5-4-3-2-3-4-5	
AZPWM2	6-2-1-3-1-2-6		4-2-3-1-3-2-4		2-4-3-5-3-4-2	
RSPWM1	3-1-5-1-3		3-1-5-1-3		3-1-5-1-3	
RSPWM2B	4-2-6-2-4		4-2-6-2-4		2-4-6-4-2	
RSPWM3	0–π/6	π/6–π/3	π/3–π/2	π/3–π/2	π/2–2π/3	2π/3–5π/6
	3-1-5-1-3	4-2-6-2-4	4-2-6-2-4	3-1-5-1-3	3-1-5-1-3	2-4-6-4-2

opposite vectors with equal time. Based on the sequence of operation, AZPWM techniques are two types AZPWM1 and AZPWM2 mentioned in Table 5 [30].

In sector-1, the zero vector is implemented by operating vectors 3 and 6 with equal time and similarly for sector 2 vectors 1 and 4, and sector 3 vectors 2 and 5.

3.3.4 Remote *S*tate PWM (RSPWM)

RSPWM facilitates the elimination of high-frequency components from the CMV and in this modulation scheme only odd vector V_1, V_3, V_5, or only even vectors V_2, V_4, V_6 are used to produce the resultant vector. Based on the selection of vectors, RSPWM is classified into RSPWM1 (formed by only odd vectors) and RSPWM2B (formed by even vectors alone). RSPWM3 combines the RSPWM1 and RSPWM2B, and their switching sequences are mentioned in Table 3 [30].

3.4 Control Scheme of the Inverter Topologies

The closed-loop control is established based on active and reactive power control, as it is imperative to match the power demand. The control scheme consists of two cascaded loops in which the outer loop is to controls the power injection to the grid from PVS while the inner loop is to controls the grid current based on the outer power control loop. The current controller generates the voltage references for the PWM modulator. A carrier-based modulation scheme is utilized for the generation of the switching pulses for the active switches of the inverter topologies. In the carrier-based modulation method, switching pulses are generated according to the control logic and by comparing the carrier signals with the SVM modulation signals. SVM modulation signals are generated from the sinusoidal modulation signals by adding the zero-sequence component [31]. The block diagram of the control scheme is illustrated in Fig. 9.

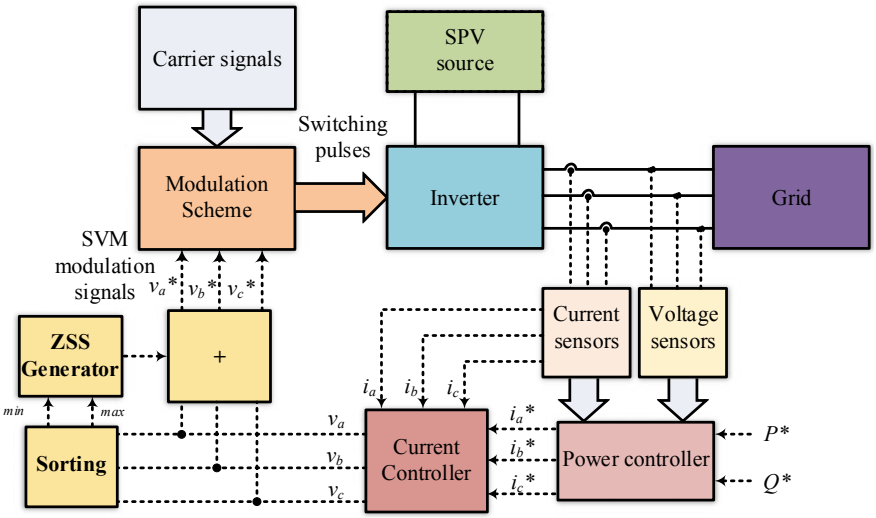

Fig. 9 Block diagram of transformerless inverter with a control structure

4 Transformerless Power Inverter Topologies

In the earlier section, the CMV of the H6 inverter is minimized by using various modulation techniques. In this section, the CMV of the inverter is going to be minimized by making topological changes to the inverter [31]. Among those inverter topologies, few are described in the following sub-sections.

4.1 H7 Inverter Topology

In the H6 inverter maximum and minimum values of the CMV, it appears at the zero vector states i.e. V_7 and V_0 states. H7 inverter shown in Fig. 10a is consists of power electronic semiconductor switch S_7 placed in its positive path [32]. During the zero vector V_7, the switch S_7 breaks the continuity of the circuit on the DC side of the inverter and results in zero CMV. The switching table of the converter corresponding to various states and its CMVs are listed in Table 6. The control strategy of the H7 inverter is modelled based on the lookup table (Table 6) and is illustrated in Fig. 10b [33]. From Table 6, it can be observed that the range of the CMV of H7 topology is 0 to 2 * V_{dc}/3.

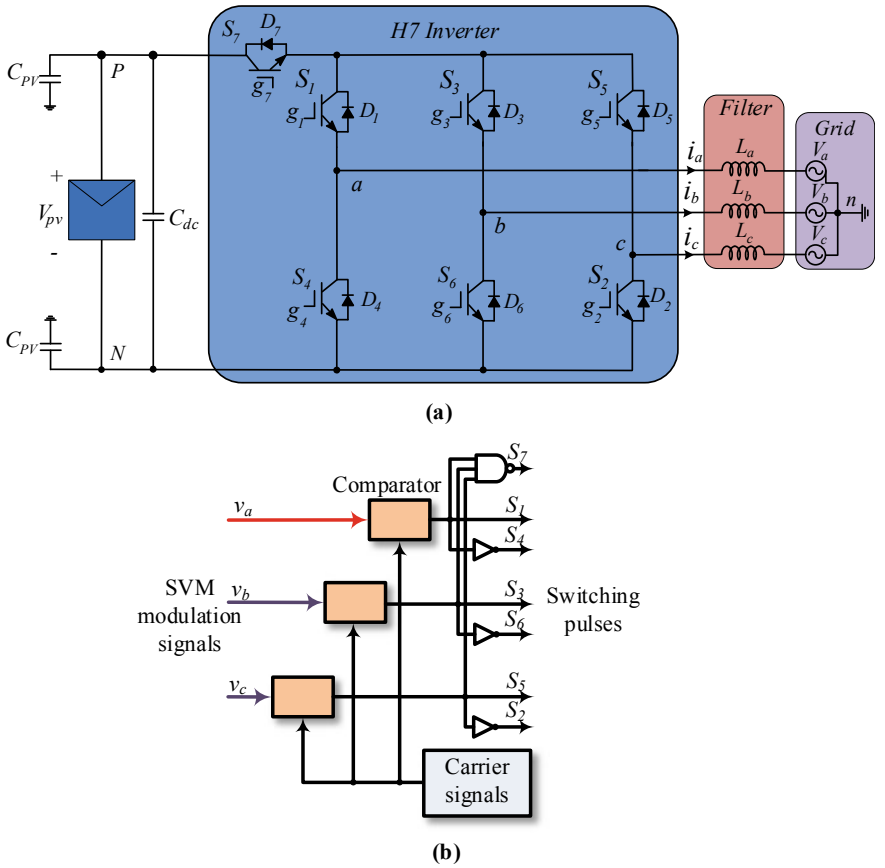

Fig. 10 H7 inverter **a** inverter topology **b** modulation scheme

Table 6 Switching states with CMVs of the H7 inverter

S_1	S_3	S_5	S_7	Vector	CMV
0	0	0	1	V_0	0
1	0	0	1	V_1	$V_{dc}/3$
1	1	0	1	V_2	$2 * V_{dc}/3$
0	1	0	1	V_3	$V_{dc}/3$
0	1	1	1	V_4	$2 * V_{dc}/3$
0	0	1	1	V_5	$V_{dc}/3$
1	0	1	1	V_6	$2 * V_{dc}/3$
1	1	1	0	V_7	0

4.2 *H8* Inverter Topology

H8 topology is similar to the H7, but in H8 both positive and negative paths are consisting of power electronic semiconductor devices illustrated in Fig. 11a. These switches isolate the DC supply from the load or grid at the time of both zero vector states i.e. at V_0 and V_7 [33].

During the vector V_7 the switch S_7 and at V_0 the switch S_8 breaks the conduction path on the DC side of the inverter. The switching states corresponding to various vectors are presented in Table 7. The modulation scheme (Fig. 11b) is developed according to the switching states. The range of CMV remains the same as the H7 inverter but the leakage current will reduce to approximately half due to discontinuous path during zero vector instant.

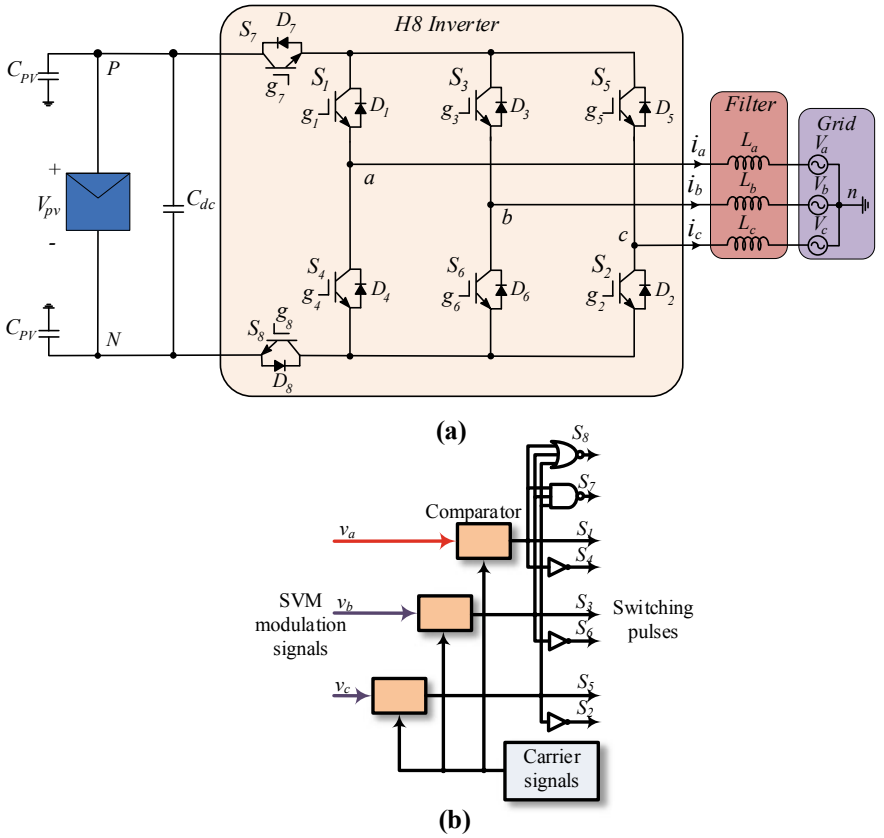

Fig. 11 H8 inverter **a** inverter topology **b** modulation scheme

Table 7 Switching states with CMVs of the H8 inverter

S_1	S_3	S_5	S_7	S_8	Vector	CMV
0	0	0	1	0	V_0	0
1	0	0	1	1	V_1	$V_{dc}/3$
1	1	0	1	1	V_2	$2 * V_{dc}/3$
0	1	0	1	1	V_3	$V_{dc}/3$
0	1	1	1	1	V_4	$2 * V_{dc}/3$
0	0	1	1	1	V_5	$V_{dc}/3$
1	0	1	1	1	V_6	$2 * V_{dc}/3$
1	1	1	0	1	V_7	0

4.3 *Three-Phase Seven Switch Inverter Topology*

The topology shown in Fig. 12a is similar to the H6 topology but the zero state V_0 and V_7 are provided by the seventh switch [34]. The 7th switch is connected to the

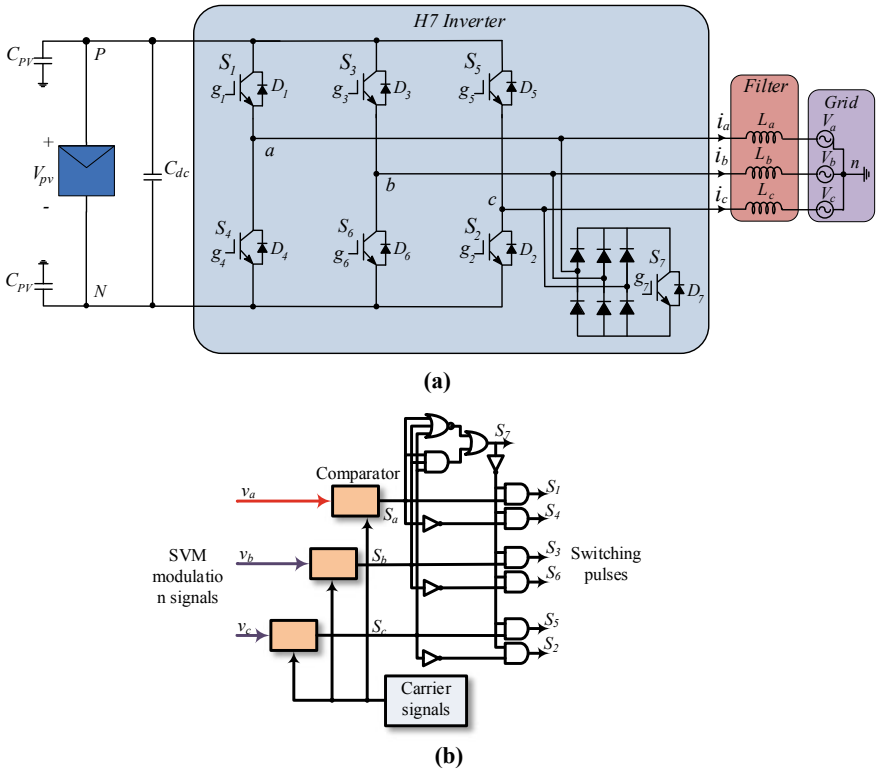

Fig. 12 Three-phase seven switch inverter **a** inverter topology **b** modulation scheme

Table 8 Switching sequence of three-phase seven switch inverter

Vector	Switching ($S_1S_3S_5S_7$)	V_{an}	V_{bn}	V_{cn}	CMV
V_1	1000	V_{dc}	0	0	$V_{dc}/3$
V_2	1100	V_{dc}	V_{dc}	0	$2 * V_{dc}/3$
V_3	0100	0	V_{dc}	0	$V_{dc}/3$
V_4	0110	0	V_{dc}	V_{dc}	$2 * V_{dc}/3$
V_5	0010	0	0	V_{dc}	$V_{dc}/3$
V_6	1010	V_{dc}	0	V_{dc}	$2 * V_{dc}/3$
V_0 & V_7	xxx1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

inverter output terminals through a three-phase diode bridge rectifier. The switch S_7 is coming to conduction during zero states i.e. during V_0 and V_7 and the CMV during these states is $V_{dc}/2$.

The switching states and corresponding CMVs of this topology are listed in Table 8. The range of the CMV of this topology is $V_{dc}/3$ to $2 * V_{dc}/3$. According to the switching states presented in Table 8, modulation scheme is developed for seven switch inverters and it's illustrated in Fig. 12b.

4.4 *Three-Phase Eight Switch Inverter Topology*

This topology presented in Fig. 13a consists of eight switches (S_1 to S_8). S_1 to S_6 switch positions are similar to the H6 inverter, during the non-zero states the switching state of the switches S_1 to S_6 remains the same as the H6 inverter and S_7 is in on and S_8 is in off. S_7 and S_8 switches are operated in a complementary manner [36].

During zero vector states, both the switches on the leg-1 (S_1 and S_4) are in off, and switching states and CMV corresponding to all states are listed in Table 9. The modulation scheme for the 8-switch converter is modelled according to Table 9 and is illustrated in Fig. 13b. Therefore, during the non-zero vector instants, CMV is the same as the conventional H6 inverter i.e. either $V_{dc}/3$ or $2 * V_{dc}/3$ and at the zero vector instant CMV is $2 * V_{dc}/5$. The range of the CMV remains the same as the three-phase seven switch topology but the step-change in CMV is different.

4.5 *Four-Leg Inverter Topology*

The four-leg inverter shown in Fig. 14a consists of an auxiliary leg along with the H6 inverter. The auxiliary leg is operated such that it always maintains the constant CMV. Generally, the four-leg inverter is controlled with the carrier-based PWM method [37, 38]. The switching table of the four-leg inverter and corresponding CMV is presented

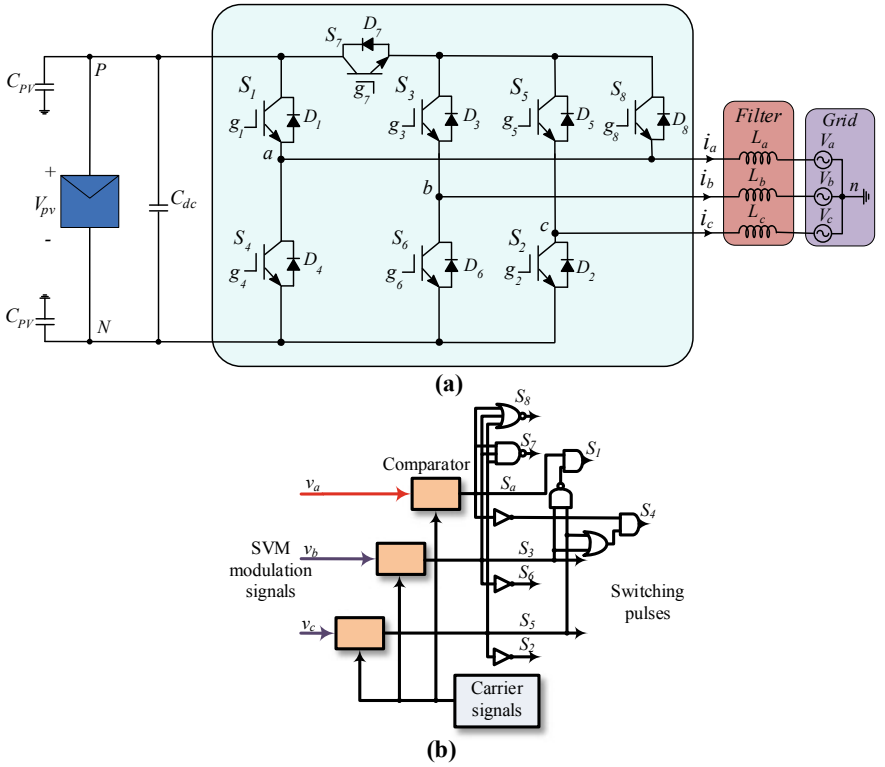

Fig. 13 Three-phase 8-switch inverter **a** inverter topology **b** modulation scheme

Table 9 Switching sequence of three-phase eight switch inverter

S_1	S_3	S_5	S_7	S_8	Vector	CMV
1	0	0	1	0	V_1	$V_{dc}/3$
1	1	0	1	0	V_2	$2 * V_{dc}/3$
0	1	0	1	0	V_3	$V_{dc}/3$
0	1	1	1	0	V_4	$2 * V_{dc}/3$
0	0	1	1	0	V_5	$V_{dc}/3$
1	0	1	1	0	V_6	$2 * V_{dc}/3$
S_1 & S_4 both *OFF*	1	1	0	1	V_7	$2 * V_{dc}/5$

in Table 10.

$$S_3 = \left(S'_a S_b + S_b S'_c + (S_a S_c)'\right) + S_b S'_{T2} = S'_4 \tag{4a}$$

$$S_5 = \left((S'_a S_c + S_c S'_b + (S_a S_b)\right)' + S_c S'_{T3} = S'_6 \tag{4b}$$

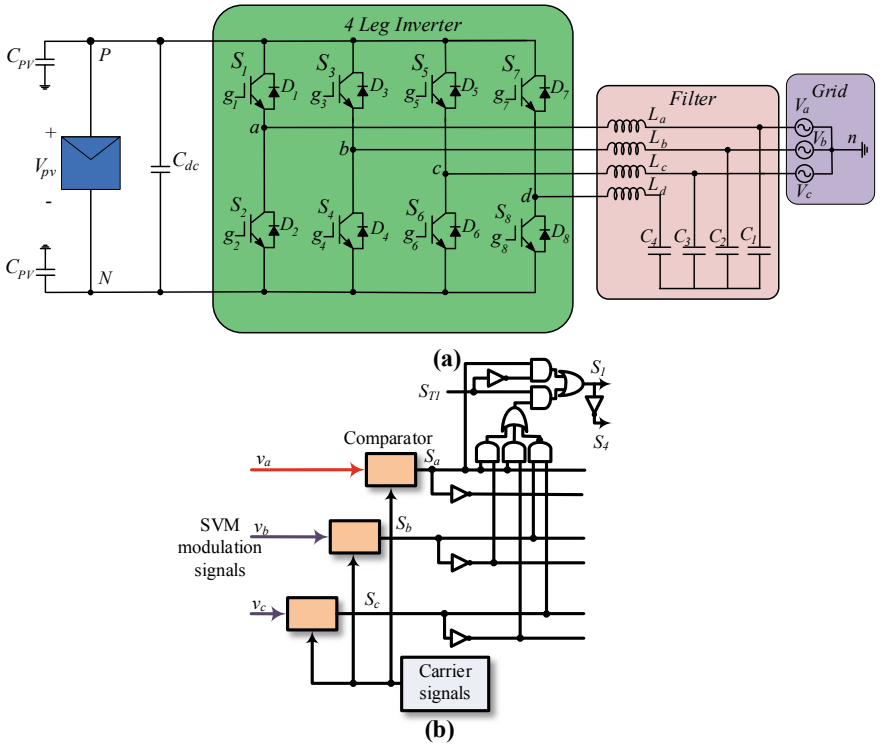

Fig. 14 Three-phase four-leg inverter **a** inverter topology **b** modulation scheme

Table 10 Switching sequence of three-phase four-leg inverter

S_1	S_3	S_5	S_7	Vector	CMV
1	0	0	1	V_1	$V_{dc}/2$
1	1	0	0	V_2	$V_{dc}/2$
0	1	0	1	V_3	$V_{dc}/2$
0	1	1	0	V_4	$V_{dc}/2$
0	0	1	1	V_5	$V_{dc}/2$
1	0	1	0	V_6	$V_{dc}/2$

$$S_7 = S_1 \oplus S_3 \oplus S_5 = S_8' \tag{4c}$$

The modulation scheme to generate switching pulse for S_1 and S_4 is illustrated in Fig. 14b and switching states corresponding to the each vector presented in Table 10. Similarly, algebraic expressions to generate switching pulses for the remaining switches are presented in Eq. (4a–c). Where S_{T1}, S_{T2}, and S_{T3} are the control signals having a pulse width of 33.33%. The zero states are obtained by operating opposite

Table 11 Switching table and capacitor voltages of DCM232 inverter

	S_1	S_3	S_5	$S_{7a} = S_{8a}$	$S_{7b} = S_{8b}$	V_{cpv1}	V_{cpv2}	V_{cpv3}	V_{cpv4}
V_1	1	0	0	1	0	$2 * V_{dc}/3$	$-V_{dc}/3$	$V_{dc}/3$	$-2 * V_{dc}/3$
V_3	0	1	0						
V_5	0	0	1						
V_2	1	1	0	0	1				
V_4	0	1	1						
V_6	1	0	1						
V_7	1	1	1	0	0				
V_0	0	0	0						

vectors at an equal time or the reference vector is generated by operating three closer vectors. The CMV of the four-leg inverter is constant at $V_{dc}/2$ irrespective of the reference vector. Due to the constant CMV across the parasitic capacitance, the change in CMV becomes zero, and results approximately zero leakage current.

4.6 DCM232 Three-Phase Inverter Topology

Generally, non-zero state vectors of the H6 inverter consist of two sets of CMVs either $V_{dc}/3$ or $2 * V_{dc}/3$, respectively. All odd vectors produce a common-mode voltage of $V_{dc}/3$ and all even vectors produce $2 * V_{dc}/3$. DCM232 is a topology that is proposed to separate these odd and even non-zero states, and power is delivered by two symmetrical isolated DC sources. DCM232 is modelled with 10 ($2 + 2 + 6$) switching devices and two isolated DC sources shown in Fig. 14a. The inner H6 operation remains the same as the conventional inverter [39].

For the odd non-zero vectors V_1, V_3, V_5, the upper voltage source V_{pv1} is connected to the H6 inverter by turn on the S_{7a} and $S_{8a;}$ and for the even non-zero vectors V_2, V_4, V_6, the lower voltage V_{pv2} is connected to the H6 inverter by turn on the S_{7b} and S_{8b}. During the zero states, S_7 and S_8 switches isolate both the sources from the load. The switching states and the voltage across the stray capacitors are listed in Table 11. The modulation scheme for this inverter corresponding to the various switching states is modelled (Fig. 15b) according to Table 11.

5 Simulation Results and Discussion

The aforementioned inverter topological configurations are simulated in MATLAB/SIMULINK software with identical parameters. For the simulation study, 480 V battery source is considered as an input, and a three-phase 2 kW resistive load is

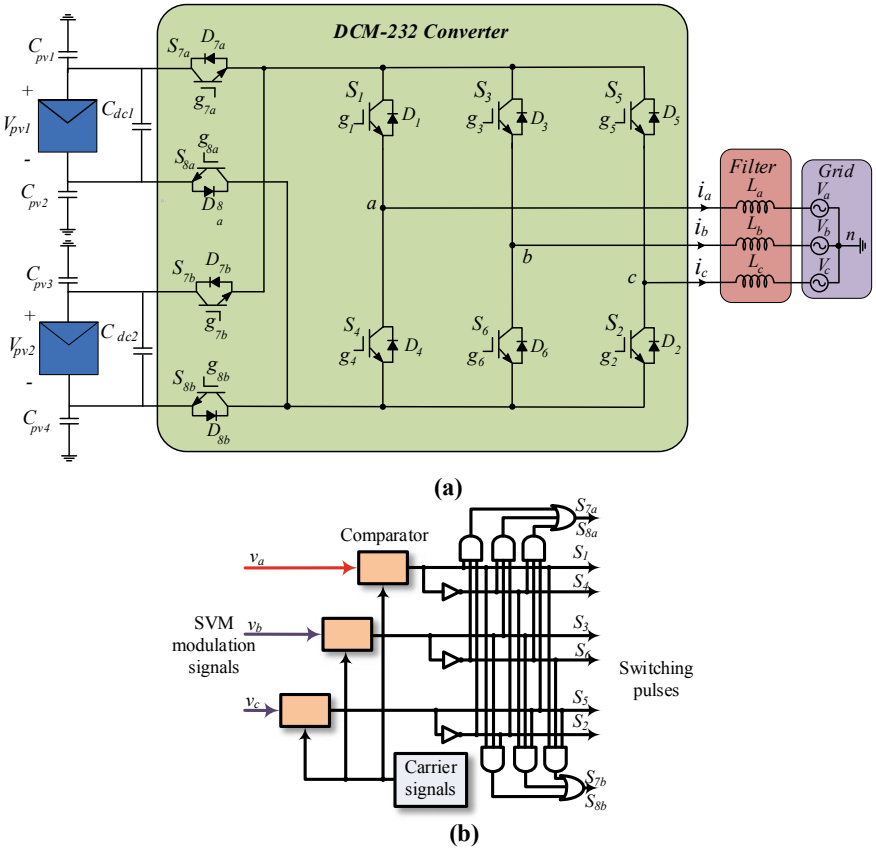

Fig. 15 Three-phase DCM232 inverter **a** inverter topology **b** modulation scheme

connected to the inverter terminals through a line inductance of 1 mH, and a 9 μF capacitor is considered as the stray capacitance of solar PV panel.

SVM-controlled H6 inverter is simulated and corresponding CMV and leakage currents are depicted in Fig. 16. H6 inverter CMV is varying from 0 to V_{dc} under the SVM modulation scheme (Fig. 16a) and the corresponding leakage current waveform and its RMS value (Red colour line) are shown in Fig. 16b. For the above specifications, the H6 inverter produces a 320-mA leakage current, thereby not within the standard limits of VDE-AR-N-4105.

A CMV and leakage current of modified SVPWM controlled H7 inverter are illustrated in Fig. 17. CMV of the inverter in Fig. 17a is varying in between 0 and 320 V (i.e. 0 to 2 * V_{dc}/3), and the leakage current corresponding to this CMV variation is shown in Fig. 17b which is having an RMS value of 230 mA. As compared to the H6 inverter, CMV variation and the leakage current of the H7 inverter are a bit lesser and within the standard limit (i.e. < 300 mA). Therefore, this topology is suitable for grid interface without using any transformer.

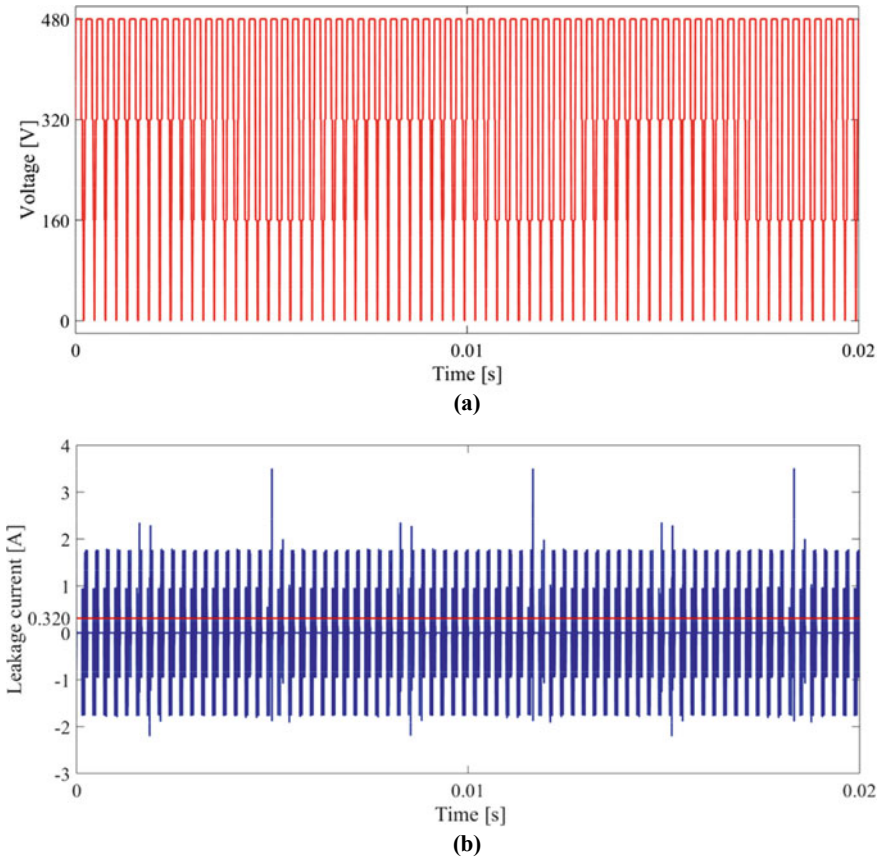

Fig. 16 Simulation results of H6 inverter using SVM **a** CMV, **b** leakage current

Similar to the H7 inverter, the H8 inverter is also simulated under the same modulation scheme and specifications. Obtained results with the H8 inverter are shown in Fig. 18. CMV (Fig. 18a) remains the same as the H7 inverter but the RMS value of the leakage current (Fig. 18b) is 165 mA; it is lesser than the H7 topology RMS leakage current i.e. 230 mA, due to the discontinuity of conduction in both the zero states.

CMV and leakage current corresponding to the three-phase seven switch inverter [30] are illustrated in Fig. 19. CMV of this inverter is varies from 160 V–240 V–320 V (i.e. $V_{dc}/3$–$V_{dc}/2$–$2 * V_{dc}/3$). It is observed that the CMV (Fig. 19a) is reduced in comparison to the earlier topologies. Therefore, leakage current is also reducing and the RMS value of the leakage current is 105 mA Fig. 19b), which complies with the VDE-AR-N-4105 standards.

Three-phase eight switch inverter CMV is depicted in Fig. 20a and is varying from 160 V–192 V–320 V ($V_{dc}/3$–$2 * V_{dc}/5$–$2 * V_{dc}/3$). The leakage current RMS

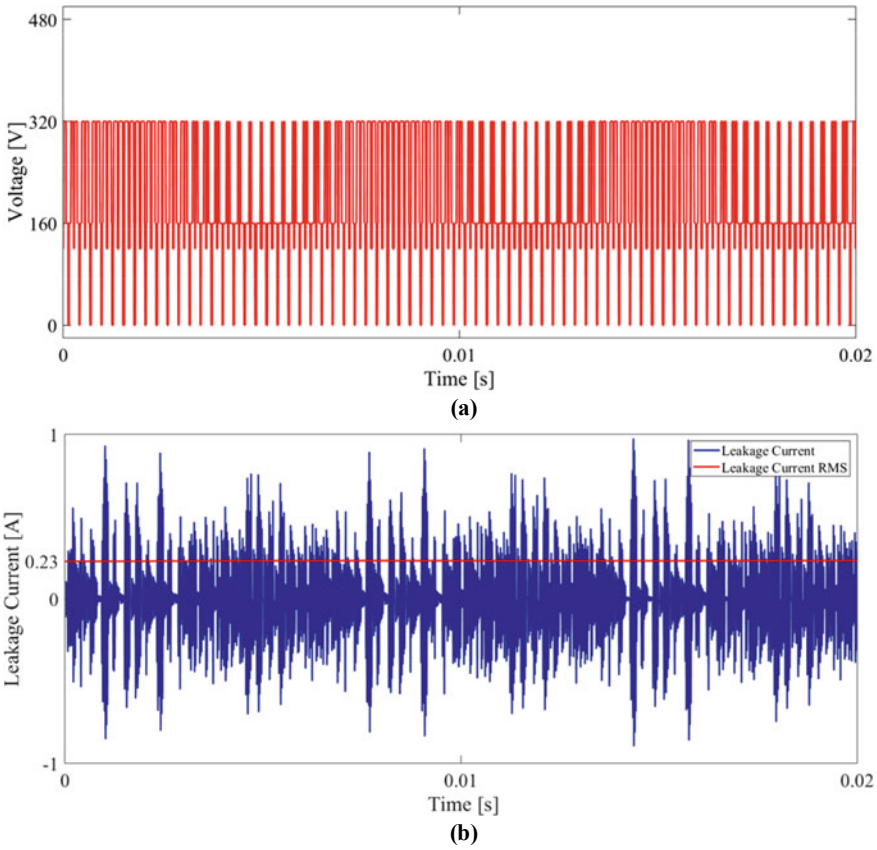

Fig. 17 Simulation results of H7 inverter **a** CMV, **b** leakage current

of the four-leg converter is shown in Fig. 20b; it was further reduced to 70 mA due to a reduction in the CMV variation across the stray capacitance.

The CMV generated by the four-leg inverter (Fig. 21a) is constant at 240 V ($V_{dc}/2$) irrespective of the state of operation. Due to the constant voltage across the parasitic capacitance, the leakage current is ideally zero. Because of the non-idealities, some amount of leakage current of 0.232 mA (RMS) is presented, and it is shown in Fig. 21b.

DCM232 inverter is having two isolated DC sources results in four stray capacitances illustrated in Fig. 15a. The voltage across these four capacitors is illustrated in Fig. 22. Due to the zero rate of change in the voltage across the stray capacitors, the leakage current associated with this topology is typically zero. The summary of the aforementioned inverter topologies is presented in Table 12.

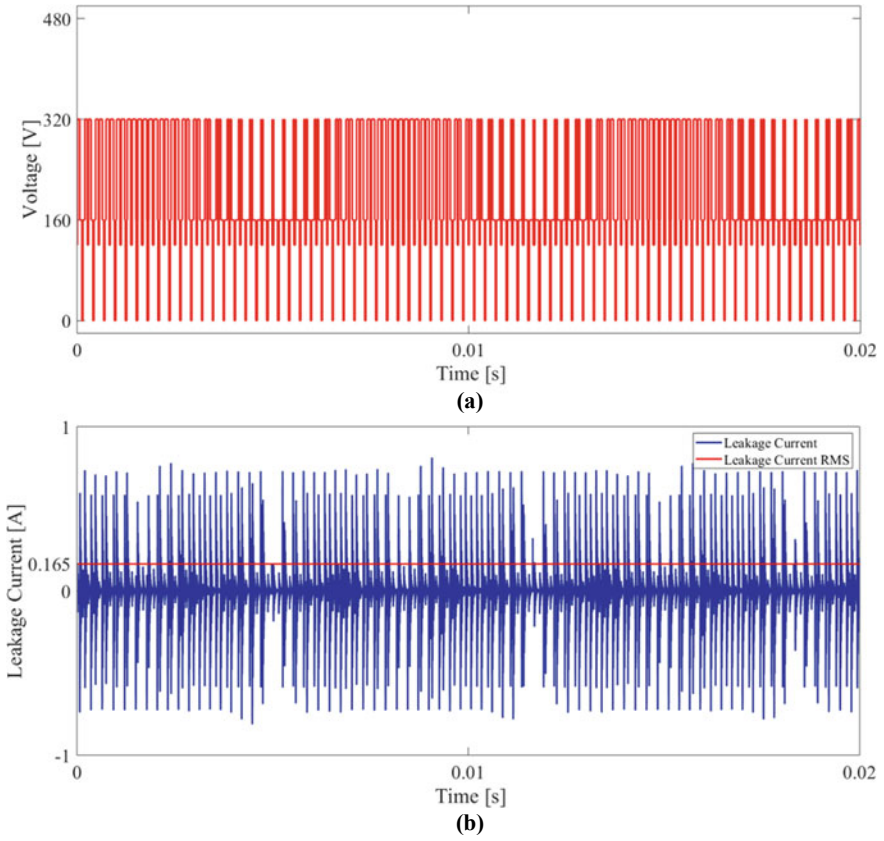

Fig. 18 Simulation results of H8 inverter **a** CMV, **b** leakage current

6 Concluding Remarks

This chapter exhaustively discussed the classification of power electronic interfaces and issues with transformerless three-phase grid-tied PV inverters. The operation and features of the leakage current minimization approaches such as advanced pulse width modulation techniques and power converter topology modifications in the transformerless grid-tied PV inverters are discussed in detail. In this chapter, a comprehensive analysis of state-of-the-art DC and AC bypass topologies derived from the conventional two-level inverter in terms of common-mode voltages and leakage currents is performed through MATLAB simulations. Most of the inverter topologies rely on the concept of disconnection of the inverter from the PV sources during zero states intervals, which enables breaking the leakage current conduction path. However, the CMV is not zero in such topologies. On the other hand, the DCM232 inverter and four-leg inverter can mitigate the leakage current with constant CMV by decoupling on DC and AC sides, respectively. It is anticipated that advanced

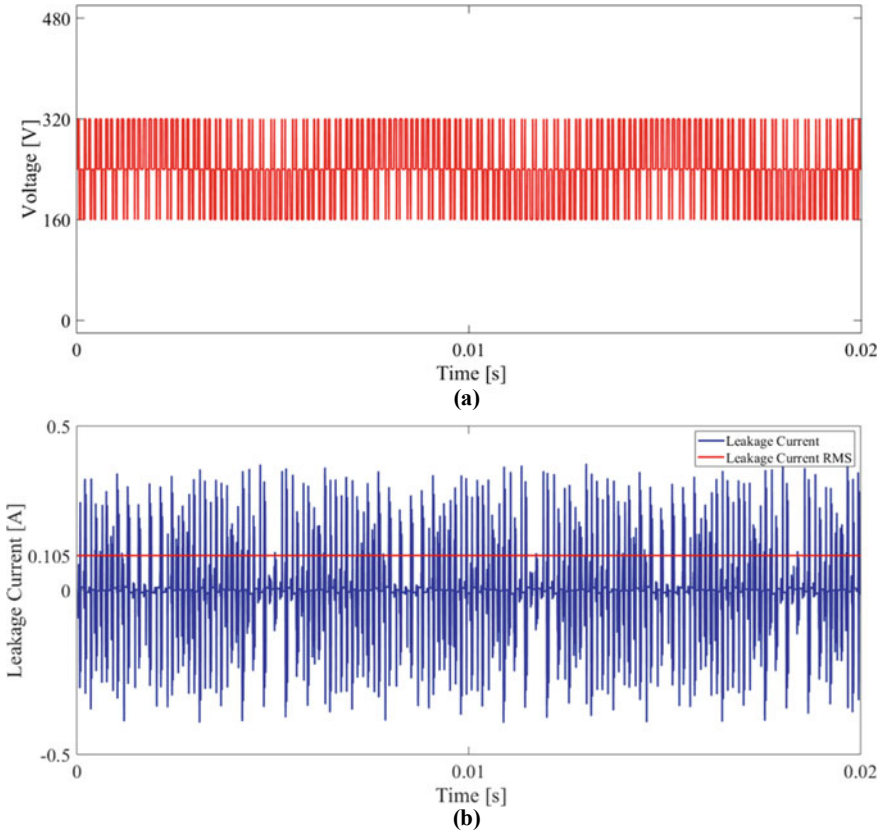

Fig. 19 Simulation results of Three-phase seven switch inverter **a** CMV, **b** leakage current

converter topologies with wideband gap devices will be dominantly used in the solar industry to achieve technical and economic benefits in near future.

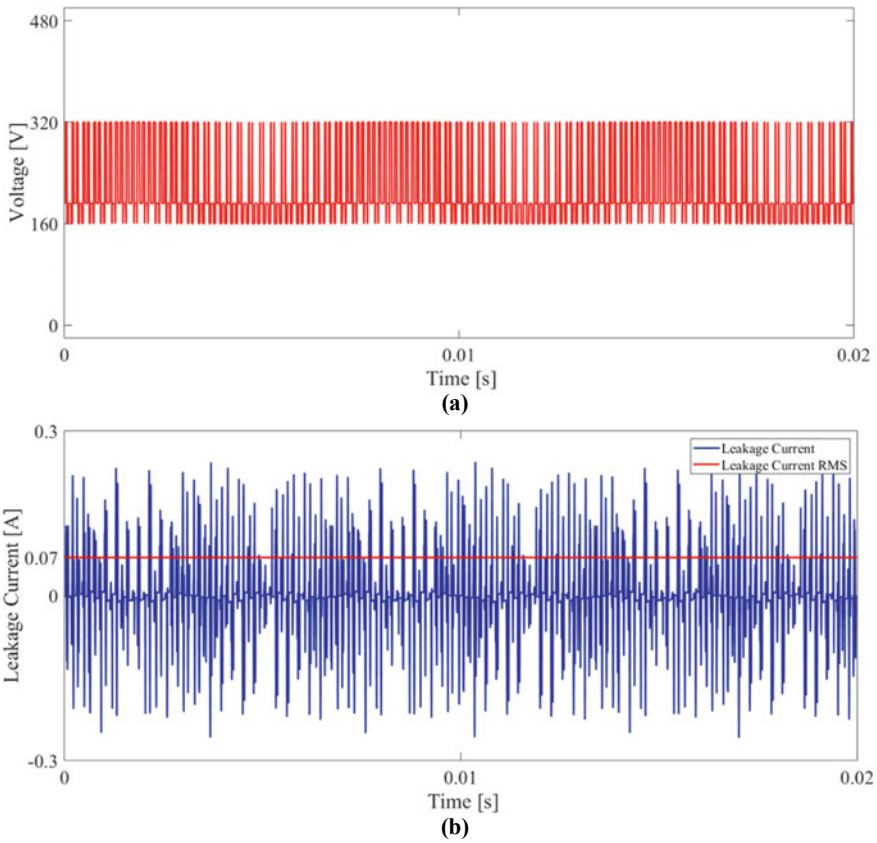

Fig. 20 Simulation results of three-phase eight switch inverter **a** CMV, **b** leakage current

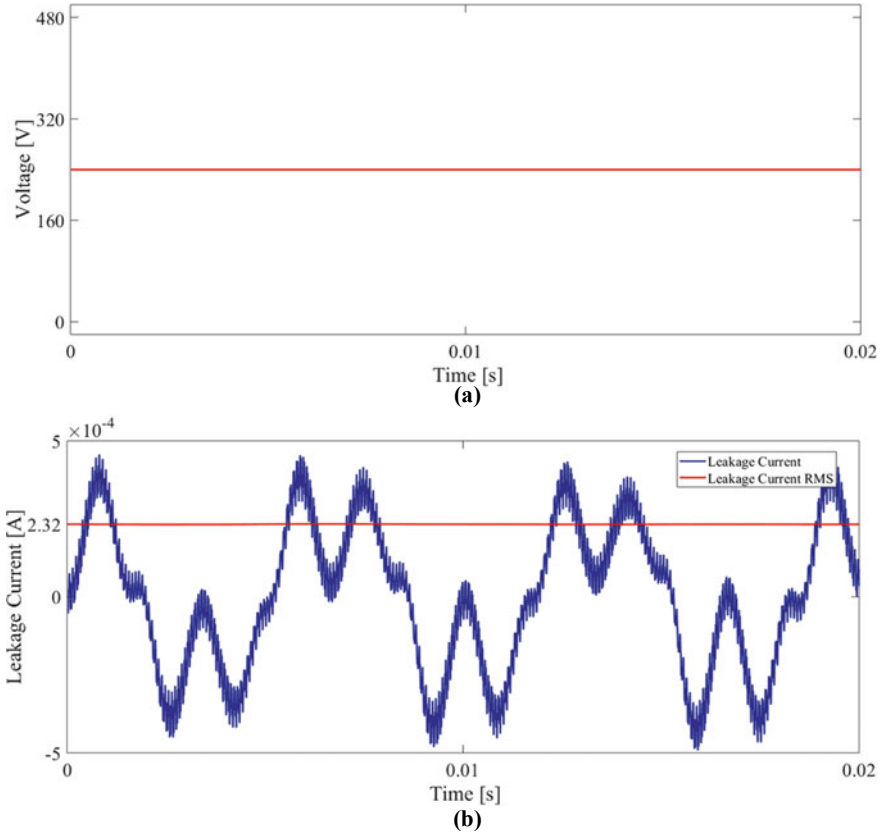

Fig. 21 Simulation results of Three-phase four-leg inverter **a** CMV, **b** leakage current

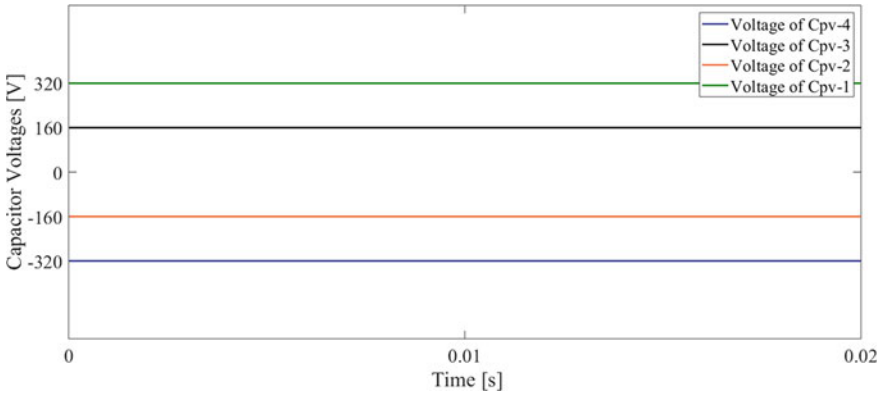

Fig. 22 Parasitic capacitance voltages of DCM232 inverter

Table 12 Summary of transformerless PV grid-tied systems

	Topology	Number of switches + Diodes	Overall variation in CMV	RMS value of leakage current (mA)	Voltage stress across the inductor	Decoupling side
1	H6 (SPWM)	6 + 0	0 to V_{dc}	343.5	V_{dc}	–
2	H6 (SVPWM)	6 + 0	0 to V_{dc}	340	V_{dc}	–
3	H7 topology [32]	7 + 0	0 to 2 * $V_{dc}/3$	238.5	V_{dc}	DC side
4	H8 topology [34]	8 + 0	0 to 2*$V_{dc}/3$	168	V_{dc}	DC side
5	7-switch inverters [35]	7 + 6	$V_{dc}/3$ to $2V_{dc}/3$	106.9	V_{dc}	AC side
6	8-switch inverters [36]	8 + 0	$V_{dc}/3$ to $2V_{dc}/3$	69.3	V_{dc}	AC side
7	Four-leg inverter [37, 38]	8 + 0	Constant	0.00626	V_{dc}	AC side
8	DCM232 3-ϕ inverter [39]	10 + 0	Constant	0	V_{dc}	DC side

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