Study of Filters for Improving the Output of Cascaded Seven-Level Inverter

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Abstract Poor quality is one of the prime problems in the electrical system. In recent times, high power demand and good quality of power are major concerns in an electrical system. In this paper, a conventional multilevel inverter topology is proposed and to design the LC filter and LCL filter that attenuate the ripple in the output waveform of the proposed MLI topology. The proposed topology used symmetrical configuration, i.e., the dc-link voltage is the same for each H-bridge cell. The performance of MLI is calculated by THD parameter, and the results of the proposed topology with LC, LCL circuit, and normal circuit are compared along with PD, POD and APOD-PWM techniques, followed by over and under modulation index.

Keywords Multilevel inverter · THD · PWM · Filter · Cascade H-Bridge

1 Introduction

A multilevel inverter is the most popular power converter device used for high power and high voltage applications [1]. The application based on renewable energy is more popular nowadays and power quality is a big challenge. The multilevel inverter is used in renewable power applications as its input is connected to the renewable energy source and its output to the grid. All the converters are nonlinear devices, so they create harmonics, and these harmonics degrade the quality of output power. To eliminate this problem the filter circuit is used at the load side. The selection

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of the filter is also a big challenge to attenuate particular harmonics. In this paper, two passive filter circuits, LC circuit and LCL circuit, are used, and the performance of these two filter circuits on a seven-level cascade H-Bridge PWM inverter was compared. The performance is measured in terms of total harmonic distortion factor.

2 Proposed Topology

The proposed topology is a conventional cascade H-Bridge seven-level inverter. It has an isolated DC voltage supply for each cell. In a seven-level topology, three H-bridge cells require and three separate DC voltage sources [2] are needed. If the DC voltage source has equal magnitude the configuration is known as symmetric configuration, and if these DC voltage sources have unequal magnitude then the configuration is known as asymmetric configuration. Table 1 shows the switches sequence to obtain voltage levels of the proposed topology. For +3 V level switch sequence 1, 3, 5, 7, 9, 11 is ON and the remaining switches are off. For +2 V level switch sequence 1, 3, 5, 7, 9 and 10 is ON. For +1 V level switch sequence 1, 3, 5, 6, 9 and 10 is ON. For +1 V level switch sequence 1, 3, 5, 6, 9, 10 is ON. For 0 V level switch sequence 1, 2, 5, 6, 9, 10 is ON. For −1 V level switch sequence 2, 4, 7, 8, 11, 12 is ON. For − 2 V level switch sequence 2, 4, 6, 8, 11, 12 is ON. For −3 V level switch sequence 2, 4, 6, 8, 10, 12 is ON. Switch configuration is chosen in such a way that stress on the switch remains low. So here use the redundancy method to select the switch to achieve the particular voltage level.

The proposed topology is suitable for high voltage and high power applications [3]. The advantage of the proposed topology is that it does not require any clamping diode and capacitor, so the required component in the proposed topology is less than the other two-diode clamped and flying capacitor topology [4, 5] (Fig. 1).

Table 1 Switching sequence of the proposed topology

Level	Magnitude	Switch configuration											
		1	2	3	4	5	6	7	8	9	10	11	12
1	+3 Level	ON		ON		ON		ON		ON		ON	
2	+2 Level	ON		ON		ON		ON		ON	ON		
3	+1 Level	ON		ON		ON	ON			ON	ON		
4	0 Level	ON	ON			ON	ON			ON	ON		
5	−1 Level		ON		ON			ON	ON			ON	ON
6	−2 Level		ON		ON		ON		ON			ON	ON
7	−3 Level		ON		ON		ON		ON		ON		ON

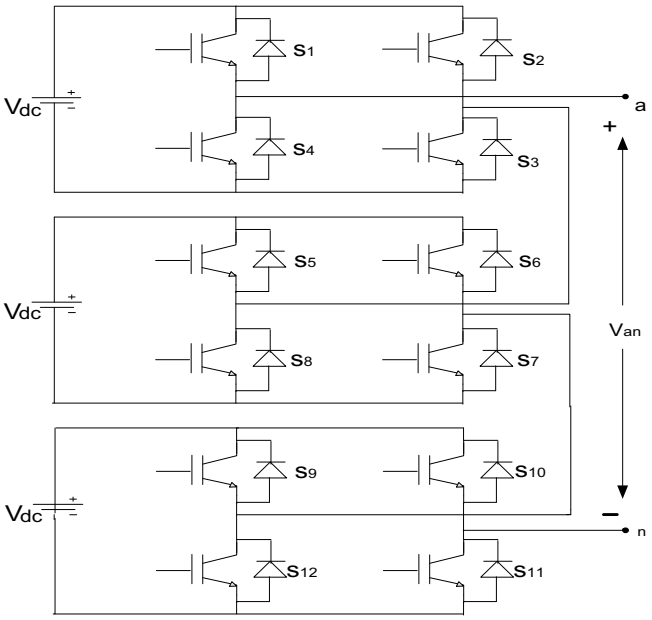


Fig. 1 Proposed topology circuit diagram

3 PWM Techniques in the Proposed Topology

The objective of PWM is to control inverter output and reduce the harmonics in the output waveform [6]. In this technique the pulses are generated according to output voltage level and this is done by comparing two waveforms. In this one waveform is a reference waveform of fundamental frequency and the other is a carrier waveform of high frequency [7], [8]. The frequency of carrier waveform is very high compared to reference waveform [9]. In this paper for the proposed topology the level-shifted PWM technique is used as given below. The proposed topology is a seven-level topology, so here the reference signal is a sinusoidal waveform of 50 Hz frequency and the number of carrier waveforms is 6 and each has 2 kHz frequency.

3.1 PDPWM

All carrier waveforms have the same magnitude and same frequency and have zero-phase shifting to adjacent waveform [10]. Figure 2 shows the configuration of PDPWM.

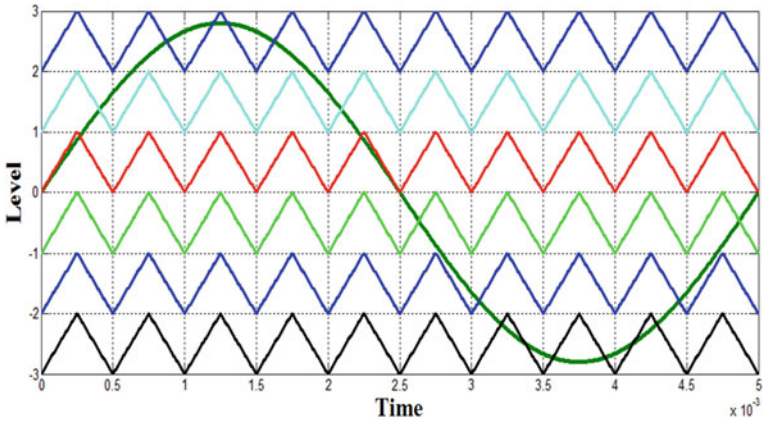


Fig.2 Reference and carrier waveform arrangement for PDPWM

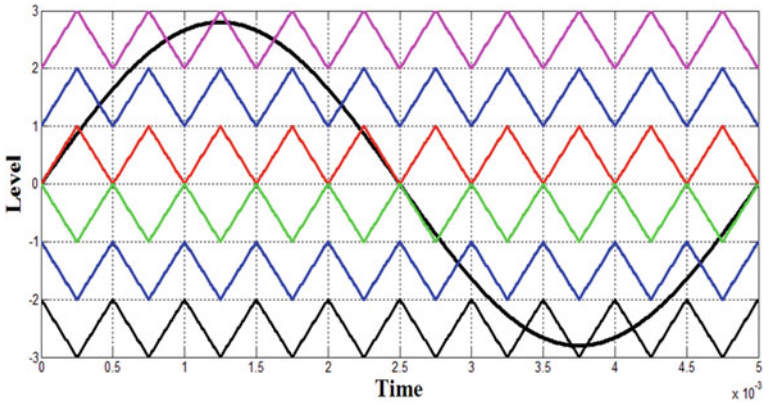


Fig.3 Reference and carrier waveform arrangement for PODPWM

3.2 PODPWM

All the carrier waveforms have the same magnitude and same frequency but the positive carrier and negative carrier groups have 180° phase shift. Figure 3 shows the PODPWM configuration.

3.3 APODPWM

All carrier waveforms have equal magnitude and frequency but adjacent carriers have 180° phase shift to each other. Figure 4 shows the APODPWM configuration.

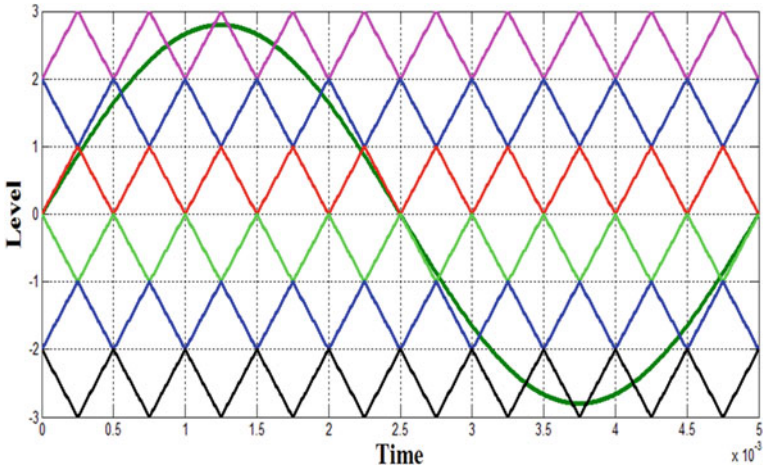
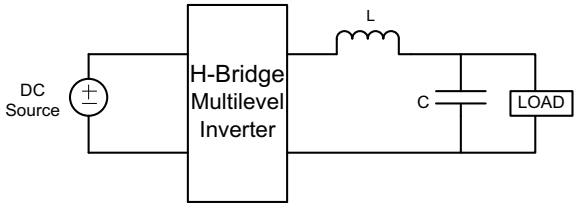


Fig. 4 Reference and carrier waveform arrangement for APODPWM

4 Passive Filter Circuit

In this paper, to improve the quality of voltage at the load side passive filter circuit is used. Passive filter circuits are of different types as single L with load, which gives less distorted output current to load. The combination of L and C has a different combination which provides the attenuation to harmonics [11]. In this paper two configurations of passive filter circuit are used, one is LCL filter circuit and the second is LC filter circuit. The LC circuit is a low pass filter circuit and it is able to attenuate the lower order harmonics in the output waveform. It is a second-order filter circuit giving −40 dB/decade attenuation and LCL circuit as high-pass filter circuit and a third-order filter circuit that gives −60 dB/decade attenuation. The elements L and C are considered lumped. The arrangement of the LC and LCL filter circuits is shown in Figs. 5 and 6.

Fig. 5 LC filter arrangement



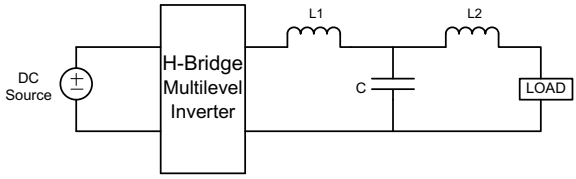


Fig. 6 LCL filter arrangement

5 Simulation Result

The simulation result for the proposed topology is derived from MATLAB Simulink 2010b software. The parameters used to simulate the results are DC input voltage is 10 V, reference waveform frequency is 50 Hz, carrier waveform frequency is 2 kHz, loads are resistive in nature and have the value of 10 Ω; filter circuit has L = 10 mH, C = 1 microfarad, L1 = 10 mH and L2 = 0.5 mH. The result simulated with over, under and unity modulation index with respect to level-shifted PWM techniques for LC, LCL filter circuit and with a normal circuit of the proposed topology (Figs. 7, 8, 9, 10, 11 and 12).

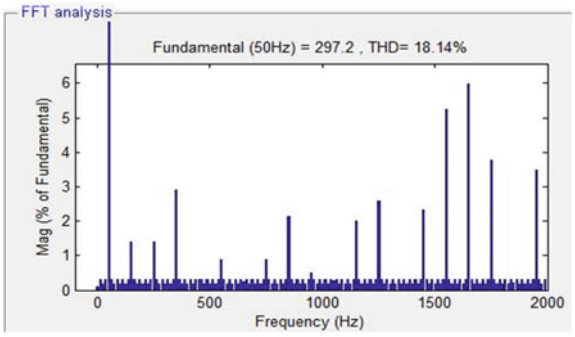


Fig. 7 THD of APOD with Ma = 1.0 (without filter circuit)

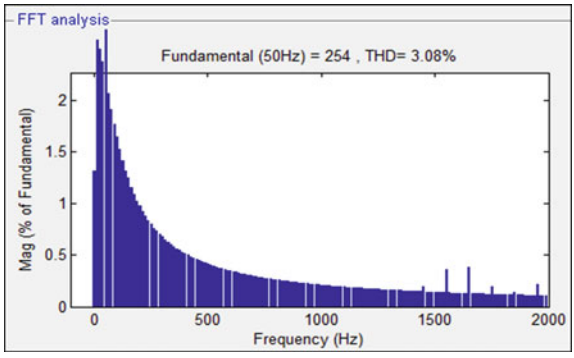


Fig. 8 THD of APOD with Ma = 1.0 (with LC filter circuit)

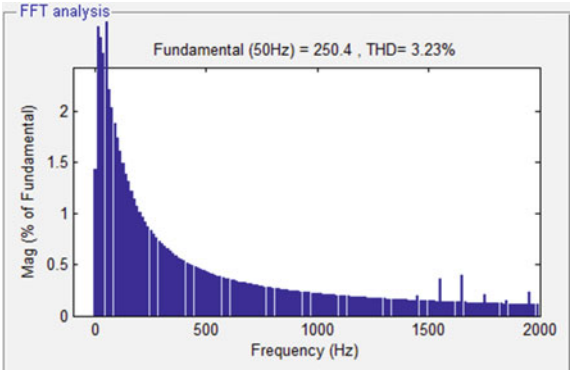


Fig. 9 THD of APOD with Ma = 1.0 (with LCL filter circuit)

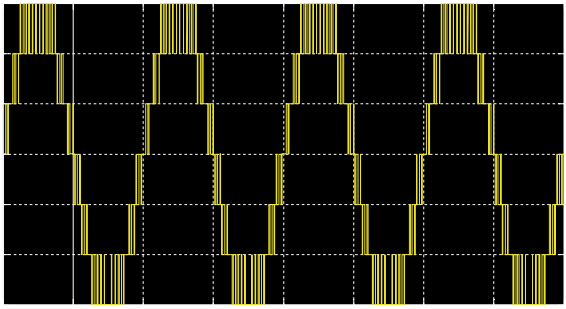


Fig. 10 Output waveform of without filter circuit

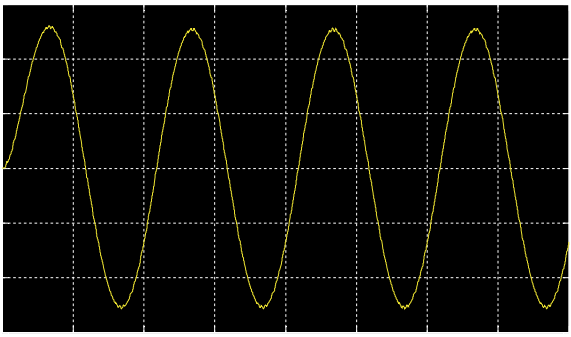


Fig. 11 Output waveform of LC filter circuit

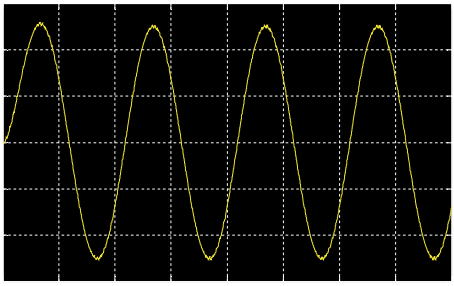


Fig. 12 Output voltage waveform of LCL filter circuit

6 Conclusion

The comparative study of total harmonic distortion analysis for the proposed topology with passive filter and normal circuit is presented in this paper. With the use of a filter circuit, the output waveform has less harmonic component, which improves the quality of power. Table 2 shows the simulation result and made a comparison between the normal circuit, LC filter circuit and LCL filter circuit. Figures 13, 14 and 15 show the comparison graph for over, unity and under modulation index, which shows the % total harmonic distortion value in the proposed topology with passive filter circuit and normal circuit followed by level-shifted PWM techniques. The LCL filter sometimes causes steady-state and transient problems due to resonance, hence the LC filter is widely used as it attenuates lower order harmonics which is more important in inverter application. The result obtained with the filter circuit is within the IEEE THD limit. This shows the usefulness of the filter circuit in the proposed topology.

Table 2 % THD result of the proposed topology

Modulation index (MI)		Without filter circuit			LCL filter circuit			LC filter circuit		
		PD	POD	APOD	PD	POD	APOD	PD	POD	APOD
Over modulation	**1.1**	17.05	16.88	17.05	3.52	3.61	3.68	3.42	3.50	3.58
Unity modulation	**1.0**	18.88	18.20	18.14	3.06	3.23	3.23	2.91	3.08	3.08
Under modulation	**0.9**	22.92	23.05	22.92	3.18	3.29	3.29	3.03	3.14	3.13

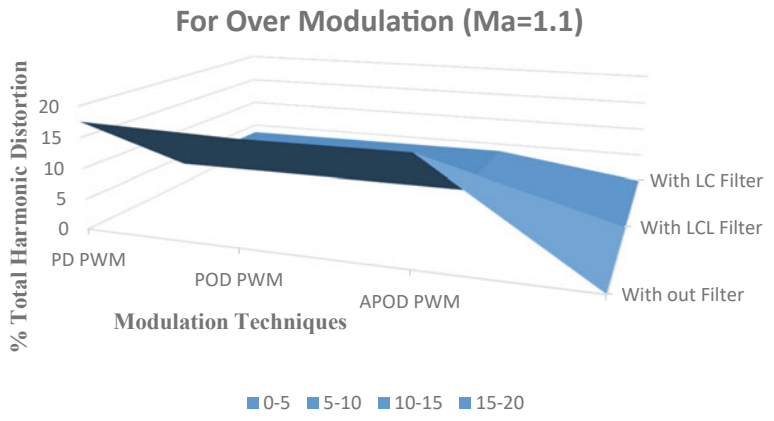


Fig. 13 Comparison graph for over modulation index

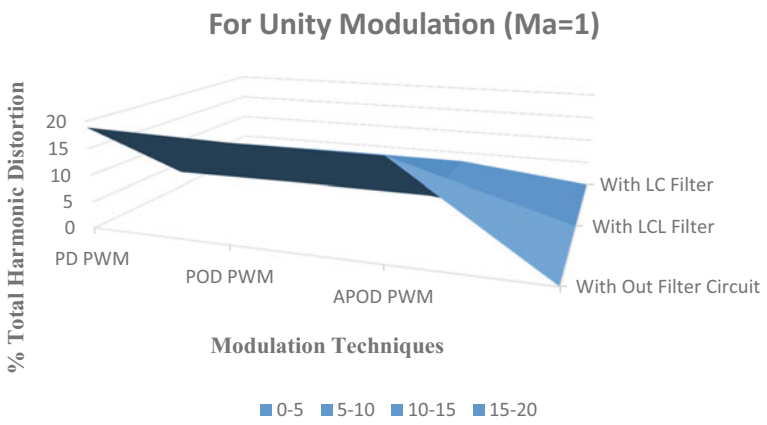


Fig. 14 Comparison graph for unity modulation index

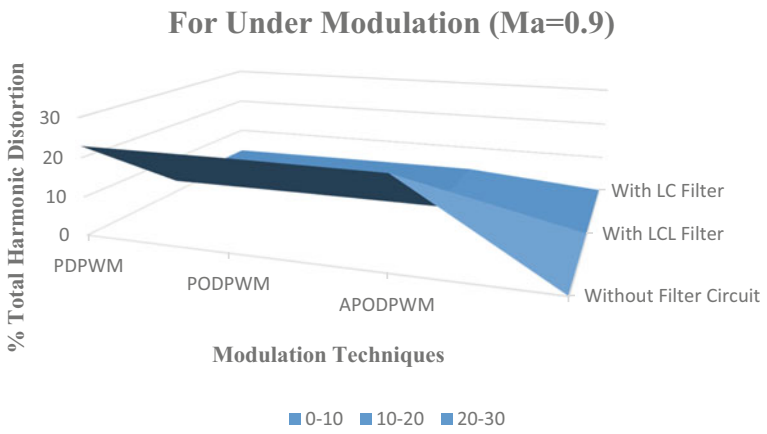


Fig. 15 Comparison graph for under modulation index

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