Performance Analysis and Comparison of Low Power Various Full Adder Circuits

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Abstract. An adder is an integral part of many digital devices, DSPs, etc. Due to the reduction in leakage power and the location, recent VSSI circuits have been created. As the technology continuously decreases, the transistor threshold voltage is also decreased and the static power discharge is therefore high. Different fulladder (FA) were modeled in this paper and evaluated afterward. Specific full Adder circuits like 90 nm have achieved leakage power consumption. The designed Diverse FA circuits are compared in terms of leak energy consumption & surface area with Cadence instruments. We designed and compared 28T, 14T, 12T, 10T and 9T Full adder circuit, in terms of area, power.

Keywords: Beam steering · Microstrip antenna · Satellite communication

1 Introduction

The energy consumption in Very Large Scale Integrated (VLSI) circuit designs is a major performance factor. However, the explosive growth of VLSI technology leads designers to seek smaller silicon areas, longer battery life, higher speeds, lower power use and higher circuit efficiency, with demand and popularity for mobile devices. The design criteria for a complete adder cell requires the transistor counts, which greatly affect the design complexity of a large number of feature units such as multiplier and algorithmic logistic units, the optical Adder ALU) [1, 2]. Speed of design is restricted due to size of transistor, the capability of the parasitic and critical path delay. Driving power of a FA is very significant since it is used primarily in the cascade setup where one output provides the input for the other different full adder circuits for design accents such as delay, area & power have been proposed. The use of a transistor logic has been commonly used for reducing power consumption [3, 4] among the designs with less transistor numbers. Pass-transistor logic & CMOS logic [5] divided into two forms. In this paper, the development of all adherence circuits within terms of lower power consumption, higher speed & less chip size has been briefly described (Fig. 1).

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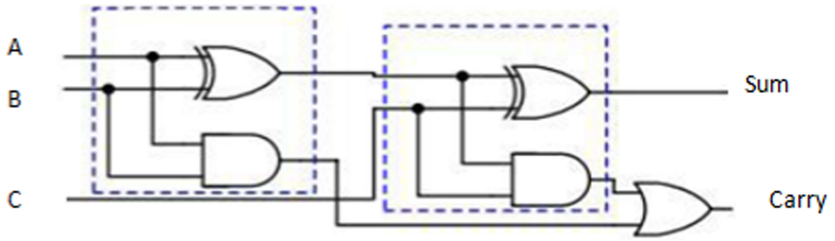

Fig. 1. Circuit diagram of full adder Circuit has three inputs A,B & C and two outputs sum and carry.

2 Techniques

Main work in electronic field is energy-efficient design of portable devices such as Desktop notebooks, mobile phones, tablets. The decrease area is one way to achieve a less efficient design. In ALU operations, binary additives play an important role. A number of adder circuits have recently been suggested. The goal of the design, however, will differ. Main focus of this paper is on power reduction [6] and the circuit field. A designer can use a large array of different techniques such as CPL, C-CMOS, DC & DC gate, GDI & 28 transistors, the complete CMOS-based adder design [7] is similar to conventional PMOS and NMOS transistors. Designer has full adder designs. By set of transistors makes full adder for bad driving ability. It covers more area, since it has a lot of transistors, another important design technique is Complementary pass transistor logic (CPL). Primary difference between complementary CMOS and CPL [8] is that pass transistor is an input from the source area. But complementary CMOS acts as source inputs on power lines. CPL logic is much better than CMOS logic due to threshold voltage drop but no more than C-CMOS. Also, this logic requires inverters at output stage to achieve sufficient instability. A transmission Gate Adder Designs Pull-up and Pull-down Transistor Complimentary Properties. There are twenty transistors. This TGA (Transmission Gate Adder) is composed of a PMOS and NMOS transistor parallel connectivity. Complementary signals control the operation of the circuit. Major drawback of TGA compared to pass-transistor logic is that it uses twice number of transistors. The primitive gates, such as the 4-transistor full adder [9] XOR gate based on the Majority function, eliminates the need for more time.

2.1 CMOS Full Adder

An adder is an electronic digital circuit used to add binary numbers. Full adder is a three-bit additional combination circuit (Fig. 2).

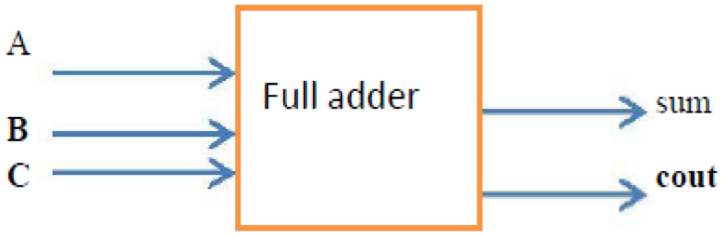

Fig. 2. Block diagram of full adder

Take a CMOS FA. This circuit consists of two operands, A & B, & an input transmission is Cin. This generates the sum

$$SUM = A \oplus B \oplus Cin$$

$$CARRY = AB + BCin + ACin$$

2.1.1 Various Full Adder Circuits Comparative Analysis

2.1.1.1 28T Full Adder Circuits

On the basis of standard CMOS topology, as exposed in Fig. 4a, traditional CMOS adder cells using 28 transistors were discussed in paper [10]. Due to the high number of transistors & PMOS transistors from pull up, its high energy consumption was defined, and this resulted in high retardation and dynamic capacity. It was based on standard CMOS structure. Therefore, the FA with 28 transistors was presented in paper. Same one as rest of the circuit & Transient waveform is shown in Fig. 3 and 4.

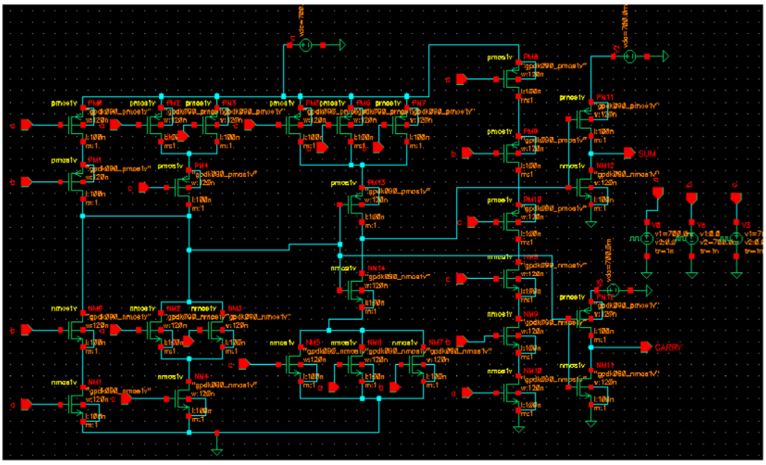

Fig. 3. Schematic of 28T full adder circuit

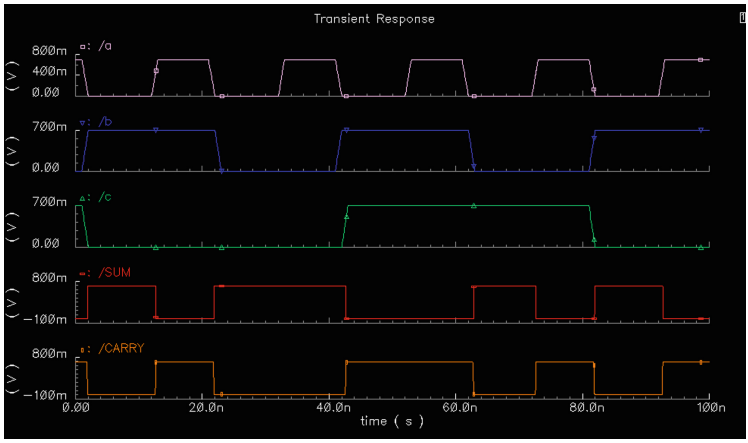

Fig. 4. Transient response of 28T full adder circuit

2.1.1.2 14T Full Adder Circuits

Paper [11], contrasts numerous current full adder circuits including many circuits such as the CMOS TG, Gate Diffusion Input (GDI), Complementary Pass transistor Logic (CPL) Low Power Full Adder, GDI-based FA, Pass Transistor Logic (PTL). Thus Fig. 5 shows 14 transistors using the full adder scheme, and Fig. 6 shows Transient Response(TR).

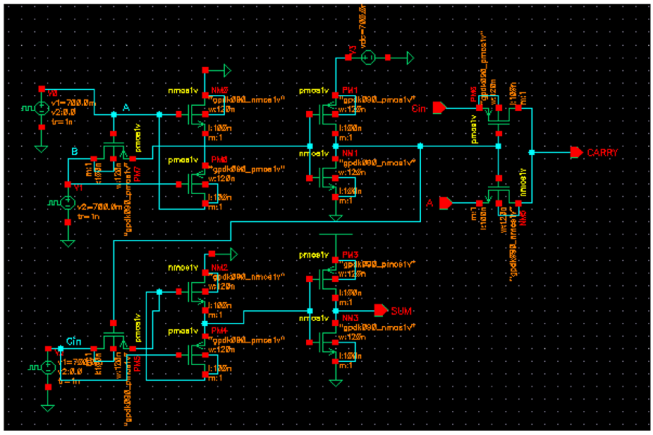

Fig. 5. Schematic of 14T full adder circuit

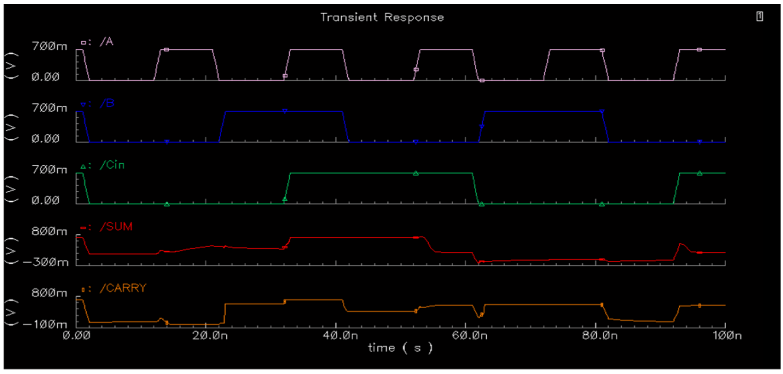

Fig. 6. Transient response of 14T full adder circuit

2.1.1.3 12T CMOS Full Adder

In the paper [12], two new designs FA for XOR transistors were added. Simulations of similar were performed at dissimilar reverse supply voltages of NMOS transistors and there was increased consumption of adder electricity. So, in that paper full adder with 12 Transistor was introduced & we choose and took the same and was compared with other circuits and the schematic 12T FA Circuit & TR is shown in Fig. 7 and 8.

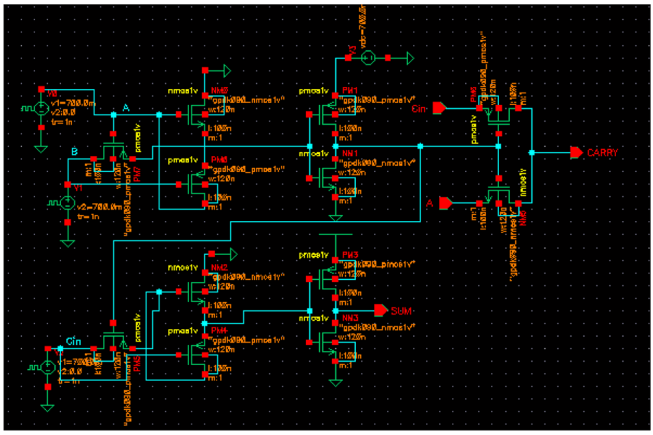

Fig. 7. Schematic of 12T full adder circuit

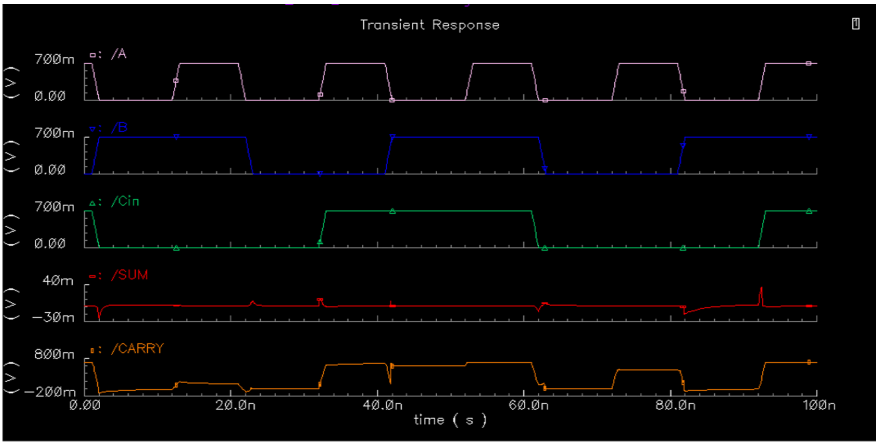

Fig. 8. Transient response of 12T full adder circuit

2.1.1.4 10T CMOS Full Adder

We required 4 Transistors XOR and XNOR circuits and 2-to-1 multiplexers to implement specific 10 CMOS full-adder transistor circuits. Figure 9 illustrations the 10T full adder schematic & Fig. 10 shows the output waveform.

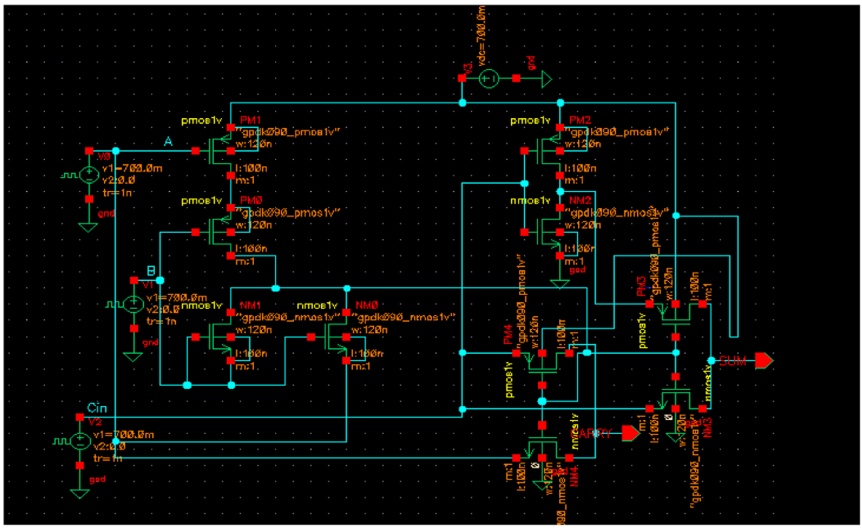

Fig. 9. Schematic of 10T full adder circuit

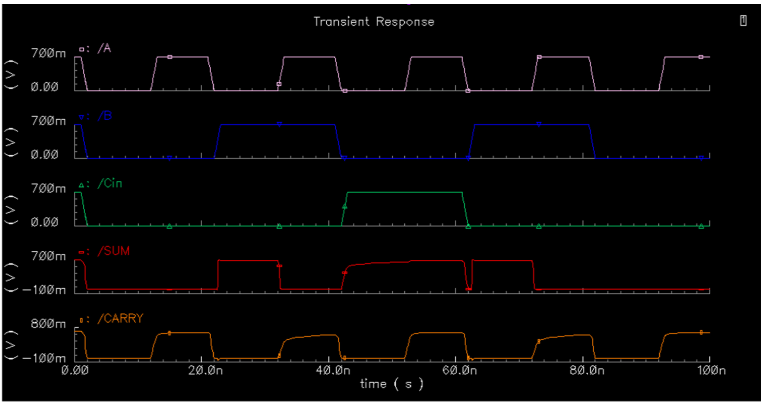

Fig. 10. Transient response of 10T CMOS full adder

2.1.1.5 9T CMOS Full Adder

New 9 T FA cell simulations at low voltages are given in paper [13]. Main aim of design was to achieve low energy consumption & total voltage swing at low supply voltage. The proposed model demonstrated its dominance in terms of energy usage, power product delays (PDP), resilience of temperatures and tolerance to noise. Therefore, in that paper, the whole adder with 9 transistors was presented and we chose the same one, which was contrasted with other circuits and the scheme 9 T Full Adder & TR is shown in Fig. 11 & 12.

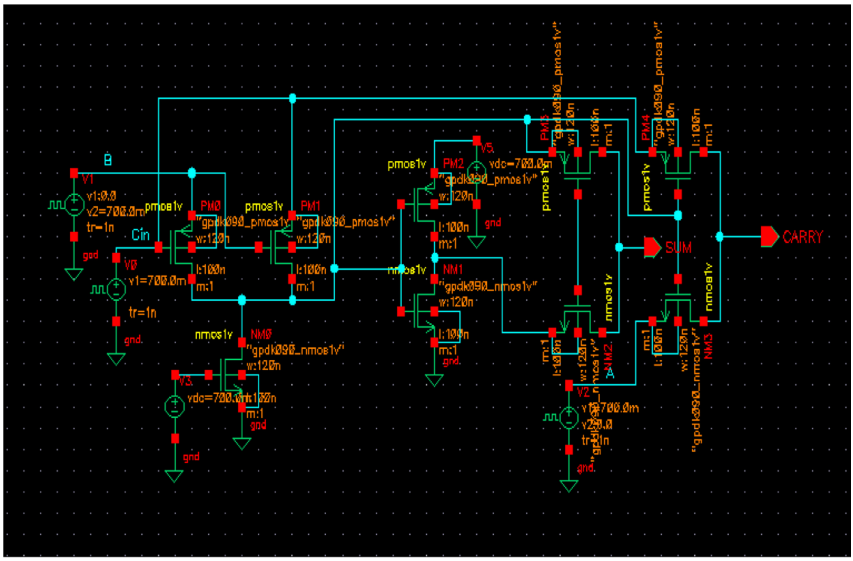

Fig. 11. Schematic of 9T CMOS full adder

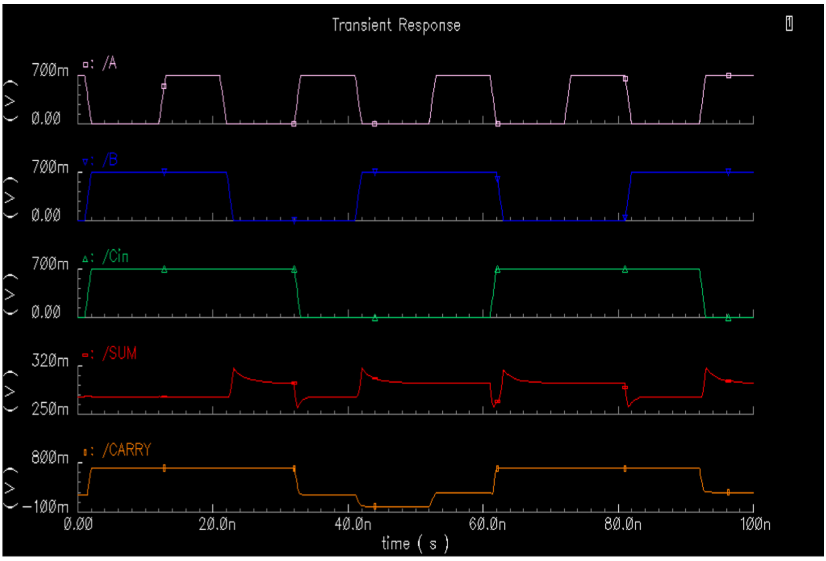

Fig. 12. Transient response of 9T CMOS full adder

3 Simulation Result

The Gate Leakage is the only main mechanism at the temperature of 27 °C. There are different techniques used to decrease power consumption and to preserve the output of the 28T, 14T, 12T, 10T and 9T Full Adder Circuit (FAC). Different Full Adder circuit

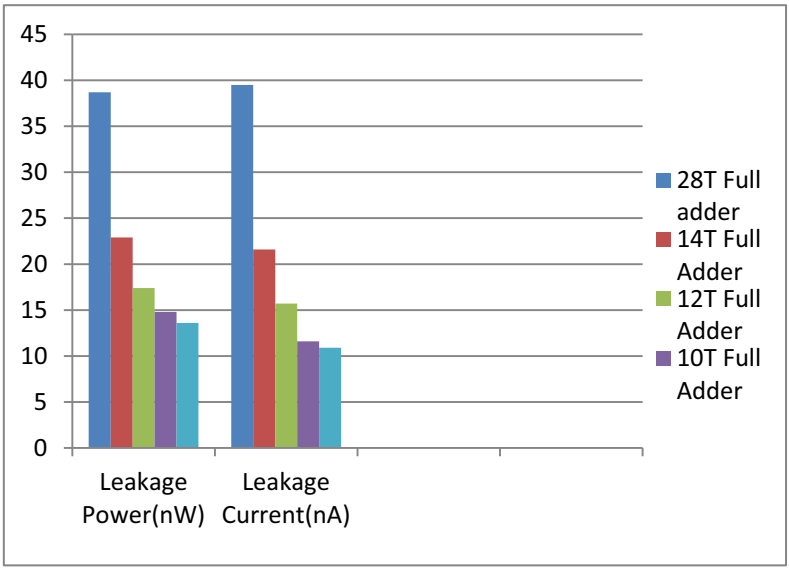

Fig. 13. Comparison graph of full adder

Simulators with 90 nm and 45 nm nominal voltage supply Vdd = 0.7 V. Its comparative analysis of Various FAC the parameter like Leakage Current and leakage power is shown in below in Graph and Table 1 respectively (Fig. 13).

3.1 Comparative Analysis Result Summary of Various FACs Shown Below Table 1

Table 1. Simulated result summary

Parameter of performance FAC	28T FAC	14T FAC	12T FAC	10T FAC	9T FAC
Technology used	90 nm	90 nm	90 nm	90 nm	90 nm
Supply voltage	0.7 V	0.7 V	0.7 V	0.7 V	0.7 V
Leakage power	38.7 nW	22.9 nW	17.4 nW	14.8 nW	
Leakage current	39.5 nA	21.6nA	15.7 nA	11.6 nA	10.9 nA
Transistor count	28	14	12	10	9
Area used	Large	Large	Large	Less	Less

4 Conclusion

Specific Full Adder circuits were planned for review in this paper. Different Full Adder designs have used leakage power and leakage current in the circuit. Different Full Adder circuits are compared with sentences of leaking capacity, leakage current and surface area. In terms of power and surface area, we built and compared 28T and 14T full adder circuit, 12T, 10T, and 9T full adder circuit. This removes problems of diving ability from other full adder modules and catches low power for use at 0.7 V. In addition, many full adder circuits have a low power consumption as far as the number of transistors needed to build a complete combination circuit is concerned from this correlation Table 1. According to Various FA circuits, transistor count and power of 9T CMOS Full Adder is less and shows the better performance in comparison to other circuits.

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