# Evaluation of Digital Circuit Methodologies in Nanotechnology Using QCA - Quantum Dot Cellular Automata


**Madhavi R. Repe and Manisha Waje**

**Abstract** Quantum dot Cellular Automata (QCA) has more popularity in the near market due to its advantages over CMOS technology such as high device density, low power consumption and high computing efficiency. The major concern in circuits is to achieve improvement in QCA parameters like number of QCA Cells, cells area, total area, delay, energy consumption and single or multilayer layout. In this paper we will discuss about various techniques or methodologies to achieve improvement in these parameters. Different methodologies need to be designed to have optimization, automation and verifications in design. These techniques are primarily based on Logic synthesis, layers, clocking in QCA, feedback in QCA, QCA cell arrangements, use of tools to design the circuits, use of 3 × 3 or 5 × 5 QCA tiles etc. In today's era, less energy consumption is also a very important parameter. The main objective of this paper is to get the details of these techniques to improve the parameters. QCADesigner 2.0.3 and QCADesigner–E software are used to get the implementations in QCA field.

**Keywords** QCA (quantum dot cellular automata) · SRAM (static random access memory) · MV (majority voter) · 5-input majority gate (MV5) · PPDD (priority-phased decomposition-driven) · CLA (carry look-ahead adder)

## 1 Introduction

International Technology Roadmap for Semiconductors (ITRS) [1] has devised Nano devices like Carbon nanotube transistors (CNT), Single Electron Transistors (SET), Resonant Tunnelling devices (RTD), Quantum dot Cellular Automata (QCA) etc. as shown in Fig. 1. These are used to overcome the limitations of CMOS devices scaling. QCA is the best nanotechnology device among all these Nano devices.

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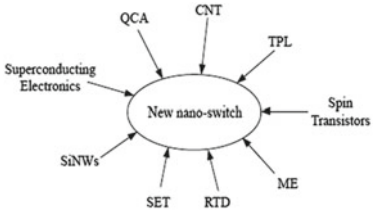



**Fig. 1** Nano devices [1]

QCA is efficient, has very high device density and low power consumption. It is transistor less and can operate at Terahertz (THz) range. CMOS technology works on current switching whereas QCA represent binary information on the cells.

QCA is now used to design digital circuits in almost all the fields. Researchers have designed the circuits with different methodologies in QCA. In this paper, these different methodologies are discussed with their method and achievements in terms of various parameters.

In the remainder of this work, in Sect. 2, earlier reported work on QCA methodology is reviewed and compared. Section 3 shows the implementations of different methodologies for different circuits. This paper is one umbrella under which different methods are compared and analyzed. In Sect. 4, the work is concluded.

## 2 Methodologies

Till now, researchers have proposed different ways to design digital circuits to achieve optimization in terms of circuit area, number of cells, speed and complexity. In this section, these different methodologies are studied, analyzed and compared with standard parameters of interest. Various methodologies used are coplanar, multilayer, novel input technique, Bottom up design approach with special cell arrangements, keeping fixed input cells, inter cellular effect technique, PPDD technique, using 3 input standard MV gate and 5 input MV gate, using only one type of cell, tile based, models based, with simplified Boolean expressions, using different clocking etc. Circuits like NOT gate, XOR gate, the one used in building almost all the complex circuits, multiplexer, full adder, parity generator, latch, RAM etc. are implemented with these methodologies. Tables 1, 2 and 3 shows the comparison of all methods with respect to parameters and circuits implemented.

Comparative table for the methodologies shows that cell interaction or intercellular effect technique is the best to implement XOR gate and parity generator (4 bit, 8 bit, 16 bit and 32 bit) with low power consumption, less number of cells, less area and increased speed. Novel input technique is the best way to implement 2:1 multiplexer. Many implementations are seen for full adder but using MV5 is the best method with least cells, area and delay as indicated in Table 4.

**Table 1** Different methodologies used to implement XOR gate

| Methodology/technique | Cell count | Area ($\mu m^2$) | Delay | Circuit implemented |
|---|---|---|---|---|
| Multilayer crossover [2] | 24 | 0.03 | 0.75 | XOR, multilayer |
| Novel input technique [3] | 29 | 0.02 | 0.75 | XOR |
| Bottom up design with special cell arrangements [4] | 54 | 0.08 | 1.5 | XOR, coplanar wire crossing |
| With fixed input cells [5] | 55 | – | 1 | XOR gate with 1 fixed cell, different phases, single layer |
| Cell interaction technique [6] | 9 | 0.009 | 0.25 | Low power XOR gate, no crossover |

**Table 2** Different methodologies used to implement multiplexer

| Methodology/technique | Cell count | Area ($\mu m^2$) | Delay | Circuit implemented |
|---|---|---|---|---|
| Multilayer crossover [2] | 24 | 0.02 | 0.75 | 2:1 mux, multilayer |
| Novel input technique [3] | 15 | 0.01 | 0.5 | 2:1 mux |
| Priority-phased decomposition-driven (PPDD) [7] | 27 | 0.04 | 0.75 | 2:1 mux using gate level method |
| With fixed input cells [5] | 41 | – | 1 | 2:1 mux, no crossover, 1 fixed cell, single layer |
| With fixed input cells [5] | 1 81 | – | 3 | 4:1 mux, 3 fixed cells, single layer, no crossover |

## 3 Implementations

This section shows the implementations of best methodologies for various circuits. QCADesigner tool is used to build the layout of various circuits and to observe the simulation result. Cell interaction method is the best method as per as cell area is concerned. Table 1 clearly indicates that, with the other methodologies the parametric values are high for XOR gate. As a case study the XOR gate implementation with other best methods is as shown in Fig. 2a–c.

Graphical representation indicates that cell interaction or intercellular effect technique [6] is the best methodology among the all as it shows the optimization in all the parameters with respect to the other methodologies. This methodology can build all other circuits using this XOR gate with best optimization. Cell count is indicated in Fig. 3, device density in Fig. 4 and delay in Fig. 5 for all methodologies considered here for different circuits.

**Table 3** Different methodologies used to implement full adder

| Methodology/technique | Cell count | Area ($\mu m^2$) | Delay | Circuit implemented |
|---|---|---|---|---|
| Using majority gate and inverter [8] | 165 | 0.1932 | 1.25 | Full adder |
| Using minority gate [8] | 60 | 0.065 | 0.75 | Full adder |
| Using multilayer wire crossing [8] | 108 | 0.0884 | 1 | Full adder |
| Using 5 input majority gate [8] | 80 | 0.0352 | 0.75 | Full adder |
| Circuits with MV5 [9] | 54 | 0.04 | 0.75 | Full adder, coplanar |
| Tools to reduce simulation time [10] | 772 | – | – | Full adder |
| Single layer, one type of cells and the interference of clocking phases [11] | 95<br>494 | 0.09<br>0.68 | 1.25<br>4.25 | 1 bit and 4 bit Full adder |
| Tiles based design approach for QCA circuits [12] | 576 | – | 8 | 1 bit full adder with 64 tiles |
| Tiles based design approach for QCA circuits [12] | 1400 | – | 15 | 1 bit full adder with 56 squares |
| Tiles based design approach for QCA Circuits [12] | 396 | – | – | Gate based 1 bit full adder |
| Simplification in majority expressions [13] | 143<br>742 | 0.17<br>1.3 | 1.25<br>4.25 | 1 bit and 4 bit Full adder |
| Standards [14] | 190<br>NA | 0.2<br>NA | No clock<br>NA | 1 bit and 4 bit Full adder |

**Table 4** Best method analyzed

| Methodology/technique | Cell count | Area ($\mu m^2$) | Delay | Circuit implemented |
|---|---|---|---|---|
| Cell interaction [6] | 9 | 0.009 | 0.25 | XOR gate |
| Cell interaction [6] | 26 | 0.029 | 0.5 | 4 bit even parity generator |
| Novel input technique [3] | 15 | 0.01 | 0.5 | 2:1 mux |
| Circuits with MV5 [9] | 54 | 0.04 | 0.75 | Full adder, coplanar |
| Multilayer crossover [2] | 32 | 0.02 | 0.75 | D latch, multilayer |

## 4 Conclusion

Optimizing key metrics like delay, cell count and cell area will help improving logic computation and information flow at the physical level implementation. Although QCA logic components can be designed with QCA gates, extra delays will be introduced, which can lead to incorrect timing relationships. These timing issues present difficulties for interconnection and feedback which can affect the performance of QCA circuits. Therefore, assigning correct and efficient clocking zones to circuits is

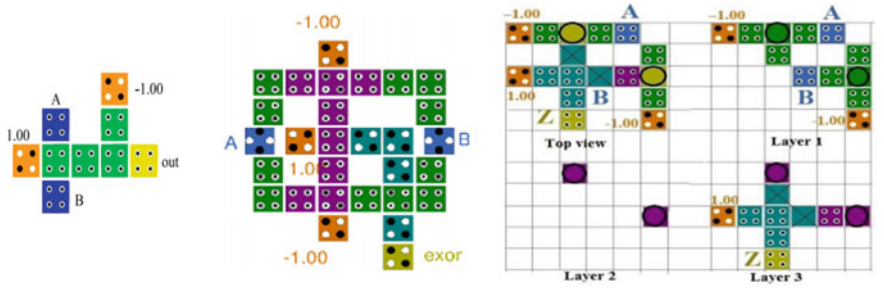



**Fig. 2** XOR gate layout with the best methodologies **a** [6], **b** [3], **c** [2]

**Fig. 3** Cell count

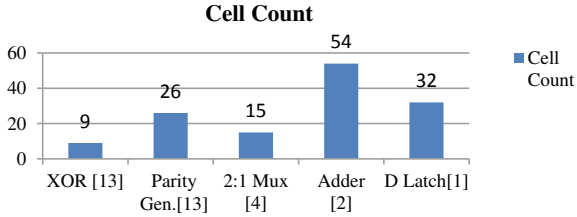



**Fig. 4** Device density

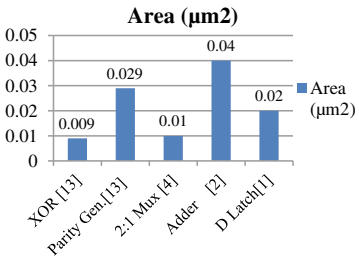
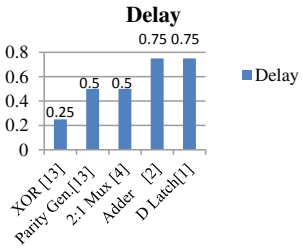



**Fig. 5** Delay




a major challenge in QCA circuit design. These all issues lead to design an efficient methodology to optimize all the parameters especially density, speed and less power consumption.

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