Analysis of Low-Power Cache Memory Design for Single Bit Architecture

Reeya Agrawal

Abstract This paper describes the analysis of low-power cache memory design for single bit architecture made up of six transistor static random access memory cell, write driver circuit, and voltage latch sense amplifier. At different values of resistance, consumption of power of cache memory design for single bit architecture has been analyzed. Process corner simulation and Monte Carlo simulation also have been done to check the robustness of the architecture. Conclusion arises that consumption of power decreases on increase in the value of resistance and 13.57 μW consumption of power done by cache memory design for single bit static random access memory cell voltage latch sense amplifier design with 13.02 ηs.

Keywords Latch sense amplifier (LSA) · Write driver circuit (WDC) · Six transistor static random access memory (STSRAM) · Voltage latch sense amplifier (VLSA)

1 Introduction

There are several memory elements within a system in contemporary computing systems, for example, main memory, cache memory, and register data [1–3]. With the latest development in the very large-scale integrated circuits (VLSI) technology, high-speed STSRAM is the industry's prime desire. Memory is the key component of a chip, and STSRAM is used as a cache memory because it is a fundamental part of memory that is important in data execution [4–6]. STSTRAM is a volatile memory since the information persists once the power is usable, which is essential and cannot be ignored in terms of reducing capacity in STSRAM. In an STSRAM architecture, the LSA is one of the elements of the data line. LSA is used to detect the difference in voltage at the input of the bit lines and to create a complete voltage swing at the output during the read operation [7]. Instead of having to measure or

R. Agrawal (✉)
GLA University, Mathura, India

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wait for the swing voltage level, the memory will simply store '0' or '1' to save time while reading.

The demand for mobile devices and a battery-operated embedded system is growing with greater breadth as VLSI industries grow. Cache memory design for single bit architecture is a central part of memory that plays a key role in data execution, cache occupying 60% to 70% of chip region [8]. As chip consumption increases rapidly, microprocessor velocity is then decreased. One million transistors also increase and degrade the efficiency of single-chip failure rates, so the industry is working to build a low-speed and low-power memory circuit, which keeps the development of the VLSI system informed. In current high-performance microprocessors, more than half of transistors are for cache memories, and in the future, this proportion is projected to increase [9]. STSRAM is usually the option for built-in stock because it is robust in such chips in a noisy environment. The device can use necessary memory cells by integrating them in SRAMC that are the right size for system requirements. Memories time for access and power consumption are calculated primarily by the configuration of LSA. LSA is one of the most important peripheral circuits in memory systems [10].

2 Literature Review

Year	Author	Features	Sensing delay (ns)	Supply voltage (V)
2002	A Chrysanthopoulos et al.	Conventional sense amplifier	7.1	2.5
2002	A Chrysanthopoulos et al.	Clamped bit line sense amplifier	0.35	2.5
2002	K.-S. Yeo et al.	Low-power current sense amplifier	1.04	2.0
2002	A Chrysanthopoulos et al.	Simple four transistor sense amplifier	1.85	2.5
2004	Chun-lung Hsu et al.	High-speed sense amplifier	0.51	1.8
2005	Z. H. Kong et al.	Ultralow-power	1.46	1.8
2007	Sandeep Patil et al.	Self-biased charge-transfer sense amplifier	0.723	1.8
2008	Ya-Chun Lai et al.	Latch type sense amplifier	0.33	1.8
2008	Anh-Tuan Do et al.	Fully current mode sense amplifier	0.38	1.8
2008	Do Anh-Tuan et al.	High-speed sense amplifier	0.26	1.8

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Year	Author	Features	Sensing delay (ns)	Supply voltage (V)
2011	Anh-Tuan Do et al.	Alpha latch sense amplifier	0.566	1
2011	Anh-Tuan Do et al.	Decoupled sense amplifier	0.214	1

3 Cache Memory Design for Single Bit Architecture

In this section, cache memory design for single bit architecture has been described with their design as shown in Fig. 1. Cache memory design for single bit architecture made up of WDC, STSRAM, and LSA [11, 12].

3.1 Circuit of Write Driver

Figure 2 shows the circuit diagram of WDC. Each of the bit-lines in the STSRAM write driver circuit is quickly discharged from pre-charge stages to below the STSRAM write margin [13].

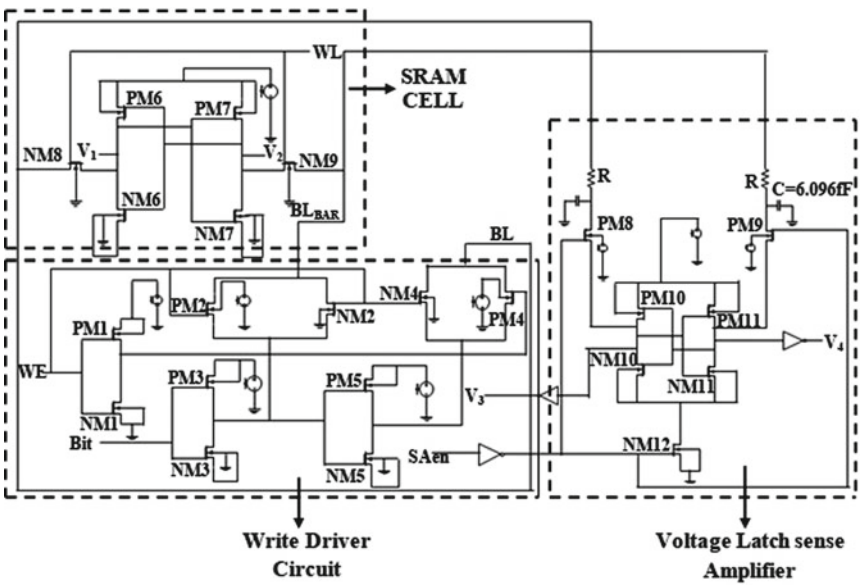

Fig. 1 Cache memory design for single bit STSRAM VLSA architecture schematic

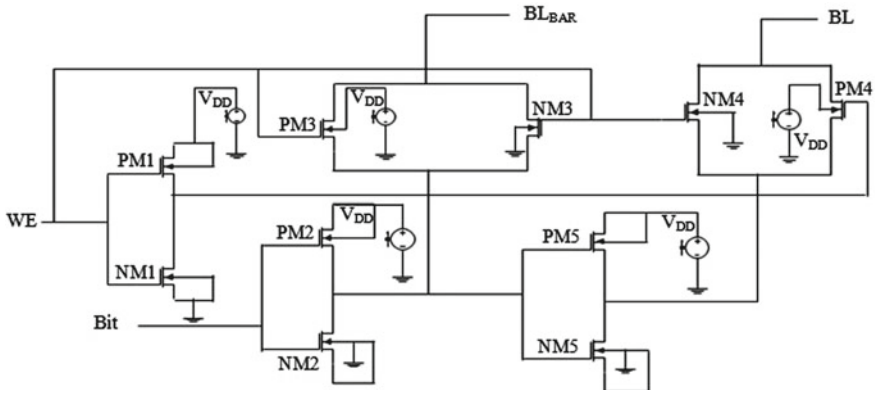

Fig. 2 Write driver circuit schematic

The write enable (WE) signal usually activates the WDC, which uses full-swing discharge to drive the bit-line from the pre-charge level to the ground. Five P_{MOS} (P_{M1}, P_{M2}, P_{M3}, P_{M4}, and P_{M5}) as well as five N_{MOS} (N_{M1}, N_{M2}, N_{M3}, N_{M4}, and N_{M5}) are used by WDC. When allowed by WE, the input data causes one of the transistors to become P_{M1} or N_{M1} through inverters, and a strong 0 is applied by discharging BTL and BTL_{BAR} from the pre-charge level to ground level [14].

3.2 Six Transistor Static Random Access Memory Cell

It is used for operations at low power, low voltage. Here, each bit is stored using bistable latching circuitry. Figure 3 shows the STSRAM cell schematic, the pull-up

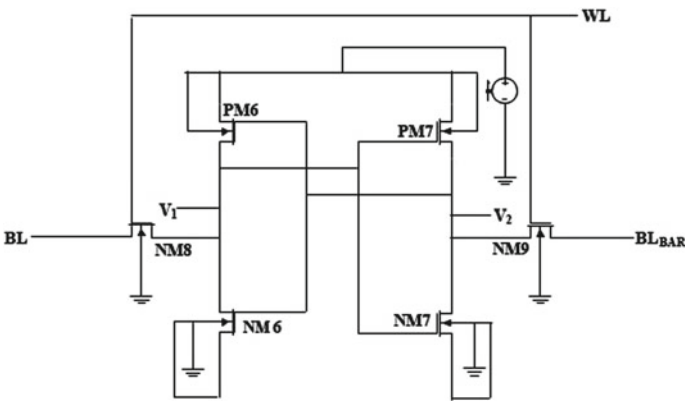

Fig. 3 Six transistor static random access memory cell schematic

transistors are M_1 and M_2 (P_{MOS}), while the driver transistors are M_3 and M_4 N_{MOS}. These bit lines enhance the margin of noise. The value of measurable output voltage swings is given by differential circuitry. Logic 0 or 1 is stored as long as the power is on, but unlike DRAM cells [15, 16]; it does not need to be refreshed. In STSRAM architecture, the size of the transistors is most important for the proper operation of the transistors.

3.3 Voltage Latch Sense Amplifier

The voltage latch sense amplifier schematics developed in this work are shown in Fig. 4. Internal nodes are pre-charged via the bit-lines in this design. The architecture of the circuit runs directly via input bit lines, based on its internal nodes [17–20].

If the word line is high pulled and followed by the amplifier sensor trigger, NM_{12} is OFF, and PM_8 and PM_9 are ON. If the voltage difference in the bit-lines increases, the random bit in the internal nodes of the LSA varies accordingly in voltage. When the LSA signal SA_{EN} is claimed, the interlinking inverters consist of PM_{10}, NM_{10}, PM_{11}, and NM_{11} raise the voltage difference to the highest swing power [21–25] as shown in Fig. 5.

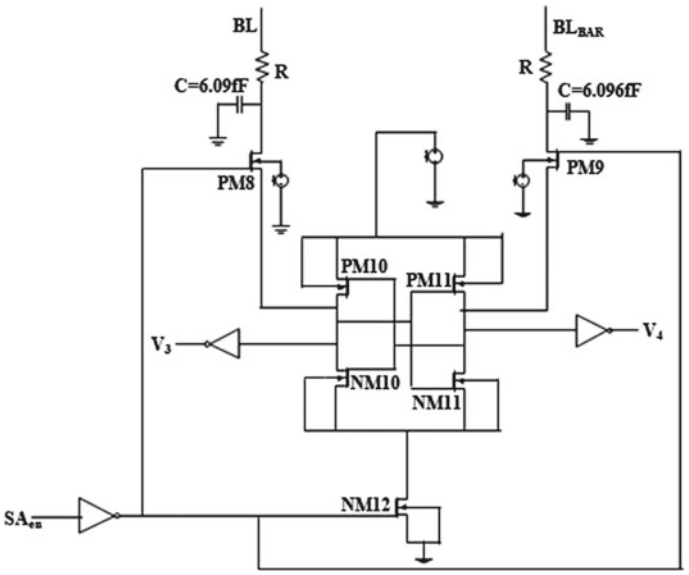

Fig. 4 Schematics of voltage latch sense amplifier

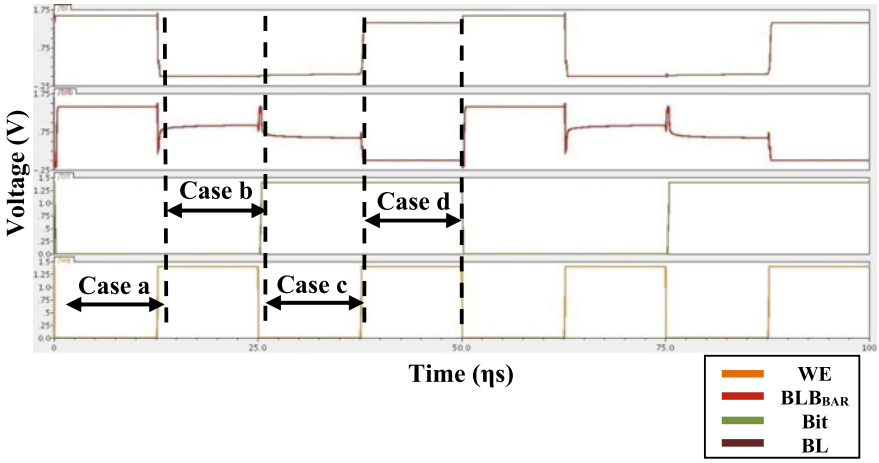

Fig. 5 WDC output waveform

4 Result Analysis

Figure 5 describes the output waveform of WDC, for cases arise: (a) when Bit = 0 V and WE = 0 V BTL = V_{DD} and BTL_{BAR} = V_{DD}, (b) Bit = 0 V WE = V_{DD} so, BTL = 0 V and BTL_{BAR} = $V_{DD}/2$, (c) Bit = V_{DD} WE = 0 V so, BTL = 0 V and BTL_{BAR} = $V_{DD}/2$ and (d) Bit = V_{DD} WE = V_{DD} so, BTL = V_{DD} and BTL_{BAR} = 0 V.

Figure 6 shows the output waveform of STSRAM which holds two operations:

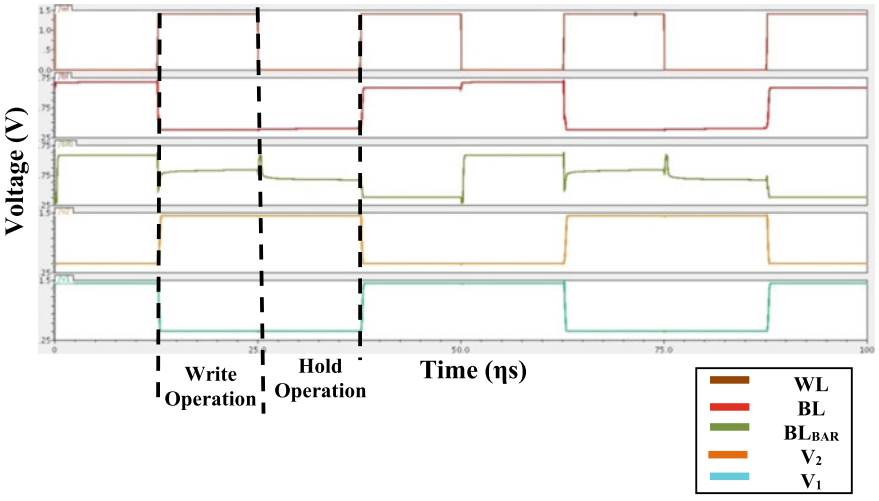

Fig. 6 STSRAM cell output waveform

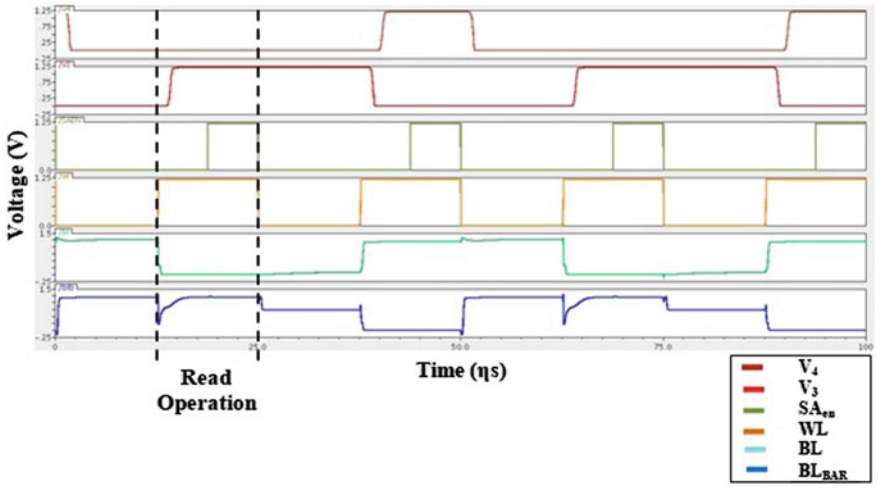

Fig. 7 Output waveform of VLSA

1. Write Operation
2. Hold Operation.

There are three types of transistors: (i) access transistors, (ii) pull-up transistor, and (iii) pull-down transistors. Figure 7 describes the read operation of VLSA when both $SA_{EN} = 1$ and $WL = 1$ at that time sense amplifier works in read operation. **Note: $P = V^2/R$ as this voltage is constant on varying the R and analyzing the power consumption.**

Figure 8 shows the process corner simulation of cache memory design for single bit architecture at six different corners, whereas Fig. 9 shows the Monte Carlo simulation for cache memory design for single bit architecture.

Table 1 depicts that consumption of power decreases as increase in value of resistance, whereas Fig. 10 shows the comparative analysis of different parameters of cache memory design for cache memory architecture using different values of resistance of Table 1 in form of a chart.

5 Conclusion

In the proposed work, cache memory design for single bit architecture has been implemented, and on different values of resistance, different parameters of cache memory design for single bit architecture have been analyzed. To check the robustness of cache memory design for single bit architecture process corner simulation and Monte Carlo simulation also have been done. Furthermore, consumption of power of

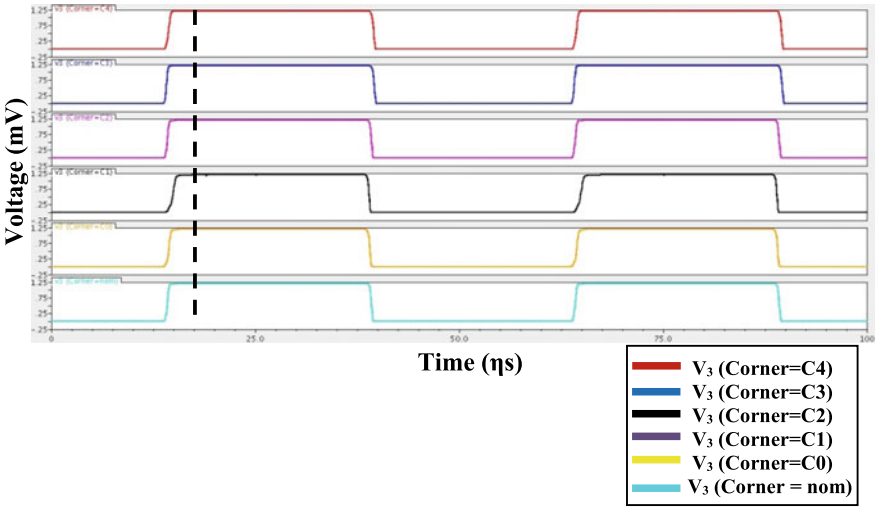

Fig. 8 Process corner simulation

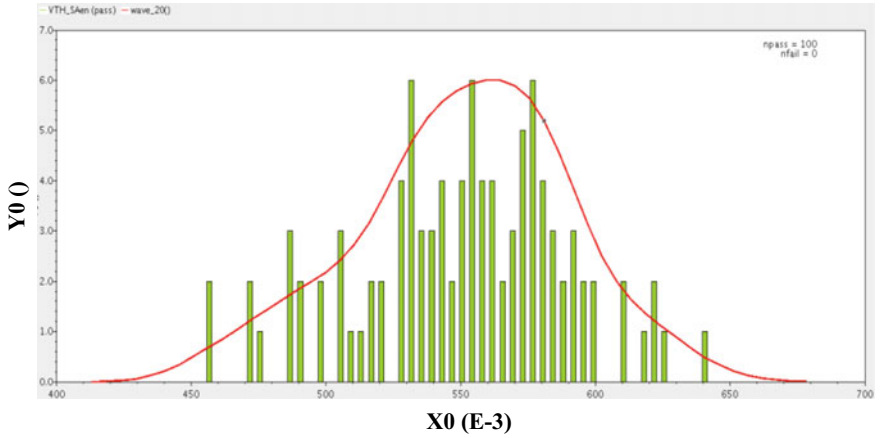

Fig. 9 Monte carlo simulation

Table 1 Analysis of different parameter of single bit SRAMC VLSA design

S. No.	Parameters	Delay in sensing (ηs)	Number of transistors	Consumption of power (μW)
1	$R = 42.3\ \Omega$	13.50	29	36.57
2	$R = 42.3\ \text{K}\Omega$	13.50	29	14.32

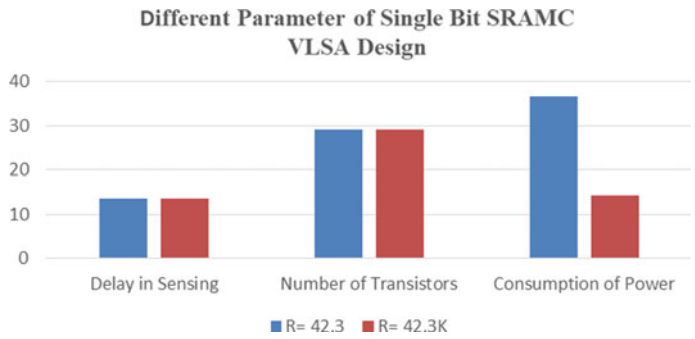

Fig. 10 Analysis of different parameter of single bit SRAMC VLSA design at different values of resistance

cache memory design for single bit architecture has been analyzed and the conclusion arises that consumption of power decreases on increasing resistance value (i.e., 14.32 μW). In the future scope, this work can be implemented in form of an array.

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