Performance Analysis of Cache Memory Architecture for Core Processor

Reeya Agrawal

Abstract A quantitative and yield analysis of single-bit cache memory architecture with different sense amplifiers such as voltage mode sense amplifier and charge-transfer sense amplifier has been done. Apart from that, power reduction techniques such as the sleep transistor technique, footer stack technique, and dual sleep technique also have been applied over different blocks of single-bit cache memory architecture to reduce the power consumption of the architecture.

Keywords Static random access memory cell (SRAMC) · Voltage mode sense amplifier (VMSA) · Charge-transfer sense amplifier (CTSA) · A sense amplifier (SA) · Write driver circuit (WDC)

1 Introduction

Improved density and efficiency of VLSI circuits have been obtained by scale-down transistors. Local connections are called wires and are used to connect transistors within integrated circuits. The clock and power routing wires within the chip are known as global links on the chip. The latency of global communication becomes essential for many applications, such as buses between cache memories and processors [1–3], as the VLSI technology scales down to the sub-micron level. With the length [4–6], the delay in this global interconnection on the chip raises four-way. Different signaling methods were suggested to transmit the signals by interconnection, and to reduce the delay, different kinds of transceivers were employed. In recent years, the design of low power storage has been powered by the exponential output of battery-operated computers. The leakage current has made the SRAM system a power-hungry block from both static and dynamic perspectives as the transistor count increases. The SRAM block is now also an important part of the SOC architecture.

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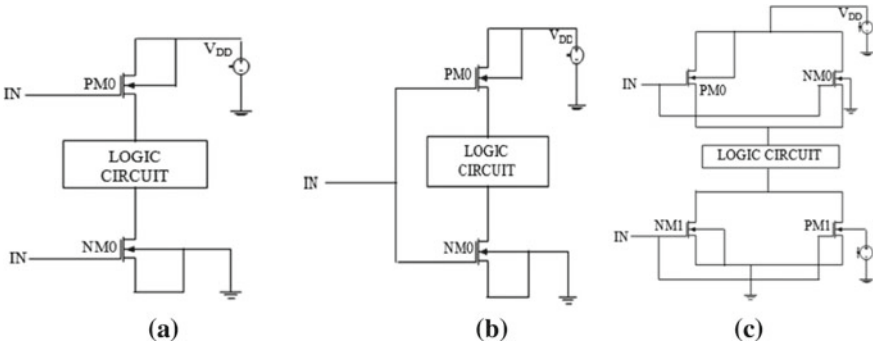

Fig. 1 a Sleep transistor technique. b Forced stack technique. c Dual sleep technique

1.1 Power Reduction Techniques

In the VLSI model, the designers suggested many strategies for reducing the power consumption of the circuit. The short descriptions of all the methods used in the circuits are given below [7].

1.1.1 Sleep Transistor Technique

The sleep transistor technique [8] is the most well-known method. A P_{MOS} transistor "Sleep" is situated between V_{DD} and network pull-up, and an N_{MOS} transistor is positioned between pull-down network and G_{ND} as shown in Fig. 1a.

1.1.2 Forced Stack Technique

Another power reduction technique is the stacking strategy, which pushes an individual transistor into two half-size transistors [9]. The result of the transistor stacking contributes to a reduction in the decrease in sub-threshold current. This strategy saves the actual state while the transistor is in the off state as shown in Fig. 1b.

1.1.3 Dual Sleep Technique

Both P_{MOS} and N_{MOS} types of transistors are used in this technique. Both P_{MOS} and N_{MOS} transistors are used in the header and footer. In on-state mode, one transistor is on and another transistor is switched off in the off-state mode. Both P_{MOS} and N_{MOS} are used in off-state mode to decrease leakage capacity as shown in Fig. 1c [10].

The single-bit cache memory architecture is clarified in Sect. 2 in depth, and SRAM architecture is explained. Experimental effects are shown in Sect. 3. Conclusions are obtained in Sect. 4.

2 Single-Bit Cache Memory Architecture

In this section, cache memory architecture has been described with their architectures as shown in Figs. 2 and 3. SRAM architecture comprises WDC, SRAMC, and SA. SA is of two types: (a) the voltage difference between the bit lines is amplified to determine the output voltage; voltage mode sense amplifier has five input pins (BL, BLB, Y_{sel}, Pch, and SA_{en}) and two output pins (V_3 and V_4); (b) charge-transfer sense amplifier, the higher bit line capacitance charge propagation can be used in narrower lines to achieve the output voltage; it has five input pins (BL, BLB, Y_{sel}, Pch, and SA_{en}) and two output pins (V_3 and V_4).

2.1 Write Driver Circuit

The write driver is responsible for rapidly discharging the bit lines to a level below the cell's write margin before or when the selected cell's word lines are involved. Two standard written drivers are seen in Fig. 4. The input of the data chooses which bit line is discharged. Just when the writing process is intended is the WE signal switched on.

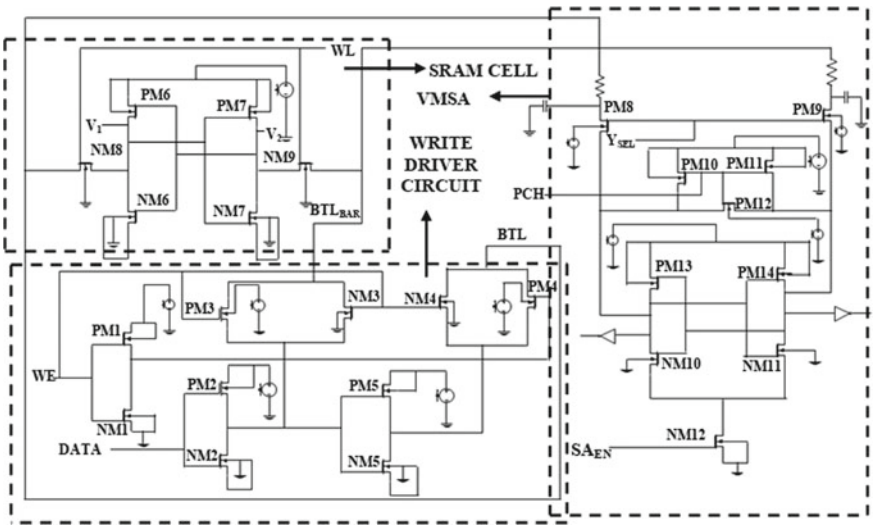

Fig. 2 Schematic of single-bit SRAM VMSA architecture

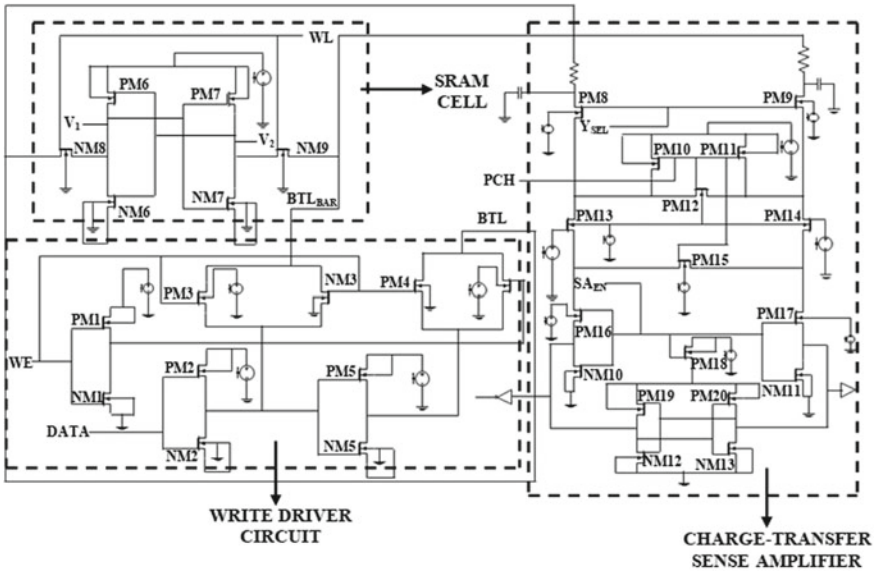

Fig. 3 Schematic of single-bit SRAM CTSA architecture

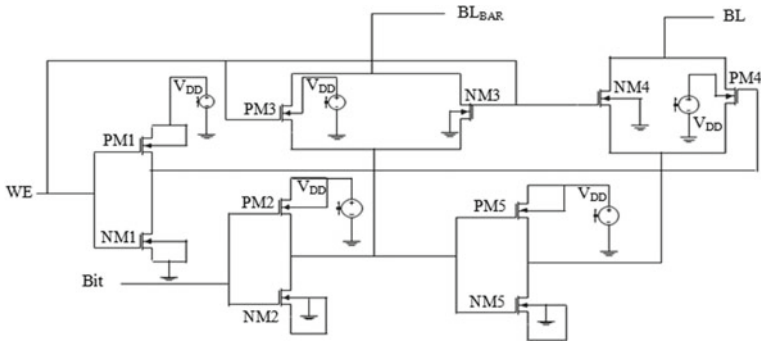

Fig. 4 Write driver circuit schematic

Otherwise, WE distinguishes the bit lines from the drivers of printing. It is quicker because, at the cost of sophistication, it has fewer stacked transistors in its discharge direction. Usually, the write operation is not a transaction that restricts speed, so the write driver is chosen for simplified setups that relax the layout specifications [11–13].

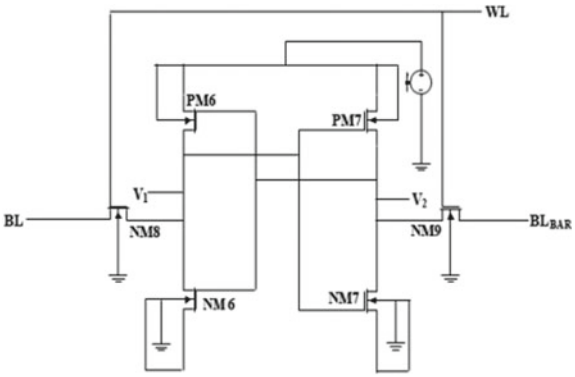

Fig. 5 SRAM cell **schematic**

2.2 Conventional SRAM

It is used for operations at low power, low voltage. Here, each bit is stored using bistable latching circuitry. Figure 5 shows the 6T SRAMC schematic, the pull-up transistors are M_1 and M_2 (P_{MOS}), while the driver transistors are M_3 and M_4 N_{MOS}. These bit lines enhance the margin of noise. The value of measurable output voltage swings is given by differential circuitry. Logic 0 or 1 is stored as long as the power is on, but unlike DRAM cells [14, 15], it does not need to be refreshed. In SRAM architecture, the size of the transistors is most important for the proper operation of the transistors.

2.3 Sense Amplifiers

The sensor amplifier amplifies a small analog differential voltage produced on the read-access bit lines. The amplification leads to a complete one-end digital output. Because of the length of the metal and because a lot of transistors take a long time to discharge the bit lines, bit lines have more power. Timing regulation and filling condenser set are hard choices for sensory amplifiers here [16].

2.3.1 Voltage Mode Sense Amplifier.

The power amplifier function is based on the differential voltage produced by the bit lines. The circuit consists of cross-connected inverters that convert the bit-line voltage difference at its entrance to full swing output, as shown in Fig. 6. The cell columns integrate BL and BLB inputs with the cell column bit lines. P_1 binds the memory cell to the P_2 sensory boost and N_3 activates the sensation boost. The inner nodes of the sensory amplifier are separated by output inverters from the external

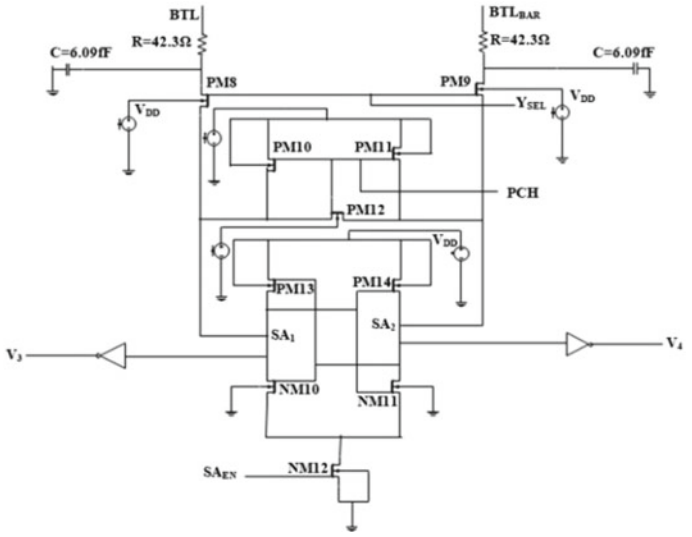

Fig. 6 Schematic of voltage mode sense amplifier

load. The sensor amplification is applied to the memory cell by returning the selected line during the evaluation process (SA_{en}) [17, 18].

2.3.2 Charge-Transfer Sense Amplifier

Figure 7 illustrates the extension of this concept to SRAM sense amplifiers, where the broad data line capacitance of the CDL is related to the limited capacitance of the sensing node, CTSA.

The basic principle behind the amplification of the charging transmission is to generate voltage gains by manipulating the conservation of charge among capacitive devices [19, 20]. The voltage on the first element and its capacity have to equal the voltage on the other element product and its capacity for a set of contacts of two capacitive elements in a device to be loaded.

3 Results and Discussion

Figure 8 describes the output waveform of WDC, for cases arise: (a) when Bit = 0 V and WE = 0 V BL = V_{DD} and BL_{BAR} = V_{DD}, (b) Bit = 0 V WE = V_{DD} so, BL = 0 V and BL_{BAR} = V_{DD}/2, c) Bit = V_{DD} WE = 0 V so, BL = 0 V and BL_{BAR} = V_{DD}/2 and d) Bit = V_{DD} WE = V_{DD} so, BL = V_{DD} and BL_{BAR} = 0 V.

Figure 9 describes both write operation and hold operation of the SRAMC. There is a pull of the n/w (PM6 and PM7), pull-down network (NM6 and NM7), and access

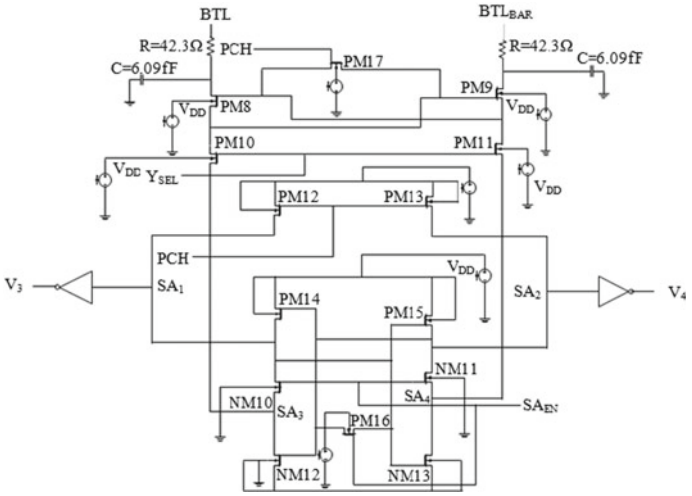

Fig. 7 Schematic of charge-transfer sense amplifier

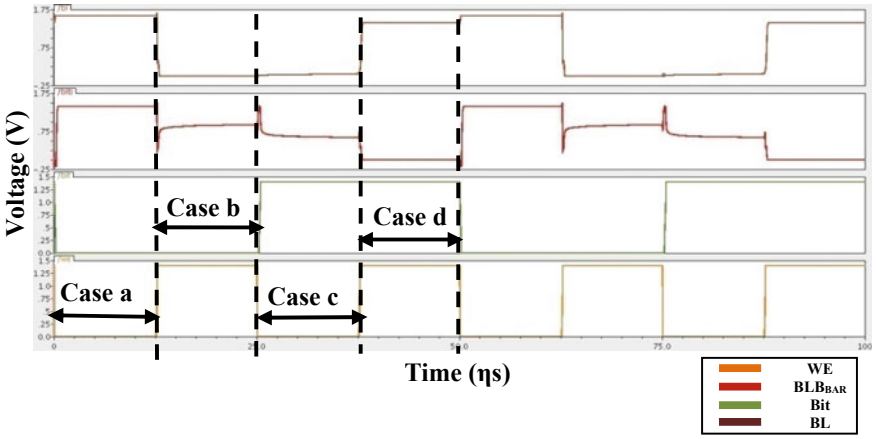

Fig. 8 Output waveform of WDC

transistor (NM8 and NM9) which allows data to store and sense amplifier to read the data.

Figures 10 and 11 describe the read operation of VMSA and CTSA when both SA_{EN} and WL are pulled high; during that time, only the SA senses the data from the SRAMC at bit lines and gives output at V_3 and V_4.

Note: $P = V^2/R$ as this voltage is constant on varying the R and analyzing the power consumption.

Table 1 describes that increase in value of resistance power consumption decreases as because resistance is a path stopper for current in a circuit and no effect on the

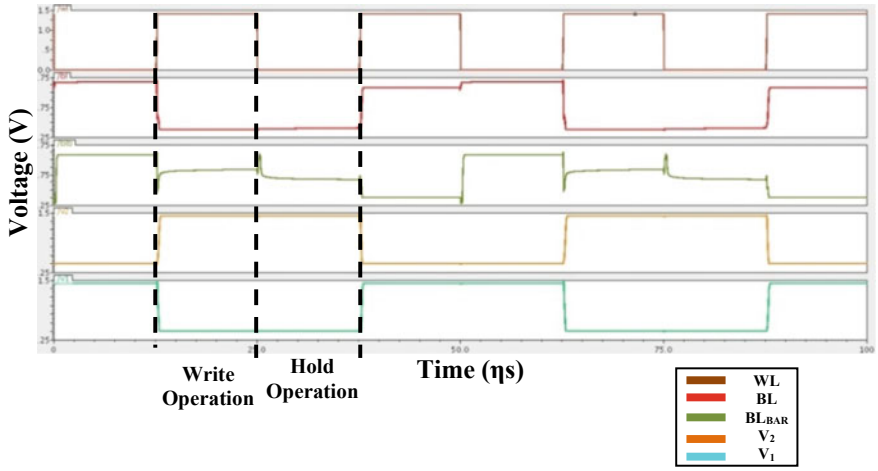

Fig. 9 Output waveform of SRAMC

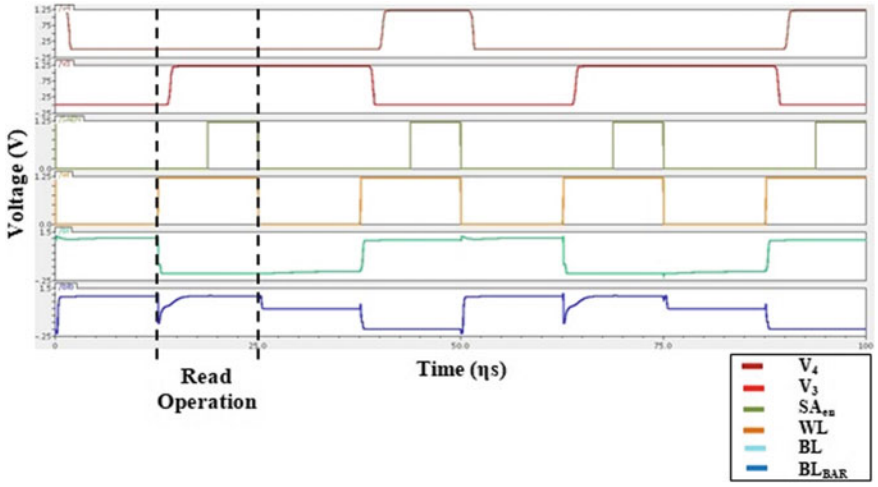

Fig. 10 Output waveform of VMSA

area, performance, and speed, whereas Fig. 12 shows the comparison of the different parameters of a single-bit SRAM VMSA architecture of Table 1 in form of a chart.

Table 2 describes that as increasing in value of resistance power consumption decreases as because resistance is a path stopper for current in a circuit and no effect on the area, performance, and speed, whereas Fig. 13 shows the comparison of the different parameters of a single-bit SRAM CTSA architecture of Table 2 in form of a chart.

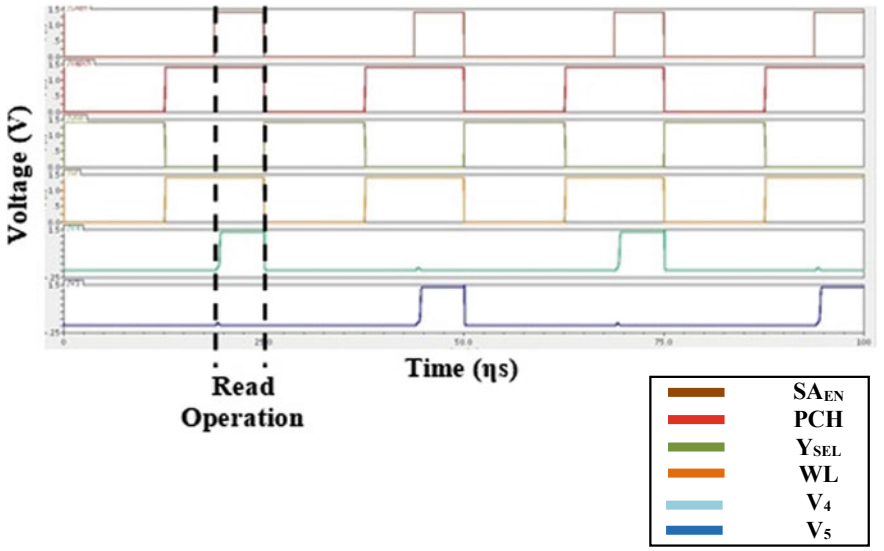

Fig. 11 Output waveform of CTSA

Table 1 Different parameters of single-bit SRAM VMSA architecture

S. No	Parameters	Single-bit SRAM VMSA architecture		
		Power consumption (μW)	No. of transistors	Sensing delay (ηs)
1	$R = 42.3\ \Omega$	13.16	30	13.14
2	$R = 42.3\ \text{K}\Omega$	11.34	30	13.14

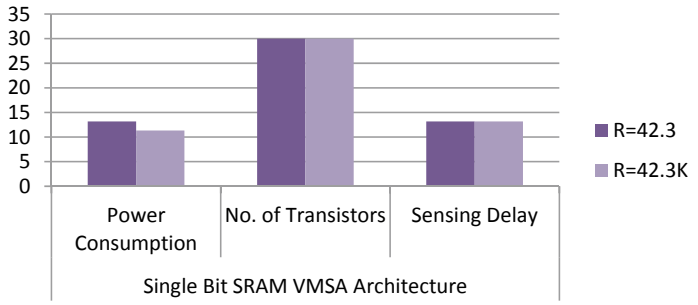

Fig. 12 Comparison of different parameters of single-bit SRAM VMSA architecture

Table 2 Different parameters of single-bit SRAM CTSA architecture

S. No	Parameters	Single-bit SRAM CTSA architecture		
		Power consumption (μW)	No. of transistors	Sensing delay (ηs)
1	$R = 42.3\Omega$	46.35	37	13.51
2	$R = 42.3\text{K}\Omega$	44.32	37	13.51

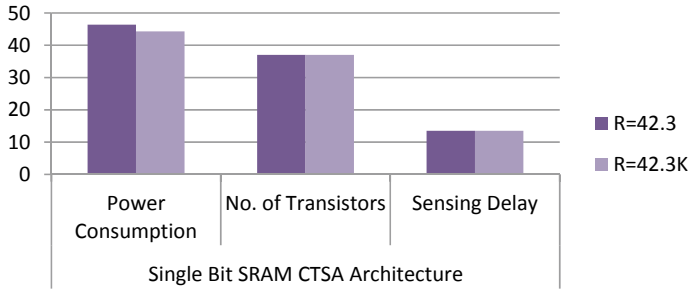

Fig. 13 Comparison of different parameters of single-bit SRAM CTSA architecture

Table 3 Power consumption of single-bit cache memory architecture

S. No		Single-bit SRAM VMSA architecture		Single-bit SRAM CTSA architecture	
		Power consumption (μW)	No. of transistor	Power consumption (μW)	No. of transistor
1	Sleep transistor	11.29	32	20.38	39
2	Forced stack	11.29	32	20.38	39
3	Dual sleep	11.03	34	21.05	41

Table 3 describes that applying power reduction technique over SA forced stack technique in single-bit cache memory architecture reduced power consumption, i.e., 11.03 μW with 34 number of the transistor, whereas Fig. 14 shows the comparison

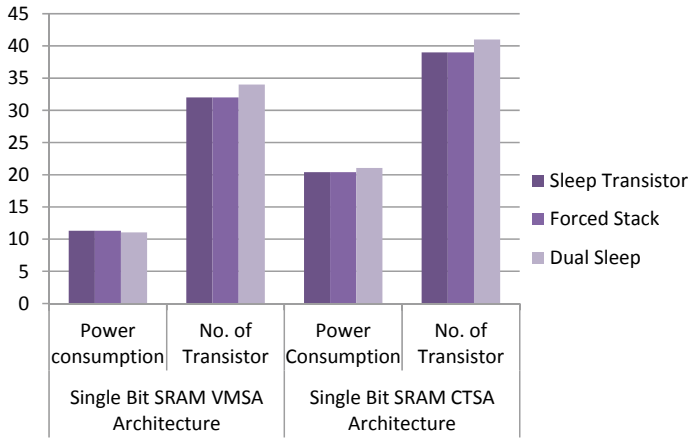

Fig. 14 Comparison of power consumption of single-bit cache memory architecture on applying power reduction techniques over SA

Table 4 Power consumption of single-bit cache memory architecture

S. No		Single-bit SRAM VMSA architecture		Single-bit SRAM CTSA architecture	
		Power consumption (μW)	No. of transistor	Power consumption (μW)	No. of transistor
1	Sleep transistor	9.18	34	18.18	41
2	Forced stack	9.108	34	18.17	41
3	Dual sleep	10.13	38	18.91	45

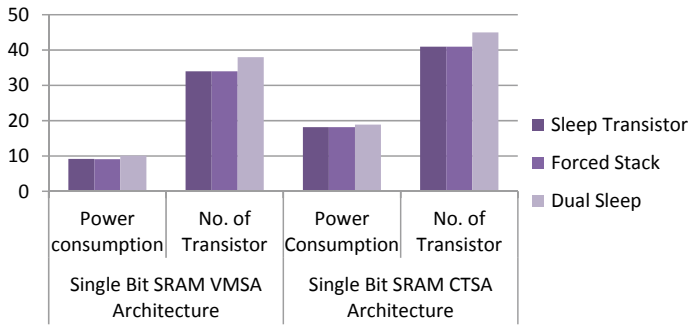

Fig. 15 Comparison of power consumption of single-bit cache memory architecture on applying power reduction techniques over SRAM and SA

of power consumption of single-bit cache memory architecture on applying power reduction techniques over SA of Table 3 in form of a chart.

Table 4 describes that applying power reduction techniques over SRAM and SA consumes up to 9.108 μW power which is lowest as compared to others, but the number of transistors increases transistor, whereas Fig. 15 shows the comparison of power consumption of single-bit cache memory architecture on applying power reduction techniques over SRAM and SA in architecture of Table 4 in form of a chart.

4 Conclusion

In this paper, single-bit cache memory with different sense amplifiers such as voltage differential sense amplifier and charge-transfer sense amplifier has been implemented and compared on different values of resistance (R) with different parameters such as power consumption, sensing delay, and several transistors. Apart from that, power reduction technique has been applied over different blocks of single-bit cache

memory architecture and results depicted that the single-bit cache memory architecture having voltage mode differential sense amplifier with forced stacked consumes the lowest power (9.108 μW). In the future scope, this work can be done in form of an array.

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